

DRV7308 Three Phase 650V, 5A, GaN Intelligent Power Module

1 Features

- Three-phase PWM motor driver with integrated 650V enhancement mode GaN FETs
- Up to 450V operating voltage
 - 650V absolute maximum voltage
- High output current capability: 5A Peak current
- Low conduction loss: Low on-state resistance per GaN FET: $205\text{m}\Omega R_{DS(ON)}$ at $T_A = 25^\circ\text{C}$
- Low switching loss: Zero reverse recovery, low output capacitance, slew rate control
- Low distortion: Ultra-low propagation delay < 135ns, Ultra-low adaptive dead time < 200ns
- Integrated gate drives with slew rate control of phase node voltage
 - Slew rate options from 5V/ns to 40V/ns
- Integrated fast bootstrap GaN rectifier
- Low-side GaN FET open source pins to support 1- or 2- or 3-shunt current sensing
- Supports up to 100kHz hard switching
- Integrates an amplifier for current sensing
- Supports 3.3V and 5V logic inputs, up to 20V
- BRAKE pin to turn on all low side GaN FETs
- Integrated temperature sensor
- >1.6mm clearance of motor phase (OUTx) to the adjacent pins.
- 2mm clearance between VM and GND
- Integrated protection features
 - GVDD and bootstrap under voltage lockout
 - Over current protection for low-side GaN FET
 - Over temperature protection
 - PWM adaptive dead time insertion
 - Current limit protection for all three phases
 - Fault condition indication pin (nFAULT)

- [Dishwasher](#)
- [Small home appliances](#)
- [Residential air conditioners](#)
- [Cooker hood](#)
- [Brushless-DC motor modules](#)

3 Description

The DRV7308 is a three-phase intelligent power module (IPM) that consists of 205mΩ, 650V e-mode Gallium-Nitride (GaN) for driving three-phase BLDC/PMSM motors up to 450V DC rails. The applications include field-oriented control (FOC), sinusoidal current control, and trapezoidal (six step) current control of BLDC motors. The device helps to achieve more than 99% efficiency for a 3-phase modulated, FOC-driven, 250W motor drive application in a QFN 12mm x 12mm package at 20kHz switching frequency, eliminating the need for heat sink. The device helps to achieve ultra quiet operation, with very low dead time. The integrated bootstrap rectifier with bootstrap current limit eliminates the need for an external bootstrap diode.

Note

For safety, TI recommends the use of isolated test equipment with overvoltage and overcurrent protection. TI recommends using a safety enclosure when operating the device.

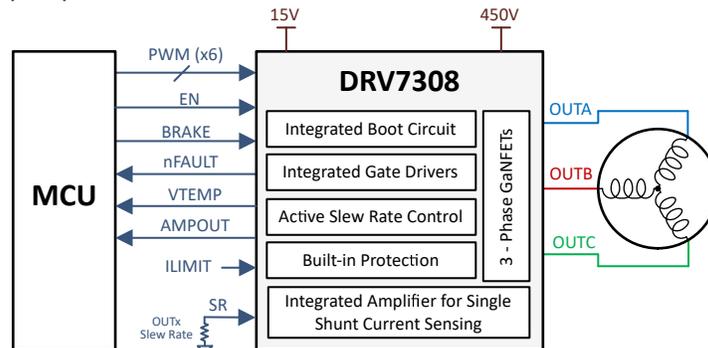
Package Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE ⁽²⁾ |
|-------------|------------------------|-----------------------------|
| DRV7308 | REN (VQFN, 65) | 12.00mm x 12.00mm |

- (1) For more information, see the [Mechanical, Packaging, and Orderable Information](#).
- (2) The package size (length x width) is a nominal value and includes pins, where applicable.

2 Applications

- [Refrigerator & freezer](#)
- [Appliances](#) and HVAC pumps and fans



Simplified Schematic



Table of Contents

| | | | |
|---|----|--|----|
| 1 Features | 1 | 13.1 Application Information..... | 19 |
| 2 Applications | 1 | 13.2 Typical Application..... | 19 |
| 3 Description | 1 | 14 Layout | 25 |
| 4 Pin Configuration and Functions | 3 | 14.1 Layout Guidelines..... | 25 |
| 5 Absolute Maximum Ratings | 5 | 14.2 Layout Example..... | 25 |
| 6 ESD Ratings | 5 | 15 Revision History | 25 |
| 7 Recommended Operating Conditions | 5 | 16 Device and Documentation Support | 27 |
| 8 Thermal Information | 6 | 16.1 Documentation Support..... | 27 |
| 9 Electrical Characteristics | 6 | 16.2 Receiving Notification of Documentation Updates.. | 27 |
| 10 Timing Diagrams | 10 | 16.3 Support Resources..... | 27 |
| 11 Typical Characteristics | 10 | 16.4 Trademarks..... | 27 |
| 12 Detailed Description | 11 | 16.5 Electrostatic Discharge Caution..... | 27 |
| 12.1 Overview..... | 11 | 16.6 Glossary..... | 27 |
| 12.2 Functional Block Diagram..... | 12 | 17 Mechanical, Packaging, and Orderable | |
| 12.3 Feature Description..... | 12 | Information | 27 |
| 12.4 Protections..... | 15 | 17.1 Tape and Reel Information..... | 28 |
| 13 Application and Implementation | 19 | | |

4 Pin Configuration and Functions

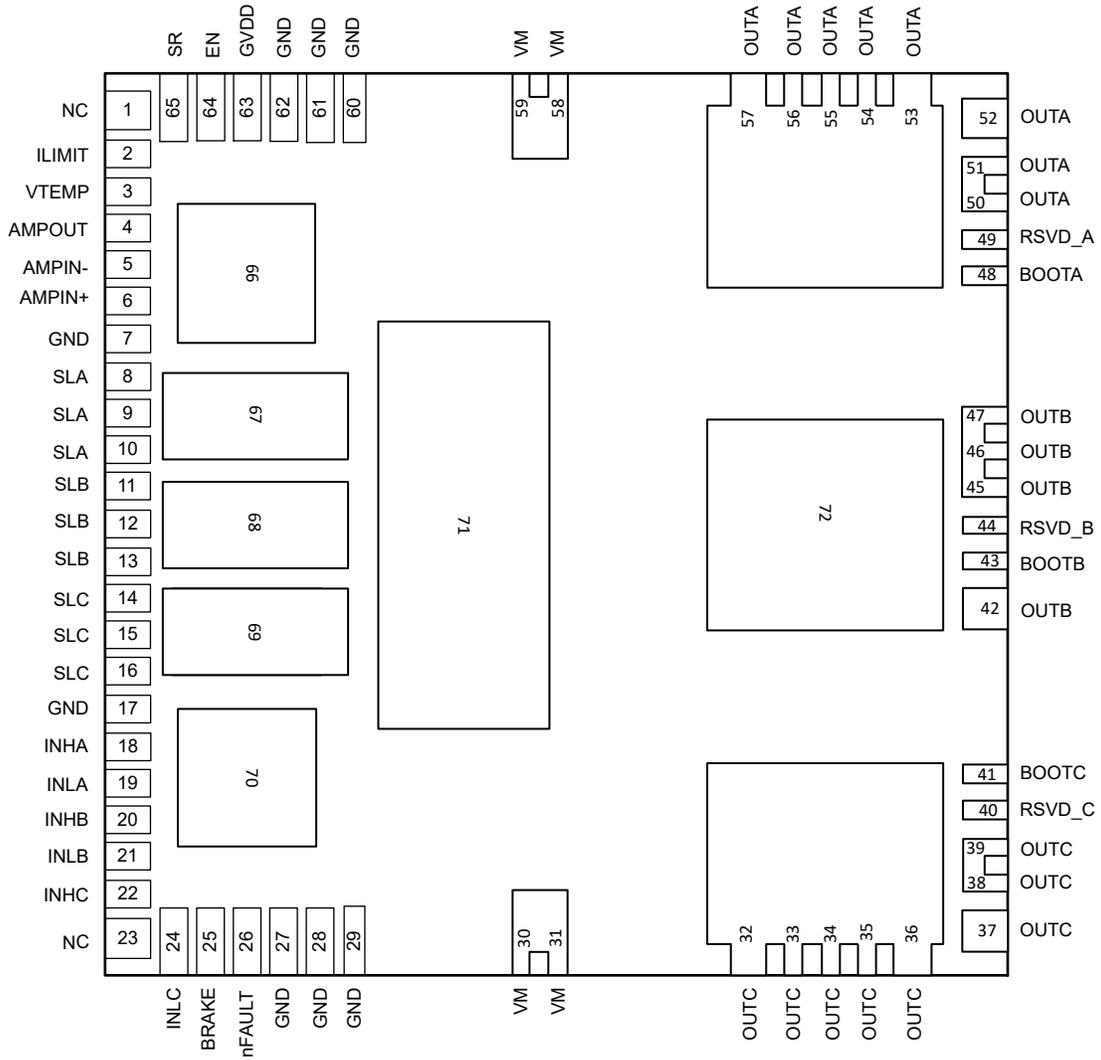


Figure 4-1. DRV7308 VQFN With Exposed Thermal Pad Top View

Table 4-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|--------|---|---------------------|--|
| NAME | NO. | | |
| AMPIN- | 5 | I | Inverting input of the operational amplifier |
| AMPIN+ | 6 | I | Non-inverting input of the operational amplifier |
| AMPOUT | 4 | O | Output terminal of the operational amplifier |
| BOOTA | 48 | P | Bootstrap supply for phase A; A GVDD rated capacitor must be placed between BOOTA and OUTA. |
| BOOTB | 43 | P | Bootstrap supply for phase B; A GVDD rated capacitor must be placed between BOOTB and OUTB. |
| BOOTC | 41 | P | Bootstrap supply for phase C; A GVDD rated capacitor must be placed between BOOTC and OUTC. |
| BRAKE | 25 | I | Motor Brake signal. Logic high on the pin turns on all the low side GaN FETs and turns off all the high side GaN FETs |
| EN | 64 | I | Driver enable pin. When this pin is logic low the device goes to shutdown mode and all the GaN FETs are turned off. A 20µs to 40µs low pulse can be used to reset fault conditions |
| nFAULT | 26 | O | Fault indication pin. Pulled logic-low on fault condition; Open-drain output requires an external pullup |
| ILIMIT | 2 | I | Reference voltage for internal overcurrent limit comparator |
| INHA | 18 | I | High-side driver control input for OUTA. This pin controls the output of the high-side GaN FET |
| INHB | 20 | I | High-side driver control input for OUTB. This pin controls the output of the high-side GaN FET |
| INHC | 22 | I | High-side driver control input for OUTC. This pin controls the output of the high-side GaN FET |
| INLA | 19 | I | Low-side driver control input for OUTA. This pin controls the output of the low-side GaN FET |
| INLB | 21 | I | Low-side driver control input for OUTB. This pin controls the output of the low-side GaN FET |
| INLC | 24 | I | Low-side driver control input for OUTC. This pin controls the output of the low-side GaN FET |
| NC | 1, 23 | | No connect, can be connected to GND |
| RSVD_A | 49 | I | Reserved pin. Connect the pin to OUTA |
| RSVD_B | 44 | I | Reserved pin. Connect the pin to OUTB |
| RSVD_C | 40 | I | Reserved pin. Connect the pin to OUTC |
| OUTA | 50-57 | P | Half bridge output A |
| OUTB | 42, 45-47, 72 | P | Half bridge output B |
| OUTC | 32-39 | P | Half bridge output C |
| GND | 7, 17, 27, 28, 29, 60, 61, 62, 66, 70, 71 | G | Device power and signal ground. Connect to system ground |
| SLA | 8, 9, 10, 67 | P | Phase A half bridge low side source |
| SLB | 11, 12, 13, 68 | P | Phase B half bridge low side source |
| SLC | 14, 15, 16, 69 | P | Phase C half bridge low side source |
| SR | 65 | I | OUTx voltage slew rate control. Connect a resistor between SR pin and GND or SR pin to GVDD to configure the slew rate |
| GVDD | 63 | P | Low voltage power supply. bypass to GND with one 1µF, GVDD rated ceramic capacitor plus one bulk capacitor rated for GVDD |
| VM | 30, 31, 58, 59 | P | Power supply. Connect to motor supply voltage; bypass to GND with a 0.1µF capacitor plus one bulk capacitor rated for VM. The pins 30 and 31 are internally connected to the pins 58 and 59. |

Table 4-1. Pin Functions (continued)

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-------|-----|---------------------|---------------------------|
| NAME | NO. | | |
| VTEMP | 3 | O | Temperature Sensor Output |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)⁽²⁾

| | MIN | MAX | UNIT |
|--|-----------|--------------------|------------------|
| Drain-source blocking voltage (FET off) (V_{DS}) | | 650 ⁽¹⁾ | V |
| DC voltage applied between VM and GND | | 450 | V |
| Drain DC current (I_{DC}) @ $T_J = 150^\circ\text{C}$ | | 4 | A |
| Phase node pin voltage referred to GND (FETs OFF) (OUTA, OUTB, OUTC), SL = GND | $-V_{SD}$ | 650 | V |
| BOOTx pin voltage referred to OUTx (BOOTA, BOOTB, BOOTC) | -0.5 | 20 | V |
| Pin voltage - GVDD to GND | -0.5 | 20 | V |
| Pin voltage - INx, EN, BRAKE, nFAULT to GND | -0.5 | 20 | V |
| Pin voltage - SLx to GND (DC) | -2.5 | +2.5 | V |
| Pin voltage - AMPIN+, AMPIN-, AMPOUT, ILIMIT, SR to GND | -0.5 | $V_{GVDD}+0.3$ | V |
| Operational amplifier output current (AMPOUT) | | 20 | mA |
| Operating ambient temperature | -40 | 125 | $^\circ\text{C}$ |
| Operating junction temperature (T_J) | -40 | 150 | $^\circ\text{C}$ |
| Storage temperature (T_{stg}) | -55 | 150 | $^\circ\text{C}$ |

(1) Product lifetime depends on V_{DS} voltage.

(2) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6 ESD Ratings

| | | | VALUE | UNIT |
|-------------|-------------------------|---|------------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ± 2000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | ± 500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|------------|--------------------------------|-----------------------|------|-----|-----|------|
| V_{VM} | DC power supply voltage | VM | 0 | | 450 | V |
| V_{GVDD} | Gate driver supply voltage | GVDD | 10.8 | | 18 | V |
| f_{PWM} | PWM frequency | OUTA, OUTB, OUTC | | 20 | 100 | kHz |
| V_{IN} | Logic Input Voltage | INHx, INLx, EN, BRAKE | -0.1 | | 20 | V |
| V_{OD} | Open drain pull up voltage | nFAULT | -0.1 | | 20 | V |
| I_{OD} | Open drain output sink current | nFAULT | 0 | | 5 | mA |

over operating temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|----------------------|-----------------------------------|-------------------------|------|-----|------|------|
| V _{SR} | Slew rate pin voltage | SR | | | GVDD | V |
| V _{SLx} | SLx pin voltage | SLA, SLB, SLC | -1 | | 1 | V |
| V _{AMPINx} | Amplifier input pin voltage | AMPIN+, AMPIN- | -0.1 | | 5 | V |
| V _{ILIMIT} | Over current protection reference | ILIMIT | 0.2 | | 2 | V |
| T _{PWIN_ON} | Minimum input pulse width | INH, INL ⁽¹⁾ | 0.5 | | | µs |
| T _A | | | -40 | | 100 | °C |
| T _J | | | -40 | | 125 | °C |

(1) The device may not make response to the input if input pulse width is less than the recommended value.

8 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | DEVICE | UNIT |
|-------------------------------|---|------------|------|
| | | REN (VQFN) | |
| | | 40 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 21.2 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 5.5 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 6.0 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 4.0 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 5.8 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance per GaNFET | 1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

9 Electrical Characteristics

T_J = -40°C to 150°C, V_{GVDD} = 15V, EN = High (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{GVDD} = 15V

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------------------|---|--|-----|-----|-----|------|
| GaN POWER TRANSISTOR | | | | | | |
| R _{DS(ON)} | GaN transistor on resistance | V _{GVDD} = 15V, I _{OUTx} = 1A, T _J = 25°C, | | 205 | 320 | mΩ |
| R _{DS(ON)} | GaN transistor on resistance | V _{GVDD} = 15V, I _{OUTx} = 1A, T _J = 150°C, | | 370 | | mΩ |
| V _{SD} | Third-quadrant mode source-drain voltage | INx = 0V, ISD = 0.1A, T _J = 25°C | | 1.5 | 2.5 | V |
| V _{SD} | Third-quadrant mode source-drain voltage | INx = 0V, ISD = 4A, T _J = 25°C | | 2.8 | | V |
| Q _{RR} | Reverse recovery charge | V _R = 300 V, I _{SD} = 4 A, dI _{SD} /dt = 0.2 A/ns | | | 0 | nC |
| SWITCHING CHARACTERISTICS | | | | | | |
| SR | Phase pin slew rate switching low to high (Rising from 20 % to 80 %) | V _{VM} = 300V, SR setting = 0 | | 4 | | V/ns |
| SR | Phase pin slew rate switching high to low (Falling from 80 % to 20 %) | V _{VM} = 300V, SR setting = 0 | | 4 | | V/ns |
| SR | Phase pin slew rate switching low to high (Rising from 20 % to 80 %) | V _{VM} = 300V, SR setting = 1 | | 10 | | V/ns |
| SR | Phase pin slew rate switching high to low (Falling from 80 % to 20 %) | V _{VM} = 300V, SR setting = 1 | | 10 | | V/ns |
| SR | Phase pin slew rate switching low to high (Rising from 20 % to 80 %) | V _{VM} = 300V, SR setting = 2 | | 20 | | V/ns |
| SR | Phase pin slew rate switching high to low (Falling from 80 % to 20 %) | V _{VM} = 300V, SR setting = 2 | | 20 | | V/ns |

$T_J = -40^{\circ}\text{C}$ to 150°C , $V_{\text{GVDD}} = 15\text{V}$, EN = High (unless otherwise noted). Typical limits apply for $T_A = 25^{\circ}\text{C}$, $V_{\text{GVDD}} = 15\text{V}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|---|--|-----|-----|-----|---------------|
| SR | Phase pin slew rate switching low to high (Rising from 20 % to 80 %) | $V_{\text{VM}} = 300\text{V}$, SR setting = 3 | | 40 | | V/ns |
| SR | Phase pin slew rate switching high to low (Falling from 80 % to 20 %) | $V_{\text{VM}} = 300\text{V}$, SR setting = 3 | | 40 | | V/ns |
| $t_{\text{pd,on}}$ | Propagation delay, turn on | $V_{\text{INHx}}, V_{\text{INLx}} = \text{logic low to high}$, $V_{\text{VM}} = 300\text{V}$, $I_{\text{D}} = 4\text{A}$, SR = 0 | | | 125 | ns |
| $t_{\text{delay,on}}$ | Turn on delay time | $V_{\text{INHx}}, V_{\text{INLx}} = \text{logic low to high}$, $V_{\text{VM}} = 300\text{V}$, $I_{\text{D}} = 4\text{A}$, SR = 0 | | 75 | | ns |
| $t_{\text{pd,off}}$ | Propagation delay, turn off | $V_{\text{INHx}}, V_{\text{INLx}} = \text{logic high to low}$, $V_{\text{VM}} = 300\text{V}$, $I_{\text{D}} = 4\text{A}$, SR = 0 | | | 135 | ns |
| $t_{\text{delay,off}}$ | Turn off delay time | $V_{\text{INHx}}, V_{\text{INLx}} = \text{logic high to low}$, $V_{\text{VM}} = 300\text{V}$, $I_{\text{D}} = 4\text{A}$, SR = 0 | | 75 | | ns |
| t_{DEAD} | Output dead time (high to low) | $V_{\text{VM}} = 300\text{V}$, $I_{\text{OUTx}} = 4\text{A}$, Current going out of phase node (OUTx) SR = 0, 1 | | 40 | | ns |
| t_{DEAD} | Output dead time (high to low) | $V_{\text{VM}} = 300\text{V}$, $I_{\text{OUTx}} = 4\text{A}$, Current going into phase node (OUTx), SR = 0 | | 100 | | ns |
| t_{DEAD} | Output dead time (high to low) | $V_{\text{VM}} = 300\text{V}$, $I_{\text{OUTx}} = 4\text{A}$, Current going into phase node (OUTx), SR = 1 or 2 or 3 | | 100 | | ns |
| t_{DEAD} | Output dead time (low to high) | $V_{\text{VM}} = 300\text{V}$, $I_{\text{OUTx}} = 4\text{A}$, Current going into phase node (OUTx) | | 40 | | ns |
| t_{start} | Start up time | $V_{\text{GVDD}} > V_{\text{GVDD_UV_ON}}$. EN = low to high, INLx = 1, low side GaNFET turns ON | | | 2 | ms |
| t_{off} | Device turn off time - to sleep | $V_{\text{GVDD}} > V_{\text{GVDD_UV_ON}}$. EN = high to low | 40 | | 80 | us |
| $t_{\text{clr_flt}}$ | Time to clear any latched fault using EN | EN = low pulse width | 15 | | 40 | us |
| t_{off} | Device turn off time- gate driver off | $V_{\text{GVDD}} > V_{\text{GVDD_UV_ON}}$. EN = high to low, INLx = 1, low side GaNFET turns OFF | | 80 | | μs |
| GVDD POWER SUPPLY | | | | | | |
| $I_{\text{GVDD,Q}}$ | GVDD operating current, driver enabled, no switching | EN = High, $V_{\text{VM}} = 300\text{V}$, INx = 0 | | 2.3 | | mA |
| $I_{\text{GVDD,3SW}}$ | GVDD average operating current, driver enabled, GaN switching, No load at OUTx pins | EN = High, Fsw = 20kHz, 3-half bridge switching at 50% complimentary PWM, $V_{\text{VM}} = 300\text{V}$, $V_{\text{GVDD}} = 15\text{V}$, SR = 0 | | 3.7 | | mA |
| $V_{\text{GVDD_UV_R}}$ | GVDD undervoltage threshold - rising | GVDD rising | | | 10 | V |
| $V_{\text{GVDD_UV_F}}$ | GVDD undervoltage threshold - falling | GVDD falling | 9 | | | V |
| $V_{\text{GVDD_UV_HYS}}$ | GVDD undervoltage detection hysteresis | GVDD rising to falling threshold | | 500 | | mV |
| $t_{\text{UVLO_GVDD}}$ | GVDD undervoltage deglitch time | | | | 20 | μs |
| BOOTSTRAP POWER SUPPLY | | | | | | |
| $R_{\text{DS_BST}}$ | Bootstrap rectifier on resistance | $V_{\text{GVDD}} = 15\text{V}$, $V_{\text{VM}} = 300\text{V}$ | | | 30 | Ω |
| $I_{\text{LMT_BST}}$ | Bootstrap rectifier current limit | EN = High, $V_{\text{GVDD}} = 15\text{V}$, $V_{\text{VM}} = 300\text{V}$, INLx = High, INHx = Low, $V_{\text{BOOTx}} - V_{\text{OUTx}} = 12\text{V}$ | 150 | | 250 | mA |
| $I_{\text{BST_PK}}$ | Bootstrap rectifier peak transient current | EN = High, $V_{\text{GVDD}} = 15\text{V}$, $V_{\text{VM}} = 300\text{V}$, INLx = High, INHx = Low, $V_{\text{BOOTx}} - V_{\text{OUTx}} = 0\text{V}$ | | 350 | | mA |
| $I_{\text{BST_Q}}$ | Bootstrap quiescent current | EN = High, INHx = Low, INLx = Low, $V_{\text{GVDD}} = 15\text{V}$, $V_{\text{BOOTx}} - V_{\text{OUTx}} = 12\text{V}$ | | 100 | 145 | μA |
| $I_{\text{BST_Q}}$ | Bootstrap quiescent current | EN = High, INHx = High, INLx = Low, $V_{\text{GVDD}} = 15\text{V}$, $V_{\text{BOOTx}} - V_{\text{OUTx}} = 12\text{V}$ | | 350 | | μA |

DRV7308

SLVSGJ9A – MAY 2024 – REVISED OCTOBER 2025

 $T_J = -40^{\circ}\text{C}$ to 150°C , $V_{\text{GVDD}} = 15\text{V}$, EN = High (unless otherwise noted). Typical limits apply for $T_A = 25^{\circ}\text{C}$, $V_{\text{GVDD}} = 15\text{V}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|--|------|-----------|------|--------------------|
| $V_{\text{BST_UV}}$ | Bootstrap supply undervoltage | BOOTx rising | | | 9 | V |
| $V_{\text{BST_UV}}$ | Bootstrap supply undervoltage | BOOTx falling | 8 | | | V |
| $V_{\text{BST_UV_HYS}}$ | Bootstrap supply undervoltage hysteresis | | | 500 | | mV |
| $t_{\text{BST_UV}}$ | Bootstrap supply undervoltage deglitch time | | | | 20 | μs |
| LOGIC-LEVEL INPUTS (EN, INHx, INLx, BRAKE) | | | | | | |
| V_{IL} | Input logic low voltage | INHx, INLx, BRAKE, EN | | | 0.8 | V |
| V_{IH} | Input logic high voltage | INHx, INLx, BRAKE, EN | 2.2 | | | V |
| V_{HYS} | Input logic hysteresis | INHx, INLx, BRAKE, EN | 300 | 450 | 650 | mV |
| I_{IL} | Input logic low current (INHx, INLx, BRAKE, EN) | $V_I = 0\text{V}$ | -1 | | 1 | μA |
| I_{IL} | Input logic low current (BRAKE, EN) | $V_I = 0\text{V}$ | -1 | | 1 | μA |
| R_{PD} | Input pulldown resistance | INHx, INLx, EN | 70 | 100 | 130 | k Ω |
| R_{PD} | Input pulldown resistance | BRAKE | 15 | 20 | 25 | k Ω |
| t_{deg} | Input logic deglitch time | INHx, INLx | 25 | | 50 | ns |
| t_{deg} | Input logic deglitch time | EN | | 80 | | μs |
| t_{deg} | Input logic deglitch time | BRAKE | 1200 | | 2000 | ns |
| MULTI-LEVEL INPUT (SR) | | | | | | |
| R_{L1} | SR setting = 0 | Tied to GND | 0 | | 1 | k Ω |
| R_{L2} | SR setting = 1 | Tied to GVDD | 0 | | 1 | k Ω |
| R_{L3} | SR setting = 2 | R tied to GND (R = 5 k Ω to 15 k Ω) | 5 | | 15 | k Ω |
| R_{L4} | SR setting = 3 | R tied to GND (R = 40 k Ω to 100 k Ω) | 40 | | 100 | k Ω |
| OPEN-DRAIN OUTPUTS (nFAULT) | | | | | | |
| V_{OL} | Output logic low voltage | $I_{\text{OD}} = 5\text{mA}$ | | | 0.4 | V |
| I_{OH} | Output logic high current | $V_{\text{OD}} = 5\text{V}$ | -1 | | 1 | μA |
| C_{OD} | Output capacitance | | | | 30 | pF |
| GaN PREDRIVER PROTECTION | | | | | | |
| $I_{\text{OCP_GaN}}$ | Low-side GaN FET overcurrent detection threshold | $V_{\text{GVDD}} = 15\text{V}$, $V_{\text{VM}} = 300\text{V}$, $T_J = 25^{\circ}\text{C}$ | 7.5 | | 24 | A |
| $I_{\text{OCP_GaN}}$ | Low-side GaN FET overcurrent detection threshold | $V_{\text{GVDD}} = 15\text{V}$, $V_{\text{VM}} = 300\text{V}$, $T_J = 125^{\circ}\text{C}$ | 5 | | | A |
| $t_{\text{OCP_GaN_BT}}$ | Blanking time (including deglitch) | $V_{\text{GVDD}} = 15\text{V}$, $V_{\text{VM}} = 300\text{V}$ | | 150 | | ns |
| $t_{\text{OCP_GaN_PD}}$ | Propagation delay (to FET turn off) | $V_{\text{GVDD}} = 15\text{V}$, $V_{\text{VM}} = 300\text{V}$ | | 50 | | ns |
| $T_{\text{SD_RISE}}$ | Thermal shutdown rising | Die temperature (T_J) | 145 | 165 | 185 | $^{\circ}\text{C}$ |
| $T_{\text{SD_FALL}}$ | Thermal shutdown falling | Die temperature (T_J) | 125 | 145 | 165 | $^{\circ}\text{C}$ |
| $T_{\text{SD_HYST}}$ | Thermal shutdown hysteresis | Die temperature (T_J) | 13 | 20 | | $^{\circ}\text{C}$ |
| CURRENT LIMIT COMPARATOR (ILIMIT) | | | | | | |
| I_{b} | Input bias current (ILIMIT) | $V_{\text{ILIMIT}} = 0.5\text{V}$ | | | 1 | μA |
| V_{off} | ILIMIT comparator input voltage offset | $V_{\text{ILIMIT}} = 1.0\text{V}$ | | ± 2.5 | | mV |
| $V_{\text{ILIMIT_DIS}}$ | Minimum ILIMIT voltage to disable ILIMIT OCP | | 2.2 | | 2.6 | V |
| V_{ILIMIT} | Operational voltage range at ILIMIT | | | | 2 | V |
| t_{blank} | Over current detection blanking on all SLx inputs, from any INHx/INLx turn on/off | | 400 | | 620 | ns |
| t_{deglitch} | Over current detection de-glitch time | | 190 | | 330 | ns |

$T_J = -40^{\circ}\text{C}$ to 150°C , $V_{\text{GVDD}} = 15\text{V}$, EN = High (unless otherwise noted). Typical limits apply for $T_A = 25^{\circ}\text{C}$, $V_{\text{GVDD}} = 15\text{V}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|--|--|------|-----------|-----|--------------------------------|
| t_{filter} | ILIMIT comparator input RC filter time (SLx) | $V_{\text{SLx}} = 0$ to 1V step, $V_{\text{ILIMIT}} = 0.63\text{V}$ | 250 | | 450 | ns |
| t_{filter} | ILIMIT reference voltage input RC filter time (ILIMIT) | $V_{\text{ILIMIT}} = 1$ to 0V step, $V_{\text{SLx}} = 0.37\text{V}$ | 600 | 1000 | | ns |
| $t_{\text{pd_OFF}}$ | Propagation delay time from ILIMIT over current detection to all GaN FETs turn off | $V_{\text{ILIMIT}} = 0.63\text{V}$, $V_{\text{SLx}} = 0$ to 1V step, $\text{INx} = \text{constant}$ | | | 1.2 | μs |
| $t_{\text{pd_FAULT}}$ | Propagation delay time from ILIMIT over current detection to nFAULT pin report | $V_{\text{ILIMIT}} = 0.63\text{V}$, $V_{\text{SLx}} = 0$ to 1V step, $\text{INx} = \text{constant}$ | | | 1 | μs |
| OPERATIONAL AMPLIFIER | | | | | | |
| V_{LINEAR} | Output voltage swing | $R_L = 10\text{k}$ to GND | 0.02 | | 4.9 | V |
| GBW | Gain bandwidth product | $R_L = 10\text{k}$, $G = +1$ | | 11 | | MHz |
| $V_{\text{SR_opamp}}$ | Output voltage slew rate | $R_L = 10\text{k}$, $G = +1$ | | 26 | | $\text{V}/\mu\text{s}$ |
| t_{set} | Settling time to $\pm 1\%$ | 2-V step, $G = +1$, $C_L = 130\text{ pF}$, $R_L = 10\text{k}$ | | 0.4 | | μs |
| A_{OL} | Open-loop voltage gain | $0.04\text{ V} < V_{\text{AMPOUT}} < 4.8\text{ V}$, $R_L = 10\text{ k}\Omega$ to GND | | 106 | | dB |
| ϕ_m | Phase margin | $G = +1$, $R_L = 10\text{k}$ | | 60 | | $^{\circ}$ |
| V_{COM} | Common mode input range | | 0 | | 5 | V |
| V_{OFF} | Input offset voltage error | $T_A = -40^{\circ}\text{C}$ to 125°C | | ± 1 | | mV |
| V_{DRIFT} | Drift offset | $T_A = -40^{\circ}\text{C}$ to 125°C | | ± 2 | | $\mu\text{V}/^{\circ}\text{C}$ |
| I_{bias} | Input bias current | $V_{\text{AMPIN-}} = V_{\text{AMPIN+}} = 2.5\text{V}$ | | ± 100 | | nA |
| $I_{\text{bias_off}}$ | Input bias offset current | $V_{\text{AMPIN-}} = V_{\text{AMPIN+}} = 2.5\text{V}$ | | ± 10 | | nA |
| CMRR | Common mode rejection ratio | $-0.1\text{ V} < V_{\text{CM}} < 5\text{ V}$, $T_A = -40^{\circ}\text{C}$ to 125°C | | 96 | | dB |
| $I_{\text{SC_opamp}}$ | Short-circuit current | | | ± 20 | | mA |
| Z_o | Open-loop output impedance | $f = 5\text{ MHz}$ | | 250 | | Ω |
| C_L | Capacitive load drive | | | | 130 | pF |
| TEMPERATURE SENSOR | | | | | | |
| V_T | Temperature sense element output (VTEMP) voltage | $T_A = 25^{\circ}\text{C}$ | | 1.98 | | V |
| R_T | Minimum load resistance on VTEMP pin | test condition of V_T | 90 | | | $\text{k}\Omega$ |
| C_T | Maximum load capacitance at VTEMP pin | test condition of V_T | | | 130 | pF |

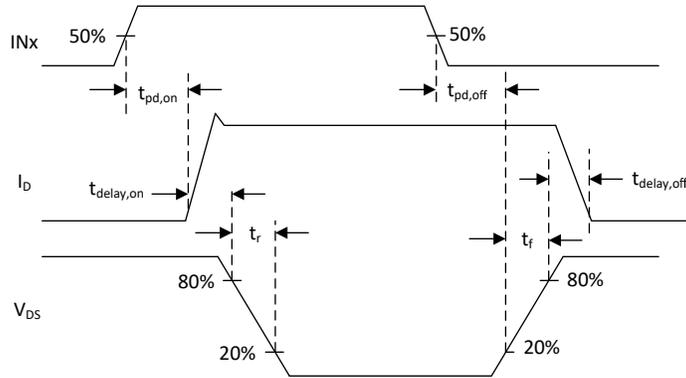


Figure 10-1. DRV7308 Turn On and Turn Off Switching Characteristics

11 Typical Characteristics

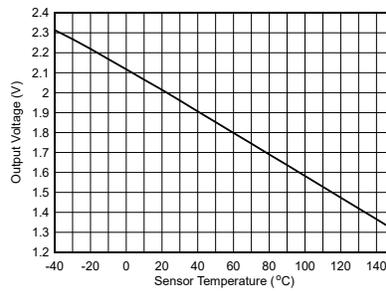


Figure 11-1. Temperature Sensor Output Across Sensor Temperature

12 Detailed Description

12.1 Overview

The DRV7308 is a three-phase IPM, with three integrated half-H-bridge 205m Ω , 650V e-mode Gallium-Nitride (GaN) for driving three-phase BLDC/PMSM motors up to 450V DC rails. The device applications include field-oriented control (FOC), sinusoidal current control, and trapezoidal current control of BLDC motors. The device integrates pre-drivers for all GaN FETs with slew rate control of phase node voltages. The low R_{DS_ON} , slew rate control, zero reverse recovery, and low output capacitance help achieve more than 99% efficiency for a 3-phase modulated, FOC driven, 250W motor drive application, eliminating the need for heat sink.

The device integrates a suite of protections including overcurrent limit, overtemperature protection, overcurrent protection for low-side GaN FETs, undervoltage protection for the GVDD and bootstrap power supplies, and adaptive dead time insertion to avoid shoot through conditions.

The device integrates a bootstrap rectifier with an integrated GaN FET and a transient current limit, which eliminates the need for an external boot diode. The DRV7308 brings out all three low-side source pins of the GaN FETs to support 3-, 2-, or 1-shunt current sensing. The device integrates an 11MHz, 15V/ μ s operational amplifier for single shunt current sensing in FOC and trapezoidal control of BLDC motors.

The low dead time helps achieve ultra quiet operations in BLDC/PMSM motors. The low propagation delay helps achieve lower distortion and accurate average current sensing.

The DRV7308 is available in a VQFN 12mm x 12mm package.

12.2 Functional Block Diagram

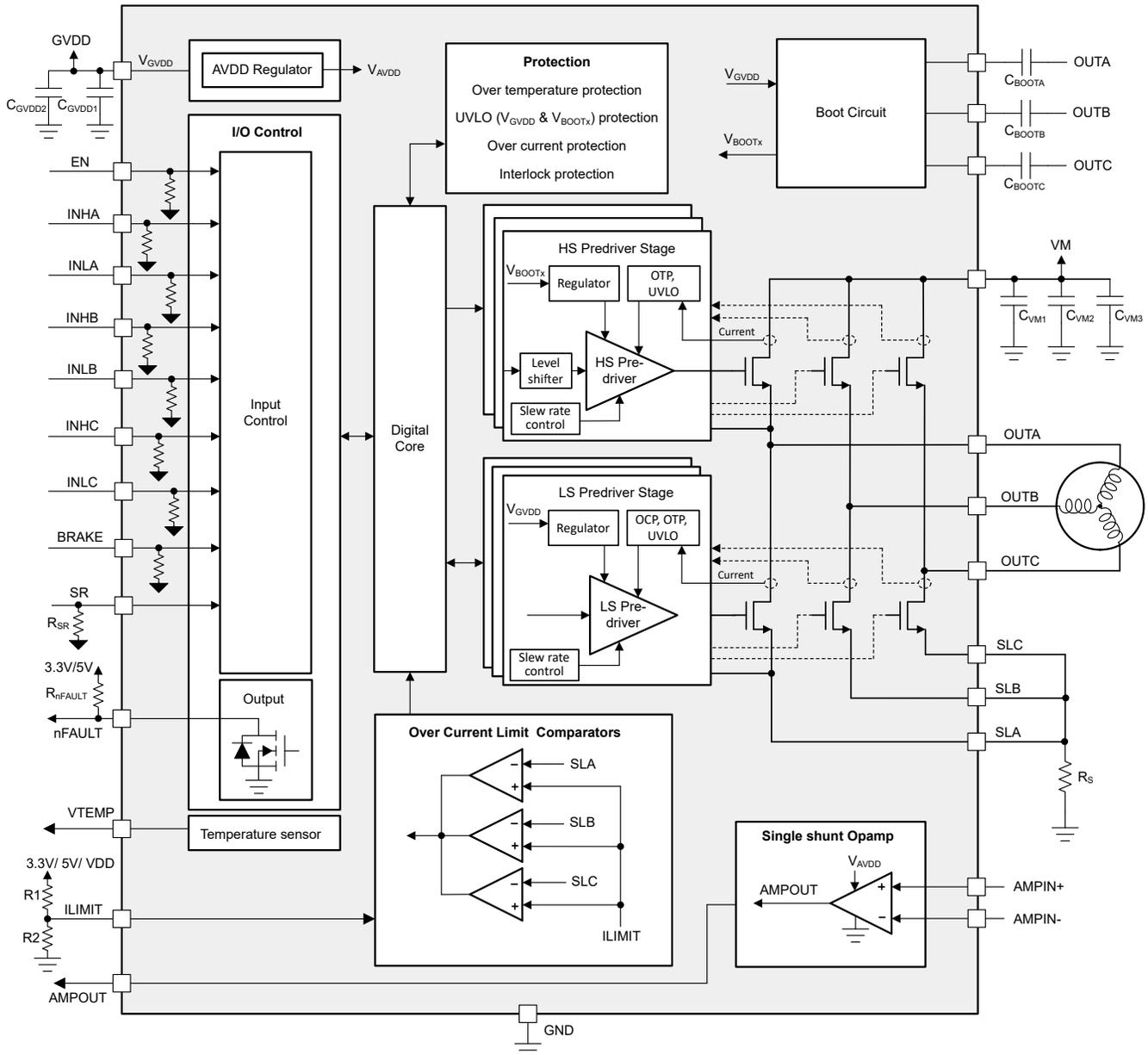


Figure 12-1. DRV7308 Block Diagram

12.3 Feature Description

12.3.1 Output Stage

The DRV7308 device consists of integrated 205mΩ (one GaN FET on-state resistance) enhancement mode GaN (EGaN) FETs connected in a three-phase bridge configuration. The device integrates a pre-driver for low-side and high-side GaN FETs using an integrated bootstrap controller and rectifier using a low voltage external power supply at GVDD. An appropriately used external bootstrap capacitor offers 100% duty cycle support for a defined time.

12.3.2 Input Control Logic

The DRV7308 controls the state of the GaN FET based on the PWM input signals at the INHx and INLx pins. The device uses the BRAKE signal to apply brake to motor drive. A logic high at the BRAKE signal overrides the INHx and INLx pins and turns on all low side GaN transistors. The device enters shutoff mode (all the gate drivers and GaN FETs in off state) and ignores the status of the INHx, INLx, and BRAKE pins when a logic low on the EN pin occurs. A 20-40µs logic low pulse at the EN pin resets the device from OCP and OTP faults. The truth table for the input control logic is shown in [Table 12-1](#).

Table 12-1. Input Control Logic

| EN | BRAKE | INHx | INLx | HIGH SIDE GAN FET | LOW SIDE GAN FET | DESCRIPTION |
|----|-------|------|------|-------------------|------------------|--|
| 0 | X | X | X | OFF | OFF | Device in shutdown and all outputs in Hi-Z |
| 1 | 1 | X | X | OFF | ON | BRAKE. All low side GaN FETs are ON and all high-side GaN FETs are OFF |
| 1 | 0 | 1 | 1 | OFF | OFF | OUTx in Hi-Z |
| 1 | 0 | 0 | 0 | OFF | OFF | OUTx in Hi-Z |
| 1 | 0 | 1 | 0 | ON | OFF | OUTx connected to VM |
| 1 | 0 | 0 | 1 | OFF | ON | OUTx connected to SLx node |

12.3.3 ENABLE (EN) Pin Function

When the EN pin is low, the device goes to a low-power sleep mode. In sleep mode, all GaNFETs are turned off—the GaN pre-drivers, integrated op amp, temperature sensor, GaN OCP, digital core LDO, and oscillators are all turned off. The t_{off} time must elapse after a falling edge on the EN pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the EN pin is pulled high. The t_{start} time must elapse before the device is ready for inputs.

Note

During power up and power down of the device through the EN pin, the nFAULT pin is held low as the internal regulators are enabled or disabled. After the regulators have enabled or disabled, the nFAULT pin is automatically released.

12.3.4 Temperature Sensor Output (VTEMP)

DRV7308 incorporates a temperature sensor that senses the device temperature. The output of the temperature sensor is an analog voltage that varies across temperature.

12.3.5 Brake Function

The BRAKE pin provides a means to turn on all the low-side GaNFETs, independent of INHx and INLx pin status. The brake pin has an internal pull down. Connect the BRAKE pin to GND externally if not used. A logic high on the BRAKE pin places the device into brake by turning on all the low-side GaNFETs.

Note

Use caution while applying the BRAKE high command, as this can cause very high current driven by the motor back EMF. During BRAKE operation, the maximum current through the GaNFET must be a value that is within the operating limits of the GaNFET current and junction temperature.

12.3.6 Slew Rate Control (SR)

The DRV7308 can optionally control the slew rate of the voltage rise and fall at the OUTx pins through the configuration of the SR pin. The user can set slew rates of 5V/ns, 10V/ns, 20V/ns, or 40V/ns by configuring the SR pin. The slew rate is controlled by adjusting the gate current of GaNFETs.

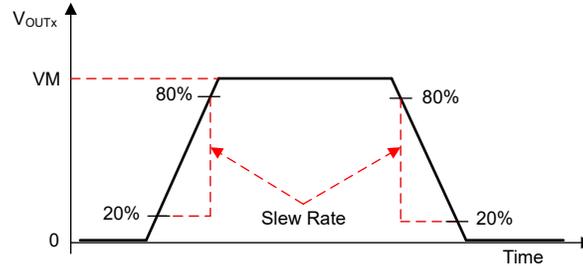


Figure 12-2. DRV7308 Slew Rate Control

Note

At higher slew rates of 20V/ns and 40V/ns, TI recommends adding a capacitor across the shunt resistors that have an RC time constant of 50ns.

12.3.7 Dead Time

The device is fully protected for any cross conduction of GaNFETs. In half-bridge configuration, the operation of the high-side and low-side GaNFETs are controlled to avoid any shoot-through currents by inserting dead time (t_{DEAD}). This process is implemented by using an adaptive dead time circuit that senses the gate-source voltage (VGS) of the low-side GaNFET and the phase node (OUTx) voltage of the same half-bridge.

12.3.8 Current Limit Functionality (ILIMIT)

The DRV7308 incorporates a current limit functionality that monitors SLx voltages. DRV7308 has three integrated comparators, each monitoring voltage at SLA, SLB, and SLC pins separately. The reference voltage of all three comparators is fed externally using the ILIMIT pin. A voltage less than 2V at the ILIMIT pin enables the current limit circuitry and when the SLx voltage goes beyond the ILIMIT pin voltage, the device turns off all GaNFETs for a time t_{FCLR} . The GaNFETs turn on again after t_{FCLR} time elapses, depending on the status of input control signals. The ILIMIT functionality can be disabled by pulling up the ILIMIT pin voltage to more than V_{ILIMIT_DIS} .

The overcurrent comparator has a blanking time of t_{blank} on every edge of INHx and INLx. The comparator also has a deglitch time of $t_{deglitch}$, when the comparator output toggles from low to high.

Note

TI recommends an ILIMIT voltage of more than 0.2V to eliminate false trips due to noise. Use system-level design considerations by selecting an appropriate voltage at ILIMIT to eliminate any noise impact and select the shunt resistor value at SLx pins accordingly.

12.3.9 Pin Diagrams

This section presents the I/O structure of all digital input and output pins.

12.3.9.1 Four-Level Input Pin

Figure 12-3 shows the structure of the four-level SR pin.

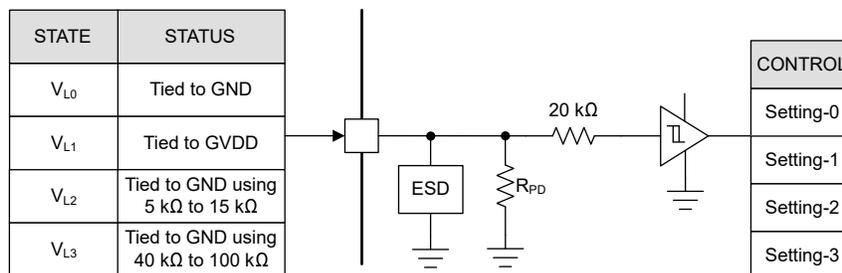


Figure 12-3. Four-Level Input Pin

12.3.9.2 Open-Drain Pin

Figure 12-4 shows the structure of the open-drain output pin, nFAULT in open-drain mode. The open-drain output requires an external pull-up resistor to function properly.

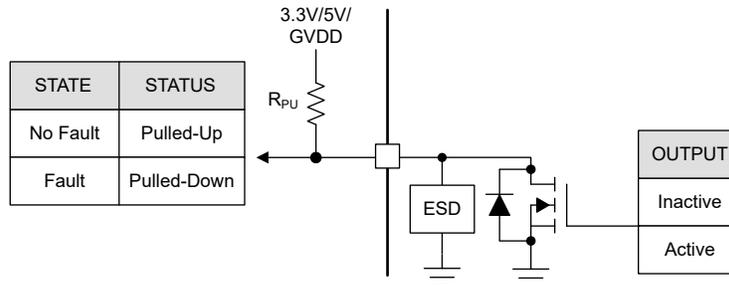


Figure 12-4. Open-Drain Pin Structure

12.3.9.3 Logic-Level Input Pin (Internal Pulldown)

Figure 12-5 shows the input structure for the logic level pins EN, INHx, INLx, ILIMIT, BRAKE. The input can be with a voltage or external resistor.

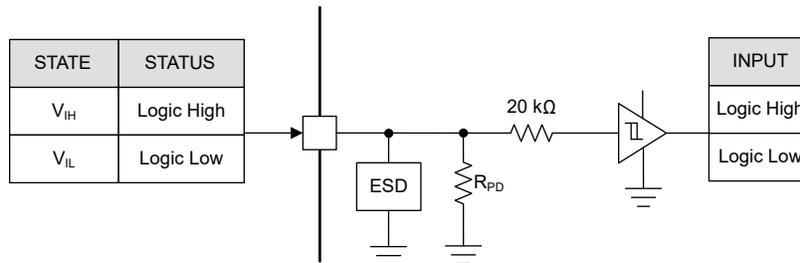


Figure 12-5. Logic-Level Input Pin Structure

12.4 Protections

The DRV7308 integrates GaN FET overcurrent protection (GaN_OCP), overtemperature shutdown (OTSD), GVDD and bootstrap supply undervoltage protection (GVDD_UVLO and VBOOT_UVLO), and current limit (ILIMIT). Table 12-2 summarizes various faults in details.

Table 12-2. Fault Action and Response

| FAULT | CONDITION | REPORT | GAN BRIDGE | RECOVERY |
|---|---|--------|---|--|
| GaN overcurrent protection (GaN_OCP) ⁽¹⁾ | Low-side GaN FET current > I_{OCP_GaN} | nFAULT | All GaN pre-drivers turn off resulting Hi-Z (all three phases) | Latched. 20μs to 40μs toggling pulse on EN pin or GVDD power recycling |
| SLx overcurrent limit (ILIMIT) | $V_{SLx} > V_{ILIMIT}$ | nFAULT | All GaN pre-drivers turn off resulting Hi-Z (all three phases) | Retry ⁽²⁾ . After a fault clear time > t_{F_CLR} |
| GVDD undervoltage | $V_{GVDD} < V_{GVDD_UV}$ | nFAULT | All GaN pre-drivers turn off resulting Hi-Z (all three phases) | Automatic: $V_{GVDD} > V_{GVDD_UVLO}$ |
| Boot supply undervoltage (voltage between BOOTx and OUTx pin) | $V_{BOOTx} < V_{BST_UV}$ | - | The impacted high-side GaN pre-drivers turn off. All other GaNFETs continue to operate. | Automatic: $V_{BOOTx} > V_{BST_UV}$ |
| Thermal shutdown (OTSD) | $T_J > T_{SD}$, for low-side GaNFET | nFAULT | All GaN pre-drivers turn off resulting Hi-Z (all three phases) | Automatic $T_J < T_{SD}$ |
| | $T_J > T_{SD}$, for high-side GaNFET | | | Latched. 20μs to 40μs toggling pulse on EN pin or GVDD power recycling |

(1) Over current detection for low-side GaN FETs only.

(2) PWM inputs (INHx, INLx) must be low before the falling edge of nFAULT.

Note

The GaN over current protection (GaN OCP) is available for low-side GaN FETs.

WARNING

The recovery condition of SL over current limit (ILIMIT) is valid if the PWM inputs (INHx, INLx) are low before the falling edge of nFAULT.

12.4.1 GVDD Undervoltage Lockout

If at any time the voltage on the GVDD pin falls lower than the V_{GVDD_UV} threshold, all integrated GaNFETs are turned off by turning off the GaN FET pre-drivers. Normal operation starts again when the GVDD_UV condition clears. The GVDD_UV is reported by driving the nFAULT pin low.

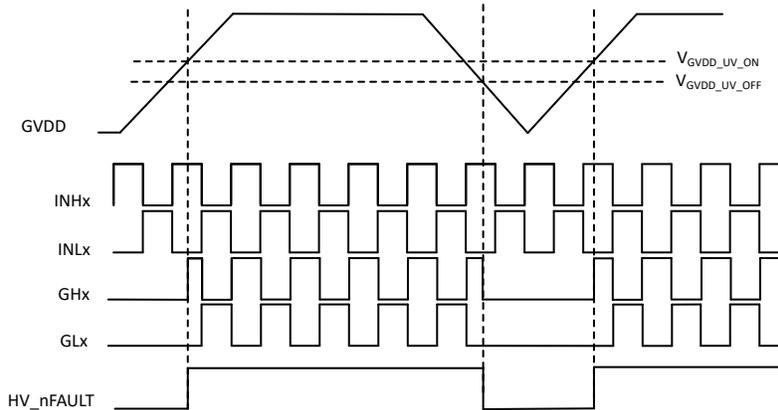


Figure 12-6. GVDD Under voltage Lockout

12.4.2 Bootstrap Undervoltage Lockout

If at any time the voltage across the bootstrap capacitor (BOOTx to OUTx voltage) pin falls lower than the V_{BST_UV} threshold, the corresponding high-side GaN FET is turned off by turning off the high-side pre-driver. All the other GaN FETs continue to work as commanded by the INx pin. Normal operation starts again at the next rising edge of INHx pulse after the BST_UV condition clears. The BOOTx undervoltage is not reported on nFAULT pin.

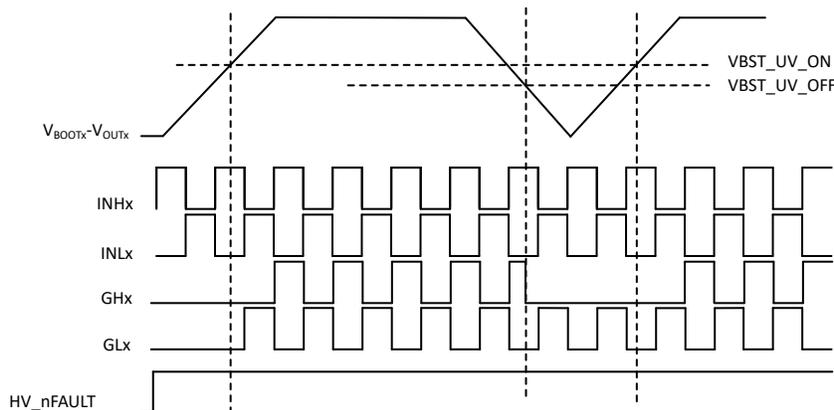


Figure 12-7. Bootstrap Undervoltage Lockout

12.4.3 Current Limit Protection

The DRV7308 integrates three comparators to protect the device, and external motor load, due to overload scenarios. DRV7308 has three integrated comparators, each monitoring voltage at SLA, SLB, and SLC pins

separately. A voltage less than 2V at the ILIMIT pin enables the current limit circuitry and when the SLx voltage goes beyond the ILIMIT pin voltage, the device turns off all GaN FETs for a time t_{F_CLR} . The GaNFETs turn on again after t_{F_CLR} time elapses, depending on the status of input control signals. The current limit is reported by driving the nFAULT pin low.

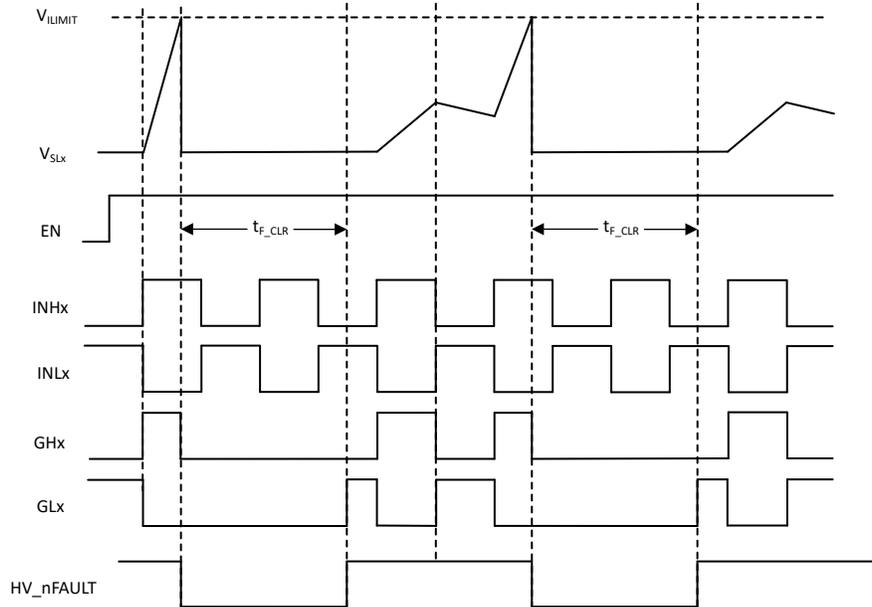


Figure 12-8. Current Limit Operation

12.4.4 GaNFET Overcurrent Protection

The DRV7308 integrates overcurrent protection for each low-side GaN FET by monitoring the VDS of the GaN FETs. If at any time, the GaN FET current goes more than I_{OCP_GaN} , all of the integrated GaNFETs are turned off by turning off the GaN FET pre-driver, and latched until cleared through a 20 μ s to 40 μ s toggling pulse on the EN pin or by a GVDD power recycling. The overcurrent event is reported by driving the nFAULT pin low.

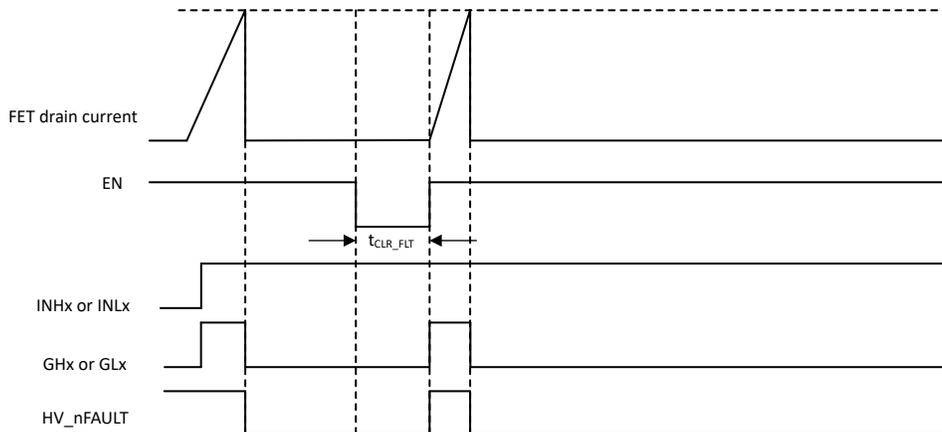


Figure 12-9. GaNFET Over current Protection

12.4.5 Thermal Shutdown (OTS)

If the die temperature near GaN FET exceeds the trip point of the thermal shutdown limit (T_{OTSD}), all the GaNFETs are disabled, and the nFAULT pin is driven low. If OTSD event is detected due to high-side GaN FET temperature rise, the normal operation starts again (driver operation and the nFAULT pin is released) when the overtemperature condition clears and the fault is cleared through a 20 μ s to 40 μ s toggling pulse on the EN pin

or by GVDD power recycling. If OTSD event is detected due to low-side GaN FET temperature rise, the normal operation starts again when the over temperature condition clears.

13 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

13.1 Application Information

The DRV7308 is primarily used in applications for three-phase brushless DC motor control. The design procedures in the highlight how to use and configure the DRV7308 device.

13.2 Typical Application

13.2.1 Application

Figure 13-1 shows a typical 3-phase motor drive application diagram of DRV7308.

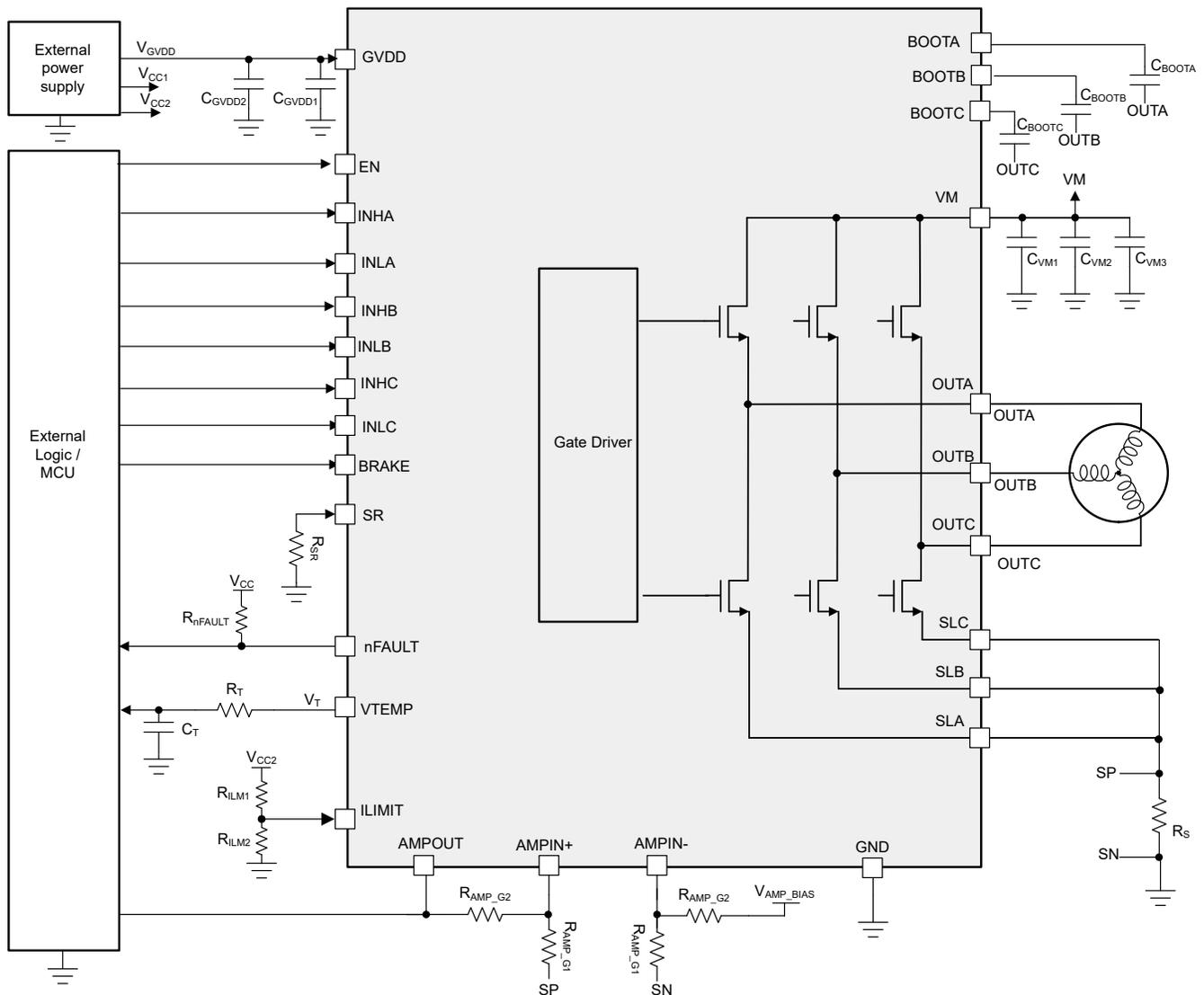


Figure 13-1. DRV7308 Typical Application Schematic

13.2.1.1 Application Information

Table 13-1 lists the recommended values of the external components for the driver.

Table 13-1. DRV7308 External Components

| COMPONENTS | PIN1 | PIN2 | RECOMMENDED |
|-----------------------|---------------------|-----------------------|--|
| C _{VM1} | VM | GND | X5R or X7R, 0.1μF, VM-rated capacitor |
| C _{VM2} | VM | GND | X5R or X7R, 0.1μF, VM-rated capacitor (optional) |
| C _{VM3} | VM | GND | ≥ 10μF, VM-rated capacitor |
| C _{GVDD1} | GVDD | GND | X5R or X7R, 0.1μF, GVDD-rated capacitor |
| C _{GVDD2} | GVDD | GND | ≥ 10μF, GVDD-rated capacitor |
| C _{BOOTA} | BOOTA | OUTA | X5R or X7R, 1μF to 220μF, GVDD-rated capacitor |
| C _{BOOTB} | BOOTB | OUTB | X5R or X7R, 1μF to 220μF, GVDD-rated capacitor |
| C _{BOOTC} | BOOTC | OUTC | X5R or X7R, 1μF to 220μF, GVDD-rated capacitor |
| R _{SR} | SR | GND | Resistor to determine slew rate setting |
| R _{nFAULT} | nFAULT | 3.3V / 5.5V / GVDD | 5.1kΩ, Pullup resistor |
| R _{ILM1} | ILIMIT | 3.3V / 5.5V / GVDD | Based on required ILIMIT threshold |
| R _{ILM2} | ILIMIT | GND | Based on required ILIMIT threshold |
| R _{VTEMP} | VTEMP | system | Optional. VTEMP output filter resistor. 100Ω, and application dependent. |
| C _{VTEMP} | VTEMP | GND | Optional. VTEMP output filter capacitor < 130pF. |
| R _{AMP_G2} | AMPOUT | AMPIN+ | Amplifier Gain Resistor 2. Application dependent. |
| R _{AMP_G1} | AMPIN+ | V _{AMP_REF} | Amplifier Gain Resistor 1. Application dependent. |
| R _S | SLx (SP) | GND(SN) | Low-side Rshunt resistor to measure motor phase current (I _{LS_PHASE}). The expected current sense output voltage = $R_S \times I_{LS_PHASE} \times R_{AMP_G2}/R_{AMP_G1} + V_{AMP_REF}$ |
| V _{CC1} | system | GND | System I/O reference voltage. 3.3V, 5V, or GVDD |
| V _{CC2} | system | GND | System I/O reference voltage. 3.3V, 5V. VCC2 needs to be separated from VCC1 only if VCC1 is higher than 5V. |
| V _{AMP_bias} | R _{AMP_G2} | system | Optional. System Current Sense measurement bias voltage |

Note

TI recommends connecting pull up on nFAULT pin even if not used.

13.2.2 Application Curves

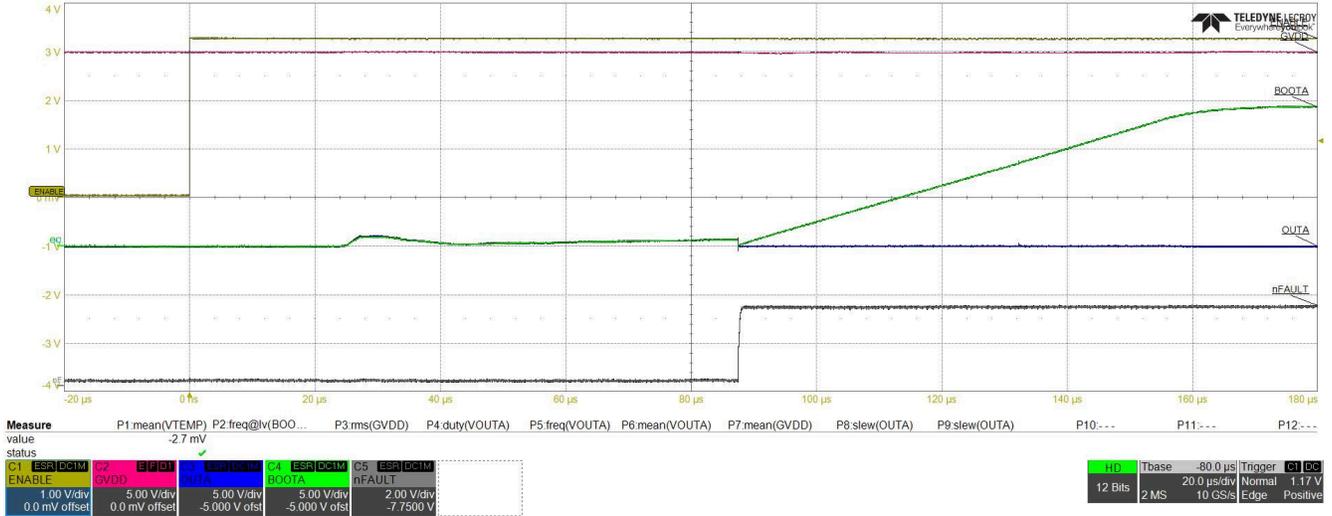


Figure 13-2. Device power up (EN pin low to high)

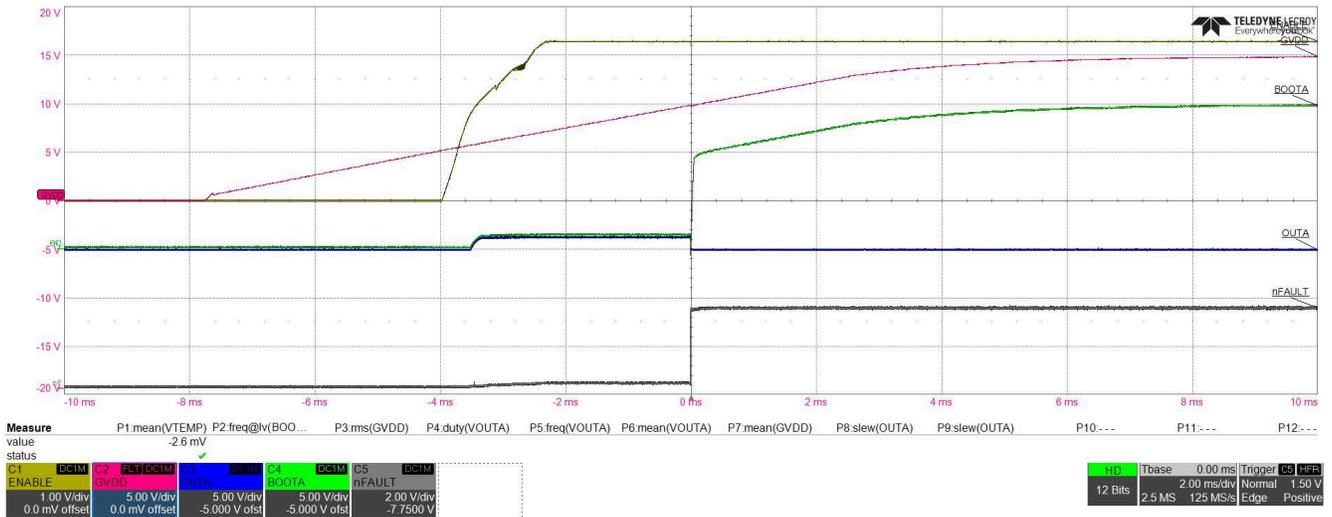


Figure 13-3. Device power up (GVDD start up)

DRV7308

SLVSGJ9A – MAY 2024 – REVISED OCTOBER 2025

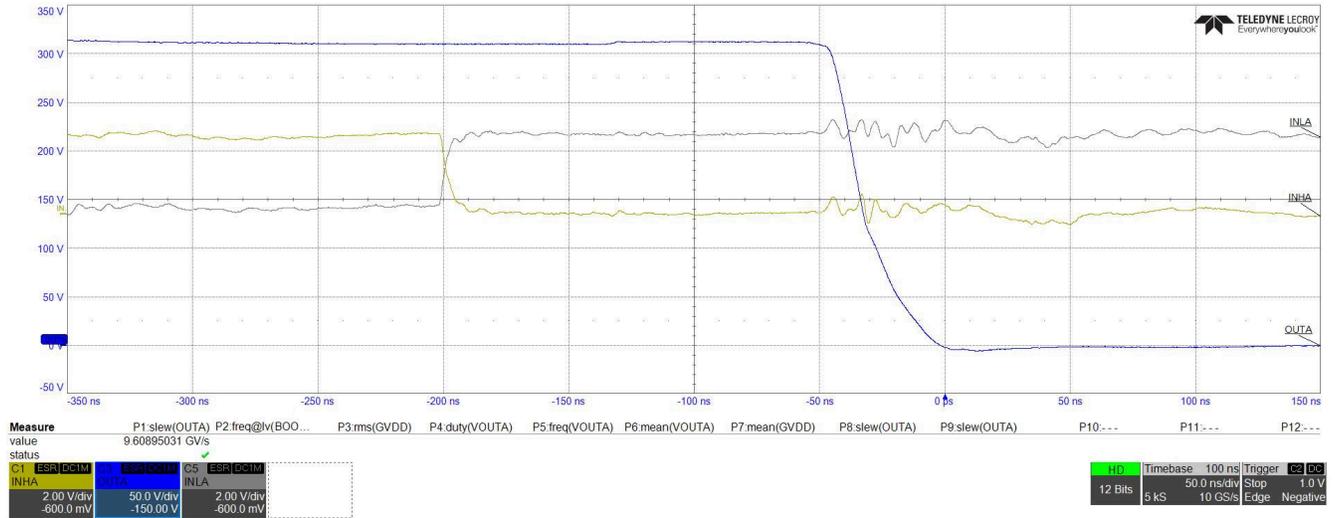


Figure 13-4. Motor phase node OUTA switching - falling edge (phase current from motor load to device)

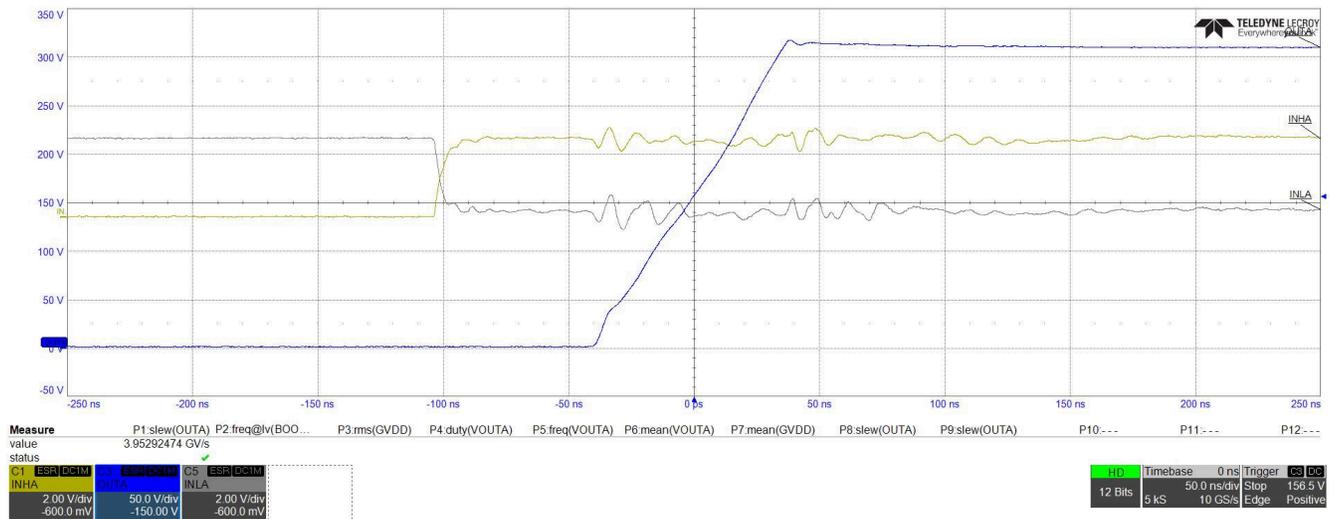


Figure 13-5. Motor phase node OUTA switching - rising edge (phase current from motor load to device)

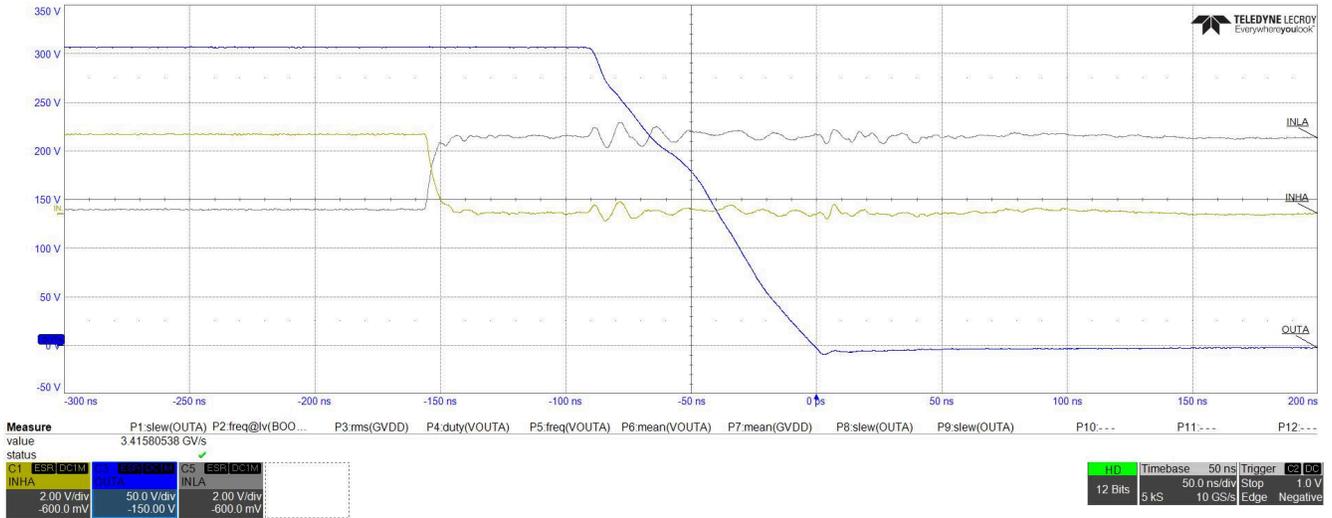


Figure 13-6. Motor phase node OUTA switching - falling edge (phase current from device to motor load)

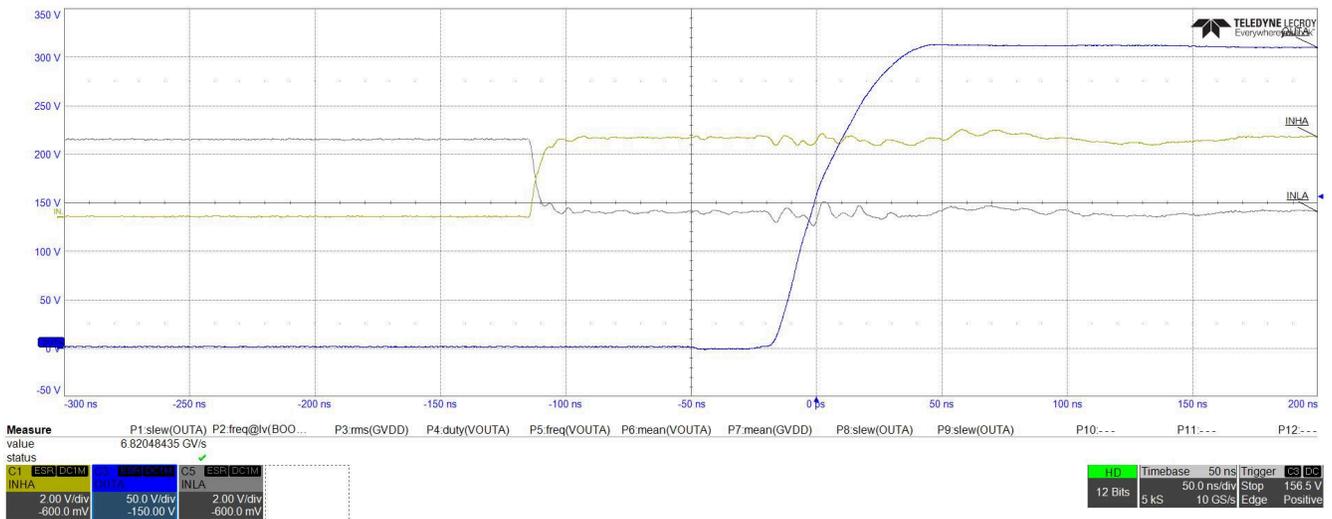


Figure 13-7. Motor phase node OUTA switching -rising edge (phase current from device to motor load)

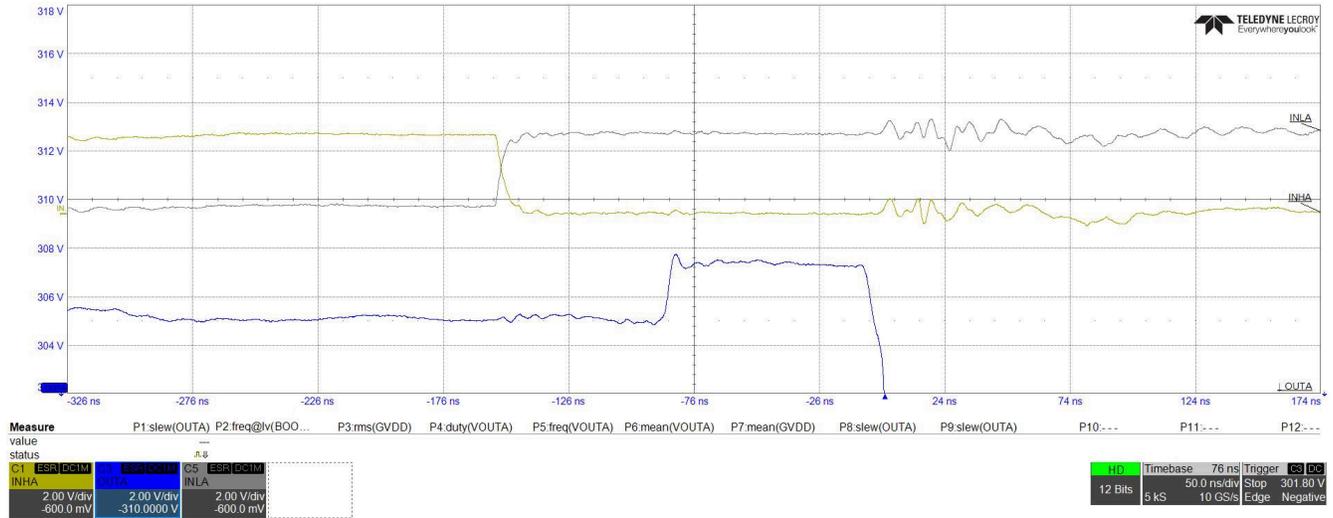


Figure 13-8. Motor phase node OUTA switching - High-side GaN FET Third Quadrant operation (phase current from motor load to device)

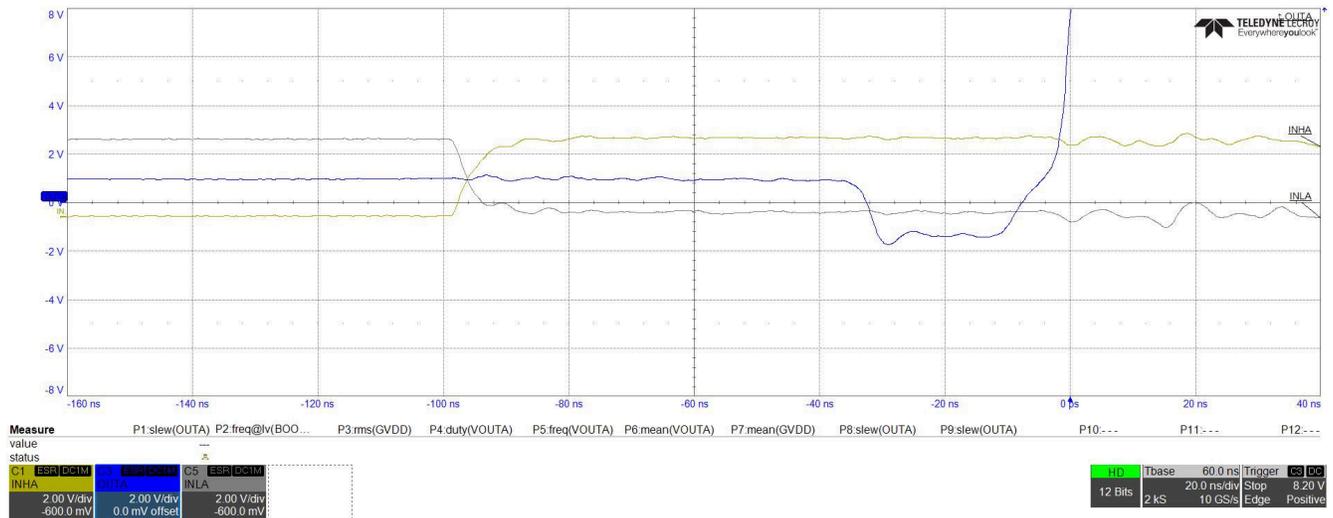


Figure 13-9. Motor phase node OUTA switching - Low-side GaN FET Third Quadrant operation (phase current from device to motor load)

14 Layout

14.1 Layout Guidelines

The bulk capacitor must be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths must be as wide as possible and numerous vias must be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors such as the GVDD decoupling capacitor, high frequency capacitor on VM pin to GND, and the bootstrap capacitors must be placed close to device pins.

To minimize the power loop area, place the shunt resistors close to the device SLx pins and use copper polygon on the end of the shunt resistor, and return the current path to the decoupling capacitor on the VM pin with a wider trace on the top layer, or through a copper polygon on the bottom layer with a sufficient number of stitching vias.

To improve thermal performance, maximize the copper planes on OUTx and GND nets. To maximize the thermal performance, use multiple stitching vias on the OUTx pads and GND pads and use larger copper planes on the top and bottom layers, as shown in the [Figure 14-1](#).

The decoupling capacitor on the VM pin can be connected to any one side VM pin or to both the pins. The VM pins are internally shorted in the device and there is no need to short externally on the PCB.

14.2 Layout Example

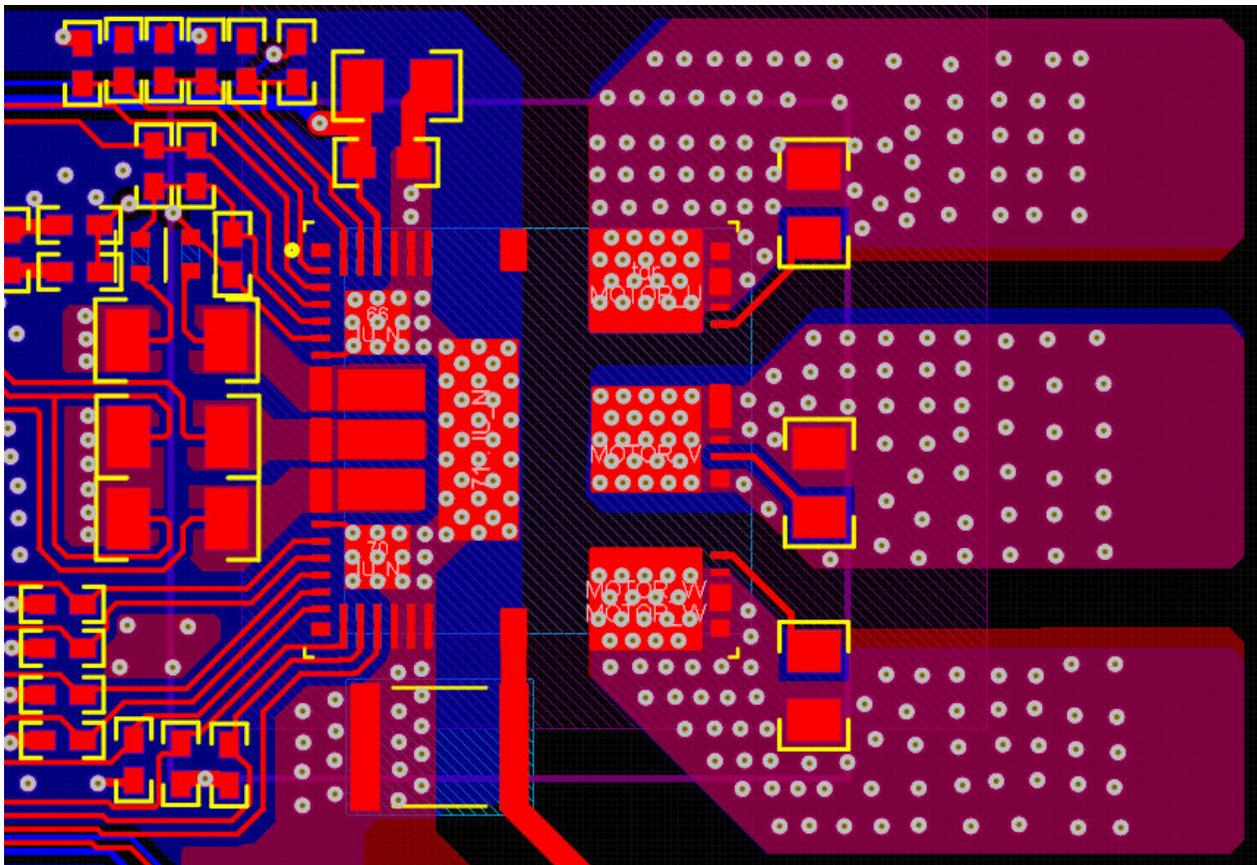


Figure 14-1. Recommended Layout for VQFN Package

15 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2024) to Revision A (October 2025)

Page

- Updated device status to production data..... **1**
-

16 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

16.1 Documentation Support

16.1.1 Related Documentation

- Texas Instruments, [Layout Design Guide with DRV7308 for Improved Thermal Performance application note, application note](#)
- Texas Instruments, [How Three-Phase Integrated GaN Technology Maximizes Motor-Drive Performance, white paper](#)
- Texas Instruments, [DRV7308 Evaluation Module User's Guide](#)
- Texas Instruments, [Achieving household energy efficiency and cost savings with GaN-based motor system designs, technical article](#)
- Texas Instruments, [Thermal calculator for the DRV7308 to estimate power loss and device temp, design tool & simulation](#)

16.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

16.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

16.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

16.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

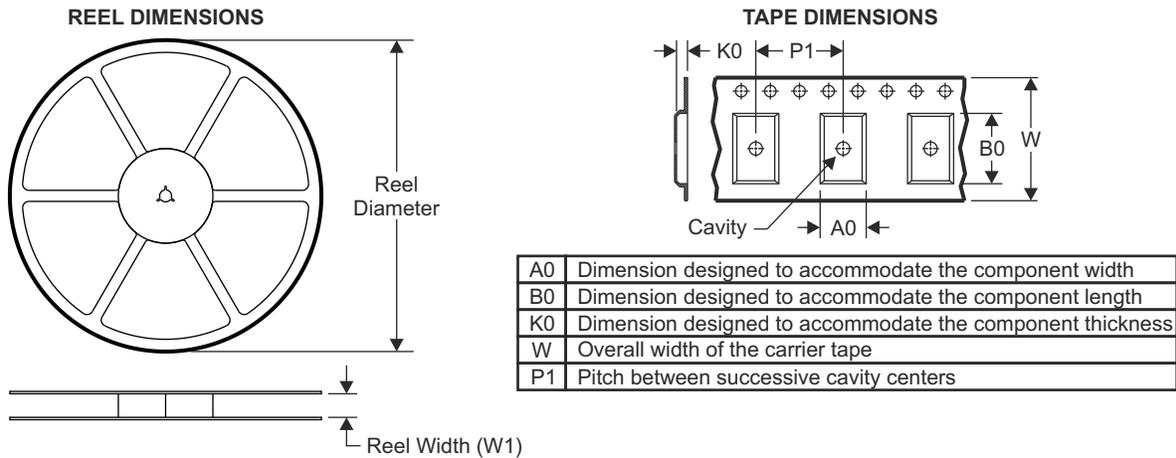
16.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

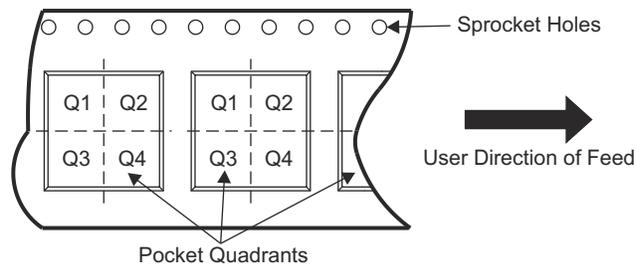
17 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

17.1 Tape and Reel Information

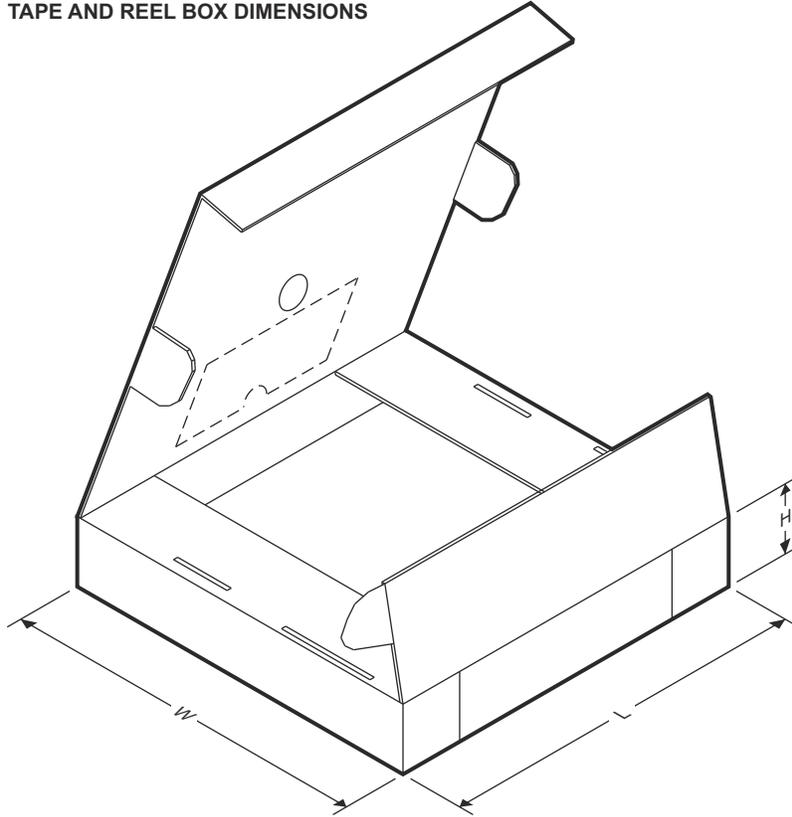


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DRV7308HREN | VQFN | REN | 65 | 2000 | 330.0 | 24.4 | 12.4 | 12.4 | 1.5 | 1.5 | 24.4 | Q1 |

TAPE AND REEL BOX DIMENSIONS



| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DRV7308HREN | VQFN | REN | 65 | 2000 | 12.4 | 12.4 | 1.5 |

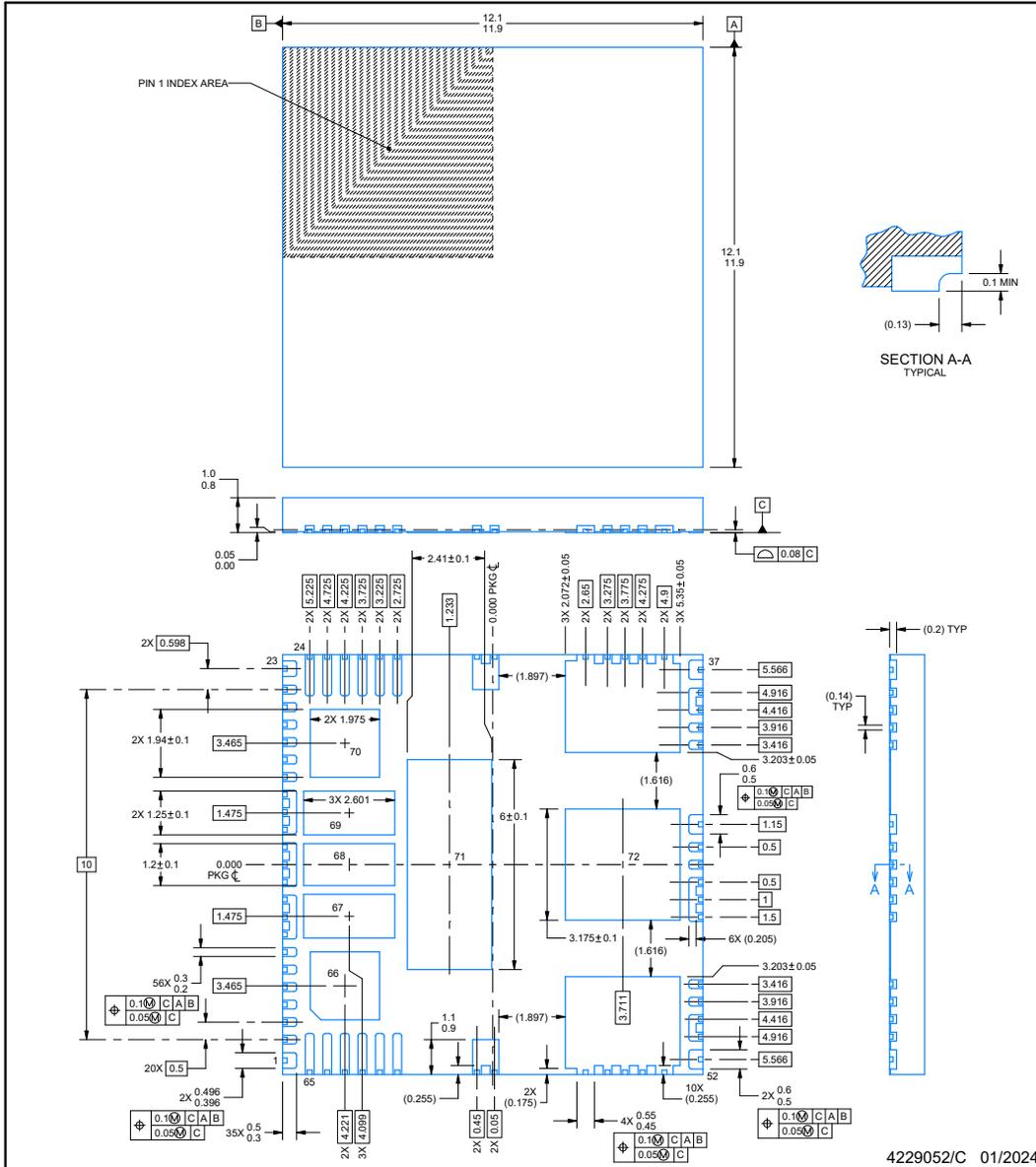


REN0065A

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

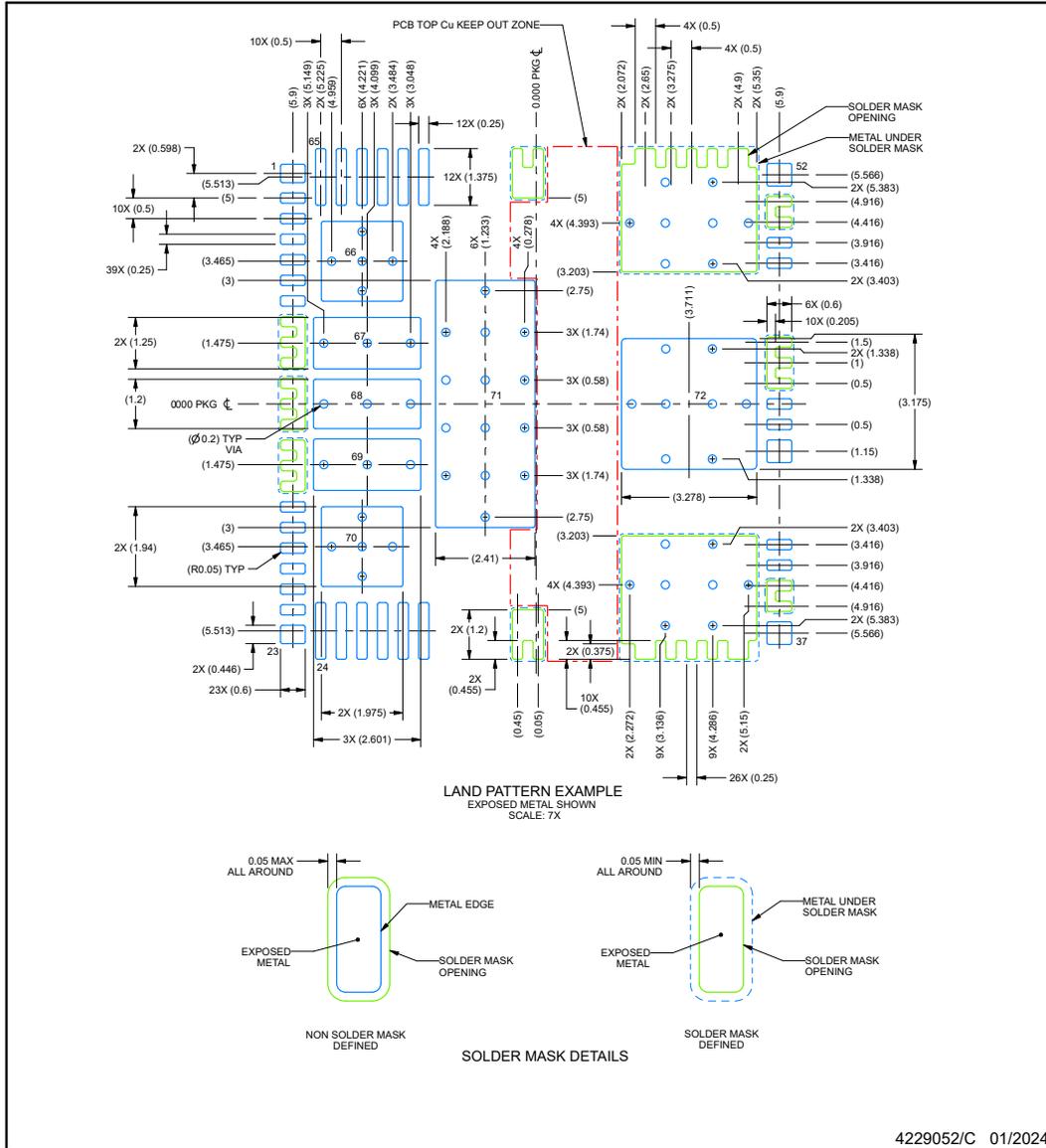
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad(s) must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

REN0065A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

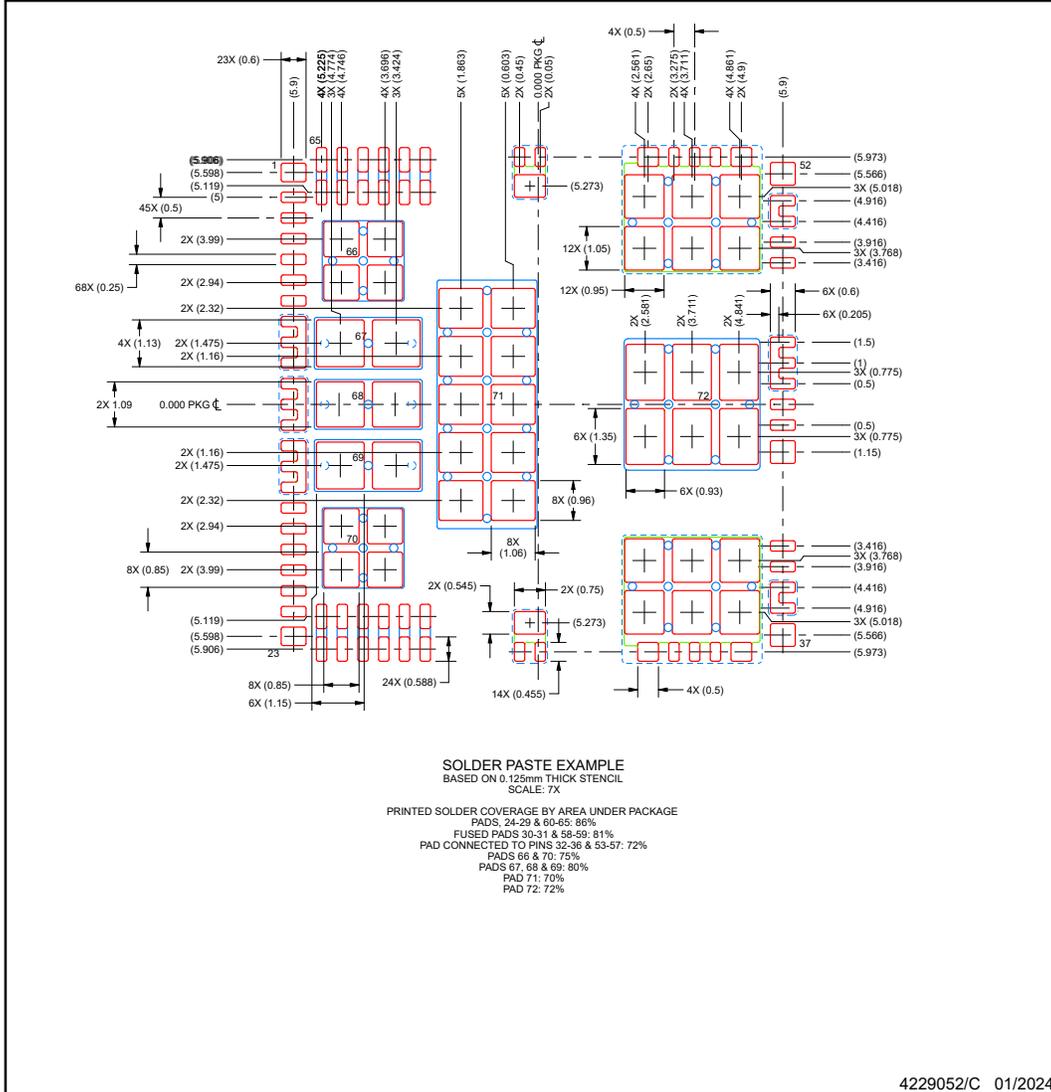
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

REN0065A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| DRV7308RENR | Active | Production | VQFN (REN) 65 | 3000 LARGE T&R | Yes | NIPDAU | Level-3-260C-168HRS | -40 to 125 | 7308 NNNNC |
| PDRV7308HRENR.A | Active | Preproduction | VQFN (REN) 68 | 3000 LARGE T&R | - | Call TI | Call TI | -40 to 125 | |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

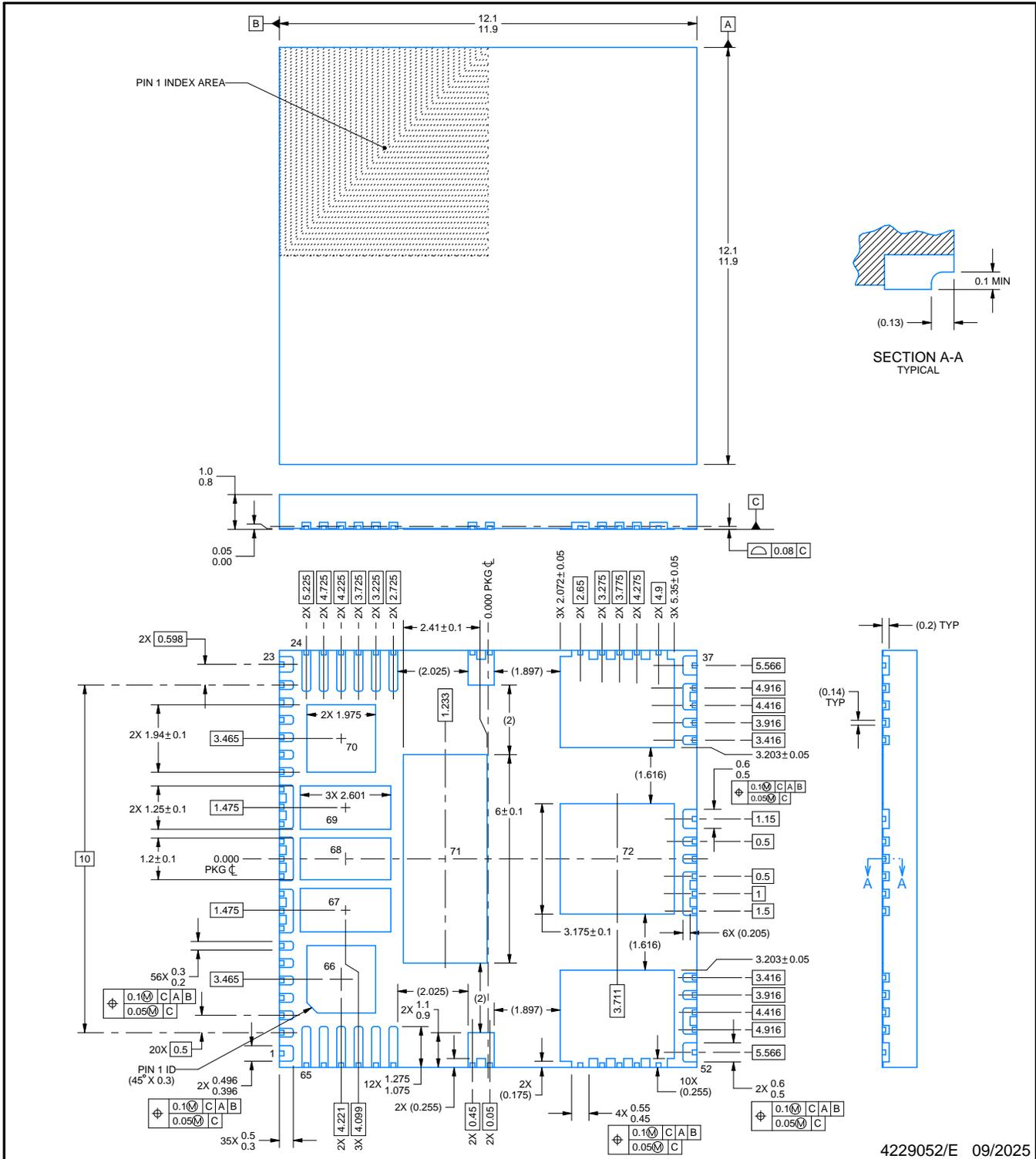
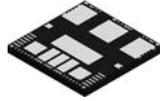
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



4229052/E 09/2025

NOTES:

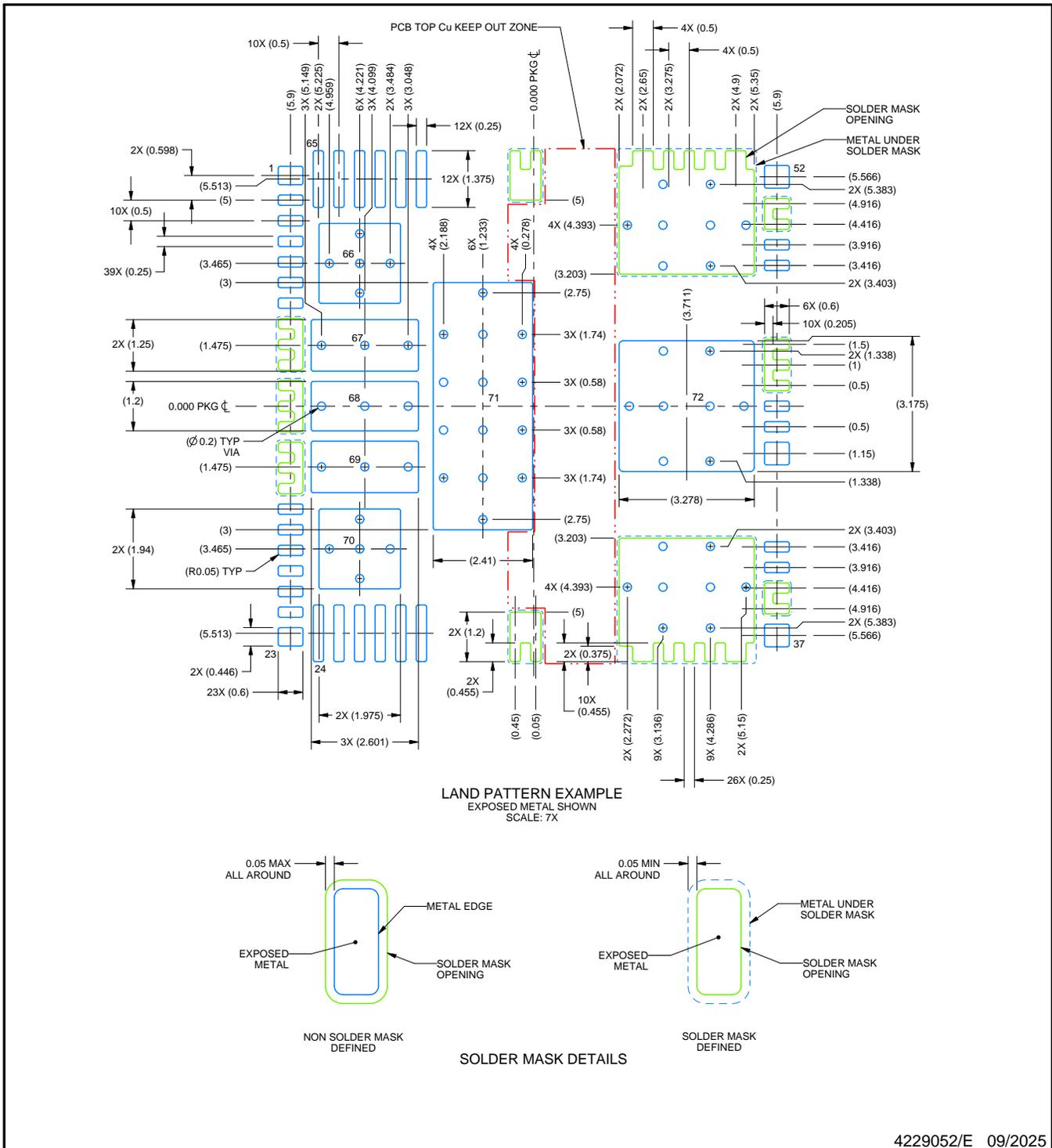
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad(s) must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

REN0065A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4229052/E 09/2025

NOTES: (continued)

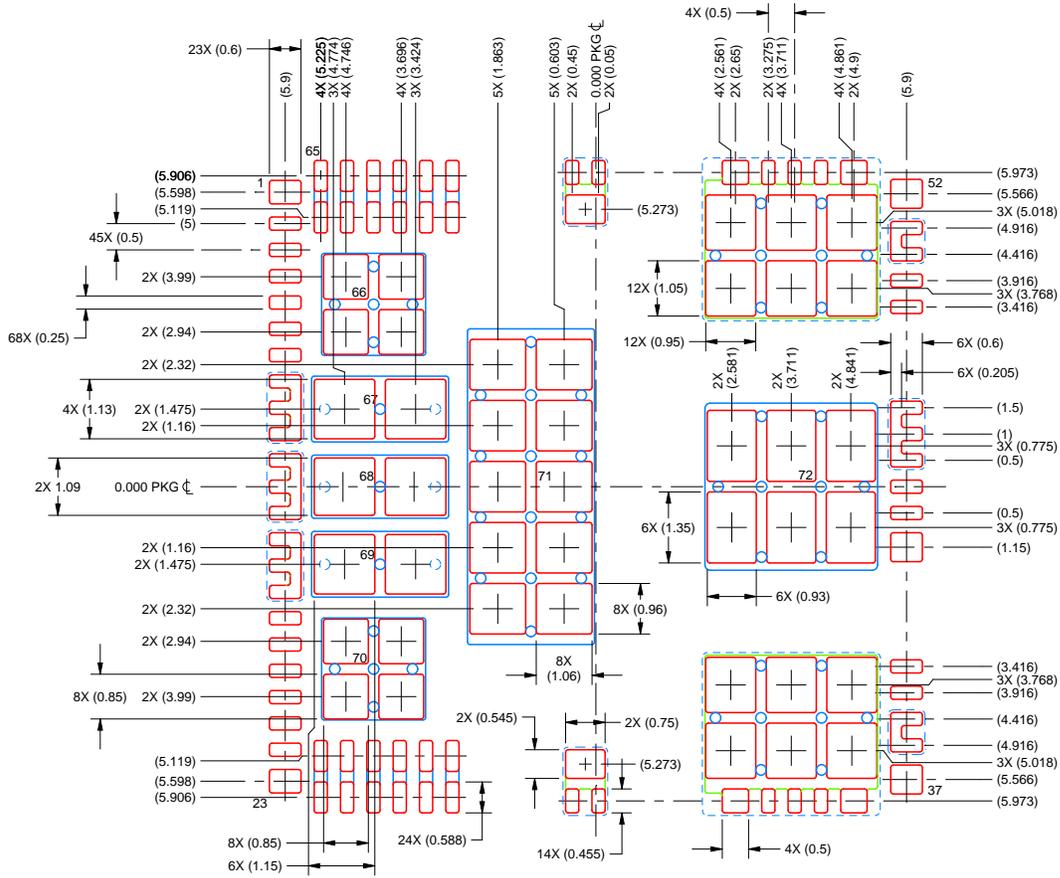
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

REN0065A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125mm THICK STENCIL
 SCALE: 7X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 PADS, 24-29 & 60-65: 86%
 FUSED PADS 30-31 & 58-59: 81%
 PAD CONNECTED TO PINS 32-36 & 53-57: 72%
 PADS 66 & 70: 75%
 PADS 67, 68 & 69: 80%
 PAD 71: 70%
 PAD 72: 72%

4229052/E 09/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025