DLPA3082 Power Management and High-Current Driver IC

1 Features

- Generation of DMD high voltage supplies
- Two high-efficiency buck converters to generate the DLPC84xx and DMD supply
- One high-efficiency, 8-bit programmable buck converter for fan driver application or general power supply. General purpose buck2 (PWR6) is currently supported.
- Two LDOs supplying auxiliary voltages
- Analog MUX for measuring internal and external nodes such as a thermistor and reference levels
- Monitoring/protections: thermal shutdown, hot die, and undervoltage lockout (UVLO)

2 Applications

Portable DLP®Pico™ projectors

3 Description

The DLPA3082 is a highly-integrated power management IC optimized for DLP® Pico™ Projector systems. The DLPA3082 contains five buck converters, two of which are dedicated for DLPC low voltage supplies. Another dedicated regulating supply generates the three timing-critical DC supplies for the DMD: VBIAS, VRST, and VOFS.

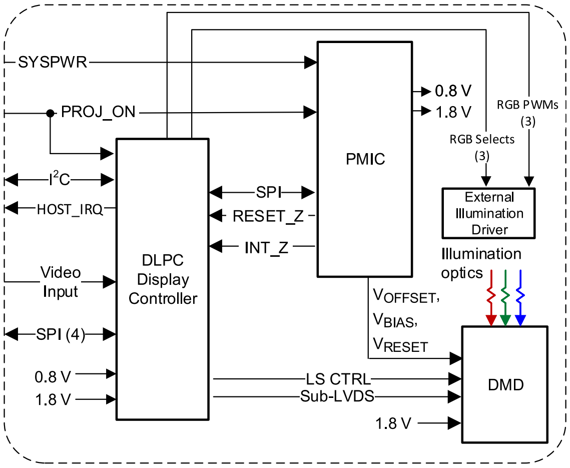
The DLPA3082 contains several auxiliary blocks which are used in a flexible way. This enables a tailor-made Pico Projector system. One 8-bit programmable buck converter isused, for instance, to make auxiliary supply line. General purpose buck2 (PWR6) is currently supported. Two LDOs are used for a lower-current supply, up to 200mA. These LDOs are predefined to 2.5V and 3.3V.

Through the SPI, all blocks of the DLPA3082 are addressed. Features included are the generation of the system reset, power sequencing, IC self-protections, and an analog MUX for routing analog information to an external ADC.

Device Information

PART NUMBER	PACKAGE	PACKAGE SIZE
DLPA3082(1)	HTQFP (100)	14.00mm × 14.00mm

(1) For more information, see the *Mechanical, Packaging, and Orderable* addendum.



Typical Simplified System

Table of Contents

4 Pin Configuration and Functions

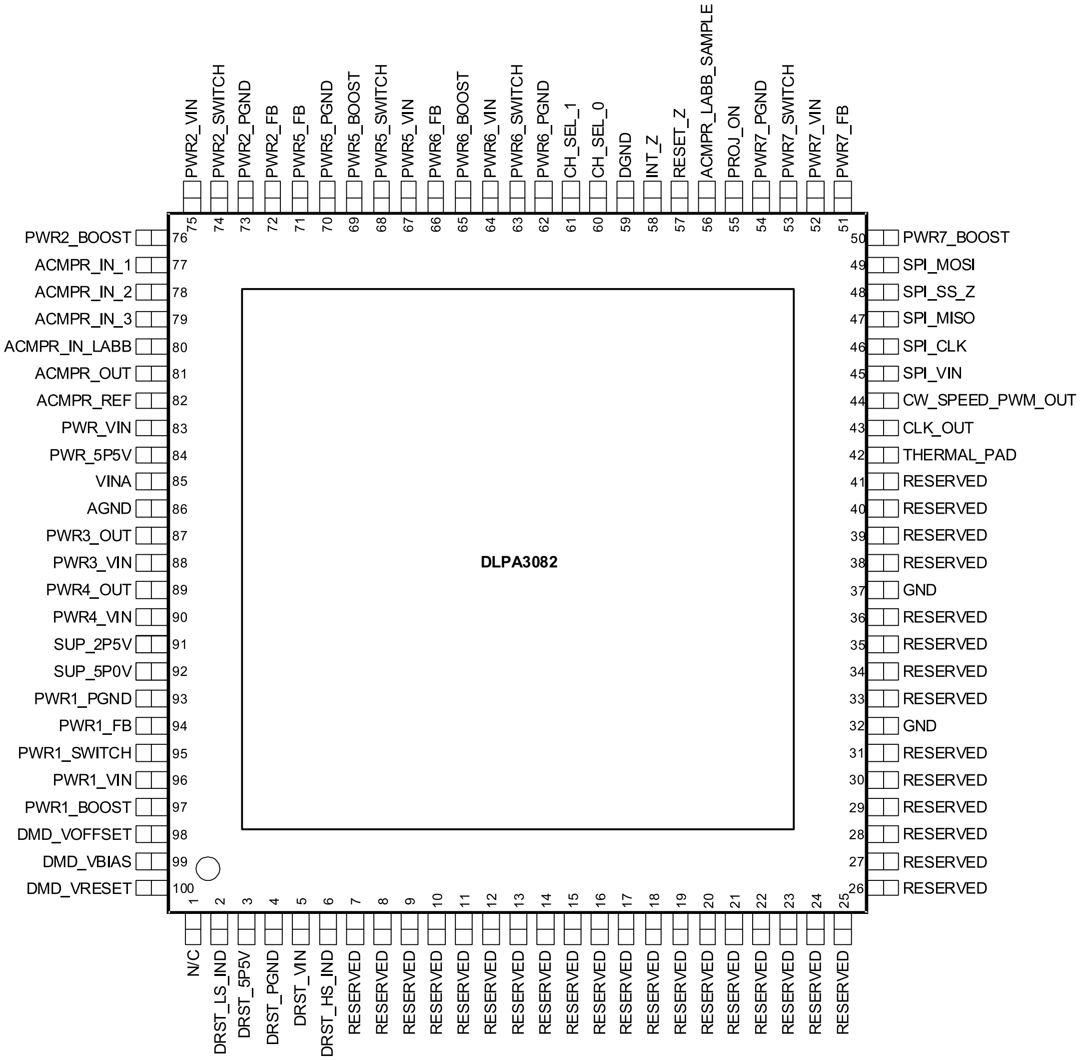


Figure 4-1. PFD Package 100-Pin HTQFP Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
N/C	1	—	No connect
DRST_LS_IND	2	I/O	Connection for the DMD SMPS-inductor (low-side switch).
DRST_5P5V	3	O	Filter pin for LDO DMD. Power supply for internal DMD reset regulator, typical 5.5V
DRST_PGND	4	GND	Power ground for DMD SMPS. Connect to ground plane.
DRST_VIN	5	POWER	Power supply input for LDO DMD. Connect to system power.
DRST_HS_IND	6	I/O	Connection for the DMD SMPS-inductor (high-side switch).
RESERVED	7	—	Connect a 10µF capacitor to ground.
RESERVED	8	—	Connect a 1µF capacitor to ground.
RESERVED	9	—	No connect
RESERVED	10	—	No connect
RESERVED	11	—	No connect
RESERVED	12	—	No connect

Table 4-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
RESERVED	13	—	No connect
RESERVED	14	—	No connect
RESERVED	15	—	No connect
RESERVED	16	—	No connect
RESERVED	17	—	No connect
RESERVED	18	—	No connect
RESERVED	19	—	No connect
RESERVED	20	—	No connect
RESERVED	21	—	No connect
RESERVED	22	—	No connect
RESERVED	23	—	No connect
RESERVED	24	—	No connect
RESERVED	25	—	No connect
RESERVED	26	—	No connect
RESERVED	27	—	No connect
RESERVED	28	—	No connect
RESERVED	29	—	No connect
RESERVED	30	—	No connect
RESERVED	31	—	Connect a pull-down 1kΩ resistor to ground.
GND	32	GND	Ground
RESERVED	33	—	No connect
RESERVED	34	—	No connect
RESERVED	35	—	No connect
RESERVED	36	—	Connect a pull-down 1kΩ resistor to ground.
GND	37	GND	Ground
RESERVED	38	—	No connect
RESERVED	39	—	No connect
RESERVED	40	—	No connect
RESERVED	41	—	No connect
THERMAL_PAD	42	GND	Thermal pad. Connect to a clean system ground.
CLK_OUT	43	O	No connect. Reserved for color wheel clock output.
CW_SPEED_PWM_OUT	44	O	No connect. Reserved for color wheel PWM output.
SPI_VIN	45	I	Supply for SPI interface
SPI_CLK	46	I	SPI clock input
SPI_MISO	47	O	SPI data output
SPI_SS_Z	48	I	SPI chip select (active low)
SPI_MOSI	49	I	SPI data input
PWR7_BOOST	50	I	No connect. Reserved for general purpose buck converter. Charge-pump-supply input for the high-side FET gate drive circuit. Connect a 100nF capacitor between PWR7_BOOST and PWR7_SWITCH pins.
PWR7_FB	51	I	No connect. Reserved for general purpose buck converter. Converter feedback input. Connect to converter output voltage.
PWR7_VIN	52	POWER	No connect. Reserved for general purpose buck converter. Power supply input for converter
PWR7_SWITCH	53	I/O	No connect. Reserved for general purpose buck converter. Switch node connection between high-side NFET and low-side NFET

Table 4-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PWR7_PGND	54	GND	No connect. Reserved for general purpose buck converter. Ground pin. Power ground return for switching circuit
PROJ_ON	55	I	Input signal to enable and or disable the IC and DLP projector
ACMPR_LABB_SAMPLE	56	I	Control signal to sample voltage at ACMPR_IN_LABB. Needs to connect a pull-down 10kΩ resistor to ground when the pin is not used.
RESET_Z	57	O	Reset output to the DLP system (active low). The pin is held low to reset DLP system.
INT_Z	58	O	Interrupt output signal (open drain, active low). Connect to the pullup resistor.
DGND	59	GND	Digital ground. Connect to ground plane.
CH_SEL_0	60	I	Control signal to enable either of CH1,2,3. Needs to connect a pull-down 10kΩ resistor to ground when the pin is not used.
CH_SEL_1	61	I	Control signal to enable either of CH1,2,3. Needs to connect a pull-down 10kΩ resistor to ground when the pin is not used.
PWR6_PGND	62	GND	Ground pin. Power ground return for switching circuit
PWR6_SWITCH	63	I/O	Switch node connection between high-side NFET and low-side NFET
PWR6_VIN	64	POWER	Power supply input for converter
PWR6_BOOST	65	I	Charge-pump-supply input for the high-side FET gate drive circuit. Connect a 100nF capacitor between PWR6_BOOST and PWR6_SWITCH pins.
PWR6_FB	66	I	Converter feedback input. Connect to output voltage.
PWR5_VIN	67	POWER	No connect. Reserved for general purpose buck converter. Power supply input for converter
PWR5_SWITCH	68	I/O	No connect. Reserved for general purpose buck converter. Switch node connection between high-side NFET and low-side NFET
PWR5_BOOST	69	I	No connect. Reserved for general purpose buck converter. Charge-pump-supply input for the high-side FET gate drive circuit. Connect 100nF capacitor between PWR5_BOOST and PWR5_SWITCH pins.
PWR5_PGND	70	GND	No connect. Reserved for general purpose buck converter. Ground pin. Power ground return for switching circuit
PWR5_FB	71	I	No connect. Reserved for general purpose buck converter. Converter feedback input. Connect to output voltage.
PWR2_FB	72	I	Converter feedback input. Connect to output voltage.
PWR2_PGND	73	GND	Ground pin. Power ground return for switching circuit
PWR2_SWITCH	74	I/O	Switch node connection between high-side NFET and low-side NFET
PWR2_VIN	75	POWER	Power supply input for converter
PWR2_BOOST	76	I	Charge-pump-supply input for the high-side FET gate drive circuit. Connect a 100nF capacitor between PWR2_BOOST and PWR2_SWITCH pins.
ACMPR_IN_1	77	I	Reserved. Input for analog sensor signal. No connect when the pin is not used.
ACMPR_IN_2	78	I	Input for analog sensor signal. No connect when the pin is not used.
ACMPR_IN_3	79	I	Input for analog sensor signal. No connect when the pin is not used.
ACMPR_IN_LABB	80	I	Input for ambient light sensor, sampled input. No connect when the pin is not used.
ACMPR_OUT	81	O	Analog comparator out. No connect when the pin is not used.
ACMPR_REF	82	I	Reference voltage input for analog comparator. No connect when the pin is not used.
PWR_VIN	83	POWER	Power supply input for LDO_Bucks. Connect to system power.
PWR_5P5V	84	O	Filter pin for LDO_BUCKS. Internal analog supply for buck converters, typical 5.5V
VINA	85	POWER	Input voltage supply pin for reference system
AGND	86	GND	Analog ground pin
PWR3_OUT	87	O	Filter pin for LDO_2 DMD/DLPC/AUX, typical 2.5V
PWR3_VIN	88	POWER	Power supply input for LDO_2. Connect to system power.
PWR4_OUT	89	O	Filter pin for LDO_1 DMD/DLPC/AUX, typical 3.3V
PWR4_VIN	90	POWER	Power supply input for LDO_1. Connect to system power.

Table 4-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SUP_2P5V	91	O	Filter pin for LDO_V2V5. Internal supply voltage, typical 2.5V
SUP_5P0V	92	O	Filter pin for LDO_V5V. Internal supply voltage, typical 5V
PWR1_PGND	93	GND	Ground pin. Power ground return for switching circuit
PWR1_FB	94	I	Converter feedback input. Connect to output voltage.
PWR1_SWITCH	95	I/O	Switch node connection between high-side NFET and low-side NFET
PWR1_VIN	96	POWER	Power supply input for converter
PWR1_BOOST	97	I	Charge-pump-supply input for the high-side FET gate drive circuit. Connect a 100nF capacitor between PWR1_BOOST and PWR1_SWITCH pins.
DMD_VOFFSET	98	O	VOFS output rail. Connect to ceramic capacitor.
DMD_VBIAS	99	O	VBIAS output rail. Connect to ceramic capacitor.
DMD_VRESET	100	O	VRESET output rail. Connect to ceramic capacitor.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	PWR_VIN, PWR1,2,3,4,6_VIN, VINA, DRST_VIN	–0.3	22	V
	PWR1,2,6_BOOST	–0.3	28	
	PWR1,2,6_BOOST (10ns transient)	–0.3	30	
	PWR1,2,6_SWITCH	–2	22	
	PWR1,2,6_SWITCH (10ns transient)	–3	27	
	PWR1,2,6_FB	–0.3	6.5	
	PWR1,2,6_BOOST vs PWR1,2,6_SWITCH	–0.3	6.5	
	DRST_LS_IND	–0.3	20	
	INT_Z, PROJ_ON	–0.3	7	
	DRST_HS_IND	–18	7	
	ACMPR_IN_1,2,3, ACMPR_REF, ACMPR_IN_LABB, ACMPR_LABB_SAMPLE, ACMPR_OUT	–0.3	3.6	
	SPI_VIN, SPI_CLK, SPI_MOSI, SPI_SS_Z, SPI_MISO, CH_SEL_0,1, RESET_Z	–0.3	3.6	
	DGND, AGND, DRST_PGND, GND, PWR1,2,6_PGND	–0.3	0.3	
	DRST_5P5V, PWR_5P5, PWR3,4_OUT, SUP_5P0V	–0.3	7	
	SUP_2P5V	–0.3	3.6	
	DMD_VOFFSET	–0.3	12	
	DMD_VBIAS	–0.3	20	
	DMD_VRESET	–18	7	
Source current	RESET_Z, ACMPR_OUT		1	mA
	SPI_DOUT		5.5	
Sink current	RESET_Z, ACMPR_OUT		1	mA
	SPI_DOUT, INT_Z		5.5	
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(2)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(3)	±500	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range	PWR_VIN, PWR1,2,3,4,6_VIN, VINA, DRST_VIN	6	20	V
	PROJ_ON	–0.1	6	
	PWR1,2,6_FB	–0.1	5	
	ACMPR_REF, CH_SEL_0,1, SPI_CLK, SPI_MOSI, SPI_SS_Z	–0.1	3.6	
	RLIM_BOT_K_1,2	–0.1	0.1	
	ACMPR_IN_1,2,3, LABB_IN_LABB	–0.1	1.5	
	SPI_VIN	1.7	3.6	
Ambient temperature range		0	70	°C
Operating junction temperature		0	120	°C

5.4 Thermal Information

THERMAL METRIC(1)		DLPA3082	UNIT
		PFD (HTQFP)	
		100 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	7.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (3)	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter (4)	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter (5)	3.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, but since the device is intended to be cooled with a heatsink from the top case of the package, the simulation includes a fan and heatsink attached to the DLPA3082. The heatsink is a 22mm × 22mm × 12mm aluminum pin fin heatsink with a 12 × 12 × 3mm stud. The base thickness is 2mm and the pin diameter is 1.5mm with an array of 6 × 6 pins. The heatsink is attached to the DLPA3082 with 100µm thick thermal grease with 3W/m-K thermal conductivity. The fan is 20 × 20 × 8mm with a 1.6cfm open volume flow rate and 0.22-inch water pressure at stagnation.

(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description is found in the ANSI SEMI standard G30-88.

(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7), but modified to include the fan and heatsink described in Note 2.

(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7), but modified to include the fan and heatsink described in Note 2.

5.5 Electrical Characteristics

Over operating free-air temperature range. V_{IN} = 12V, T_A = 0 to +70°C, typical values are at T_A = 25°C, Configuration according to *Section 7.2* (V_{IN} =12V) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLIES						
INPUT VOLTAGE						
V_{IN}	Input voltage range	VINA – pin	6(6)	12	20	V
V_{UVLO} (7)	UVLO threshold	VINA falling (through a 5-bit trim function, 0.5V steps)	3.9	6.22	18.4	V
	Hysteresis	VINA rising		90		mV
$V_{STARTUP}$	Startup voltage	DMD_VBIAS, DMD_VOFFSET, DMD_VRESET loaded with 10mA	6			V
INPUT CURRENT						
I_{IDLE}	Idle current	IDLE mode, all VIN pins combined		15		µA
I_{STD}	Standby current	STANDBY mode, analog, internal supplies and LDOs enabled, DMD and BUCK CONVERTERS disabled.		3.7		mA
I_{Q_DMD}	Quiescent current (DMD)	Quiescent current DMD block (in addition to I_{STD}), VINA + DRST_VIN		0.49		mA
I_{Q_BUCK}	Quiescent current (per BUCK)	Quiescent current per BUCK converter (in addition to I_{STD}), Normal mode, VINA + PWR_VIN + PWR1,2,6_VIN, PWR1,2,6_VOUT = 1V		4.3		mA
		Quiescent current per BUCK converter (in addition to I_{STD}), Normal mode, VINA + PWR_VIN + PWR1,2,6_VIN, PWR1,2,6_VOUT = 5V		15		
		Quiescent current per BUCK converter (in addition to I_{STD}), Cycle-skipping mode, VINA + PWR_VIN + PWR1,2,6_VIN = 1V		0.41		
		Quiescent current per BUCK converter (in addition to I_{STD}), Cycle-skipping mode, VINA + PWR_VIN + PWR1,2,6_VIN = 5V		0.46		
I_{Q_TOTAL}	Quiescent current (Total)	Typical Application: ACTIVE mode, all VIN pins combined, DMD, and PWR1,2 enabled, PWR3,4,6 disabled.		38		mA
INTERNAL SUPPLIES						
V_{SUP_5P5V}	Internal supply, analog			5		V
V_{SUP_2P5V}	Internal supply, logic			2.5		V
DMD — LDO DMD						
V_{DRST_VIN}			6	12	20	V
V_{DRST_5P5V}				5.5		V
PGOOD	Power good DRST_5P5V	Rising		80%		
		Falling		60%		
OVP	Overvoltage protection DRST_5P5V			7.2		V
	Regulator dropout	At 25mA, VDRST_VIN= 5.5V		56		mV
	Regulator current limit(2)		300	340	400	mA
DMD — REGULATOR						
$R_{DS(ON)}$	MOSFET ON-resistance	Switch A (from DRST_5P5V to DRST_HS_IND)		920		mΩ
		Switch B (from DRST_LS_IND to DRST_PGND)		450		

5.5 Electrical Characteristics (continued)

Over operating free-air temperature range. V_{IN} = 12V, T_A = 0 to +70°C, typical values are at T_A = 25°C, Configuration according to *Section 7.2* (V_{IN} =12V) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FW}	Forward voltage drop	Switch C (from DRST_LS_IND to DRST_VBIAS(1)), VDRST_LS_IND = 2V, I_F = 100mA		1.21		V
		Switch D (from DRST_LS_IND to DRST_VOFFSET(1)), VDRST_LS_IND = 2V, I_F = 100mA		1.22		
t_{DIS}	Rail Discharge time	C_{OUT}= 1µF			40	µs
t_{PG}	Power-good timeout	Not tested in production		15		ms
I_{LIMIT}	Switch current limit			610		mA
VOFFSET REGULATOR						
V_{OFFSET}	Output voltage			10		V
	DC output voltage accuracy	I_{OUT}= 10mA	-0.3		0.3	V
	DC Load regulation	I_{OUT}= 0mA to 10mA		–10		V/A
	DC Line regulation	I_{OUT}= 10mA, DRST_VIN = 8V to 20V		–5		mV/V
V_{RIPPLE}	Output ripple	I_{OUT}= 10mA, C_{OUT}= 1µF		200		mVpp
I_{OUT}	Output current		0.1		10	mA
PGOOD	Power-good threshold (fraction of nominal output voltage)	VOFFSET rising		86%		
		VOFFSET falling		66%		
C	Output capacitor	Recommended value(5) (use same value as output capacitor on VRESET)	1			µF
		$t_{DISCHARGE}$ <40µs at VIN = 8V			1	
VBIAS REGULATOR						
V_{BIAS}	Output voltage			18		V
	DC output voltage accuracy	I_{OUT}= 10mA	–0.3		0.3	V
	DC Load regulation	I_{OUT}= 0 to 10mA		–18		V/A
	DC Line regulation	I_{OUT}= 10mA, DRST_VIN = 8V to 20V		–3		mV/V
V_{RIPPLE}	Output ripple	I_{OUT}= 10mA, C_{OUT}= 470nF		200		mVpp
I_{OUT}	Output current		0.1		10	mA
PGOOD	Power-good threshold (fraction of nominal output voltage)	VBIAS rising		86%		
		VBIAS falling		66%		
C	Output capacitor	Recommended value(5) (use same or smaller value as output capacitors VOFFSET / VRESET)	470			nF
		$t_{DISCHARGE}$ <40µs at VIN = 8V			470	
VRESET REGULATOR						
V_{RST}	Output voltage			–14		V
	DC output voltage accuracy	I_{OUT}= 10mA	-0.3		0.3	V
	DC Load regulation	I_{OUT}= 0 to 10mA		–4		V/A
	DC Line regulation	I_{OUT}= 10mA, DRST_VIN = 8 to 20V		–2		mV/V
V_{RIPPLE}	Output ripple	I_{OUT}= 10mA, C_{OUT}= 1µF		120		mVpp
I_{OUT}	Output current		0.1		10	mA
PGOOD	Power-good threshold			90%		
C	Output capacitor	Recommended value(5) (use same value as output capacitor on VOFFSET)	1			µF
		$t_{DISCHARGE}$ <40µs at VIN = 8V			1	

5.5 Electrical Characteristics (continued)

Over operating free-air temperature range. V_{IN} = 12V, T_A = 0 to +70°C, typical values are at T_A = 25°C, Configuration according to *Section 7.2* (V_{IN} =12V) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DMD — BUCK CONVERTERS						
OUTPUT VOLTAGE						
$V_{PWR\_1\_VOUT}$	Output Voltage			0.8		V
$V_{PWR\_2\_VOUT}$	Output Voltage			1.8		V
	DC output voltage accuracy	I_{OUT}= 0mA	–3%		3%	
MOSFET						
$R_{ON,H}$	High side switch resistance	25°C, $V_{PWR\_1,2\_Boost} - V_{PWR1,2\_SWITCH}$ = 5.5V		150		mΩ
$R_{ON,L}$	Low side switch resistance(2)	25°C		85		mΩ
LOAD CURRENT						
	Allowed Load Current(3)				3	A
I_{OCL}	Current limit(2)	L_{OUT}= 3.3µH	3.2	3.6	4.2	A
ON-TIME TIMER CONTROL						
t_{ON}	On time	V_{IN} = 12V, V_O = 5V		120		ns
$t_{OFF(MIN)}$	Minimum off time(2)	T_A = 25°C, V_{FB} = 0V		270		ns
START-UP						
	Soft start		1	2.5	4	ms
PGOOD						
$Ratio_{OV}$	Overvoltage protection			120%		
$Ratio_{PG}$	Relative power good level	Low to high		72%		
BUCK CONVERTERS — LDO_BUCKS						
V_{PWR_VIN}	Input voltage range PWR1,2,6_VIN		6	12	20	V
V_{PWR_5P5V}	PWR_5P5V			5.5		V
PGOOD	Power good PWR_5P5V	Rising		80%		
		Falling		60%		
OVP	Overvoltage Protection PWR_5P5V			7.2		V
	Regulator dropout	At 25mA, V_{PWR_VIN}= 5.5V		41		mV
	Regulator current limit(2)		300	340	400	mA
BUCK CONVERTER — GENERAL PURPOSE BUCK CONVERTER (8)						
OUTPUT VOLTAGE						
V_{PWR6_VOUT}	Output Voltage (General Purpose Buck2)	8-bit programmable	1		5	V
	DC output voltage accuracy	I_{OUT}= 0mA	–3.5%		3.5%	
MOSFET						
$R_{ON,H}$	High side switch resistance	25°C, $V_{PWR6\_Boost} - V_{PWR6\_SWITCH}$ = 5.5V		150		mΩ
$R_{ON,L}$	Low side switch resistance(2)	25°C		85		mΩ
LOAD CURRENT						
	Allowed Load Current PWR6(3).			2		A
I_{OCL}	Current limit(2) (3)	L_{OUT}= 3.3µH	3.2	3.6	4.2	A
ON-TIME TIMER CONTROL						

5.5 Electrical Characteristics (continued)

Over operating free-air temperature range. V_{IN} = 12V, T_A = 0 to +70°C, typical values are at T_A = 25°C, Configuration according to *Section 7.2* (V_{IN} =12V) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	On time	V_{IN} = 12V, V_O = 5V		120		ns
$t_{OFF(MIN)}$	Minimum off time[2]	T_A = 25°C, V_{FB} = 0V		270	310	ns
START-UP						
	Soft start		1	2.5	4	ms
PGOOD						
$Ratio_{OV}$	Overvoltage protection			120%		
$Ratio_{PG}$	Relative power good level	Low to high		72%		
AUXILIARY LDOs						
$V_{PWR3,4\_VIN}$	Input voltage range	LDO1 (PWR4), LDO2 (PWR3)	3.3	12	20	V
PGOOD	Power good PWR3,4_VOUT	PWR3,4_VOUT rising		80%		
		PWR3,4_VOUT falling		60%		
OVP	Overvoltage Protection PWR3,4_VOUT			7		V
	DC output voltage accuracy PWR3,4_VOUT	I_{OUT}= 0mA	–3%		3%	
	Regulator current limit[2]		300	340	400	mA
t_{ON}	Turn-on time	to 80% of V_{OUT} = PWR3 and PWR4, C= 1µF		40		µs
LDO2 (PWR3)						
V_{PWR3_VOUT}	Output Voltage PWR3_VOUT			2.5		V
	Load Current capability			200		mA
	DC Load regulation PWR3_VOUT	V_{OUT}= 2.5V, I_{OUT}= 5 to 200mA		–70		mV/A
	DC Line regulation PWR3_VOUT	V_{OUT}= 2.5V, I_{OUT}= 5mA, PWR3_VIN = 3.3 to 20V		30		µV/V
LDO1 (PWR4)						
V_{PWR4_VOUT}	Output Voltage PWR4_VOUT			3.3		V
	Load Current capability			200		mA
	DC Load regulation PWR4_VOUT	V_{OUT}= 3.3V, I_{OUT}= 5 to 200mA		–70		mV/A
	DC Line regulation PWR4_VOUT	V_{OUT}= 3.3V, I_{OUT}= 5mA, PWR4_VIN= 4 to 20V		30		µV/V
	Regulator dropout	At 25mA, V_{OUT}= 3.3V, V_{PWR4_VIN}= 3.3V		48		mV
MEASUREMENT SYSTEM						
LABB						
t_{RC}	Settling time	To 1% of final value[2].		4.6	6.6	µs
		To 0.1% of final value[2]		7	10	
$V_{ACMPR\_IN\_LABB}$	Input voltage range ACMPR_IN_LABB		0		1.5	V
	Sampling window ACMPR_IN_LABB	Programmable per 7µs	7		28	µs
DIGITAL CONTROL — LOGIC LEVELS AND TIMING CHARACTERISTICS						
V_{SPI_VIN}	SPI supply voltage range	SPI_VIN	1.7		3.6	V

5.5 Electrical Characteristics (continued)

Over operating free-air temperature range. V_{IN} = 12V, T_A = 0 to +70°C, typical values are at T_A = 25°C, Configuration according to *Section 7.2* (V_{IN} =12V) (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output low-level	RESET_Z, ACMPR_OUT, CLK_OUT. I_O = 0.3mA sink current	0		0.3	V
		SPI_DOUT. I_O = 5mA sink current	0		0.3 × V_{SPI_VIN}	
		INT_Z. I_O = 1.5mA sink current	0		0.3 × V_{SPI_VIN}	
V_{OH}	Output high-level	RESET_Z, ACMPR_OUT, CLK_OUT. I_O = 0.3mA source current	1.3		2.5	V
		SPI_DOUT. I_O = 5mA source current	0.7 × V_{SPI_VIN}		V_{SPI_VIN}	
V_{IL}	Input low-level	PROJ_ON, CH_SEL0, CH_SEL1	0		0.4	V
		SPI_CSZ, SPI_CLK, SPI_DIN	0		0.3 × V_{SPI_VIN}	
V_{IH}	Input high-level	PROJ_ON, CH_SEL0, CH_SEL1	1.2			V
		SPI_CSZ, SPI_CLK, SPI_DIN	0.7 × V_{SPI_VIN}		V_{SPI_VIN}	
I_{BIAS}	Input bias current	V_{IO}= 3.3V, any digital input pin			0.1	µA
SPI_CLK	SPI clock frequency(4)	Normal SPI mode, DIG_SPI_FAST_SEL = 0, f_{OSC} = 9MHz	0		36	MHz
		Fast SPI mode, DIG_SPI_FAST_SEL = 1, V_{SPI_VIN}> 2.3V, f_{OSC} = 9MHz	20		40	
$t_{DEGLITCH}$	Deglitch time	CH_SEL0, CH_SEL1(2).		300		ns
INTERNAL OSCILLATOR						
f_{OSC}	Oscillator frequency			9		MHz
	Frequency accuracy	T_A= 0 to 70°C	–5%		5%	
THERMAL SHUTDOWN						
T_{WARN}	Thermal warning (HOT threshold)			120		°C
	Hysteresis			10		
T_{SHTDWN}	Thermal shutdown (TSD threshold)			150		°C
	Hysteresis			15		

(1) Including rectifying diode
(2) Not production tested
(3) Take care to not exceed the max power dissipation. Refer to *Thermal Considerations*.
(4) Maximum depends linearly on oscillator frequency f_{OSC}.
(5) Take care that the capacitor has the specified capacitance at the related voltage, that is V_{OFFSET}, V_{BIAS}, or V_{RESET}.
(6) VIN must be higher than the UVLO voltage setting, including after accounting for AC noise on VIN, for the DLPA3082 to fully operate. While 6.0V is the minimum VIN voltage supported, TI recommends that the UVLO is never set below 6.21V for a fault fast power down. 6.21V gives a margin above 6.0V to protect against the case where someone suddenly removes the VIN's power supply which causes the VIN voltage to drop rapidly. Failure to keep VIN above 6.0V before the mirrors are parked and VOFS, VRST, and VBIAS supplies are properly shut down results in permanent damage to the DMD. Since 6.21V is .21V above 6.0V, when UVLO trips there is time for the DLPA3082 and DLPC84xx to park the DMD mirrors and do a fast shutdown of supplies VOFS, VRST, and VBIAS. For whatever UVLO setting is used, if VIN's power supply is suddenly removed enough bulk capacitance can be included on VIN inside the projector to keep VIN above 6.0V for at least 100µs after UVLO trips.
(7) UVLO cannot be used for normal power down operation, it is meant as a protection from power loss.
(8) General purpose buck2 (PWR6) is currently supported.

5.6 SPI Timing Parameters

SPI_VIN = 3.6V ± 5%, T_A = 0 to 70°C, C_L = 10pF (unless otherwise noted).

		MIN	NOM	MAX	UNIT
f_{CLK}	Serial clock frequency	0		40	MHz
t_{CLKL}	Pulse width low, SPI_CLK, 50% level	10			ns
t_{CLKH}	Pulse width high, SPI_CLK, 50% level	10			ns
t_t	Transition time, 20% to 80% level, all signals	0.2		4	ns
t_{CSCR}	SPI_SS_Z falling to SPI_CLK rising, 50% level	8			ns
t_{CFCS}	SPI_CLK falling to SPI_CSZ rising, 50% level			1	ns
t_{CDS}	SPI_MOSI data setup time, 50% level	7			ns
t_{CDH}	SPI_MOSI data hold time, 50% level	6			ns
t_{iS}	SPI_MISO data setup time, 50% level	10			ns
t_{iH}	SPI_MISO data hold time, 50% level	0			ns
t_{CFDO}	SPI_CLK falling to SPI_MISO data valid, 50% level		13		ns
t_{CSZ}	SPI_CSZ rising to SPI_MISO HiZ		6		ns

6 Detailed Description

6.1 Overview

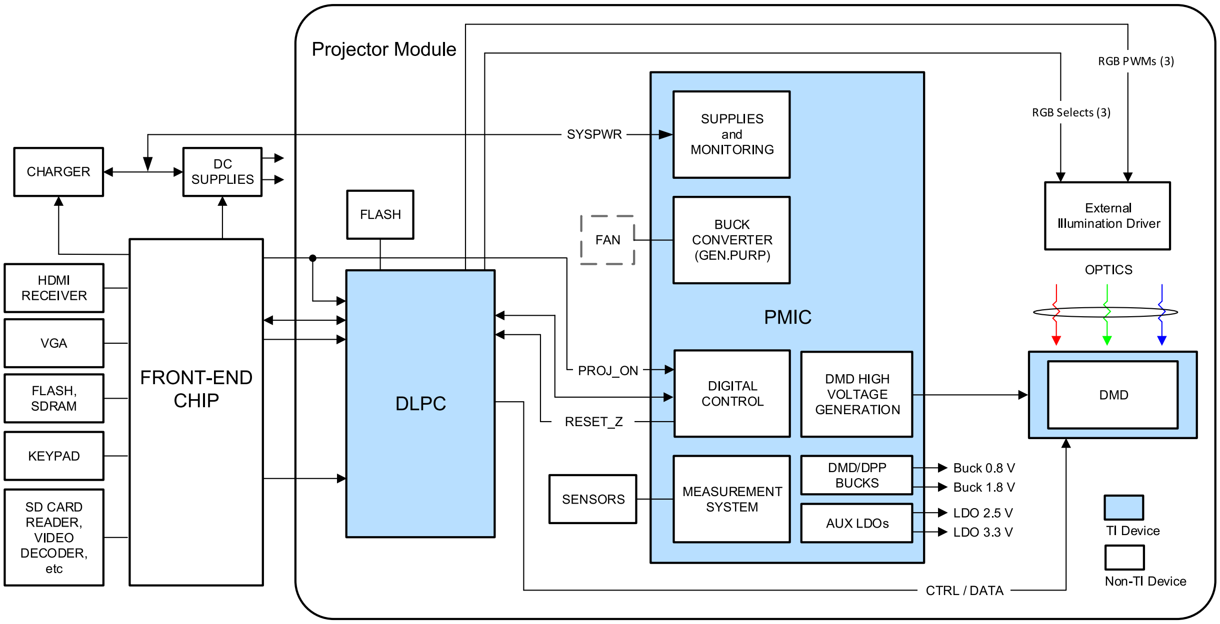
The DLPA3082 is a highly integrated power management IC optimized for DLP Pico Projector systems. The device targets accessory applications up to several hundreds of lumen.Section 6.2 shows a typical DLP Pico Projector implementation using the DLPA3082.

Part of the projector is the projector module, which is an optimized combination of components consisting of, for instance, DLPA3082, DMD, DLPC chip, memory, and optional sensors and fan. The frontend chip controls the projector module. More information about the system and projector module configuration can be found in a separate application note.

Within the DLPA3082, several blocks are distinguished. The blocks are listed below and subsequently discussed in detail:

- Supply and monitoring: Creates internal supply and reference voltages and has function such as thermal protection
- DMD: Generates voltages and specific timing for the DMD. Contains regulators and DMD/DLPC buck converters
- Buck converter: General purpose buck converter
- Auxilairy LDOs: Fixed voltage LDOs for customer usage
- Measurement system: Analog frontend to measure internal and external signals
- Digital control: SPI, digital control

6.2 Functional Block Description



6.3 Feature Description

6.3.1 Supply and Monitoring

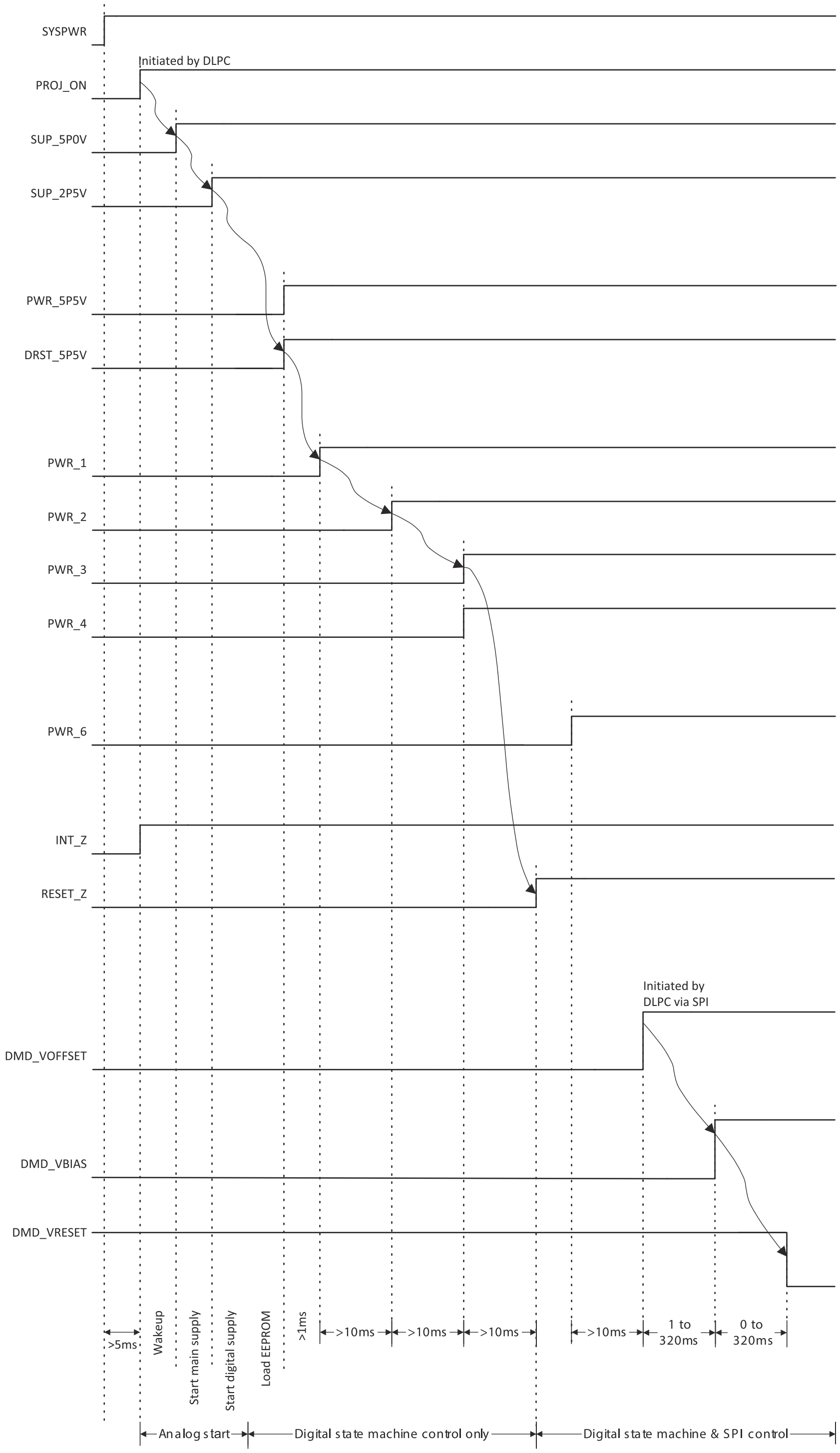
This block takes care of creating several internal supply voltages and monitors correct behavior of the device.

6.3.1.1 Supply

SYSPWR is the main supply of the DLPA3082. It ranges from 6V to 20V, where the typical is 12V. At power-up, several (internal) power supplies are started one after the other to make the system work correctly (Figure 6-1). A sequential startup ensures that all the different blocks start in a certain order and prevent excessive startup currents. The main control to start the DLPA3082 is the control pin *PROJ_ON*. Once set high the *basic* analog circuitry is started that is needed to operate the digital and SPI interface. This circuitry is supplied by two LDO regulators that generate 2.5V (SUP_2P5V) and 5V (SUP_5P0V). These regulator voltages are for internal use only and cannot be loaded by an external application. The output capacitors of those LDOs can be 2.2μF for the 2.5V LDO, and 4.7μF for the 5V LDO, pin 91 and 92, respectively. Once these are up the digital core is started, and the DLPA3082 Digital State Machine (DSM) takes over.

Subsequently, the 5.5V LDOs for various blocks are started: PWR_5P5V and DRST_5P5V. Next, the buck converters and DMD LDOs are started (PWR_1 to PWR_4). The DLPA30085 is now awake and ready to be controlled by the DLPC (indicated by RESET_*Z* going high).

The general purpose buck converter (PWR_6) can be started (if used) as well as the regulator that supplies the DMD. The DMD regulator generates the timing critical VOFFSET, VBIAS, and VRESET supplies.



1. Arrows indicate the sequence of events automatically controlled by the digital state machine. Other events are initiated under SPI control.
2. SUP_5P0V and SUP_2P5V rise to a precharge level with SYSPWR, and reach the full level potential after PROJ_ON is pulled high.

Figure 6-1. Powerup Timing

6.3.1.2 Monitoring

Several possible faults are monitored by the DLPA3082. If a fault occurred and the type of the fault is read in the Main Status register (0x0C). Subsequently, an interrupt could be generated if a fault occurs. The fault conditions that generate an interrupt could be configured in the Interrupt Mask register (0x0D).

6.3.1.2.1 Block Faults

Fault conditions for several supplies can be observed such as the low voltage supplies SUPPLY_FAULT (0x0C, bit 7). DMD_FAULT (0x0C, bit 4) monitors the correct function of the DMD block. The PROJ_ON_INT (0x0C, bit 5) indicates if PROJ_ON was asserted.

6.3.1.2.2 Thermal Protection

The chip temperature is monitored constantly to prevent overheating of the device. There are two levels of a fault condition. The first is TS_WARN (0x0C, bit 0) to warn of overheating. This is an indication that the chip temperature rises to a critical temperature. The next level of warning is TS_SHUT (0x0C, bit 1). This occurs at a higher temperature than TS_WARN (0x0C, bit 0) and shuts down the chip to prevent permanent damage. Both temperature faults have hysteresis on each level to prevent rapid switching around the temperature threshold.

6.3.2 DMD Supplies

This block contains all the supplies needed for the DMD and DLPC (Figure 6-2). The block comprises:

- LDO_DMD: for internal supply
- DMD_HV: regulator generates high voltage supplies
- Two buck converters: for DLPC/DMD voltages

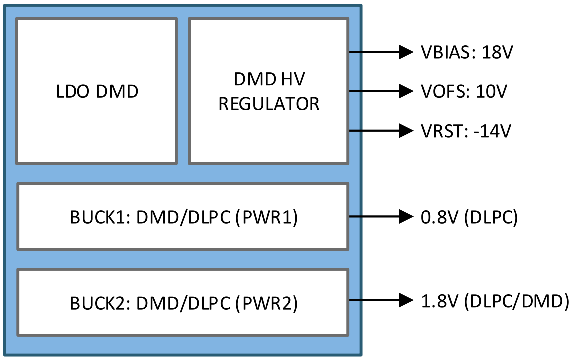


Figure 6-2. DMD Supplies Blocks

The DMD supplies block is designed to work with the DMD and the related DLPC. The DMD has a DMD-specific set of supply voltage requirements. Besides the three high voltages, two supplies are needed for the DMD and the related DLPC (DLPC84xx-family for instance). These supplies are made by two buck converters.

6.3.2.1 LDO DMD

This regulator is dedicated to the DMD supplies block and provides an analog supply voltage of 5.5V to the internal circuitry. Use a 1µF capacitor in parallel with a 10µF capacitor on the input and a 10µF capacitor on the output of the LDO. Make the voltage rating of the capacitor equal to or greater than two times the applied voltage across the capacitor in the application.

6.3.2.2 DMD HV Regulator

The DMD HV regulator generates three high-voltage supplies: DMD_VRESET, DMD_VBIAS, and DMD_VOFFSET (Figure 6-3). The DMD HV regulator uses a switching regulator (switch A-D), where the inductor is time-shared between all three supplies. The inductor is charged up to a certain current value (current limit) and then discharged into one of the three supplies. If not all supplies need charging, the time available is equally shared between those that do need charging. The recommended value for the capacitors is 1µF for V_{RST} and V_{OFS}, and 470nF for V_{BIAS}. The inductor value is 10µH.

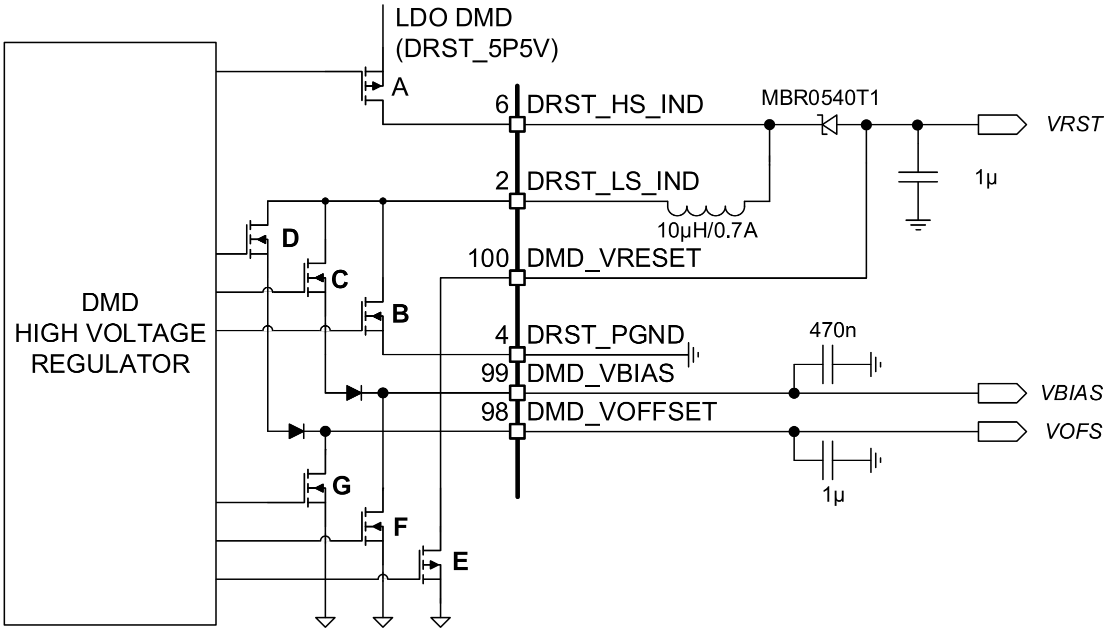


Figure 6-3. DMD High Voltage Regulator

6.3.2.3 DMD/DLPC Buck Converters

Each of the two DMD buck converters creates a supply voltage for the DMD and DLPC. The values of the voltages for the DMD and DLPC used, for instance:

- DMD+DLPC84xx: 0.8V (DLPC) and 1.8V (DLPC/DMD)

The topology of the buck converters is the same as the general-purpose buck converter discussed later in this document. How to configure the inductor and capacitor is discussed in Section 6.3.3.

A typical configuration is 3.3µH for the inductor and 2× 22µF for the output capacitor.

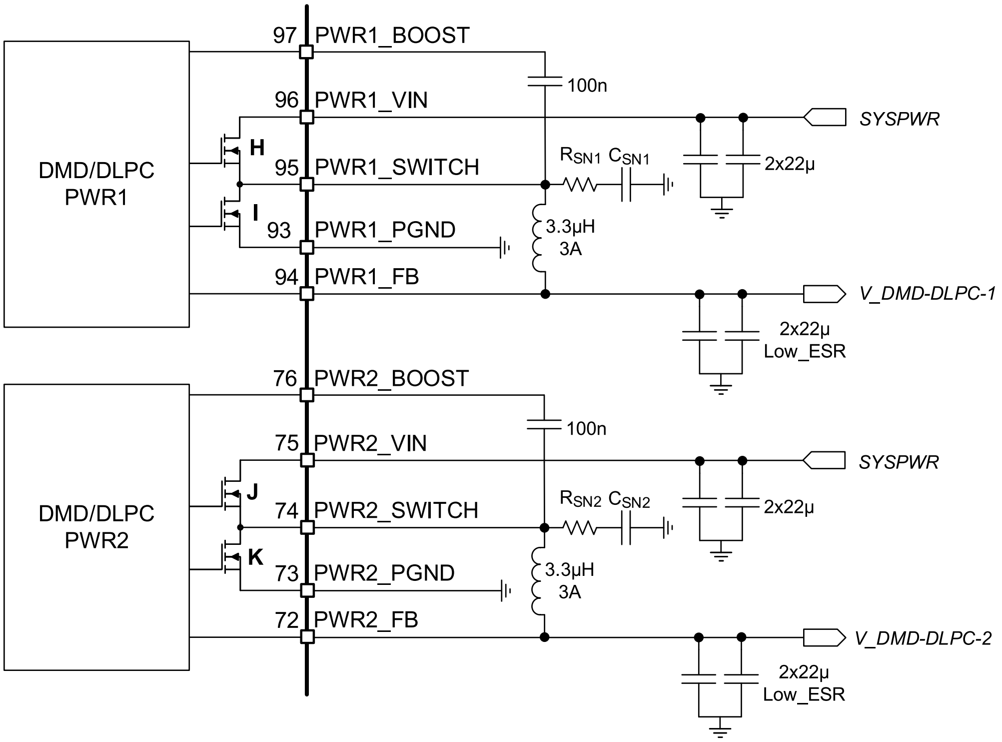


Figure 6-4. DMD/DLPC Buck Converters

6.3.2.4 DMD Monitoring

The DMD block is continuously monitored for failures to prevent damage to the DLPA3082 and the DMD. Several possible failures are monitored such that the DMD voltages can be ensured. Failures can be, for instance, a broken control loop or a too high or too low converter output voltage. The overall DMD fault bit is in Main Status register (0x0C), DMD_FAULT. If any of the failures in Table 6-1 occur, the DMD_FAULT bit is set high.

Table 6-1. DMD FAULT Indication

POWER GOOD		
BLOCK	**REGISTER BIT**	**THRESHOLD**
HV Regulator	DMD_PG_FAULT	DMD_VRESET: 90%, DMD_VOFFSET and DMD_VBIAS: 86% rising, 66% falling
PWR1	BUCK_DMD1_PG_FAULT	Ratio: 72%
PWR2	BUCK_DMD2_PG_FAULT	Ratio: 72%
PWR3 (LDO_2)	LDO_GP2_PG_FAULT / LDO_DMD1_PG_ FAULT	80% rising, 60% falling
PWR4 (LDO_1)	LDO_GP1_PG_FAULT / LDO_DMD1_PG_ FAULT	80% rising, 60% falling
OVERVOLTAGE		
BLOCK	**REGISTER BIT**	**THRESHOLD** (V)
PWR1	BUCK_DMD1_OV_FAULT	Ratio: 120%
PWR2	BUCK_DMD2_OV_FAULT	Ratio: 120%
PWR3 (LDO_2)	LDO_GP2_OV_FAULT / LDO_DMD1_OV_FAULT	7
PWR4 (LDO_1)	LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT	7

6.3.2.4.1 Power Good

The DMD HV regulator, DMD buck converters, auxiliary LDOs and the LDO DMD that supports the HV regulator, all have a power good indication.

The DMD HV regulator is continuously monitored to check if the output rails DMD_VRESET, DMD_VOFFSET, and DMD_VBIAS are in regulation. If either one of the output rails drops out of regulation (for example, due to a shorted output or overloading) the DMD_ PG_FAULT bit in Detailed Status Register3 (0x29) is set. The threshold for DMD_VRESET is 90% and the thresholds for DMD_VOFFSET/ DMD_VBIAS are 86% (rising edge) and 66% (falling edge).

The power good signal for the two DMD buck converters indicates if the output voltages (PWR1_FB and PWR2_FB) are within a defined window. The relative power good ratio is 72%. This means that if the output voltage is below 72% of the set output voltage the power good bit is asserted. The power good bits are in Detailed Status Register3 (0x29), bits BUCK_DMD1_PG_FAULT and BUCK_DMD2_PG_FAULT.

LDO_1 and LDO_2 output voltages are also monitored. When the power good fault of the LDO is asserted it implies that the LDO voltage is below 80% (rising edge) or 60% (falling edge) of its intended value. The power good indication for the LDOs is in Detailed Status Register3 (0x29), bits LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT and LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT.

6.3.2.4.2 Overvoltage Fault

An overvoltage fault occurs when an output voltage rises above a pre-defined threshold. Overvoltage faults are indicated for the DMD buck converters, auxiliary LDOs, and the LDO DMD supporting the DMD HV regulator. The overvoltage faults of LDO_1 and LDO_2 are not incorporated in the overall DMD_FAULT when the LDOs are used as general-purpose LDOs. Table 6-1 provides an overview of the possible DMD overvoltage faults and the faults' threshold levels.

6.3.3 Buck Converters

The DLPA3082 contains one general-purpose buck converter and a supporting LDO (LDO_BUCKS). The programmable 8-bit buck converter can generate a voltage between 1V and 5V, and have an output current limit of 3A. General purpose buck2 (PWR6) is currently supported. One buck converter and the LDO_BUCKS are depicted in Figure 6-5.

The two DMD/DLPC buck converters discussed earlier in Section 6.3.2 have the same architecture as the buck converter and can be configured in the same way.

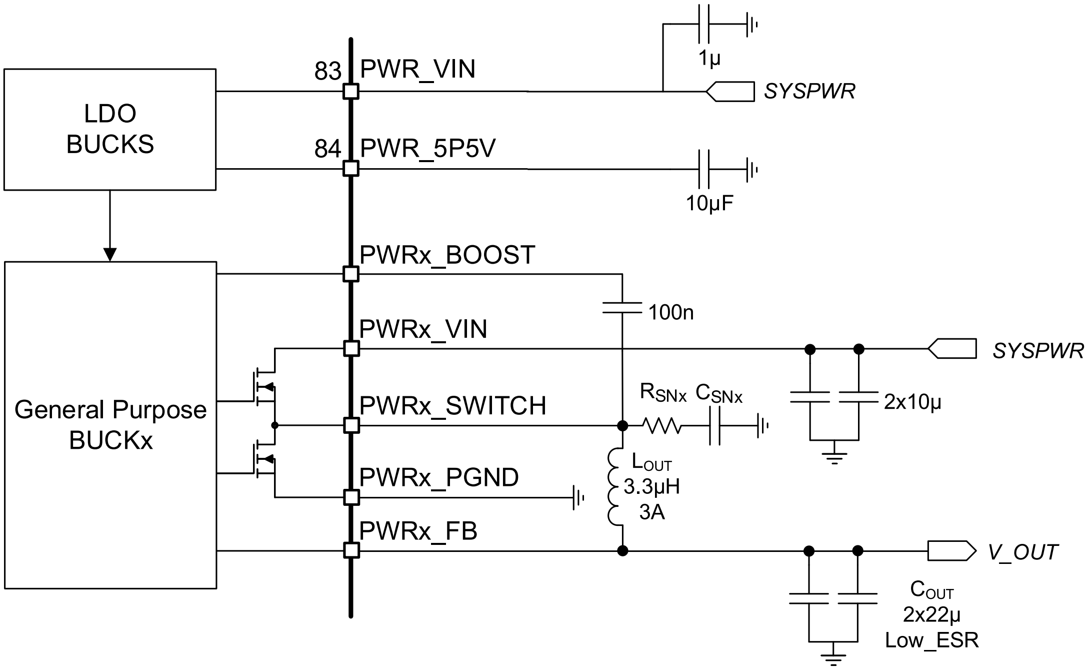


Figure 6-5. Buck Converter

6.3.3.1 LDO Bucks

This regulator supports the general-purpose buck converter and the two DMD/DLPC buck converters and provides an analog voltage of 5.5V to the internal circuitry. Use a 1µF capacitor on the input and a 10µF capacitor on the output of the LDO.

6.3.3.2 General Purpose Buck Converters

The buck converter is for general-purpose use (Figure 6-5). The converter can be enabled or disabled through Enable Register (0x01): BUCK_GP2_EN.

General purpose buck2 (PWR6) has a current capability of 2A.

The buck converter can operate in two switching modes: Normal, 600kHz switching frequency mode and the skip mode. The skip mode is designed to increase light load efficiency. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to the point that the current's rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the MOSFET's zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage.

6.3.3.3 Buck Converter Monitoring

The buck converter block is continuously monitored for system failures to prevent damage to the DLPA3082 and peripherals. Several possible failures are monitored such as a too high or too low output voltage. The possible faults are summarized in Table 6-2.

Table 6-2. Buck Converter Fault Indication

POWER GOOD		
BLOCK	**REGISTER BIT**	**THRESHOLD (RISING EDGE)**
Gen.Buck2	BUCK_GP2_PG_FAULT	Ratio 72%
OVERVOLTAGE		
Gen.Buck2	BUCK_GP2_OV_FAULT	Ratio 120%

6.3.3.3.1 Power Good

The buck converter as well as the supporting LDO_BUCK have a power good indication. The buck converter has a separate indication.

The power good for the buck converter indicates if the output voltage (PWR6_FB) is within a defined window. The relative power good ratio is 72%. This means that if the output voltage is below 72% of the set voltage the PG_fault bit is set high. The power good bit of the buck converter is in Detailed Status Register1 (0x27) bit:

- BUCK_GP2_PG_FAULT for BUCK2 (PWR6)

6.3.3.3.2 Overvoltage Fault

An overvoltage fault occurs when an output voltage rises above a predefined threshold. Overvoltage faults are indicated for the buck converter and LDO_BUCKS. The overvoltage fault of the LDO_BUCKS is asserted if the LDO voltage is above 7.2V. The overvoltage of the general-purpose buck converter is 120% of the set value and can be read through Detailed Status Register2 (0x28), bit BUCK_GP2_OV_FAULT.

6.3.3.4 Buck Converter Efficiency

Figure 6-6 shows an overview of the efficiency of the buck converter for an input voltage of 12V. The efficiency is shown for several output voltage levels where the load current is swept.

Figure 6-7 depicts the buck converter efficiency versus input voltage (V_{IN}) for a load current (I_{OUT}) of 1A for various output voltage levels (V_{OUT}).

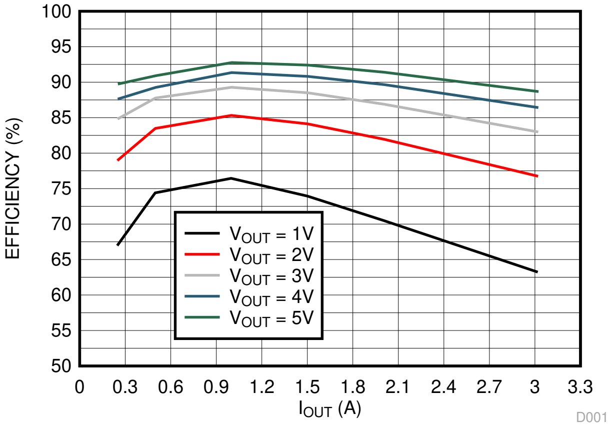


Figure 6-6. Buck Converter Efficiency vs I_{OUT} (V_{IN} = 12V)

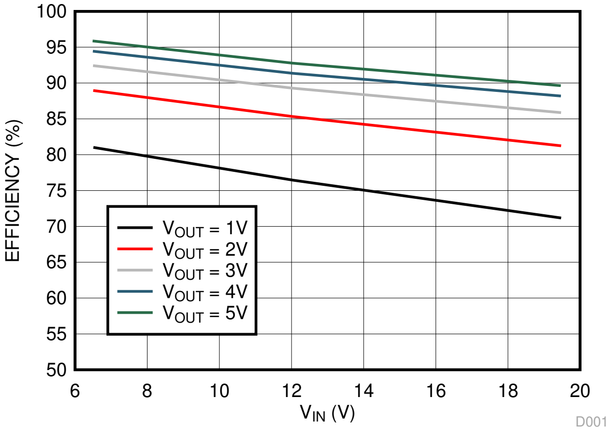


Figure 6-7. Buck Converter Efficiency vs V_{IN} (I_{OUT} = 1A) Schematic

6.3.4 Auxiliary LDOs

LDO_1 and LDO_2 are the two auxiliary LDOs that can be used by an additional external application. All other LDOs are for internal usage only and cannot be loaded. LDO_1 (PWR4) is a fixed voltage of 3.3V, while LDO_2 (PWR3) is a fixed voltage of 2.5V. Both LDOs are capable of delivering 200mA.

6.3.5 Measurement System

The measurement system (Figure 6-8) is designed to sense internal and external nodes and convert them to digital by the implemented AFE comparator. The reference signal for this comparator, ACMPR_REF, is a low-pass filtered PWM signal coming from the DLPC. To be able to cover a wide range of input signals, a variable gain amplifier (VGA) is added with three gain settings (1x, 9.5x, and 18x). The maximum input voltage of the VGA is 1.5V. However, some of the internal voltages are too large to be handled by the VGA and are divided down first.

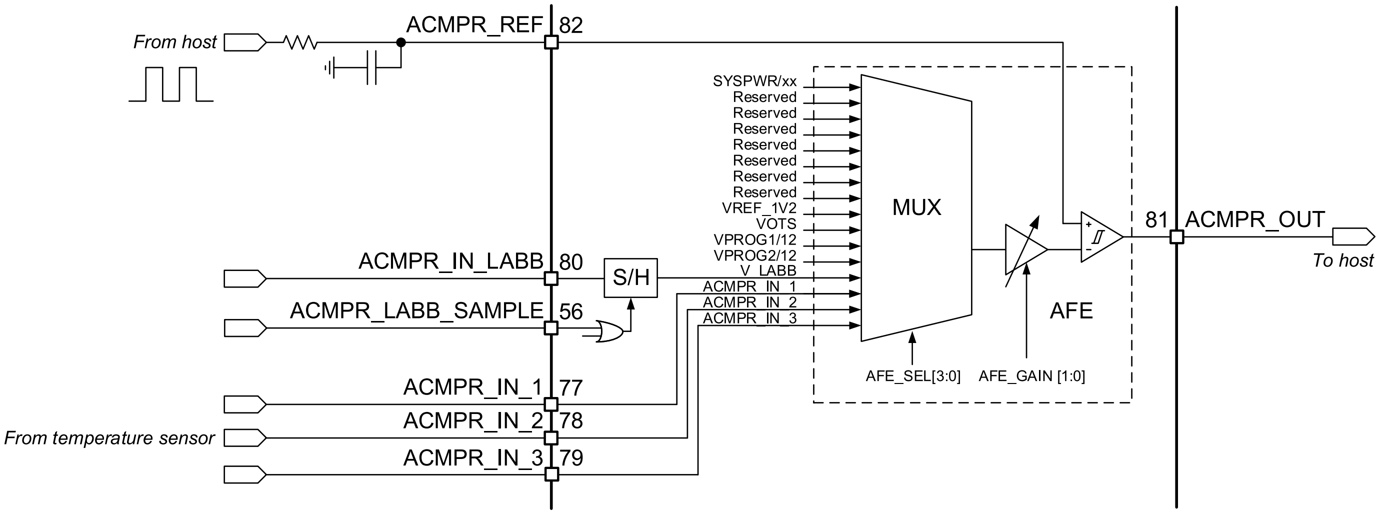


Figure 6-8. Measurement System Schematic

The system input voltage SYSPWR can be measured by selecting the SYSPWR/xx input of the MUX. Before the system input voltage is supplied to the MUX, the voltage needs to be divided. This is because the variable gain amplifier (VGA) can handle voltages up to 1.5V, whereas the system voltage can be as high as 20V. The division is done internally in the DLPA3082.

VOTS is connected to an on-chip temperature sensor. The voltage is a measure of the chip's junction temperature: Temperature (°C) = 300 × VOTS (V) – 270.

LABB is a feature that stands for Local Area Brightness Boost. LABB locally increases the brightness while maintaining good contrast and saturation. Connect the sensor this feature to pin ACMPR_IN_LABB.

ACMPR_IN_1,2,3 can measure external signals from for instance a temperature sensor. Ensure the voltage on the input does not exceed 1.5V.

6.4 Device Functional Modes

Table 6-3. Modes of Operation

MODE	DESCRIPTION
OFF	This is the lowest-power mode of operation. All power functions are turned off, registers are reset to default values, and the IC does not respond to SPI commands. RESET_Z pin is pulled low. The IC enters OFF mode whenever the PROJ_ON pin is low.
WAIT	The DMD regulators are turned off, but the IC does respond to the SPI. The device enters WAIT mode whenever PROJ_ON is set high, DMD_EN(1) bit is set to 0 or a FAULT is resolved.
STANDBY	The device also enters STANDBY mode when a fault condition is detected(2). (See Section 6.5.2). Once the fault condition is resolved, WAIT mode is entered.
ACTIVE	The DMD supplies are enabled. PROJ_ON pin must be high, DMD_EN bit must be set to 1.

(1) Settings can be done through Enable register, bit DMD_EN.
(2) Power-good faults, overvoltage, overtemperature shutdown, and undervoltage lockout.

Table 6-4. Device State as a Function of Control-Pin Status

PROJ_ON Pin	STATE
LOW	OFF
HIGH	WAIT STANDBY ACTIVE (Device state depends on DMD_EN bit and whether there are any fault conditions.)

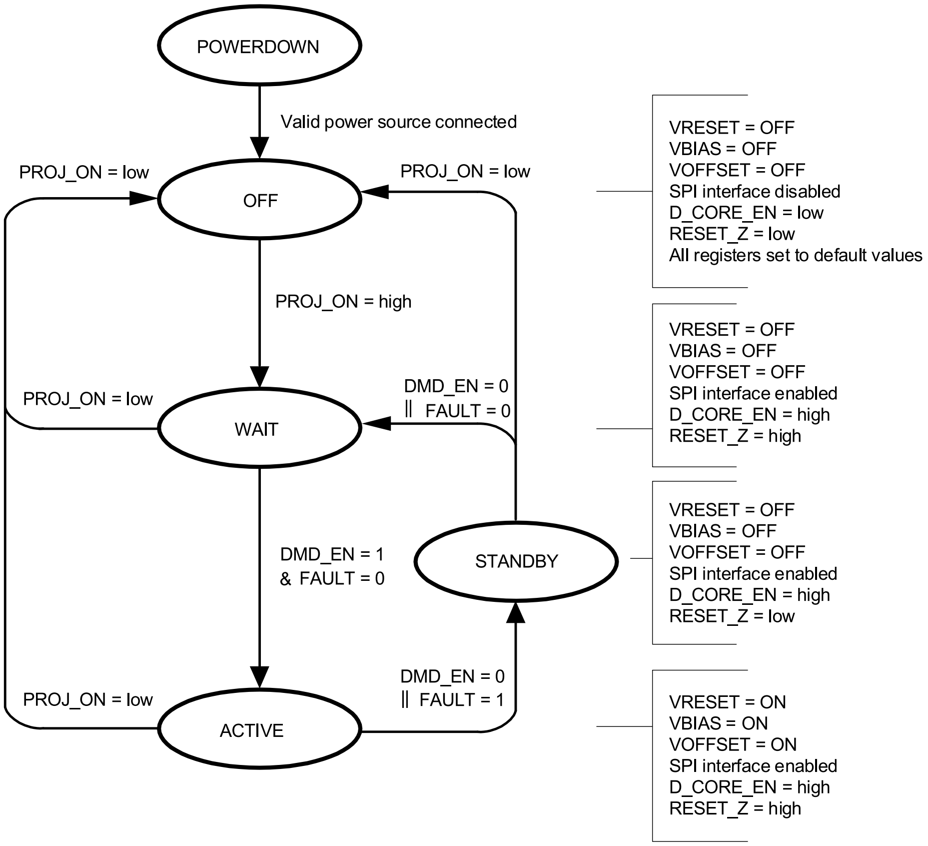


Figure 6-9. State Diagram

A. || = OR, & = AND
B. FAULT = Undervoltage on any supply, thermal shutdown, or UVLO detection
C. UVLO detection, per the diagram, causes the DLPA3082 to go into the standby state. This is not the lowest power state. If lower power is desired, PROJ_ON must be set low.
D. DMD_EN register bit can be reset or set by SPI writes. DMD_EN defaults to 0 when PROJ_ON goes from low to high and then the DLPC ASIC software automatically sets DMD_EN to 1. Also, FAULT = 1 causes the DMD_EN register bit to be reset.
E. D_CORE_EN is a signal internal to the DLPA3082. This signal turns on the VCORE regulator.

6.5 Programming

This section discusses the serial protocol interface (SPI) of the DLPA3082 as well as the interrupt handling, device shutdown, and register protection.

6.5.1 SPI

The DLPA3082 provides a 4-wire SPI port that supports two SPI clock frequency modes: 0MHz to 36MHz and 20MHz to 40MHz. The clock frequency mode can be set in register DIG_SPI_FAST_SEL. The interface supports both read and write operations. The SPI_SS_Z input serves as the active low chip select for the SPI port. The SPI_SS_Z input must be forced low for writing to or reading from registers. When SPI_SS_Z is forced high, the data at the SPI_MOSI input is ignored, and the SPI_MISO output is forced to a high-impedance state. The SPI_MOSI input serves as the serial data input for the port; the SPI_MISO output serves as the serial data output. The SPI_CLK input serves as the serial data clock for both the input and output data. Data at the SPI_MOSI input is latched on the rising edge of SPI_CLK, while data is clocked out of the SPI_MISO output on the falling edge of SPI_CLK. Figure 6-10 illustrates the SPI port protocol. Byte 0 is referred to as the command byte, where the most significant bit is the write/not-read bit. For the W/nR bit, a 1 indicates a write operation, while a 0 indicates a read operation. The remaining seven bits of the command byte are the register address targeted by the write or read operation. The SPI port supports write and read operations for multiple sequential register addresses through the implementation of an auto-increment mode. As shown in Figure 6-10, the auto-increment mode is invoked by simply holding the SPI_SS_Z input low for multiple data bytes. The register address is automatically incremented after each data byte transferred, starting with the address specified by the command byte. After reaching address 0x7Fh the address pointer jumps back to 0x00h.

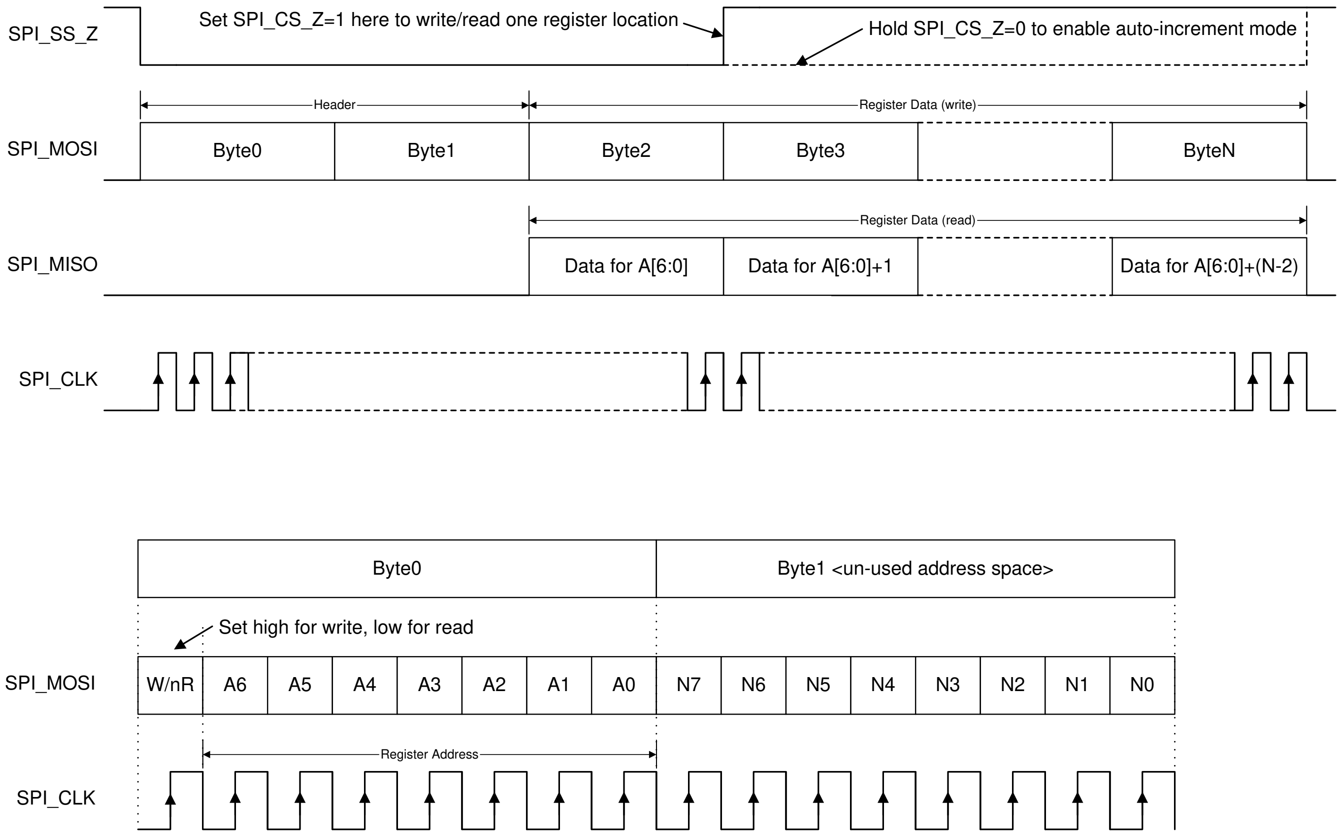


Figure 6-10. SPI Protocol

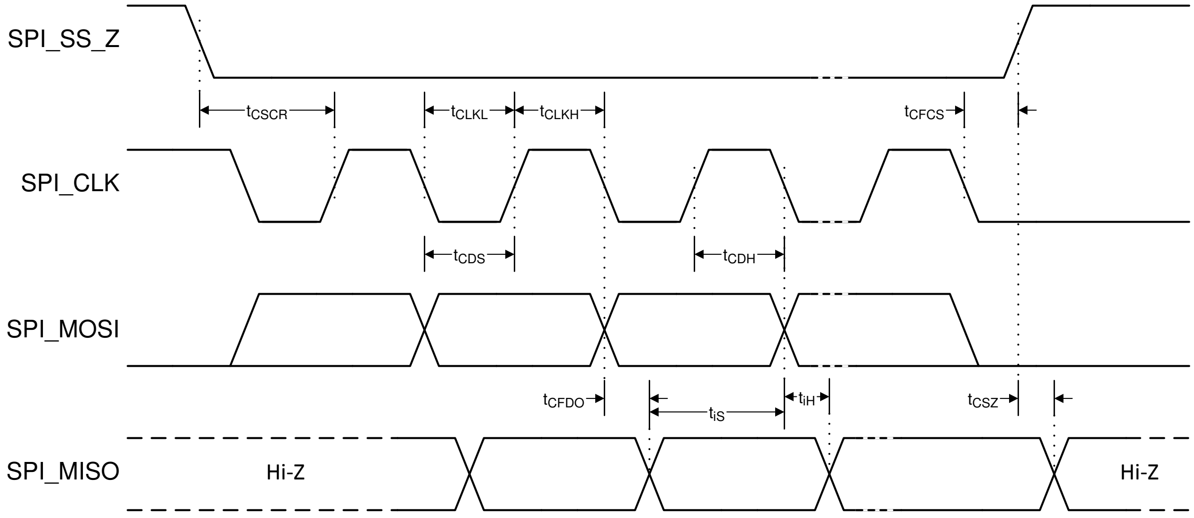


Figure 6-11. SPI Timing Diagram

6.5.2 Interrupt

The DLPA3082 has the capability to flag several faults in the system, such as overheating, power good, and overvoltage faults. If a certain fault condition occurs, one or more bits in the Table 6-5 are set. The setting of a bit in Main Status register (0x0C) triggers an interrupt event, which pulls down the INT_Z pin. Interrupts can be masked by setting the respective MASK bits in Interrupt Mask register . Setting a MASK bit prevents the INT_Z is pulled low for the particular fault condition. The high-level faults can be read in Main Status register (0x0C) , while the lower-level faults can be read in Detailed status register1 (0x27) through Detailed status register4 (0x2A). Table 6-5 provides an overview of the faults and how they are related.

Table 6-5. Interrupt Registers

HIGH-LEVEL	MID-LEVEL	LOW-LEVEL
SUPPLY_FAULT	DMD_FAULT	DMD_PG_FAULT
		BUCK_DMD1_PG_FAULT
		BUCK_DMD1_OV_FAULT
		BUCK_DMD2_PG_FAULT
		BUCK_DMD2_OV_FAULT
		LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT
		LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT
		LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT
		LDO_GP2_OV_FAULT / LDO_DMD2_OV_FAULT
	BUCK_GP2_PG_FAULT	
	BUCK_GP2_OV_FAULT	
PROJ_ON_INT		
TS_SHUT		
TS_WARN		

6.5.3 Fast-Shutdown in Case of Fault

The DLPA3082 has two shutdown modes: a normal shutdown initiated after pulling PROJ_ON level low and a fast power-down mode. The fast power-down feature can be enabled or disabled through register Main Status register (0x01), bit 7, FAST_SHUTDOWN_EN. By default, the mode is enabled.

When the fast power-down feature is enabled, a fast shutdown is initiated for specific faults. This shutdown happens autonomously from the DLPC. The DLPA3082 enters the fast-shutdown mode only for specific faults, thus not for all the faults flagged by the DLPA3082. The faults for which the DLPA3082 goes into fast shutdown are listed in Table 6-6.

Table 6-6. Faults that Trigger a Fast-Shutdown

HIGH-LEVEL	LOW-LEVEL
TS_SHUT	
DMD_FAULT	DMD_PG_FAULT
	BUCK_DMD1_PG_FAULT
	BUCK_DMD1_OV_FAULT
	BUCK_DMD2_PG_FAULT
	BUCK_DMD2_OV_FAULT
	LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT
	LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT
	LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT
	LDO_GP2_OV_FAULT / LDO_DMD2_OV_FAULT

6.6 Register Maps

Register Address, Default, R/W, Register name. **Boldface** settings are the hardwired defaults.

Table 6-7. Register Map

NAME	BITS	DESCRIPTION
0x00, 40, R/W, Chip Identification		
CHIPID	[7:4]	Chip identification number: 3 (hex)
REVID	[3:0]	Revision number, 0 (hex)
0x01, 82, R/W, Enable Register		
FAST_SHUTDOWN_EN	[7]	0: Fast shutdown disabled **1: Fast shutdown enabled**
CW_EN	[6]	Reserved
BUCK_GP3_EN	[5]	Reserved, value default as 0
BUCK_GP2_EN	[4]	**0: General purpose buck2 disabled** 1: General purpose buck2 enabled
BUCK_GP1_EN	[3]	Reserved, value default as 0
Reserved	[2]	Reserved
Reserved	[1]	Reserved
DMD_EN	[0]	**0: DMD regulators disabled** 1: DMD regulators enabled
0x0C, 00, R, Main Status Register		
SUPPLY_FAULT	[7]	**0: No PG or OV failures for any of the LV Supplies** 1: PG failures for a LV Supplies
Reserved	[6]	Reserved
PROJ_ON_INT	[5]	**0: PROJ_ON = HIGH** 1: PROJ_ON = LOW
DMD_FAULT	[4]	**0: DMD_FAULT = LOW** 1: DMD_FAULT = HIGH
BAT_LOW_SHUT	[3]	Reserved
BAT_LOW_WARN	[2]	Reserved
TS_SHUT	[1]	**0: Chip temperature < 132.5°C and no violation in V5V0** 1: Chip temperature > 156.5°C, or violation in V5V0
TS_WARN	[0]	**0: Chip temperature < 121.4°C** 1: Chip temperature > 123.4°C

Table 6-7. Register Map (continued)

NAME	BITS	DESCRIPTION
0x0D, F5, Interrupt Mask Register		
SUPPLY_FAULT_MASK	[7]	0: Not masked for SUPPLY_FAULT interrupt **1: Masked for SUPPLY_FAULT interrupt**
Reserved	[6]	Reserved
PROJ_ON_INT_MASK	[5]	0: Not masked for PROJ_ON_INT interrupt **1: Masked for PROJ_ON_INT interrupt**
DMD_FAULT_MASK	[4]	0: Not masked for DMD_FAULT interrupt **1: Masked for DMD_FAULT interrupt**
BAT_LOW_SHUT_MASK	[3]	Reserved, value default as 0
BAT_LOW_WARN_MASK	[2]	Reserved, value default as 1
TS_SHUT_MASK	[1]	**0: Not masked for TS_SHUT interrupt** 1: Masked for TS_SHUT interrupt
TS_WARN_MASK	[0]	0: Not masked for TS_WARN interrupt **1: Masked for TS_WARN interrupt**
0x27, 00, R, Detailed status register1 (Power good failures for general purpose block)		
BUCK_GP3_PG_FAULT	[7]	**Reserved, value default as 0**
BUCK_GP1_PG_FAULT	[6]	**Reserved, value default as 0**
BUCK_GP2_PG_FAULT	[5]	**0: No fault** 1: General purpose buck2 power good failure. Does not initiate a fast shutdown.
Reserved	[4]	Reserved
Reserved	[3]	Reserved
Reserved	[2]	Reserved
Reserved	[1]	**Reserved, value always 0**
Reserved	[0]	**Reserved, value always 0**
0x28, 00, R, Detailed status register2 (Overvoltage failures for general purpose block)		
BUCK_GP3_OV_FAULT	[7]	**Reserved, value default as 0**
BUCK_GP1_OV_FAULT	[6]	**Reserved, value default as 0**
BUCK_GP2_OV_FAULT	[5]	**0: No fault** 1: General purpose buck2 overvoltage failure. Does not initiate a fast shutdown.
Reserved	[4]	**Reserved, value always 0**
Reserved	[3]	Reserved
Reserved	[2]	Reserved
Reserved	[1]	**Reserved, value always 0**
Reserved	[0]	**Reserved, value always 0**
0x29, 00, R, Detailed status register3 (Power good failure for DMD related blocks)		
Reserved	[7]	**Reserved, value always 0**
DMD_PG_FAULT	[6]	**0: No fault** 1: VBIAS, VOFS and/or VRST power good failure. Initiates a fast shutdown.
BUCK_DMD1_PG_FAULT	[5]	**0: No fault** 1: Buck1 (used to create DMD voltages) power good failure. Initiates a fast shutdown.
BUCK_DMD2_PG_FAULT	[4]	**0: No fault** 1: Buck2 (used to create DMD voltages) power good failure. Initiates a fast shutdown.
Reserved	[3]	**Reserved, value always 0**
Reserved	[2]	**Reserved, value always 0**
LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT	[1]	**0: No fault** 1: LDO1 (used as general purpose or DMD specific LDO) power good failure. Initiates a fast shutdown.
LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT	[0]	**0: No fault** 1: LDO2 (used as general purpose or DMD specific LDO) power good failure. Initiates a fast shutdown.

Table 6-7. Register Map (continued)

NAME	BITS	DESCRIPTION
0x2A, 00, R, Detailed status register4 (Overvoltage failures for DMD related blocks and Color Wheel)		
Reserved	[7]	**Reserved, value always 0**
Reserved	[6]	**Reserved, value always 0**
BUCK_DMD1_OV_FAULT	[5]	**0: No fault** 1: Buck1 (used to create DMD voltage) overvoltage failure
BUCK_DMD2_OV_FAULT	[4]	**0: No fault** 1: Buck2 (used to create DMD voltage) overvoltage failure
Reserved	[3]	**Reserved, value always 0**
Reserved	[2]	**Reserved, value always 0**
LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT	[1]	**0: No fault** 1: LDO1 (used as general purpose or DMD specific LDO) overvoltage failure
LDO_GP2_OV_FAULT / LDO_DMD2_OV_FAULT	[0]	**0: No fault** 1: LDO2 (used as general purpose or DMD specific LDO) overvoltage failure

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

In display applications, using the DLPA3082 provides all needed analog functions. Each DLP application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC84xx DLP controller chips.

7.2 Typical Application

A common application when using DLPA3082 is to use it with a 0.47-inch 4K DMD (DLP472TP) and DLPC84xx controller for creating a small, ultra-portable projector. The DLPC84xx in the projector typically receives images from a PC or video player using HDMI or VGA analog as shown in Figure 7-1. Card readers and Wi-Fi can also receive images if the appropriate peripheral chips are added.

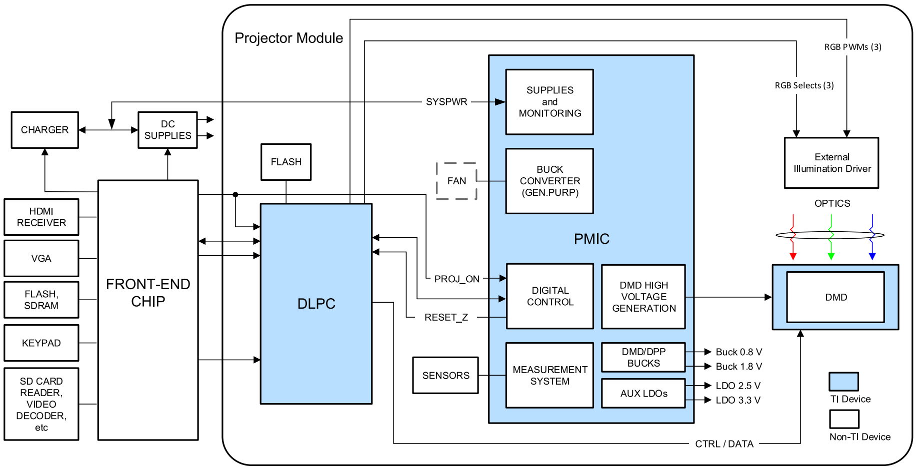


Figure 7-1. Typical Setup Using DLPA3082

7.2.1 Design Requirements

An ultra-portable projector can be created by using a DLP chipset comprised of a DMD, DLPC84xx controller, and the DLPA3082 PMIC. The DLPC84xx manages the digital image processing, the DLPA3082 provides the needed analog functions for the projector, and the DMD is the display device for producing the projected image. In addition to the three DLP chips in the chipset, other chips can be included. At a minimum, a Flash part is needed to store the software and firmware to control the DLPC84xx. To connect the DLPC84xx to the frontend chip for receiving images, use the parallel interface. While using the parallel interface, connect the I^2C to the frontend chip for inputting commands to the DLPC84xx.

The DLPA3082 has three built-in buck-switching regulators to serve as projector system power supplies. Two of the regulators are fixed to 0.8V and 1.8V for powering the DLP chipset. The remaining buck regulator is available for general-purpose use and its voltage is programmable. The regulator can be used to drive a variable-speed fan or to power other projector chips such as the frontend chip. The only power supply needed at the DLPA3082 input is SYSPWR from an external DC power supply. The entire projector can be turned on and off by using a single signal called PROJ_ON. When PROJ_ON is high, the projector turns on and begins displaying images. When PROJ_ON is set low, the projector turns off and draws just microamps of current on SYSPWR.

7.2.2 Detailed Design Procedure

To connect the 0.47-inch 4K DMD (DLP472TP), the DLPC84xx, and the DLPA3082 devices, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Layout guidelines must be followed to achieve reliable projector operation. The optical engine that has the illumination package and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

7.2.2.1 Component Selection for General-Purpose Buck Converter

The theory of operation of a buck converter is explained in application note, *Understanding Buck Power Stages in Switchmode Power Supplies*, SLVA057. This section is limited to the component selection. For proper operation, selection of the external components is very important, especially the inductor L_{OUT} and the output capacitor C_{OUT}. For best efficiency and ripple performance, choose an inductor and capacitor with low equivalent series resistance (ESR).

7.3 System Example with DLPA3082 Internal Block Diagram

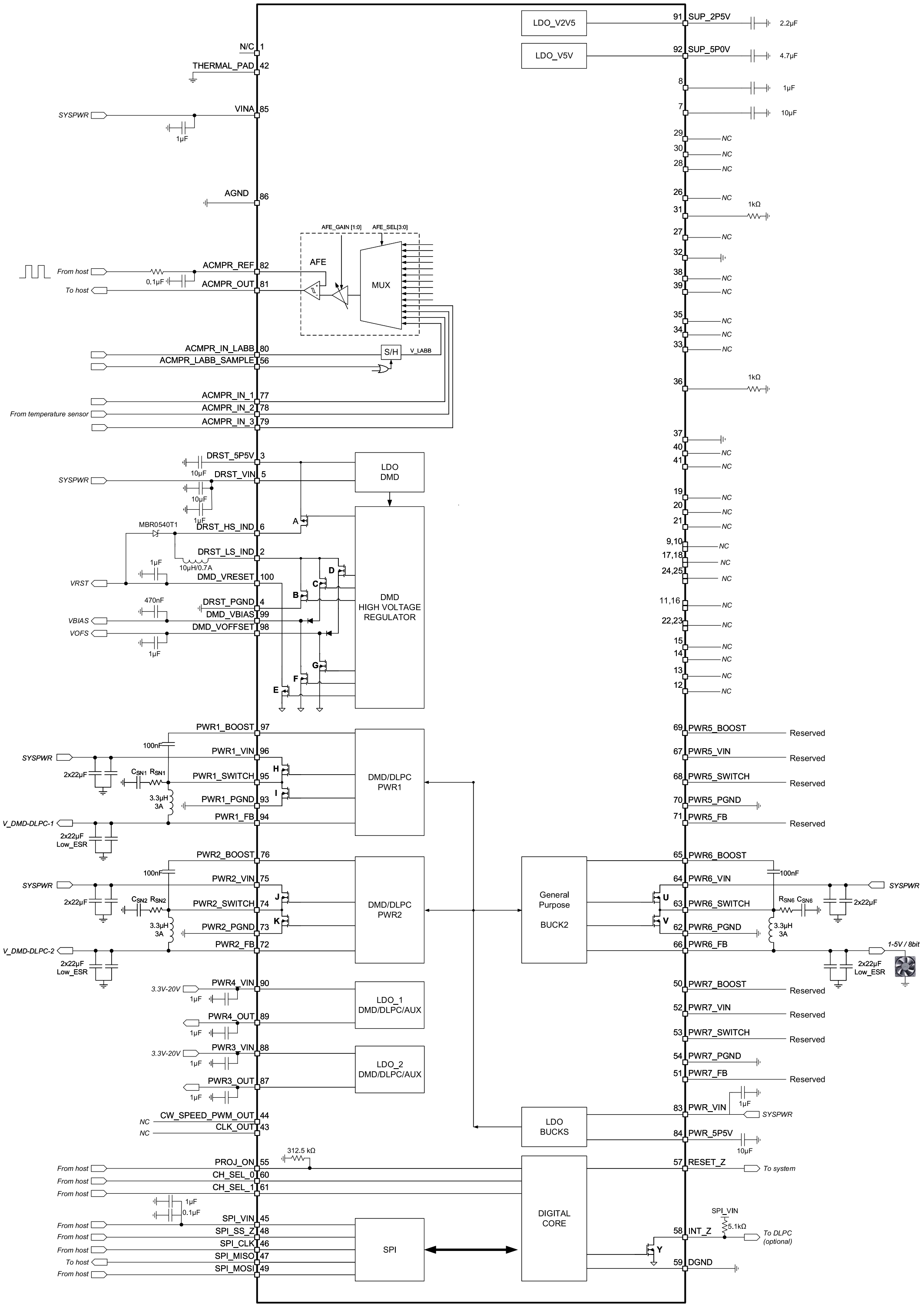


Figure 7-2. Typical Application: V_{IN} = 12V

7.4 Power Supply Recommendations

The DLPA3082 is designed to operate from a 6V to 20V input voltage supply. To avoid insufficient supply current due to line drop, ringing due to trace inductance at the VIN terminals, or supply peak current limitations, additional bulk capacitance is possibly required. In the case of ringing caused by the interaction with the ceramic input capacitors, an electrolytic or tantalum-type capacitor is needed for damping.

Evaluate the amount of bulk capacitance required, such that the input voltage can remain in spec long enough for a proper fast shutdown to occur for the VOFFSET, VRESET, and VBIAS supplies. The shutdown begins when the input voltage drops below the programmable UVLO threshold such as when the external power supply is suddenly removed from the system.

7.4.1 Power-Up and Power-Down Timing

The power-up and power-down sequence is important to ensure the correct operation of the DLPA3082 and to prevent damage to the DMD. The DLPA3082 controls the correct sequencing of the DMD_VRESET, DMD_VBIAS, and DMD_VOFFSET to ensure a reliable operation of the DMD.

The general startup sequence of the supplies is described in *Supply and Monitoring*. The power-up sequence of the high voltage DMD lines is especially important to not damage the DMD. Avoid a too large delta voltage between DMD_VBIAS and DMD_VOFFSET, which can cause damage.

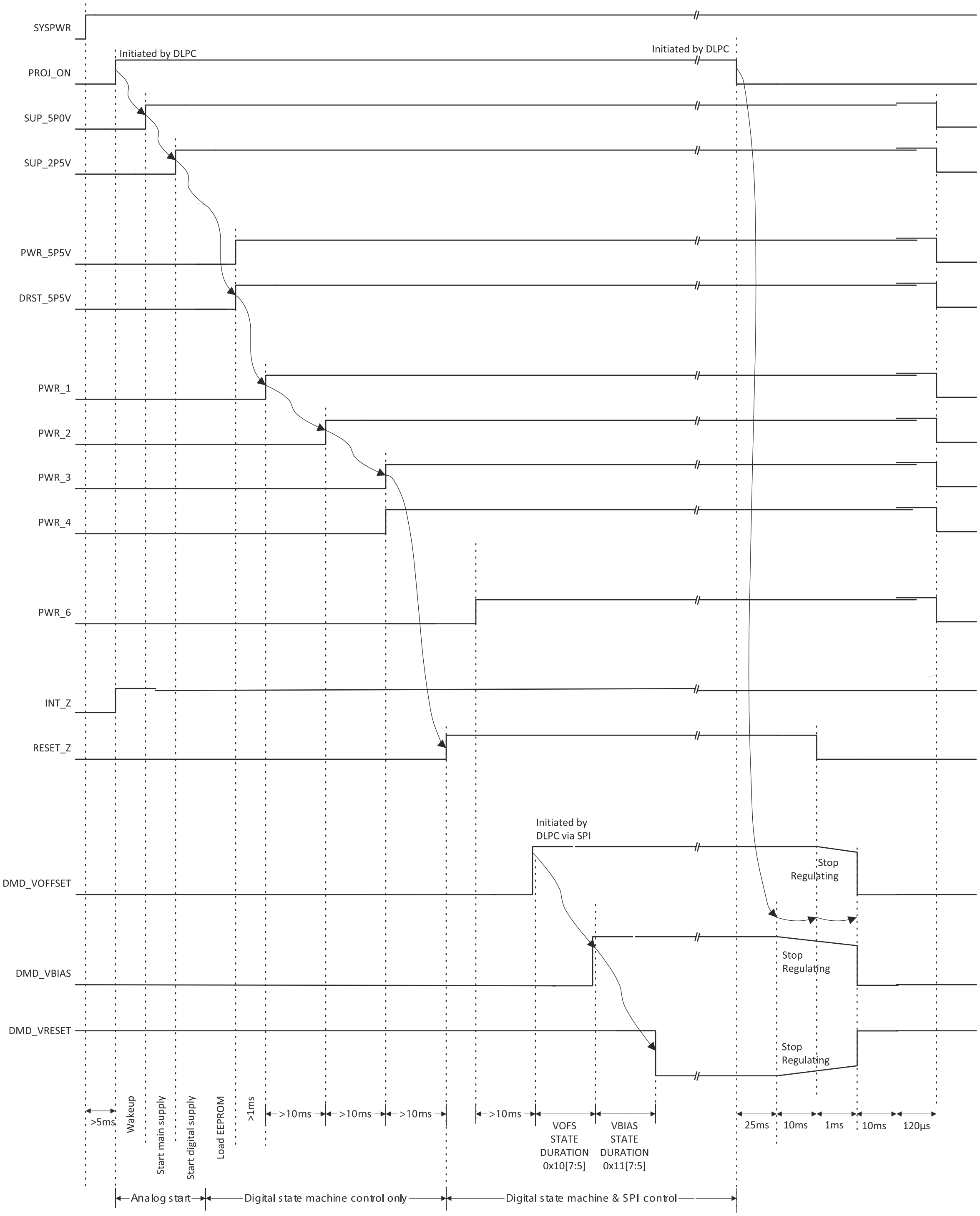
After PROJ_ON is pulled high, the DMD buck converters and LDOs are powered (PWR1-4) and the DMD high voltage lines (HV) are sequentially enabled. First, DMD_VOFFSET is enabled. After a delay, DMD_VBIAS is enabled. Finally, after another delayDMD_VRESET is enabled. Now the DLPA3082 is fully powered and ready for starting projection.

For power down there are two sequences, normal power down (Figure 7-3) and a fault fast power down used in case a fault occurs (Figure 7-4).

In normal power down mode, the power down is initiated after pulling PROJ_ON pin low. 25ms after PROJ_ON is pulled low, first DMD_VBIAS and DMD_VRESET stop regulating, 10ms later, DMD_VOFFSET stops regulating. When DMD_VOFFSET stopped regulating, RESET_Z is pulled low. 1ms after the DMD_VOFFSET stops regulating, all other supplies are turned off. INT_Z remains high during the power down sequence since no fault occurred. During power down it is ensured that the HV levels do not violate the DMD specifications on these three lines. For this to occur, it is important to select the capacitors such that $C_{VOFFSET}$ is equal to C_{VRESET} and C_{VBIAS} is ≤ $C_{VOFFSET}$, C_{VRESET}.

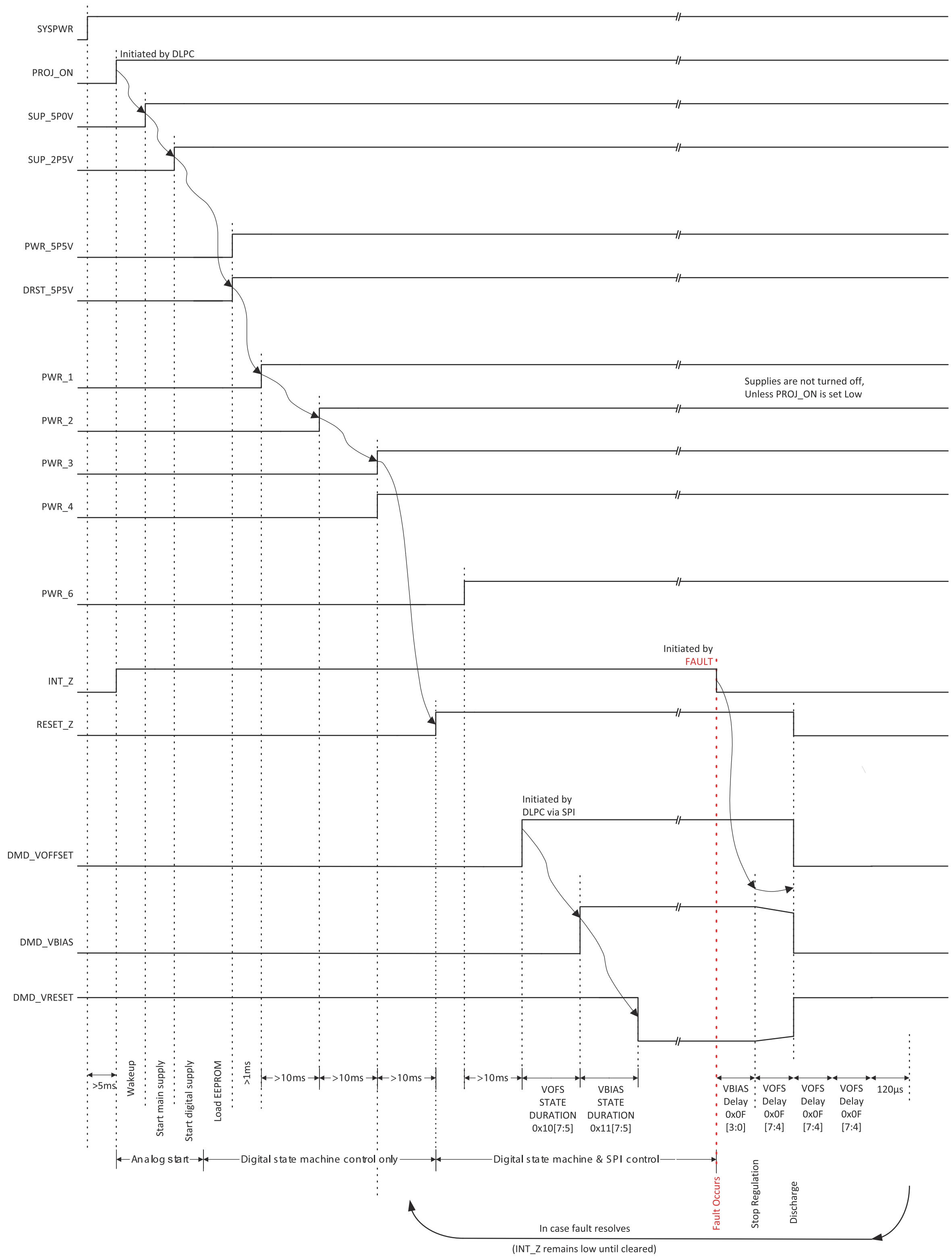
The fast power down mode (Figure 7-4) is started in case a fault occurs (INT_Z is pulled low), for instance, due to overheating. The fast power down mode can be enabled or disabled through Main Status register (0x01), bit 7, FAST_SHUTDOWN_EN. By default, the mode is enabled. After the fault occurs, the regulation of DMD_VBIAS and DMD_VRESET is stopped. There is 540µs default delay time between fault and stop of regulation. After the regulation stops, there is a 4µs default delay time before all three DMD_VRESET, DMD_VBIAS, and DMD_VOFFSET high voltages lines are discharged and RESET_Z is pulled low.

Now the DLPA3082 is in a standby state. It remains in standby state until the fault resolves. In case the fault resolves a restart is initiated. It starts then by powering up PWR_3 and follows the regular power-up as depicted in Figure 7-4. Again, for proper discharge timing and levels, the capacitors must be selected such that $C_{VOFFSET}$ is equal to C_{VRESET} and C_{VBIAS} is ≤ $C_{VOFFSET}$, C_{VBIAS}.



1. Arrows indicate the sequence of events automatically controlled by the digital state machine. Other events are initiated under SPI control.
2. SUP_5P0V and SUP_2P5V rise to a precharge level with SYSPWR, and reach the full level potential after PROJ_ON is pulled high.

Figure 7-3. Power Sequence Normal Shutdown Mode



1. Arrows indicate the sequence of events automatically controlled by the digital state machine. Other events are initiated under SPI control.
2. SUP_5P0V and SUP_2P5V rise to a precharge level with SYSPWR, and reach the full level potential after PROJ_ON is pulled high.

Figure 7-4. Power Sequence Fault Fast Shutdown Mode

7.5 Layout

7.5.1 Layout Guidelines

For switching power supplies, the layout is an important step in the design, especially when it concerns high peak currents and high switching frequencies. If the layout is not done carefully, the regulator can show stability issues and EMI problems. Therefore, use wide and short traces for high current paths and the return power ground paths. For the DMD HV regulator, place the input capacitor, output capacitor, and the inductor as close as possible to the IC. To minimize ground noise coupling between different buck converters, separate the grounds and connect them at a central point under the part. For the DMD HV regulator, the recommended value for the capacitors is 1μF for VRST and VOFS, and 470nF for VBIAS. The inductor value is 10μH.

The high currents of the buck converter concentrate around pins VIN, SWITCH, and PGND (Figure 7-5). The voltage at the pins VIN, PGNDm, and FB are DC voltages while the pin SWITCH has a switching voltage between VIN and PGND. In case the FET between pins 63–4 is closed, the red line indicates the current flow while the blue line indicates the current flow when the FET between pins 62–63 is closed.

These paths carry the highest currents and must be kept as short as possible.

For the LDO DMD, use a 1μF capacitor in parallel with a 10μF capacitor on the input and a 10μF capacitor on the output of the LDO. Make the voltage rating of the capacitor equal to or greater than two times the applied voltage across the capacitor in the application.

For LDO bucks, use a 1μF capacitor on the input and a 10μF capacitor on the output of the LDO. Make the voltage rating of the capacitor equal to or greater than two times the applied voltage across the capacitor in the application.

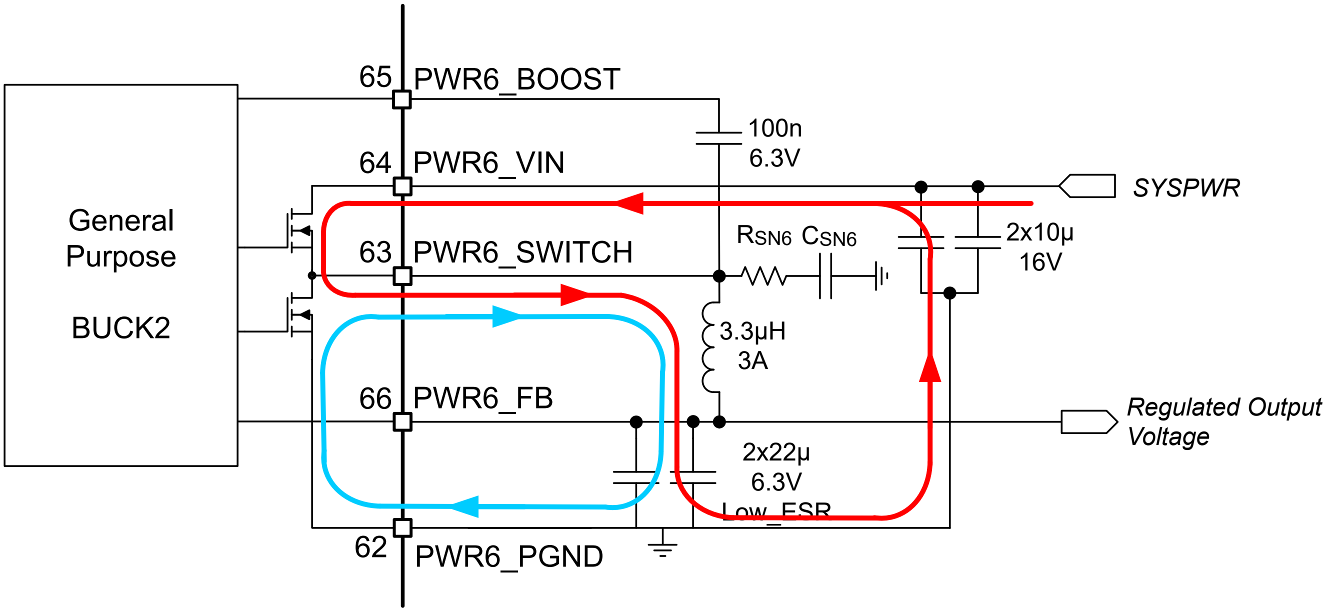


Figure 7-5. High AC Current Paths in a Buck Converter

The trace to the VIN pin carries high AC currents; therefore, the trace must be low resistive to prevent a voltage drop across the trace. Additionally, place the decoupling capacitors as close to the VIN pin as possible.

The SWITCH pin is connected alternately to the VIN or GND. This means a square wave voltage is present on the SWITCH pin with an amplitude of VIN, and containing high frequencies. This can lead to EMI problems if not properly handled. To reduce EMI problems, place a snubber network (RSN6 and CSN6) at the SWITCH pin to prevent and suppress unwanted high-frequency ringing at the moment of switching.

The PGND pin sinks high current. Connect the PGND pin to a star ground point so it does not interfere with other ground connections.

The FB pin is the sense connection for the regulated output voltage, which is a DC voltage; nothing flows through this pin. The voltage on the FB pin is compared with the internal reference voltage to control the loop. Make the FB connection at the load so that the I•R drop does not affect the sensed voltage.

7.5.1.1 SPI Connections

The SPI interface consists of several digital lines and the SPI supply. If routing the interface lines is not done properly, communication errors can occur. Prevent SPI lines from picking up noise and keep other possible interfering sources from the interface.

Pickup of noise can be prevented by ensuring that the SPI ground line is routed together with the digital lines as much as possible to the respective pins. The SPI interface can be connected by a separate ground connection to the DGND of the DLPA3082 in Figure 7-6. This prevents ground noise between SPI ground references of DLPA3082 and DLPC due to the high current in the system.

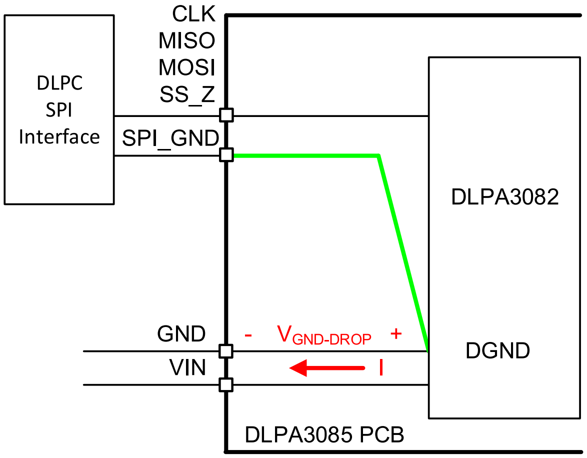


Figure 7-6. SPI Connections

Keep interfering sources away from the interface lines as much as possible. If any power lines are routed too close to the SPI_CLK, it can lead to false clock pulses and thus communication errors.

7.5.2 Layout Example

A layout example of a buck converter is shown in Figure 7-7, illustrating the optimal routing and placement of components around the DLPA3082. This can be used as a reference for a general-purpose buck2 (PWR6). The layout example illustrates the inductor and the accompanying capacitors as close as possible to the corresponding pins using the thickest possible traces. The capacitors use multiple vias to the ground layer to ensure a low resistance path and minimize the distance between the ground connections of the output capacitors and the ground connections of the buck converter.

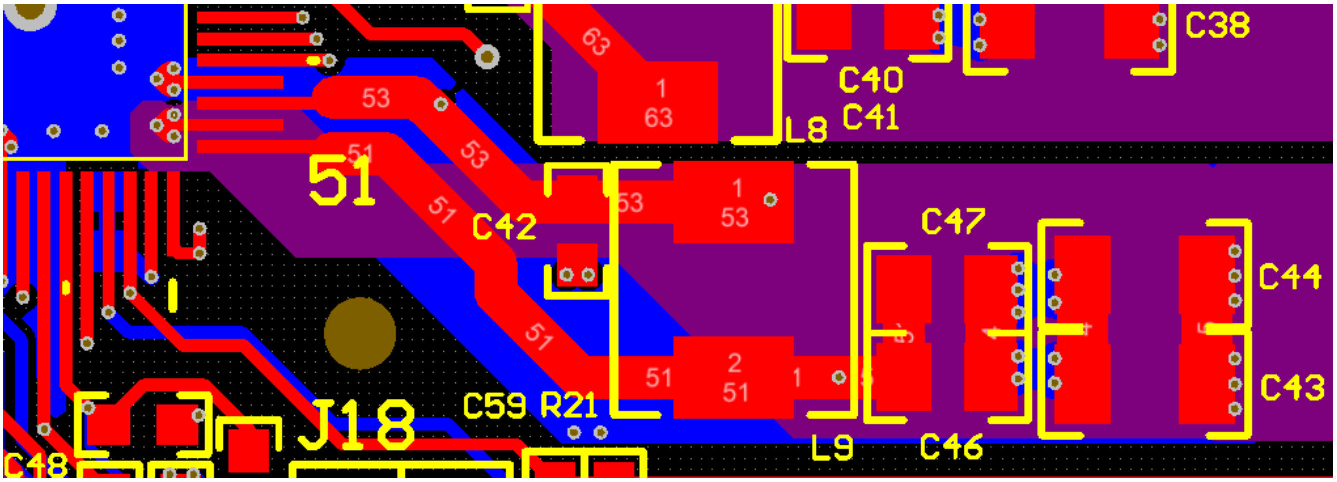


Figure 7-7. Practical Layout

A proper layout requires short traces and separate power grounds to avoid losses from trace resistance and to avoid ground shifting. Use high-quality capacitors with low ESR to keep capacitor losses minimal and to maintain an acceptable voltage ripple at the output.

Use an RC snubber network to avoid EMI that can occur when switching high currents at high frequencies. There is a possibility the EMI has a higher amplitude and frequency than the switching voltage.

7.5.3 Thermal Considerations

Power dissipation must be considered when implementing integrated circuits in low-profile and fine-pitch surface-mount packages. Many system-related issues affect power dissipation: thermal coupling, airflow, adding heat sinks and convection surfaces, and the presence of other heat-generating components. In general,there are three basic methods that can be used to improve thermal performance:

- Improving the heat-sinking capability of the PCB
- Reducing thermal resistance to the environment of the chip by adding or increasing heat sink capability on top of the package
- Adding or

  increasing

  airflow in the system

The recommended junction temperature for the DLPA3082 is below 120°C during operation. The equation that relates junction temperature, $T_{junction}$, is given by:

$$T_{junction} = T_{ambient} + P_{diss} \times R_{\theta JA} \quad (1)$$

where $T_{ambient}$ is the ambient temperature, P_{diss} is the total power dissipation, and $R_{\theta JA}$ is the thermal resistance from junction to ambient.

The total power dissipation can vary depending on the application of the DLPA3082. The main contributors in the DLPA3082 are typically:

- Buck converters
- LDOs

For the buck converter, the power dissipation is given by:

$$P_{diss\_buck} = P_{in} - P_{out} = P_{out}\left(\frac{1}{\eta_{buck}} - 1\right) \quad (2)$$

where η_{buck} is the efficiency of the buck converter, P_{in} is the power delivered to the input of the buck converter, and P_{out} is the power delivered to the load of the buck converter. For the buck converter PWR1,2,6, the efficiency can be determined using the curves in Figure 6-6.

For the LDO, the power dissipation is given by:

$$P_{diss\_LDO} = (V_{in} - V_{out}) \times I_{load} \tag{3}$$

where V_{in} is the input supply voltage, V_{out} is the output voltage of the LDO, and I_{load} is the load current of the LDO. The voltage drop over the LDO (V_{in}–V_{out}) can be relatively large; a small load current can result in significant power dissipation. For this situation, a general-purpose buck converter can be a more efficient solution.

The LDO DMD provides power to the boost converter, and the boost converter provides high voltages for the DMD; that is, V_{BIAS}, V_{OFS}, and V_{RST}. The current load on these lines can increase up to $I_{load,\ max}$ = 10mA. Assuming the efficiency of the boost converter, η_{boost} is 80%, the maximum boost converter power dissipation, $P_{diss\_DMD\_boost,\ max}$, can be calculated as:

$$P_{diss\_DMD\_boost,\max} = I_{load,\max}\left(V_{BIAS} + V_{OFS} + |V_{RST}|\right) \times \left(\frac{1}{\eta_{boost}} - 1\right) \approx 0.1W \tag{4}$$

In general, the power dissipation of the boost converter is negligible. However, the power dissipation of the LDO DMD, $P_{diss\_LDO\_DMD}$ must be considered in the case of a high supply voltage. The worst-case load current for the LDO is given by:

$$I_{load\_LDO,max} = \frac{1}{\eta_{boost}} \frac{\left(V_{BIAS} + V_{OFS} + |V_{RST}|\right)}{V_{DRST\_5P5V}} I_{load,max} \approx 100mA \tag{5}$$

where the output voltage of the LDO is V_{DRST_5P5V}= 5.5V.

The worst-case power dissipation of the LDO DMD is approximately 1.5W when the input supply voltage is 19.5V. For your specific application, check the LDO current level. Therefore, the total power dissipation of the DLPA3082 can be described as:

$$P_{diss\_DLPA3082} = \sum P_{buck\_converter} + \sum P_{LDOs} \tag{6}$$

The following examples calculate the maximum ambient temperature and the junction temperature based on known information.

If it is assumed that the total dissipation $P_{diss\_DLPA3082}$= 2.5W, $T_{junction,max}$= 120°C, and $R_{\theta JA}$= 7°C/W (refer to *Section 5.4*), then the maximum ambient temperature can be calculated using Equation 1.

$$T_{ambient,max} = T_{junction,max} - P_{diss} \times R_{\theta JA} = 120°C - 2.5W \times 7°C/W = 102.5°C \tag{7}$$

If the total power dissipation and the ambient temperature are known as:

$$T_{ambient} = 50°C,\ R_{\theta JA} = 7°C/W,\ P_{diss\_DLPA3082} = 4W. \tag{8}$$

the junction temperature can be calculated:

$$T_{junction} = T_{ambient} + P_{diss} \times R_{\theta JA} = 50°C + 4W \times 7°C/W = 78°C \tag{9}$$

If the combination of ambient temperature and the total power dissipation of the DLPA3082 does not produce an acceptable junction temperature, that is, <120°C, there are two approaches:

1. Use a larger heat sink or more airflow to reduce $R_{\theta JA}$.
2. Reduce power dissipation in DLPA3082:
    - Use an external buck converter instead of an internal general-purpose buck converter.
    - Reduce load current for the buck converter.

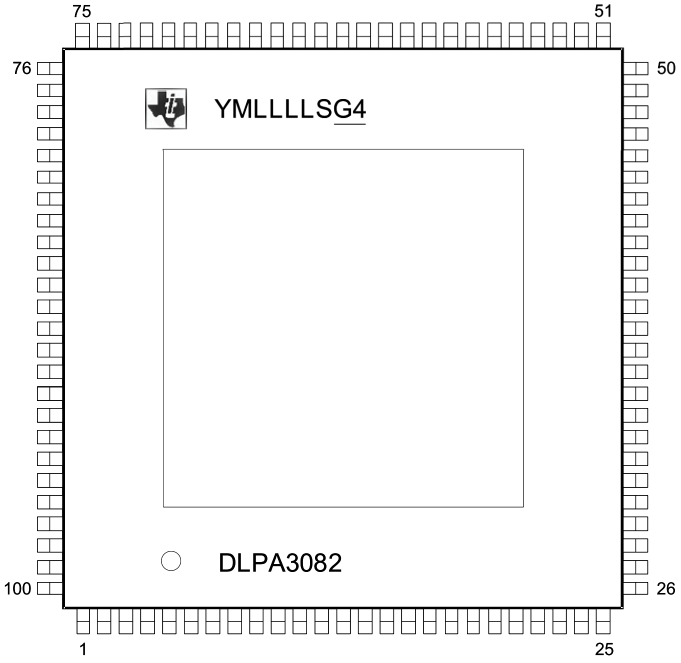
8 Device and Documentation Support

8.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

8.2 Device Support

8.2.1 Device Nomenclature



YM = YEAR / MONTH
LLLL = LOT TRACE CODE
S = ASSEMBLY SITE CODE
○ = pin 1 Marking (White Dot)

Figure 8-1. Package Marking DLPA3082 (Top View)

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

Pico™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
DLP® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLPA3082PFDR	Active	Production	HTQFP (PFD) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	DLPA3082
DLPA3082PFDR.B	Active	Production	HTQFP (PFD) | 100	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	DLPA3082

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

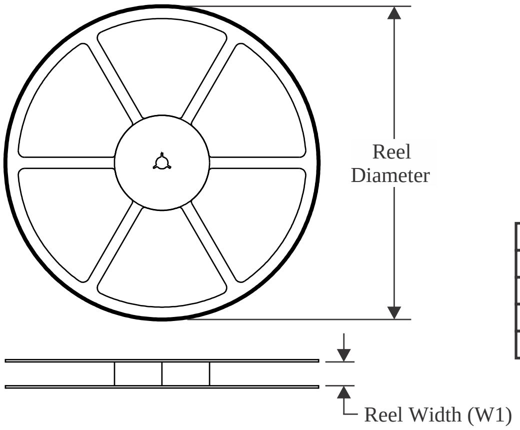
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

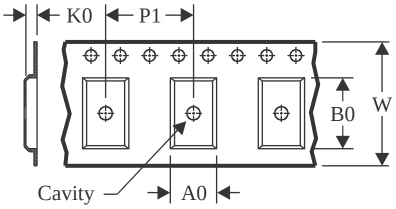
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

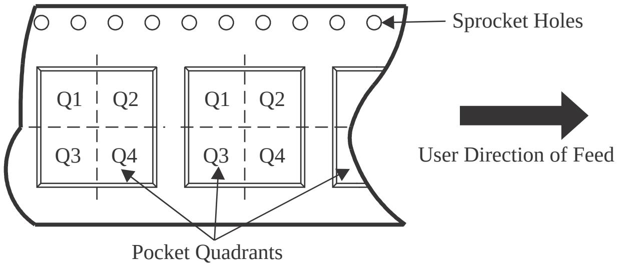


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

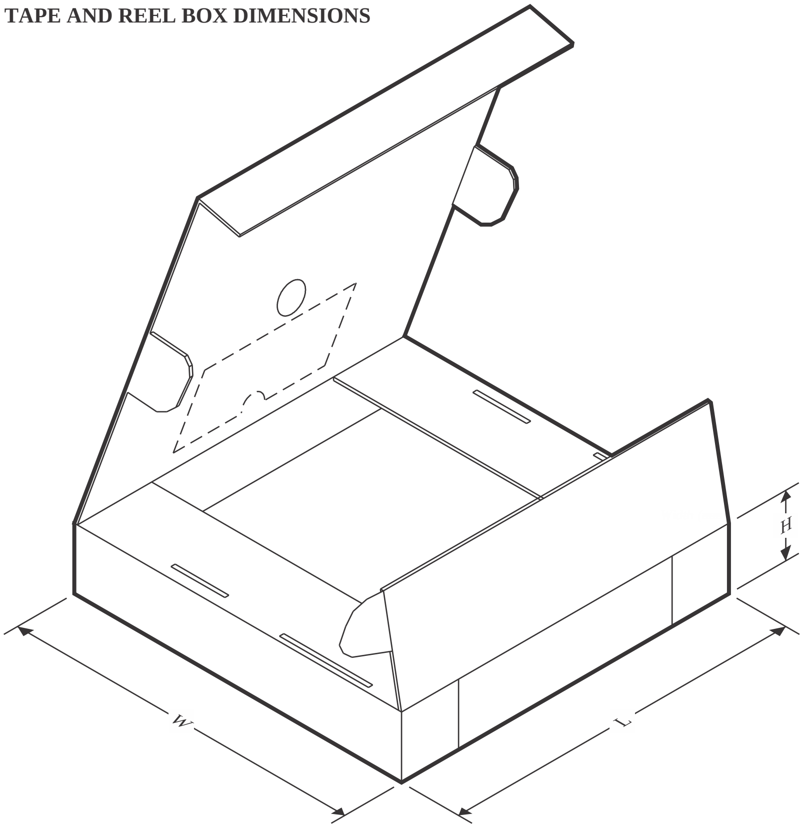
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DLPA3082PFDR	HTQFP	PFD	100	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

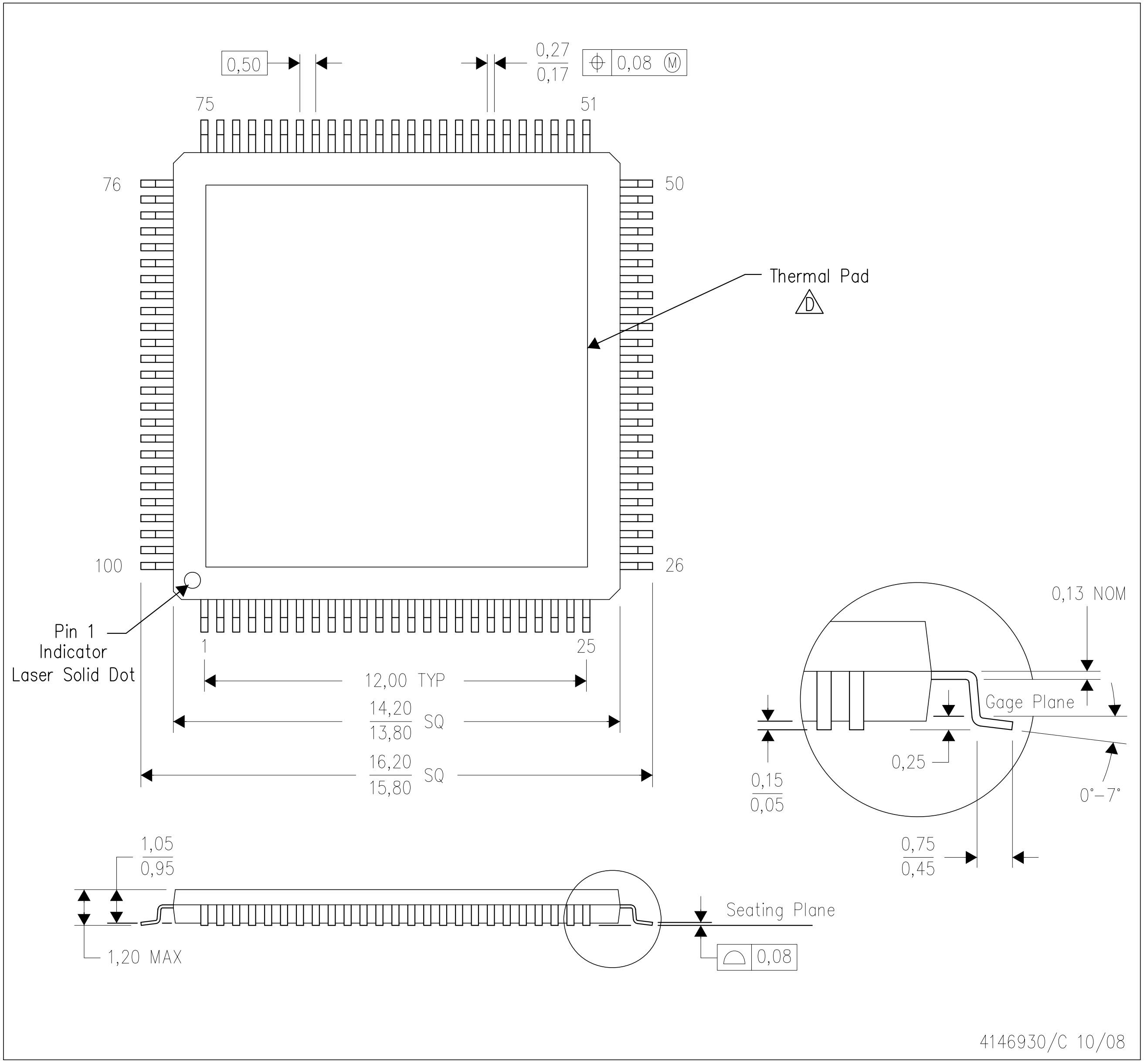
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DLPA3082PFDR	HTQFP	PFD	100	1000	350.0	350.0	43.0

PFD (S-PQFP-G100) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

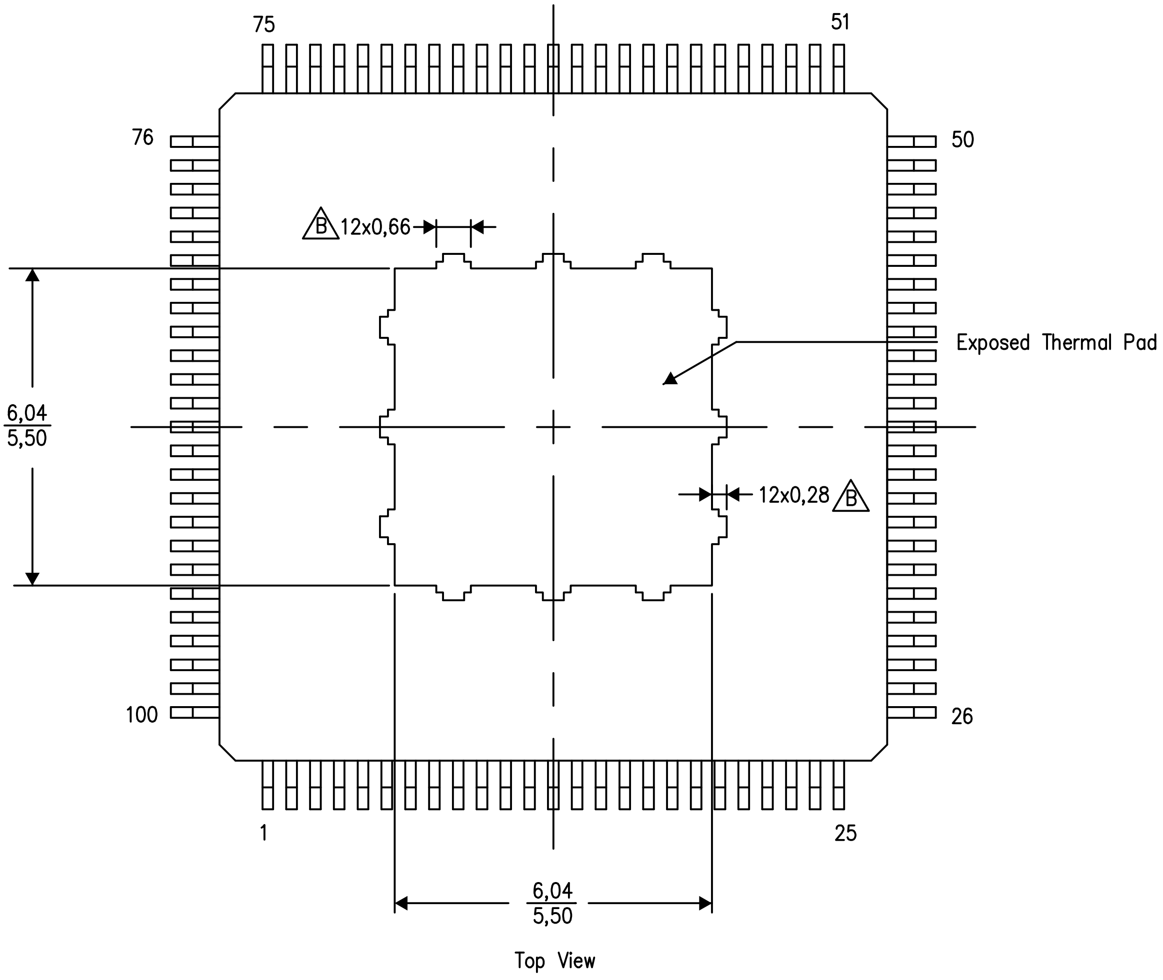
PFD (S-PQFP-G100) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

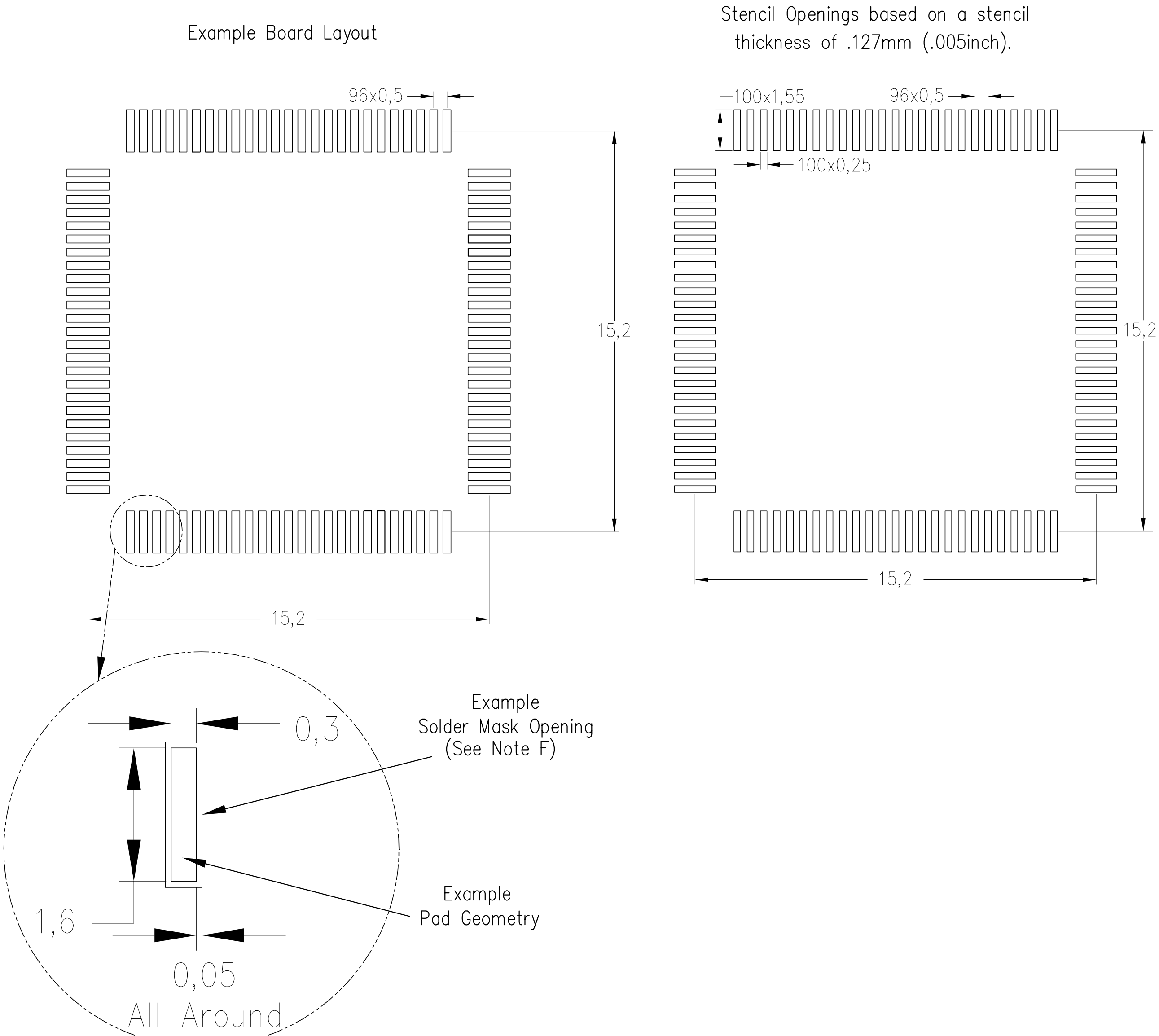
4211595-3/B 06/14

NOTE: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PFD (S-PQFP-G100) PowerPAD™ PLASTIC QUAD FLATPACK



4211596/A 03/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025