CC1350 SimpleLink™ Ultra-Low-Power Dual-Band Wireless MCU

1 Device Overview

1.1 Features

- World's First Dual-Band (Sub-1 GHz and 2.4 GHz) Wireless Microcontroller
- Microcontroller
  - Powerful Arm® Cortex®-M3 Processor
  - EEMBC CoreMark® Score: 142
  - EEMBC ULPBench™ Score: 158
  - Clock Speed up to 48-MHz
  - 128KB of In-System Programmable Flash
  - 8KB of SRAM for Cache (or as General-Purpose RAM)
  - 20KB of Ultra-Low-Leakage SRAM
  - 2-Pin cJTAG and JTAG Debugging
  - Supports Over-the-Air (OTA) Update
- Ultra-Low-Power Sensor Controller
  - Can Run Autonomously From the Rest of the System
  - 16-Bit Architecture
  - 2KB of Ultra-Low-Leakage SRAM for Code and Data
- Efficient Code-Size Architecture, Placing Parts of TI-RTOS, Drivers, *Bluetooth*® low energy Controller and Bootloader in ROM
- RoHS-Compliant Package
  - 7-mm × 7-mm RGZ VQFN48 (30 GPIOs)
  - 5-mm × 5-mm RHB VQFN32 (15 GPIOs)
  - 4-mm × 4-mm RSM VQFN32 (10 GPIOs)
- Peripherals
  - All Digital Peripheral Pins Can Be Routed to Any GPIO
  - Four General-Purpose Timer Modules (Eight 16-Bit or Four 32-Bit Timers, PWM Each)
  - 12-Bit ADC, 200 ksamples/s, 8-Channel Analog MUX
  - Continuous Time Comparator
  - Ultra-Low-Power Clocked Comparator
  - Programmable Current Source
  - UART
  - 2× SSI (SPI, MICROWIRE, TI)
  - I^2C, I2S
  - Real-Time Clock (RTC)
  - AES-128 Security Module
  - True Random Number Generator (TRNG)
  - Support for Eight Capacitive Sensing Buttons
  - Integrated Temperature Sensor
- External System
  - On-Chip Internal DC/DC Converter
  - Seamless Integration With the SimpleLink™ CC1190 and CC2592 Range Extender
- Low Power
  - Wide Supply Voltage Range: 1.8 to 3.8 V
  - RX: 5.4 mA (Sub-1 GHz), 6.4 mA (Bluetooth low energy, 2.4 GHz)
  - TX at +10 dBm: 13.4 mA (Sub-1 GHz)
  - TX at +9 dBm: 22.3 mA (Bluetooth low energy, 2.4 GHz)
  - TX at +0 dBm: 10.5 mA (Bluetooth low energy, 2.4 GHz)
  - Active-Mode MCU 48 MHz Running Coremark: 2.5 mA (51 µA/MHz)
  - Active-Mode MCU: 48.5 CoreMark/mA
  - Active-Mode Sensor Controller at 24 MHz: 0.4 mA + 8.2 µA/MHz
  - Sensor Controller, One Wakeup Every Second Performing One 12-Bit ADC Sampling: 0.95 µA
  - Standby: 0.7 µA (RTC Running and RAM and CPU Retention)
  - Shutdown: 185 nA (Wakeup on External Events)
- RF Section
  - 2.4-GHz RF Transceiver Compatible With Bluetooth low energy 4.2 Specification
  - Excellent Receiver Sensitivity –124 dBm Using Long-Range Mode, –110 dBm at 50 kbps (Sub-1 GHz), –87 dBm at Bluetooth low energy
  - Excellent Selectivity (±100 kHz): 56 dB
  - Excellent Blocking Performance (±10 MHz): 90 dB
  - Programmable Output Power up to +15 dBm (Sub-1 GHz) and +9 dBm at 2.4 GHz (Bluetooth low energy)
  - Single-Ended or Differential RF Interface
  - Suitable for Systems Targeting Compliance With Worldwide Radio Frequency Regulations
    - ETSI EN 300 220, EN 303 204 (Europe)
    - EN 300 440 Class 2 (Europe)
    - EN 300 328 (Europe)
    - FCC CFR47 Part 15 (US)
    - ARIB STD-T66 (Japan)
    - ARIB STD-T108 (Japan)

- Wireless M-Bus (EN 13757-4) and IEEE® 802.15.4g PHY
- Tools and Development Environment
  - Full-Feature and Low-Cost Development Kits
  - Multiple Reference Designs for Different RF Configurations
  - Packet Sniffer PC Software
  - Sensor Controller Studio
  - SmartRF™ Studio
  - SmartRF Flash Programmer 2
  - IAR Embedded Workbench® for Arm
  - Code Composer Studio™ (CCS) IDE
  - CCS UniFlash

1.2 Applications

- 315-, 433-, 470-, 500-, 779-, 868-, 915-, 920-MHz and 2.4-GHz ISM and SRD Systems
- Low-Power Wireless Systems With 50-kHz to 5-MHz Channel Spacing
- Home and Building Automation
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control
- Bluetooth low energy Beacon Management
- Bluetooth low energy Commissioning
- Smart Grid and Automatic Meter Reading
- Wireless Healthcare Applications
- Wireless Sensor Networks
- Active RFID
- IEEE 802.15.4g, IP-Enabled Smart Objects (6LoWPAN), Wireless M-Bus, KNX Systems, Wi-SUN™, and Proprietary Systems
- Energy-Harvesting Applications
- Electronic Shelf Label (ESL)
- Long-Range Sensor Applications
- Heat-Cost Allocators

1.3 Description

The CC1350 device is a cost-effective, ultra-low-power, dual-band RF device from Texas Instruments™ that is part of the SimpleLink™ microcontroller (MCU) platform. The platform consists of Wi-Fi®, *Bluetooth*® low energy, Sub-1 GHz, Ethernet, Zigbee®, Thread, and host MCUs. These devices all share a common, easy-to-use development environment with a single core software development kit (SDK) and a rich tool set. A one-time integration of the SimpleLink platform enables users to add any combination of devices from the portfolio into their design, allowing 100 percent code reuse when design requirements change. For more information, visit www.ti.com/simplelink.

With very low active RF and MCU current consumption, in addition to flexible low-power modes, the device provides excellent battery life and allows long-range operation on small coin-cell batteries and in energy harvesting applications.

The CC1350 is a device in the CC13xx and CC26xx family of cost-effective, ultra-low-power wireless MCUs capable of handling both Sub-1 GHz and 2.4-GHz RF frequencies. The CC1350 device combines a flexible, very low-power RF transceiver with a powerful 48-MHz Arm® Cortex®-M3 microcontroller in a platform supporting multiple physical layers and RF standards. A dedicated Radio Controller (Cortex®-M0) handles low-level RF protocol commands that are stored in ROM or RAM, thus ensuring ultra-low power and flexibility to handle both Sub-1 GHz protocols and 2.4 GHz protocols (for example Bluetooth low energy). This enables the combination of a Sub-1 GHz communication solution that offers the best possible RF range together with a Bluetooth low energy smartphone connection that enables great user experience through a phone application. The Sub-1 GHz only device in this family is the CC1310.

The CC1350 device is a highly integrated, true single-chip solution incorporating a complete RF system and an on-chip DC/DC converter.

Sensors can be handled in a very low-power manner by a dedicated autonomous ultra-low-power MCU that can be configured to handle analog and digital sensors; thus the main MCU (Arm® Cortex®-M3) can maximize sleep time.

The power and clock management and radio systems of the CC1350 device require specific configuration and handling by software to operate correctly, which has been implemented in the TI-RTOS. TI recommends using this software framework for all application development on the device. The complete TI-RTOS and device drivers are offered free of charge in source code.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CC1350F128RGZ	VQFN (48)	7.00 mm × 7.00 mm
CC1350F128RHB	VQFN (32)	5.00 mm × 5.00 mm
CC1350F128RSM	VQFN (32)	4.00 mm × 4.00 mm

(1) For more information, see Section 9.

1.4 Functional Block Diagram

Figure 1-1 shows a block diagram for the CC1350 device.

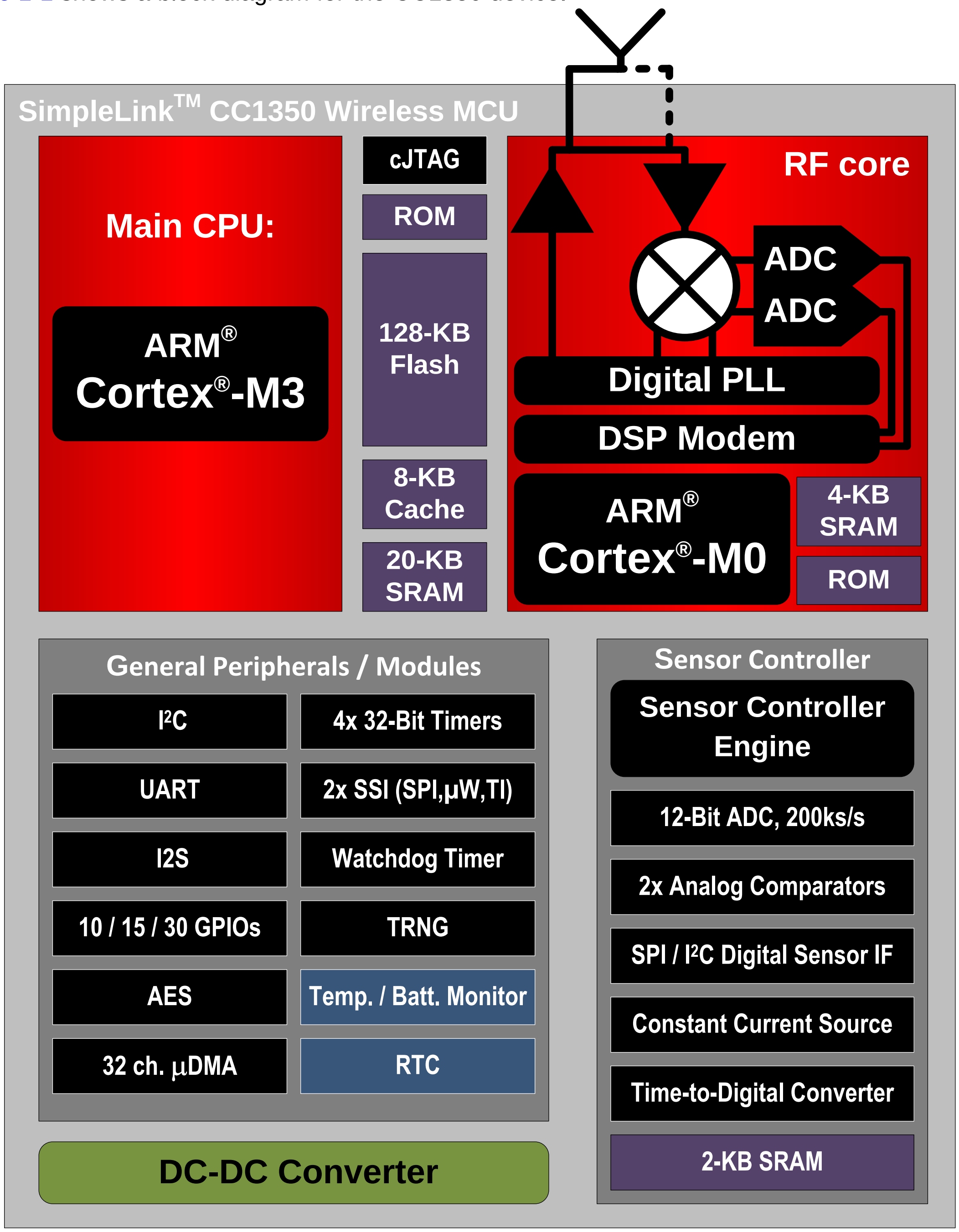

Figure 1-1. CC1350 Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 20, 2016 to July 13, 2018 **Page**

Changes from June 20, 2016 to November 20, 2016 **Page**

3 Device Comparison

Table 3-1 lists the device family overview.

Table 3-1. Device Family Overview

DEVICE	RADIO SUPPORT	FLASH (KB)	RAM (KB)	GPIOs	PACKAGE SIZE
CC1350F128RGZ	Proprietary, Wireless M-Bus, IEEE 802.15.4g, Bluetooth low energy	128	20	30	RGZ (7 mm × 7 mm VQFN48)
CC1350F128RHB	Proprietary, Wireless M-Bus, IEEE 802.15.4g, Bluetooth low energy	128	20	15	RHB (5 mm × 5 mm VQFN32)
CC1350F128RSM	Proprietary, Wireless M-Bus, IEEE 802.15.4g, Bluetooth low energy	128	20	10	RSM (4 mm × 4 mm VQFN32)
CC1310	Sub-1 GHz Proprietary, Wireless M-Bus, IEEE 802.15.4g	128 64/32	20 16	10-30	RGZ (7 mm × 7 mm VQFN48) RHB (5 mm × 5 mm VQFN32) RSM (4 mm × 4 mm VQFN32)
CC2640R2	Bluetooth 5 low energy 2.4-GHz proprietary FSK-based formats	128	20	10-31	RGZ (7 mm × 7 mm VQFN48) RHB (5 mm × 5 mm VQFN32) RSM (4 mm × 4 mm VQFN32) YFV (2.7 mm × 2.7 mm DSBGA34)
CC1312R	Sub-1 GHz Proprietary, Wireless M-Bus, IEEE 802.15.4g	352	80	30	RGZ (7 mm × 7 mm VQFN48)
CC1352R	Dual-band (2.4-GHz and Sub-1 GHz) Multiprotocol	352	80	28	RGZ (7 mm × 7 mm VQFN48)
CC2642R	Bluetooth 5 low energy 2.4-GHz proprietary FSK-based formats	352	80	31	RGZ (7 mm × 7 mm VQFN48)
CC2652R	Multiprotocol Bluetooth 5 low energy Zigbee Thread 2.4-GHz proprietary FSK-based formats	352	80	31	RGZ (7 mm × 7 mm VQFN48)

3.1 Related Products

Wireless Connectivity The wireless connectivity portfolio offers a wide selection of low-power RF solutions suitable for a broad range of application. The offerings range from fully customized solutions to turnkey offerings with precertified hardware and software (protocol).

Sub-1 GHz Long-range, low power wireless connectivity solutions are offered in a wide range of Sub-1 GHz ISM bands.

Companion Products Review products that are frequently purchased or used with this product.

4 Terminal Configuration and Functions

4.1 Pin Diagram – RSM Package

Figure 4-1 shows the RSM pinout diagram.

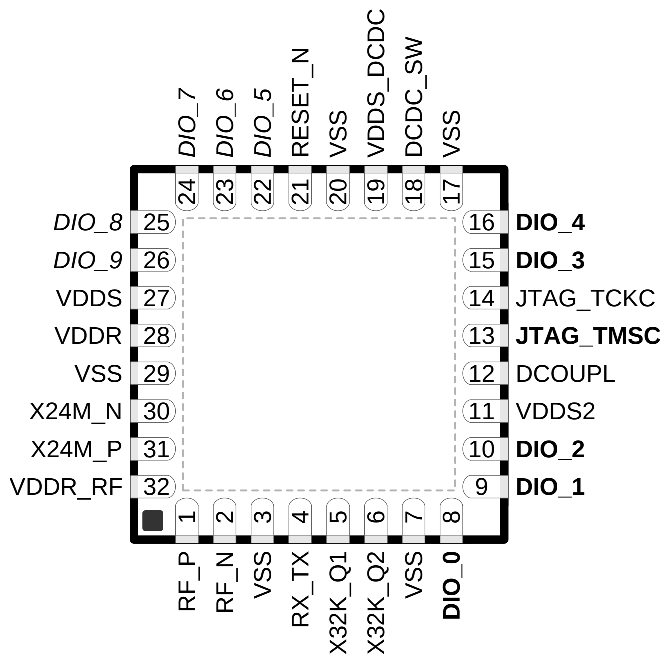

Figure 4-1. RSM (4-mm × 4-mm) Pinout, 0.4-mm Pitch
Top View

I/O pins marked in Figure 4-1 in **bold** have high-drive capabilities; they are as follows:

- Pin 8, DIO_0
- Pin 9, DIO_1
- Pin 10, DIO_2
- Pin 13, JTAG_TMSC
- Pin 15, DIO_3
- Pin 16, DIO_4

I/O pins marked in Figure 4-1 in *italics* have analog capabilities; they are as follows:

- Pin 22, DIO_5
- Pin 23, DIO_6
- Pin 24, DIO_7
- Pin 25, DIO_8
- Pin 26, DIO_9

4.2 Signal Descriptions – RSM Package

Table 4-1. Signal Descriptions – RSM Package

PIN		TYPE	DESCRIPTION
NAME	NO.		
DCDC_SW	18	Power	Output from internal DC/DC[1]
DCOUPL	12	Power	1.27-V regulated digital-supply decoupling capacitor[2]
DIO_0	8	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_1	9	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_2	10	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_3	15	Digital I/O	GPIO, high-drive capability, JTAG_TDO
DIO_4	16	Digital I/O	GPIO, high-drive capability, JTAG_TDI
DIO_5	22	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_6	23	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_7	24	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_8	25	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_9	26	Digital or analog I/O	GPIO, Sensor Controller, analog
EGP	–	Power	Ground; exposed ground pad
JTAG_TMSC	13	Digital I/O	JTAG TMSC
JTAG_TCKC	14	Digital I/O	JTAG TCKC[3]
RESET_N	21	Digital input	Reset, active low. No internal pullup.
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
RX_TX	4	RF I/O	Optional bias pin for the RF LNA
VDDS	27	Power	1.8-V to 3.8-V main chip supply[1]
VDDS2	11	Power	1.8-V to 3.8-V GPIO supply[1]
VDDS_DCDC	19	Power	1.8-V to 3.8-V DC/DC supply
VDDR	28	Power	1.7-V to 1.95-V supply, connect to output of internal DC/DC[2][4]
VDDR_RF	32	Power	1.7-V to 1.95-V supply, connect to output of internal DC/DC[2][5]
VSS	3, 7, 17, 20, 29	Power	Ground
X32K_Q1	5	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	6	Analog I/O	32-kHz crystal oscillator pin 2
X24M_N	30	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	31	Analog I/O	24-MHz crystal oscillator pin 2

(1) See the technical reference manual listed in Section 8.3 for more details.
(2) Do not supply external circuitry from this pin.
(3) For design consideration regrading noise immunity for this pin, see the *JTAG Interface* chapter in the *CC13x0, CC26x0 SimpleLink™ Wireless MCU Technical Reference Manual*.
(4) If internal DC/DC is not used, this pin is supplied internally from the main LDO.
(5) If internal DC/DC is not used, this pin must be connected to VDDR for supply from the main LDO.

4.3 Pin Diagram – RHB Package

Figure 4-2 shows the RHB pinout diagram.

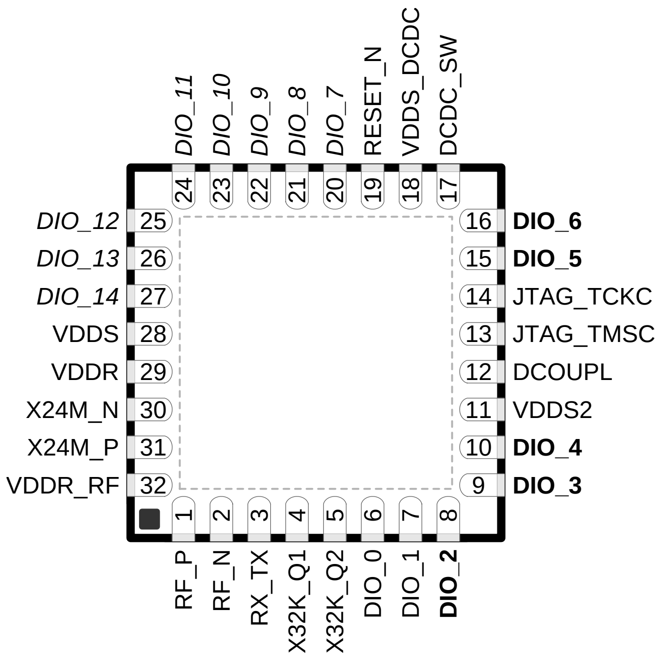

Figure 4-2. RHB (5-mm × 5-mm) Pinout, 0.5-mm Pitch
Top View

I/O pins marked in Figure 4-2 in **bold** have high-drive capabilities; they are as follows:

- Pin 8, DIO_2
- Pin 9, DIO_3
- Pin 10, DIO_4
- Pin 15, DIO_5
- Pin 16, DIO_6

I/O pins marked in Figure 4-2 in *italics* have analog capabilities; they are as follows:

- Pin 20, DIO_7
- Pin 21, DIO_8
- Pin 22, DIO_9
- Pin 23, DIO_10
- Pin 24, DIO_11
- Pin 25, DIO_12
- Pin 26, DIO_13
- Pin 27, DIO_14

4.4 Signal Descriptions – RHB Package

Table 4-2. Signal Descriptions – RHB Package

PIN		TYPE	DESCRIPTION
NAME	NO.		
DCDC_SW	17	Power	Output from internal DC/DC(1)
DCOUPL	12	Power	1.27-V regulated digital-supply decoupling(2)
DIO_0	6	Digital I/O	GPIO, Sensor Controller
DIO_1	7	Digital I/O	GPIO, Sensor Controller
DIO_2	8	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_3	9	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_4	10	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_5	15	Digital I/O	GPIO, high-drive capability, JTAG_TDO
DIO_6	16	Digital I/O	GPIO, high-drive capability, JTAG_TDI
DIO_7	20	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_8	21	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_9	22	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_10	23	Digital or analog I/O	GPIO, Sensor Controller, Analog
DIO_11	24	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_12	25	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_13	26	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_14	27	Digital or analog I/O	GPIO, Sensor Controller, analog
EGP	–	Power	Ground; exposed ground pad
JTAG_TMSC	13	Digital I/O	JTAG TMSC, high-drive capability
JTAG_TCKC	14	Digital I/O	JTAG TCKC(3)
RESET_N	19	Digital input	Reset, active low. No internal pullup.
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
RX_TX	3	RF I/O	Optional bias pin for the RF LNA
VDDR	29	Power	1.7-V to 1.95-V supply, connect to output of internal DC/DC(2)(4)
VDDR_RF	32	Power	1.7-V to 1.95-V supply, connect to output of internal DC/DC(2)(5)
VDDS	28	Power	1.8-V to 3.8-V main chip supply(1)
VDDS2	11	Power	1.8-V to 3.8-V GPIO supply(1)
VDDS_DCDC	18	Power	1.8-V to 3.8-V DC/DC supply
X24M_N	30	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	31	Analog I/O	24-MHz crystal oscillator pin 2
X32K_Q1	4	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	5	Analog I/O	32-kHz crystal oscillator pin 2

(1) For more details, see the technical reference manual listed in Section 8.3.
(2) Do not supply external circuitry from this pin.
(3) For design consideration regrading noise immunity for this pin, see the *JTAG Interface* chapter in the *CC13x0, CC26x0 SimpleLink™ Wireless MCU Technical Reference Manual*.
(4) If internal DC/DC is not used, this pin is supplied internally from the main LDO.
(5) If internal DC/DC is not used, this pin must be connected to VDDR for supply from the main LDO.

4.5 Pin Diagram – RGZ Package

Figure 4-3 shows the RGZ pinout diagram.

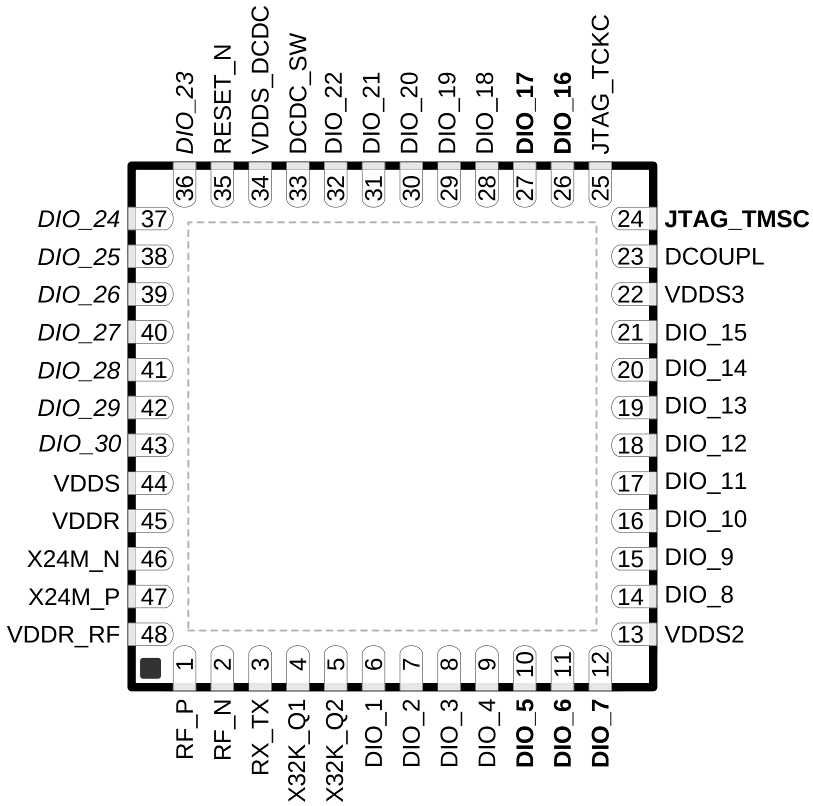

Figure 4-3. RGZ (7-mm × 7-mm) Pinout, 0.5-mm Pitch
Top View

I/O pins marked in Figure 4-3 in **bold** have high-drive capabilities; they are as follows:

- Pin 10, DIO_5
- Pin 11, DIO_6
- Pin 12, DIO_7
- Pin 24, JTAG_TMSC
- Pin 26, DIO_16
- Pin 27, DIO_17

I/O pins marked in Figure 4-3 in *italics* have analog capabilities; they are as follows:

- Pin 36, DIO_23
- Pin 37, DIO_24
- Pin 38, DIO_25
- Pin 39, DIO_26
- Pin 40, DIO_27
- Pin 41, DIO_28
- Pin 42, DIO_29
- Pin 43, DIO_30

4.6 Signal Descriptions – RGZ Package

Table 4-3. Signal Descriptions – RGZ Package

PIN		TYPE	DESCRIPTION
NAME	NO.		
DCDC_SW	33	Power	Output from internal DC/DC(1)(2)
DCOUPL	23	Power	1.27-V regulated digital-supply (decoupling capacitor)(2)
DIO_1	6	Digital I/O	GPIO, Sensor Controller
DIO_2	7	Digital I/O	GPIO, Sensor Controller
DIO_3	8	Digital I/O	GPIO, Sensor Controller
DIO_4	9	Digital I/O	GPIO, Sensor Controller
DIO_5	10	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_6	11	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_7	12	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_8	14	Digital I/O	GPIO
DIO_9	15	Digital I/O	GPIO
DIO_10	16	Digital I/O	GPIO
DIO_11	17	Digital I/O	GPIO
DIO_12	18	Digital I/O	GPIO
DIO_13	19	Digital I/O	GPIO
DIO_14	20	Digital I/O	GPIO
DIO_15	21	Digital I/O	GPIO
DIO_16	26	Digital I/O	GPIO, JTAG_TDO, high-drive capability
DIO_17	27	Digital I/O	GPIO, JTAG_TDI, high-drive capability
DIO_18	28	Digital I/O	GPIO
DIO_19	29	Digital I/O	GPIO
DIO_20	30	Digital I/O	GPIO
DIO_21	31	Digital I/O	GPIO
DIO_22	32	Digital I/O	GPIO
DIO_23	36	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_24	37	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_25	38	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_26	39	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_27	40	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_28	41	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_29	42	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_30	43	Digital or analog I/O	GPIO, Sensor Controller, analog
EGP	–	Power	Ground; exposed ground pad
JTAG_TMSC	24	Digital I/O	JTAG TMSC, high-drive capability
JTAG_TCKC	25	Digital I/O	JTAG TCKC(3)
RESET_N	35	Digital input	Reset, active-low. No internal pullup.
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX

(1) See technical reference manual listed in Section 8.3 for more details.
(2) Do not supply external circuitry from this pin.
(3) For design consideration regrading noise immunity for this pin, see the *JTAG Interface* chapter in the *CC13x0, CC26x0 SimpleLink™ Wireless MCU Technical Reference Manual*.

Table 4-3. Signal Descriptions – RGZ Package (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
VDDR	45	Power	1.7-V to 1.95-V supply, connect to output of internal DC/DC[2][4]
VDDR_RF	48	Power	1.7-V to 1.95-V supply, connect to output of internal DC/DC[2][5]
VDDS	44	Power	1.8-V to 3.8-V main chip supply[1]
VDDS2	13	Power	1.8-V to 3.8-V DIO supply[1]
VDDS3	22	Power	1.8-V to 3.8-V DIO supply[1]
VDDS_DCDC	34	Power	1.8-V to 3.8-V DC/DC supply
X24M_N	46	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	47	Analog I/O	24-MHz crystal oscillator pin 2
RX_TX	3	RF I/O	Optional bias pin for the RF LNA
X32K_Q1	4	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	5	Analog I/O	32-kHz crystal oscillator pin 2

(4) If internal DC/DC is not used, this pin is supplied internally from the main LDO.
(5) If internal DC/DC is not used, this pin must be connected to VDDR for supply from the main LDO.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

		MIN	MAX	UNIT
Supply voltage (VDDS, VDDS2, and VDDS3)		–0.3	4.1	V
Voltage on any digital pin[3][4]		–0.3	VDDSn + 0.3, max 4.1	V
Voltage on crystal oscillator pins X32K_Q1, X32K_Q2, X24M_N, and X24M_P		–0.3	VDDR + 0.3, max 2.25	V
Voltage on ADC input (V_{in})	Voltage scaling enabled	–0.3	VDDS	V
	Voltage scaling disabled, internal reference	–0.3	1.49	
	Voltage scaling disabled, VDDS as reference	–0.3	VDDS / 2.9	
Input RF level			10	dBm
Storage temperature (T_{stg})		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground, unless otherwise noted.
(3) Including analog-capable DIO.
(4) Each pin is referenced to a specific VDDSn (VDDS, VDDS2 or VDDS3). For a pin-to-VDDS mapping table, see Table 6-3.

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS001[1]	All pins	±3000	V
		Charged device model (CDM), per JESD22-C101[2]	All pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Ambient temperature			–40	85	°C
Operating supply voltage (VDDS)	For operation in battery-powered and 3.3-V systems (internal DC/DC can be used to minimize power consumption)		1.8	3.8	V
Operating supply voltages (VDDS2 and VDDS3)		VDDS < 2.7 V	1.8	3.8	V
Operating supply voltages (VDDS2 and VDDS3)		VDDS ≥ 2.7 V	1.9	3.8	V
Rising supply voltage slew rate			0	100	mV/µs
Falling supply voltage slew rate			0	20	mV/µs
Falling supply voltage slew rate, with low-power flash setting[1]				3	mV/µs
Positive temperature gradient in standby[2]	No limitation for negative temperature gradient, or outside standby mode			5	°C/s

(1) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-µF VDDS input capacitor must be used to ensure compliance with this slew rate.
(2) Applications using RCOSC_LF as sleep timer must also consider the drift in frequency caused by a change in temperature (see).

5.4 Power Consumption Summary

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design unless otherwise noted. T_c = 25°C, V_{DDS} = 3.6 V with DC/DC enabled, unless otherwise noted. Using boost mode (increasing VDDR to 1.95 V), will increase currents in this table by 15% (does not apply to TX 14-dBm setting where this current is already included).

PARAMETER		TEST CONDITIONS	TYP	UNIT
I_{core}	Core current consumption	Reset. RESET_N pin asserted or VDDS below power-on-reset threshold	100	nA
		Shutdown. No clocks running, no retention	185	
		Standby. With RTC, CPU, RAM, and (partial) register retention. RCOSC_LF	0.7	µA
		Standby. With RTC, CPU, RAM, and (partial) register retention. XOSC_LF	0.8	
		Idle. Supply Systems and RAM powered.	570	
		Active. MCU running CoreMark at 48 MHz	1.2 mA + 25.5 µA/MHz	
		Active. MCU running CoreMark at 48 MHz	2.5	mA
		Active. MCU running CoreMark at 24 MHz	1.9	
		Radio RX, measured on CC1350EM-7XD-Dual Band reference design, 868 MHz	5.4	mA
		Radio RX, measured on CC1350EM-7XD-Dual Band reference design, Bluetooth low energy, 2440 MHz	6.4	mA
		Radio TX, 10-dBm output power, (G)FSK, 868 MHz	13.4	mA
		Radio TX, 10-dBm output power, measured on CC1350EM-7XD-DualBand reference design, 868 MHz	14.2	mA
		Radio TX, OOK modulation, 10-dBm output power, AVG, 868 MHz	11.2	mA
		Radio TX, boost mode (VDDR = 1.95 V), 14-dBm output power, (G)FSK, 868 MHz	23.5	mA
		Radio TX, boost mode (VDDR = 1.95 V), 14-dBm output power, measured on CC1350EM-7XD-Dual Band reference design, 868 MHz	24.4	mA
		Radio TX, OOK modulation, boost mode (VDDR = 1.95 V), 14-dBm, AVG, 868 MHz	14.8	mA
		Radio TX Bluetooth low energy, 0-dBm output power, measured on CC1350EM-7XD-DualBand reference design, 2440 MHz	10.5	mA
		Radio TX Bluetooth low energy, boost mode (VDDR = 1.95 V), 9-dBm output power, measured on CC1350EM-7XD-Dual Band reference design, 2440 MHz	22.3	mA
		Radio TX, boost mode (VDDR = 1.95 V), 15-dBm output power, (G)FSK, measured on CC1310EM-7XD-4251, 433.92 MHz	25.1	mA
		Radio TX, 10-dBm output power, measured on CC1310EM-7XD-4251, 433.92 MHz	13.2	mA
PERIPHERAL CURRENT CONSUMPTION				
I_{peri}	Peripheral power domain	Delta current with domain enabled	20	µA
	Serial power domain	Delta current with domain enabled	13	
	RF core	Delta current with power domain enabled, clock enabled, RF core idle	237	
	µDMA	Delta current with clock enabled, module idle	130	
	Timers	Delta current with clock enabled, module idle	113	
	I^2C	Delta current with clock enabled, module idle	12	
	I2S	Delta current with clock enabled, module idle	36	
	SSI	Delta current with clock enabled, module idle	93	
	UART	Delta current with clock enabled, module idle	164	

5.5 RF Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
Frequency bands	287 (1)		351 (1)	MHz
	359 (1)		439 (1)	
	431		527	
	718 (1)		878 (1)	
	861		1054	
	2152		2635	

(1) These frequency bands are functionally verified. Radio settings for specific physical layer parameters can be made available upon request.

5.6 Receive (RX) Parameters, 861 MHz to 1054 MHz

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC/DC enabled, f_{RF} = 868 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Data rate			Up to 4 Mbps		bps
Data rate offset tolerance, IEEE 802.15.4g PHY	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-3}		1600		ppm
Data rate step size			1.5		bps
Digital channel filter programmable bandwidth	Using VCO divide by 5 setting	40		4000	kHz
Receiver sensitivity, 50 kbps	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}. 868 MHz and 915 MHz		–110		dBm
Receiver saturation	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		10		dBm
Selectivity, ±200 kHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		44, 47		dB
Selectivity, ±400 kHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		48, 53		dB
Blocking ±1 MHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		59, 62		dB
Blocking ±2 MHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		64, 65		dB
Blocking ±5 MHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		67, 68		dB
Blocking ±10 MHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		76, 76		dB
Spurious emissions 1 GHz to 13 GHz (VCO leakage at 3.5 GHz) and 30 MHz to 1 GHz	Conducted emissions measured according to ETSI EN 300 220		–70		dBm

Receive (RX) Parameters, 861 MHz to 1054 MHz *(continued)*

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC/DC enabled, f_{RF} = 868 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Image rejection (image compensation enabled, the image compensation is calibrated in production), 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		44		dB
RSSI dynamic range	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode). Starting from the sensitivity limit. This range will give an accuracy of ±2 dB.		95		dB
RSSI accuracy	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode). Starting from the sensitivity limit across the given dynamic range.		±2		dB
Receiver sensitivity, 500 kbps	GFSK, 175-kHz deviation, 1.243-MHz RX bandwidth, BER = 10^{-2}		–97		dBm
Blocking, ±2 MHz, 500 kbps	Wanted signal 3 dB above sensitivity limit. 500 kbps, GFSK, 175-kHz deviation, 1.243-MHz RX bandwidth, BER = 10^{-2}		35, 36		dB
Blocking, ±10 MHz, 500 kbps	Wanted signal 3 dB above sensitivity limit. 500 kbps, GFSK, 175-kHz deviation, 1.243-MHz RX bandwidth, BER = 10^{-2}		55, 47		dB
Receiver sensitivity, long-range mode, 5 kbps	20 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 2, 49-kHz RX bandwidth, BER = 10^{-2}. 868 MHz and 915 MHz		–119		dBm
Receiver sensitivity, long-range mode, 2.5 kbps	20 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 4, 49-kHz RX bandwidth, BER = 10^{-2}. 868 MHz and 915 MHz		–120		dBm
Receiver sensitivity, long-range mode, 1.25 kbps	20 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 49-kHz RX bandwidth, BER = 10^{-2}. 868 MHz and 915 MHz		–121		dBm
Selectivity, ±100 kHz, long-range mode, 5 kbps	Wanted signal 3 dB above sensitivity limit. 20 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 2, 49-kHz RX bandwidth, BER = 10^{-2}		47, 47		dB
Selectivity, ±200 kHz, long-range mode, 5 kbps	Wanted signal 3 dB above sensitivity limit. 20 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 2, 49-kHz RX bandwidth, BER = 10^{-2}		54, 55		dB
Selectivity, ±300 kHz, long-range mode, 5 kbps	Wanted signal 3 dB above sensitivity limit. 20 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 2, 49-kHz RX bandwidth, BER = 10^{-2}		57, 56		dB
Blocking, ±1 MHz, long-range mode, 5 kbps	Wanted signal 3 dB above sensitivity limit. 20 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 2, 49-kHz RX bandwidth, BER = 10^{-2}		68, 67		dB
Blocking, ±2 MHz, long-range mode, 5 kbps	Wanted signal 3 dB above sensitivity limit. 20 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 2, 49-kHz RX bandwidth, BER = 10^{-2}		74, 74		dB
Blocking, ±10 MHz, long-range mode, 5 kbps	Wanted signal 3 dB above sensitivity limit. 20 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 2, 49-kHz RX bandwidth, BER = 10^{-2}		85, 85		dB
Image rejection (image compensation enabled, the image compensation is calibrated in production), long-range mode, 5 kbps	Wanted signal 3 dB above sensitivity limit. 20 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 2, 49-kHz RX bandwidth, BER = 10^{-2}		52		dB
Receiver sensitivity, wM-BUS S2-mode, 32.768 kbps	f_{RF} = 868.3 MHz, 32.768 ksym/s, Manchester coding, FSK, 50-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		–111		dBm

Receive (RX) Parameters, 861 MHz to 1054 MHz *(continued)*

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC/DC enabled, f_{RF} = 868 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, ±200 kHz, wM-BUS S2-mode, 32.768 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.3 MHz, 32.768 ksym/s, Manchester coding, FSK, 50-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		42, 43		dB
Selectivity, ±400 kHz, wM-BUS S2-mode, 32.768 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.3 MHz, 32.768 ksym/s, Manchester coding, FSK, 50-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		41, 47		dB
Blocking, ±1 MHz, wM-BUS S2-mode, 32.768 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.3 MHz, 32.768 ksym/s, Manchester coding, FSK, 50-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		43, 52		dB
Blocking, ±2 MHz, wM-BUS S2-mode, 32.768 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.3 MHz, 32.768 ksym/s, Manchester coding, FSK, 50-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		52, 55		dB
Blocking, ±10 MHz, wM-BUS S2-mode, 32.768 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.3 MHz, 32.768 ksym/s, Manchester coding, FSK, 50-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		68, 72		dB
Image rejection (image compensation enabled, the image compensation is calibrated in production), wM-BUS S2-mode, 32.768 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.3 MHz, 32.768 ksym/s, Manchester coding, FSK, 50-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		43		dB
Receiver sensitivity, wM-BUS C-mode, 100 kbps	f_{RF} = 868.95 MHz, 100 ksym/s, NRZ coding, FSK, 45-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		–107		dBm
Selectivity, ±400 kHz, wM-BUS C-mode, 100 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.95 MHz, 100 ksym/s, NRZ coding, FSK, 45-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		41, 46		dB
Selectivity, ±800 kHz, wM-BUS C-mode, 100 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.95 MHz, 100 ksym/s, NRZ coding, FSK, 45-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		41, 50		dB
Blocking, ±1 MHz, wM-BUS C-mode, 100 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.95 MHz, 100 ksym/s, NRZ coding, FSK, 45-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		43, 51		dB
Blocking, ±2 MHz, wM-BUS C-mode, 100 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.95 MHz, 100 ksym/s, NRZ coding, FSK, 45-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		51, 53		dB
Blocking, ±5 MHz, wM-BUS C-mode, 100 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.95 MHz, 100 ksym/s, NRZ coding, FSK, 45-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		55, 61		dB
Blocking, ±10 MHz, wM-BUS C-mode, 100 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.95 MHz, 100 ksym/s, NRZ coding, FSK, 45-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		67, 68		dB
Receiver sensitivity, wM-BUS T-mode, 100 kbps	f_{RF} = 868.95 MHz, 100 ksym/s, 3 out of 6 coding, FSK, 45-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		–105		dBm
Selectivity, ±400 kHz, wM-BUS T-mode, 100 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.95 MHz, 100 ksym/s, 3 out of 6 coding, FSK, 45-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		41, 46		dB
Selectivity, ±800 kHz, wM-BUS T-mode, 100 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.95 MHz, 100 ksym/s, 3 out of 6 coding, FSK, 45-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		41, 50		dB
Blocking, ±1 MHz, wM-BUS T-mode, 100 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.95 MHz, 100 ksym/s, 3 out of 6 coding, FSK, 45-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		42, 51		dB

Receive (RX) Parameters, 861 MHz to 1054 MHz *(continued)*

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC/DC enabled, f_{RF} = 868 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Blocking, ±2 MHz, wM-BUS T-mode, 100 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.95 MHz, 100 ksym/s, 3 out of 6 coding, FSK, 45-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		51, 52		dB
Blocking, ±5 MHz, wM-BUS T-mode, 100 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.95 MHz, 100 ksym/s, 3 out of 6 coding, FSK, 45-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		54, 60		dB
Blocking, ±10 MHz, wM-BUS T-mode, 100 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 868.95 MHz, 100 ksym/s, 3 out of 6 coding, FSK, 45-kHz deviation, 196-kHz RX bandwidth, BER = 10^{-2}		67, 68		dB
Receiver sensitivity, WideBand-DSSS (WB-DSSS), 30 kbps	f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 8, 622-kHz RX bandwidth, BER = 10^{-2}		–109		dBm
Blocking, ±1 MHz, WB-DSSS, 30 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 8, 622-kHz RX bandwidth, BER = 10^{-2}		57, 57		dB
Blocking, ±2 MHz, WB-DSSS, 30 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 8, 622-kHz RX bandwidth, BER = 10^{-2}		58, 58		dB
Blocking, ±5 MHz, WB-DSSS, 30 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 8, 622-kHz RX bandwidth, BER = 10^{-2}		59, 57		dB
Blocking, ±10 MHz, WB-DSSS, 30 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 8, 622-kHz RX bandwidth, BER = 10^{-2}		71, 68		dB
Receiver sensitivity, WideBand-DSSS (WB-DSSS), 60 kbps	f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 4, 622-kHz RX bandwidth, BER = 10^{-2}		–108		dBm
Blocking, ±1 MHz, WB-DSSS, 60 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 4, 622-kHz RX bandwidth, BER = 10^{-2}		56, 56		dB
Blocking, ±2 MHz, WB-DSSS, 60 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 4, 622-kHz RX bandwidth, BER = 10^{-2}		57, 57		dB
Blocking, ±5 MHz, WB-DSSS, 60 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 4, 622-kHz RX bandwidth, BER = 10^{-2}		57, 56		dB
Blocking, ±10 MHz, WB-DSSS, 60 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 4, 622-kHz RX bandwidth, BER = 10^{-2}		70, 67		dB
Receiver sensitivity, WideBand-DSSS (WB-DSSS), 120 kbps	f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 2, 622-kHz RX bandwidth, BER = 10^{-2}		–106		dBm
Blocking, ±1 MHz, WB-DSSS, 120 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 2, 622-kHz RX bandwidth, BER = 10^{-2}		54, 54		dB
Blocking, ±2 MHz, WB-DSSS, 120 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 2, 622-kHz RX bandwidth, BER = 10^{-2}		55, 55		dB

Receive (RX) Parameters, 861 MHz to 1054 MHz *(continued)*

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC/DC enabled, f_{RF} = 868 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Blocking, ±5 MHz, WB-DSSS, 120 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 2, 622-kHz RX bandwidth, BER = 10^{-2}		55, 54		dB
Blocking, ±10 MHz, WB-DSSS, 120 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 2, 622-kHz RX bandwidth, BER = 10^{-2}		69, 65		dB
Receiver sensitivity, WideBand-DSSS (WB-DSSS), 240 kbps	f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 1, 622-kHz RX bandwidth, BER = 10^{-2}		–105		dBm
Blocking, ±1 MHz, WB-DSSS, 240 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 1, 622-kHz RX bandwidth, BER = 10^{-2}		53, 53		dB
Blocking, ±2 MHz, WB-DSSS, 240 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 1, 622-kHz RX bandwidth, BER = 10^{-2}		53, 54		dB
Blocking, ±5 MHz, WB-DSSS, 240 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 1, 622-kHz RX bandwidth, BER = 10^{-2}		53, 54		dB
Blocking, ±10 MHz, WB-DSSS, 240 kbps	Wanted signal 3 dB above sensitivity limit. f_{RF} = 915 MHz, 480 ksym/s, GFSK, 195-kHz deviation, FEC (half rate), DSSS = 1, 622-kHz RX bandwidth, BER = 10^{-2}		68, 64		dB
Receiver sensitivity, 10 kbps	GFSK, 19-kHz deviation, 78-kHz RX bandwidth, BER = 10^{-2}		–114		dBm
Selectivity, ±100 kHz, 10 kbps	Wanted signal 3 dB above sensitivity limit. 10 kbps, GFSK, 19-kHz deviation, 78-kHz RX bandwidth, BER = 10^{-2}		40, 40		dB
Selectivity, ±200 kHz, 10 kbps	Wanted signal 3 dB above sensitivity limit. 10 kbps, GFSK, 19-kHz deviation, 78-kHz RX bandwidth, BER = 10^{-2}		46, 44		dB
Selectivity, ±400 kHz, 10 kbps	Wanted signal 3 dB above sensitivity limit. 10 kbps, GFSK, 19-kHz deviation, 78-kHz RX bandwidth, BER = 10^{-2}		50, 45		dB
Blocking, ±2 MHz, 10 kbps	Wanted signal 3 dB above sensitivity limit. 10 kbps, GFSK, 19-kHz deviation, 78-kHz RX bandwidth, BER = 10^{-2}		62, 61		dB
Blocking, ±10 MHz, 10 kbps	Wanted signal 3 dB above sensitivity limit. 10 kbps, GFSK, 19-kHz deviation, 78-kHz RX bandwidth, BER = 10^{-2}		76, 72		dB
Image rejection (image compensation enabled, the image compensation is calibrated in production), 10 kbps	Wanted signal 3 dB above sensitivity limit. 10 kbps, GFSK, 19-kHz deviation, 78-kHz RX bandwidth, BER = 10^{-2}		43		dB
Receiver sensitivity, 4.8 kbps	GFSK, 5.2-kHz deviation, 49-kHz RX bandwidth, BER = 10^{-2}		–114		dBm
Selectivity, ±100 kHz, 4.8 kbps	Wanted signal 3 dB above sensitivity limit. 4.8 kbps, GFSK, 5.2-kHz deviation, 49-kHz RX bandwidth, BER = 10^{-2}		44, 43		dB
Selectivity, ±200 kHz, 4.8 kbps	Wanted signal 3 dB above sensitivity limit. 4.8 kbps, GFSK, 5.2-kHz deviation, 49-kHz RX bandwidth, BER = 10^{-2}		49, 48		dB

Receive (RX) Parameters, 861 MHz to 1054 MHz *(continued)*

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC/DC enabled, f_{RF} = 868 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, ±400 kHz, 4.8 kbps	Wanted signal 3 dB above sensitivity limit. 4.8 kbps, GFSK, 5.2-kHz deviation, 49-kHz RX bandwidth, BER = 10^{-2}		52, 49		dB
Blocking, ±2 MHz, 4.8 kbps	Wanted signal 3 dB above sensitivity limit. 4.8 kbps, GFSK, 5.2-kHz deviation, 49-kHz RX bandwidth, BER = 10^{-2}		64, 63		dB
Blocking, ±10 MHz, 4.8 kbps	Wanted signal 3 dB above sensitivity limit. 4.8 kbps, GFSK, 5.2-kHz deviation, 49-kHz RX bandwidth, BER = 10^{-2}		73, 72		dB
Image rejection (image compensation enabled, the image compensation is calibrated in production), 4.8 kbps	Wanted signal 3 dB above sensitivity limit. 4.8 kbps, GFSK, 5.2-kHz deviation, 49-kHz RX bandwidth, BER = 10^{-2}		43		dB
Receiver sensitivity, CC1101 compatible mode, 2.4 kbps	GFSK, 5.2-kHz deviation (commonly used settings on CC1101), 49-kHz RX bandwidth, BER = 10^{-2}		–116		dBm
Selectivity, ±100 kHz, CC1101 compatible mode, 2.4 kbps	Wanted signal 3 dB above sensitivity limit. 2.4 kbps, GFSK, 5.2-kHz deviation (commonly used settings on CC1101), 49-kHz RX bandwidth, BER = 10^{-2}		45, 44		dB
Selectivity, ±200 kHz, CC1101 compatible mode, 2.4 kbps	Wanted signal 3 dB above sensitivity limit. 2.4 kbps, GFSK, 5.2-kHz deviation (commonly used settings on CC1101), 49-kHz RX bandwidth, BER = 10^{-2}		51, 47		dB
Blocking, ±2 MHz, CC1101 compatible mode, 2.4 kbps	Wanted signal 3 dB above sensitivity limit. 2.4 kbps, GFSK, 5.2-kHz deviation (commonly used settings on CC1101), 49-kHz RX bandwidth, BER = 10^{-2}		63, 62		dB
Blocking, ±10 MHz, CC1101 compatible mode, 2.4 kbps	Wanted signal 3 dB above sensitivity limit. 2.4 kbps, GFSK, 5.2-kHz deviation (commonly used settings on CC1101), 49-kHz RX bandwidth, BER = 10^{-2}		76, 71		dB
Image rejection (image compensation enabled, the image compensation is calibrated in production), CC1101 compatible mode, 2.4 kbps	Wanted signal 3 dB above sensitivity limit. 2.4 kbps, GFSK, 5.2-kHz deviation (commonly used settings on CC1101), 49-kHz RX bandwidth, BER = 10^{-2}		45		dB
Receiver sensitivity, CC1101 compatible mode, 1.2 kbps	GFSK, 5.2-kHz deviation (commonly used settings on CC1101), 49-kHz RX bandwidth, BER = 10^{-2}		–117		dBm
Selectivity, ±100 kHz, CC1101 compatible mode, 1.2 kbps	Wanted signal 3 dB above sensitivity limit. 1.2 kbps, GFSK, 5.2-kHz deviation (commonly used settings on CC1101), 49-kHz RX bandwidth, BER = 10^{-2}		45, 44		dB
Selectivity, ±200 kHz, CC1101 compatible mode, 1.2 kbps	Wanted signal 3 dB above sensitivity limit. 1.2 kbps, GFSK, 5.2-kHz deviation (commonly used settings on CC1101), 49-kHz RX bandwidth, BER = 10^{-2}		51, 47		dB
Blocking, ±2 MHz, CC1101 compatible mode, 1.2 kbps	Wanted signal 3 dB above sensitivity limit. 1.2 kbps, GFSK, 5.2-kHz deviation (commonly used settings on CC1101), 49-kHz RX bandwidth, BER = 10^{-2}		63, 62		dB
Blocking, ±10 MHz, CC1101 compatible mode, 1.2 kbps	Wanted signal 3 dB above sensitivity limit. 1.2 kbps, GFSK, 5.2-kHz deviation (commonly used settings on CC1101), 49-kHz RX bandwidth, BER = 10^{-2}		81, 81		dB
Image rejection (image compensation enabled, the image compensation is calibrated in production), CC1101 compatible mode, 1.2 kbps	Wanted signal 3 dB above sensitivity limit. 1.2 kbps, GFSK, 5.2-kHz deviation (commonly used settings on CC1101), 49-kHz RX bandwidth, BER = 10^{-2}		45		dB
Receiver sensitivity, legacy long-range mode, 625 bps	10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}. 868 MHz and 915 MHz.		–124		dBm
Selectivity, ±100 kHz, legacy long-range mode, 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		56, 56		dB
Blocking ±1 MHz, legacy long-range mode, 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		73, 77		dB

Receive (RX) Parameters, 861 MHz to 1054 MHz *(continued)*

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC/DC enabled, f_{RF} = 868 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Blocking ±2 MHz, legacy long-range mode, 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		79, 79		dB
Blocking ±10 MHz, legacy long-range mode, 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		91, 91		dB
Receiver sensitivity, OOK, 4.8 kbps	4.8 kbps, OOK, 40-kHz RX bandwidth, BER = 10^{-2}. 868 MHz and 915 MHz		–115		dBm

5.7 Receive (RX) Parameters, 431 MHz to 527 MHz

Measured on the Texas Instruments CC1310EM-7XD-4251 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC/DC enabled, f_{RF} = 433.92 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity, 50 kbps	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		–110		dBm
Receiver saturation	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		10		dBm
Selectivity, ±200 kHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		40, 42		dB
Selectivity, ±400 kHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		42, 50		dB
Blocking ±1 MHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		53, 58		dB
Blocking ±2 MHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		59, 60		dB
Blocking ±10 MHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		74, 74		dB
Spurious emissions 1 GHz to 13 GHz (VCO leakage at 3.5 GHz) and 30 MHz to 1 GHz	Conducted emissions measured according to ETSI EN 300 220		–74		dBm
Image rejection (image compensation enabled, the image compensation is calibrated in production), 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		43		dB
Receiver sensitivity, long-range mode, 5 kbps	20 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 2, 49-kHz RX bandwidth, BER = 10^{-2}. 433 MHz		–119		dBm
Receiver sensitivity, long-range mode, 2.5 kbps	20 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 4, 49-kHz RX bandwidth, BER = 10^{-2}. 433 MHz		–120		dBm
Receiver sensitivity, long-range mode, 1.25 kbps	20 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 49-kHz RX bandwidth, BER = 10^{-2}. 433 MHz		–121		dBm

Receive (RX) Parameters, 431 MHz to 527 MHz *(continued)*

Measured on the Texas Instruments CC1310EM-7XD-4251 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC/DC enabled, f_{RF} = 433.92 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity, legacy long-range mode, 625 bps	10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}. 868 MHz and 915 MHZ.		–124		dBm
Selectivity, ±100 kHz, legacy long-range mode, 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		56, 56		dB
Selectivity, ±200 kHz, legacy long-range mode, 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		62, 65		dB
Blocking ±1 MHz, legacy long-range mode, 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		68, 73		dB
Blocking ±2 MHz, legacy long-range mode, 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		74, 74		dB
Blocking ±10 MHz, legacy long-range mode, 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		88, 89		dB
Image rejection (image compensation enabled, the image compensation is calibrated in production), legacy long-range mode, 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		55		dB

5.8 Transmit (TX) Parameters, 861 MHz to 1054 MHz

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC/DC enabled, f_{RF} = 868 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum output power, boost mode		VDDR = 1.95 V Minimum VDDS for boost mode is 2.1 V 868 MHz and 915 MHz		14		dBm
Maximum output power		868 MHz and 915 MHz		12		dBm
Output power programmable range				24		dB
Output power variation		Tested at +10-dBm setting		±0.9		dB
Output power variation, boost mode		+14 dBm		±0.5		dB
Spurious emissions (excluding harmonics)(1)	30 MHz to 1 GHz	Transmitting +14 dBm ETSI restricted bands		<–59		dBm
		Transmitting +14 dBm outside ETSI restricted bands		<–51		
	1 GHz to 12.75 GHz	Transmitting +14 dBm measured in 1-MHz bandwidth (ETSI)		<–37		
Harmonics	Second harmonic	Transmitting +14 dBm, conducted 868 MHz, 915 MHz		–52, –55		dBm
	Third harmonic	Transmitting +14 dBm, conducted 868 MHz, 915 MHz		–58, –55		
	Fourth harmonic	Transmitting +14 dBm, conducted 868 MHz, 915 MHz		–56, –56		
Spurious emissions out-of-band, 915 MHz(1)	30 MHz to 88 MHz (within FCC restricted bands)	Transmitting +14 dBm, conducted		<–66		dBm
	88 MHz to 216 MHz (within FCC restricted bands)	Transmitting +14 dBm, conducted		<–65		
	216 MHz to 960 MHz (within FCC restricted bands)	Transmitting +14 dBm, conducted		<–65		
	960 MHz to 2390 MHz and above 2483.5 MHz (within FCC restricted band)	Transmitting +14 dBm, conducted		<–52		
	1 GHz to 12.75 GHz (outside FCC restricted bands)	Transmitting +14 dBm, conducted		<–43		
Spurious emissions out-of-band, 920.6 MHz(1)	Below 710 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–50		dBm
	710 MHz to 900 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–60		
	900 MHz to 915 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–57		
	930 MHz to 1000 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–57		
	1000 MHz to 1215 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–59		
	Above 1215 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–45		

(1) Suitable for systems targeting compliance with EN 300 220, EN 54-25, EN 303 204, FCC CFR47 Part 15, ARIB STD-T108.

5.9 Transmit (TX) Parameters, 431 MHz to 527 MHz

Measured on the Texas Instruments CC1310EM-7XD-4251 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC/DC enabled, f_{RF} = 433.92 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum output power, boost mode		VDDR = 1.95 V Minimum VDDS for boost mode is 2.1 V		15		dBm
Maximum output power				14		dBm
Spurious emissions (excluding harmonics)(1)	30 MHz to 1 GHz	Transmitting +10 dBm, 433 MHz Inside ETSI restricted bands		<–63		dBm
		Transmitting +10 dBm, 433 MHz Outside ETSI restricted bands		<–39		
	1 GHz to 12.75 GHz	Transmitting +10 dBm, 433 MHz Outside ETSI restricted bands, measured in 1-MHz bandwidth (ETSI)		<–52		
		Transmitting +10 dBm, 433 MHz Inside ETSI restricted bands, measured in 1-MHz bandwidth (ETSI)		<–58		

(1) Suitable for systems targeting compliance with EN 300 220, EN 54-25, EN 303 204, FCC CFR47 Part 15, ARIB STD-T108.

5.10 1-Mbps GFSK (Bluetooth low energy) – RX

Measured on the TI CC1350_7XD-Dual Band reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz, unless otherwise noted. All tests with Bluetooth low energy PHY (1 Mbps), 37-byte payload unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	Differential mode. Measured at the CC1350_7XD-Dual Band SMA connector, 37-byte payload BER = 10^{-3}		–87		dBm
Receiver sensitivity	Differential mode. Measured at the CC1350_7XD-Dual Band SMA connector, 255-byte payload BER = 10^{-3}		–86		dBm
Receiver saturation	Differential mode. Measured at the CC1350_7XD-Dual Band SMA connector, BER = 10^{-3}		0		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency. Input signal 10 dB above sensitivity limit	–350		350	kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate. Input signal 10 dB above sensitivity limit	–750		750	ppm
Co-channel rejection(1)	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}		–6		dB
Selectivity, ±1 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		7 / 4(2)		dB
Selectivity, +2 MHz(1)	Wanted signal at –67 dBm, modulated interferer at +2 MHz, BER = 10^{-3}		38		dB
Selectivity, ±3 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}. Note that –3 MHz is –1 MHz from the image frequency.		36 / 41(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		39 / 38(2)		dB
Selectivity, ±5 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±5 MHz, BER = 10^{-3}		35 / 39(2)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ≥ ±6 MHz, BER = 10^{-3}		42 / 37(2)		dB
Selectivity, ±15 MHz or more(1)	Wanted signal at –67 dBm, modulated interferer at ≥ ±15 MHz or more, BER = 10^{-3}		55		dB

(1) Numbers given as I/C dB.
(2) X / Y, where X is +N MHz and Y is –N MHz.

1-Mbps GFSK (Bluetooth low energy) – RX *(continued)*

Measured on the TI CC1350_7XD-Dual Band reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz, unless otherwise noted. All tests with Bluetooth low energy PHY (1 Mbps), 37-byte payload unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, Image frequency (image compensation enabled, the image compensation is calibrated in production)(1)	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		37		dB
Selectivity, Image frequency ±1 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image (–3 MHz and –1 MHz from wanted) frequency, BER = 10^{-3}		4 / 41(2)		dB
Out-of-band blocking(3)	30 MHz to 2000 MHz		–25		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		>–20		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		>–20		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		>–30		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz, respectively, at the given power level		–30		dBm
Spurious emissions, 30 to 1000 MHz	Conducted measurement in a 50-Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–72		dBm
Spurious emissions, 1 to 12.75 GHz	Conducted measurement in a 50-Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–65		dBm
RSSI dynamic range			70		dB
RSSI accuracy			±4		dB

(3) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification.

5.11 1-Mbps GFSK (Bluetooth low energy) – TX

Measured on the TI CC1350_7XD-Dual Band reference design with T_c = 25°C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power, boost mode	Differential mode, delivered to a single-ended 50-Ω load through a balun. VDDR = 1.95 V Minimum VDDS for boost mode is 2.1 V.		9		dBm
Output power	Differential mode, delivered to a single-ended 50-Ω load through a balun.		5		dBm
Output power, lowest setting	Delivered to a single-ended 50-Ω load through a balun		–21		dBm
Spurious emission conducted measurement(1)	f < 1 GHz, outside restricted bands		–59		dBm
	f < 1 GHz, restricted bands ETSI		–55		
	f < 1 GHz, restricted bands FCC		–61		
	f > 1 GHz, including harmonics		–47		

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

5.12 PLL Parameters

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise in the 868-MHz band	±100-kHz offset		–101		dBc/Hz
	±200-kHz offset		–108		
	±400-kHz offset		–115		
	±1000-kHz offset		–124		
	±2000-kHz offset		–131		
	±10000-kHz offset		–140		
Phase noise in the 915-MHz band	±100-kHz offset		–98		dBc/Hz
	±200-kHz offset		–106		
	±400-kHz offset		–114		
	±1000-kHz offset		–122		
	±2000-kHz offset		–130		
	±10000-kHz offset		–140		

5.13 ADC Characteristics

T_c = 25°C, V_{DDS} = 3.0 V, DC/DC disabled. Input voltage scaling enabled, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range		0		V_{DDS}	V
	Resolution			12		Bits
	Sample rate				200	ksamples/s
	Offset	Internal 4.3-V equivalent reference(2)		2.1		LSB
	Gain error	Internal 4.3-V equivalent reference(2)		–0.14		LSB
DNL(3)	Differential nonlinearity			>–1		LSB
INL(4)	Integral nonlinearity			±2		LSB
ENOB	Effective number of bits	Internal 4.3-V equivalent reference(2), 200 ksamples/s, 9.6-kHz input tone		10.0		Bits
		VDDS as reference, 200 ksamples/s, 9.6-kHz input tone		10.2		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksamples/s, 300-Hz input tone		11.1		
THD	Total harmonic distortion	Internal 4.3-V equivalent reference(2), 200 ksamples/s, 9.6-kHz input tone		–65		dB
		VDDS as reference, 200 ksamples/s, 9.6-kHz input tone		–72		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksamples/s, 300-Hz input tone		–75		
SINAD and SNDR	Signal-to-noise and distortion ratio	Internal 4.3-V equivalent reference(2), 200 ksamples/s, 9.6-kHz input tone		62		dB
		VDDS as reference, 200 ksamples/s, 9.6-kHz input tone		63		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksamples/s, 300-Hz input tone		69		

(1) Using IEEE Std 1241™ 2010 for terminology and test methods.
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V. Applied voltage must be within the absolute maximum ratings (see Section 5.1) at all times.
(3) No missing codes. Positive DNL typically varies from 0.3 to 1.7, depending on the device (see Figure 5-7).
(4) For a typical example, see Figure 5-6.

ADC Characteristics *(continued)*

T_c = 25°C, V_{DDS} = 3.0 V, DC/DC disabled. Input voltage scaling enabled, unless otherwise noted.[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SFDR	Spurious-free dynamic range	Internal 4.3-V equivalent reference[2], 200 ksamples/s, 9.6-kHz input tone		74		dB
		VDDS as reference, 200 ksamples/s, 9.6-kHz input tone		75		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksamples/s, 300-Hz input tone		75		
	Conversion time	Including sampling time		5		µs
	Current consumption	Internal 4.3-V equivalent reference[2]		0.66		mA
	Current consumption	VDDS as reference		0.75		mA
	Reference voltage	Equivalent fixed internal reference(voltage scaling enabled) [2] For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1.		4.3		V
	Reference voltage	Fixed internal reference (input voltage scaling disabled). [2] For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: V_{ref} = 4.3 V × 1408 / 4095		1.48		V
	Reference voltage	VDDS as reference (Also known as RELATIVE) (input voltage scaling enabled)		VDDS		V
	Reference voltage	VDDS as reference (Also known as RELATIVE) (input voltage scaling disabled)		VDDS / 2.82		V
	Input Impedance	200 ksamples/s, voltage scaling enabled. Capacitive input, input impedance depends on sampling frequency and sampling time		>1		MΩ

5.14 Temperature Sensor

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			4		°C
Range		–40		85	°C
Accuracy			±5		°C
Supply voltage coefficient[1]			3.2		°C/V

(1) Automatically compensated when using supplied driver libraries.

5.15 Battery Monitor

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			50		mV
Range		1.8		3.8	V
Accuracy			13		mV

5.16 Continuous Time Comparator

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
External reference voltage		0		V_{DDS}	V
Internal reference voltage	DCOUPL as reference		1.27		V
Offset			3		mV
Hysteresis			<2		mV
Decision time	Step from –10 mV to 10 mV		0.72		µs
Current consumption when enabled (1)			8.6		µA

(1) Additionally, the bias module must be enabled when running in standby mode.

5.17 Low-Power Clocked Comparator

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
Clock frequency			32.8		kHz
Internal reference voltage, VDDS / 2			1.49 to 1.51		V
Internal reference voltage, VDDS / 3			1.01 to 1.03		V
Internal reference voltage, VDDS / 4			0.78 to 0.79		V
Internal reference voltage, DCOUPL / 1			1.25 to 1.28		V
Internal reference voltage, DCOUPL / 2			0.63 to 0.65		V
Internal reference voltage, DCOUPL / 3			0.42 to 0.44		V
Internal reference voltage, DCOUPL / 4			0.33 to 0.34		V
Offset			<2		mV
Hysteresis			<5		mV
Decision time	Step from –50 mV to 50 mV		1		clock-cycle
Current consumption when enabled			362		nA

5.18 Programmable Current Source

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current source programmable output range			0.25 to 20		µA
Resolution			0.25		µA
Current consumption (1)	Including current source at maximum programmable output		23		µA

(1) Additionally, the bias module must be enabled when running in standby mode.

5.19 DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25°C, V_{DDS} = 1.8 V					
GPIO VOH at 8-mA load	IOCURR = 2, high-drive GPIOs only	1.32	1.54		V
GPIO VOL at 8-mA load	IOCURR = 2, high-drive GPIOs only		0.26	0.32	V
GPIO VOH at 4-mA load	IOCURR = 1	1.32	1.58		V
GPIO VOL at 4-mA load	IOCURR = 1		0.21	0.32	V
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		71.7		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		21.1		µA
GPIO high/low input transition, no hysteresis	IH = 0, transition between reading 0 and reading 1		0.88		V
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.07		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.74		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 voltage transition points		0.33		V
T_A = 25°C, V_{DDS} = 3.0 V					
GPIO VOH at 8-mA load	IOCURR = 2, high-drive GPIOs only		2.68		V
GPIO VOL at 8-mA load	IOCURR = 2, high-drive GPIOs only		0.33		V
GPIO VOH at 4-mA load	IOCURR = 1		2.72		V
GPIO VOL at 4-mA load	IOCURR = 1		0.28		V
T_A = 25°C, V_{DDS} = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		277		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		113		µA
GPIO high/low input transition, no hysteresis	IH = 0, transition between reading 0 and reading 1		1.67		V
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.94		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		1.54		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 voltage transition points		0.4		V
VIH	Lowest GPIO input voltage reliably interpreted as a *High*			0.8	VDDS (1)
VIL	Highest GPIO input voltage reliably interpreted as a *Low*	0.2			VDDS (1)

(1) Each GPIO is referenced to a specific VDDS pin. See the technical reference manual listed in Section 8.3 for more details.

5.20 Thermal Characteristics

THERMAL METRIC[1]		CC1350			UNIT[2]
		RSM (VQFN)	RHB (VQFN)	RGZ (VQFN)	
		32 PINS	32 PINS	48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.9	32.8	29.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.3	24.0	15.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.6	6.8	6.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.3	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.4	6.8	6.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	1.9	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.

5.21 Timing and Switching Characteristics

5.21.1 Reset Timing

Table 5-1. Reset Timing

PARAMETER	MIN	TYP	MAX	UNIT
RESET_N low duration	1			µs

5.21.2 Wakeup Timing

Table 5-2. Wakeup Timing

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted. The times listed here do not include RTOS overhead.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCU, Idle → Active			14		µs
MCU, Standby → Active			174		µs
MCU, Shutdown → Active			1097		µs

5.21.3 Clock Specifications

Table 5-3. 24-MHz Crystal Oscillator (XOSC_HF)

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted. Section 5.21.1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ESR equivalent series resistance Section 5.21.2	6 pF < C_L ≤ 9 pF		20	60	Ω
ESR equivalent series resistance Section 5.21.2	5 pF < C_L ≤ 6 pF			80	Ω
L_M motional inductance Section 5.21.2	Relates to load capacitance (C_L in Farads)	< 1.6 × 10^{-24} / $C_L^{\ 2}$			H
C_L crystal load capacitance Section 5.21.2		5		9	pF
Crystal frequency Section 5.21.2			24		MHz
Start-up time			150		µs

Table 5-4. 32.768-kHz Crystal Oscillator (XOSC_LF)

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.(1)

	MIN	TYP	MAX	UNIT
Crystal frequency		32.768		kHz
ESR equivalent series resistance		30	100	kΩ
Crystal load capacitance (C_L)	6		12	pF

(1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.

Table 5-5. 48-MHz RC Oscillator (RCOSC_HF)

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Frequency		48		MHz
Uncalibrated frequency accuracy		±1%		
Calibrated frequency accuracy(1)		±0.25%		
Startup time		5		µs

(1) Accuracy relative to the calibration source (XOSC_HF)

Table 5-6. 32-kHz RC Oscillator (RCOSC_LF)

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Calibrated frequency(1)		32.768		kHz
Temperature coefficient		50		ppm/°C

(1) The frequency accuracy of the Real Time Clock (RTC) is not directly dependent on the frequency accuracy of the 32-kHz RC Oscillator. The RTC can be calibrated by measuring the frequency error of RCOSC_LF relative to XOSC_HF and compensating for the RTC tick speed.

5.21.4 Flash Memory Characteristics

Table 5-7. Flash Memory Characteristics

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supported flash erase cycles before failure		100			k Cycles
Flash page or sector erase current	Average delta current		12.6		mA
Flash page or sector erase time (1)			8		ms
Flash page or sector size			4		KB
Flash write current	Average delta current, 4 bytes at a time		8.15		mA
Flash write time (1)	4 bytes at a time		8		µs

(1) This number is dependent on flash aging and increases over time and erase cycles.

5.21.5 Synchronous Serial Interface (SSI) Characteristics

Table 5-8. Synchronous Serial Interface (SSI) Characteristics

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER NO.	PARAMETER		MIN	TYP	MAX	UNIT
S1	t_{clk_per}	SSIClk cycle time	12		65024	system clocks
S2 (1)	t_{clk_high}	SSIClk high time		0.5 × t_{clk_per}		
S3 (1)	t_{clk_low}	SSIClk low time		0.5 × t_{clk_per}		

(1) See the SSI timing diagrams, Figure 5-1, Figure 5-2, and Figure 5-3.

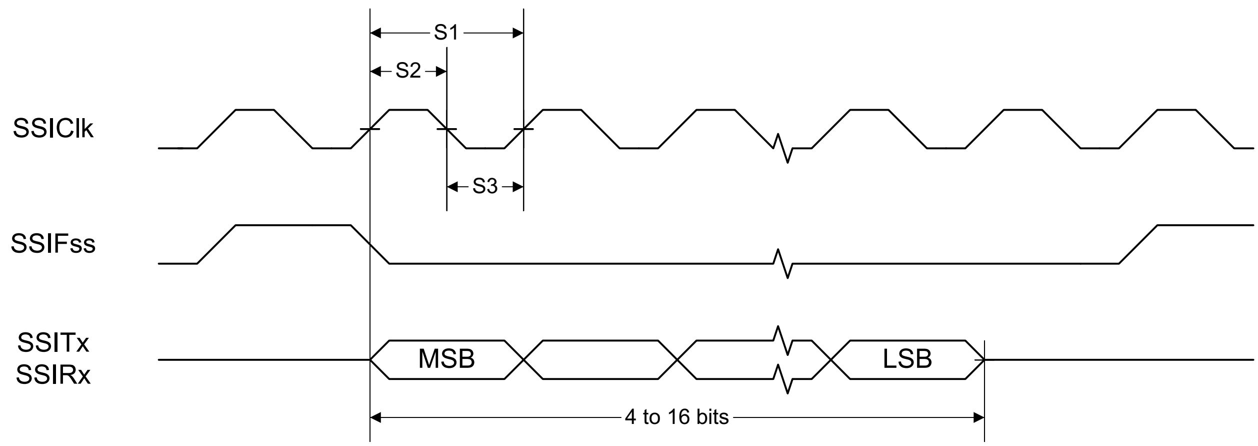

Figure 5-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

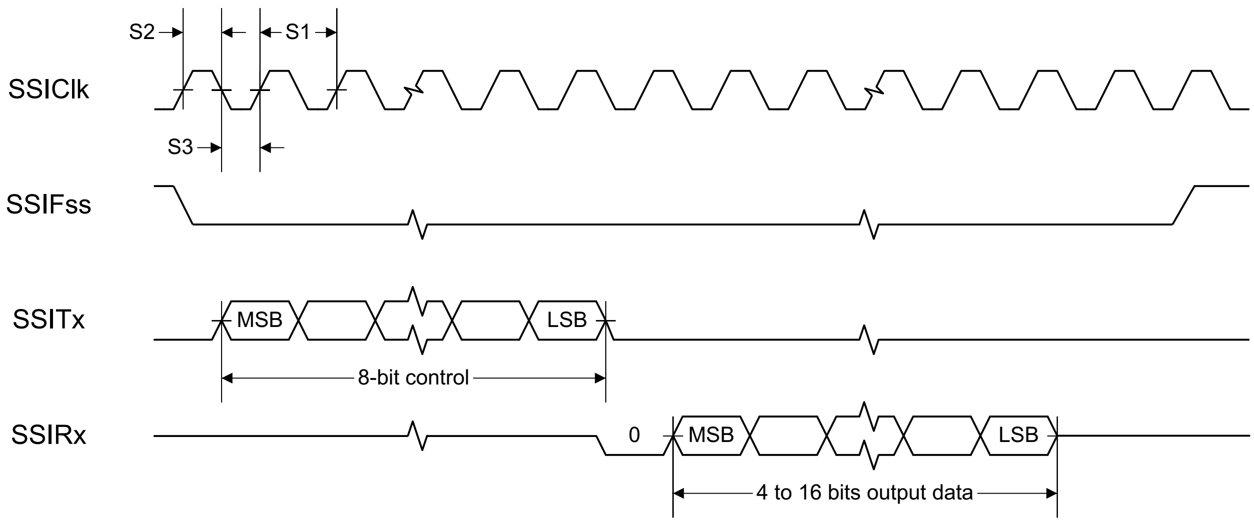

Figure 5-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

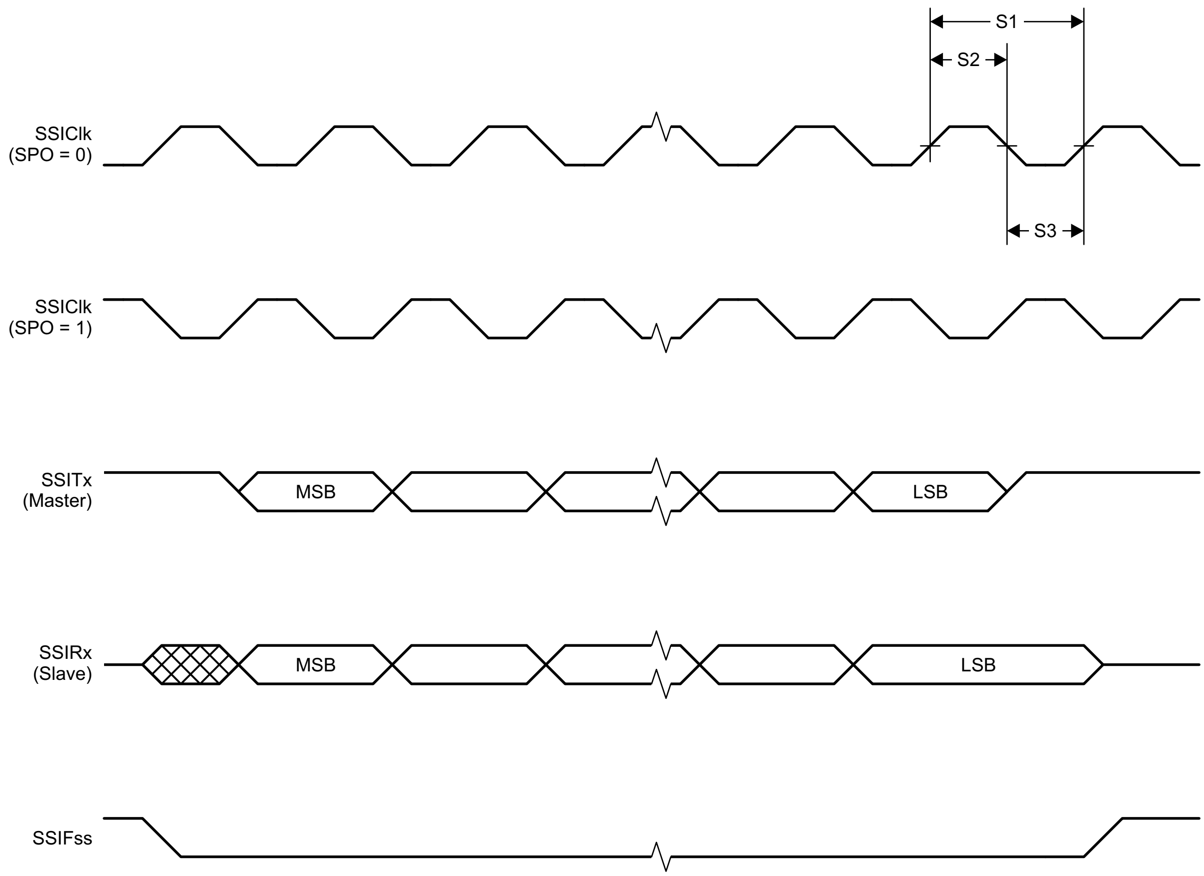

Figure 5-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

5.22 Typical Characteristics

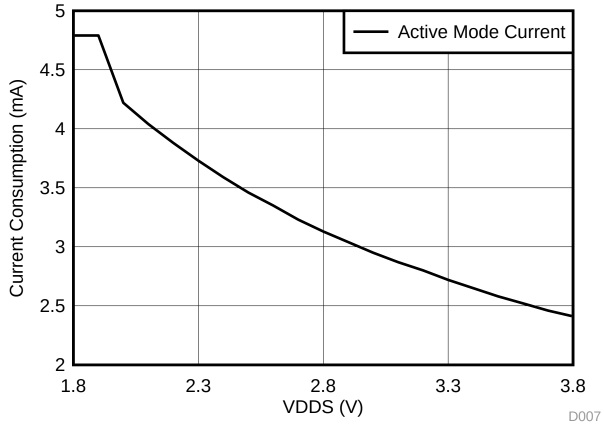

Figure 5-4. Active Mode (MCU) Current Consumption vs Supply Voltage (VDDS)

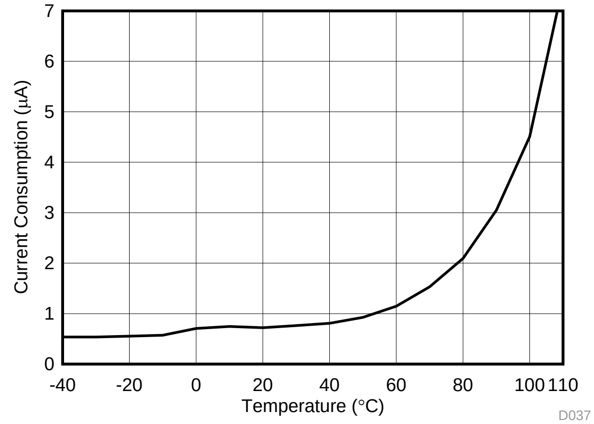

Figure 5-5. Standby MCU Current Consumption, 32-kHz Clock, RAM and MCU Retention

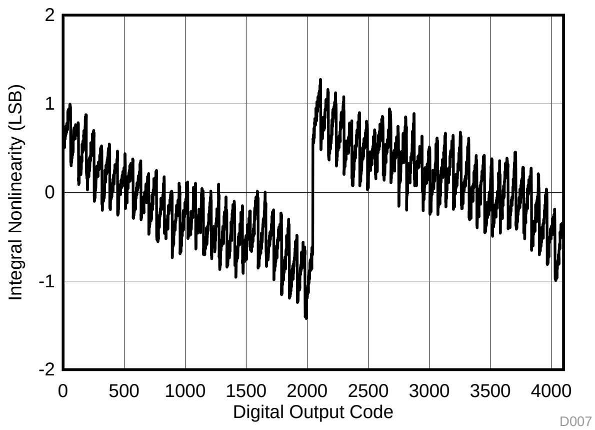

Figure 5-6. SoC ADC, Integral Nonlinearity vs Digital Output Code

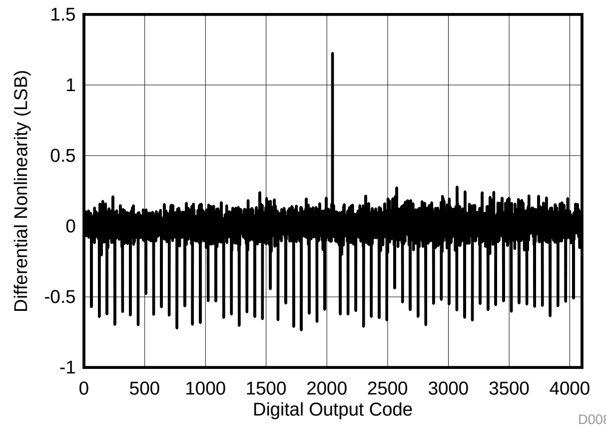

Figure 5-7. SoC ADC, Differential Nonlinearity vs Digital Output Code

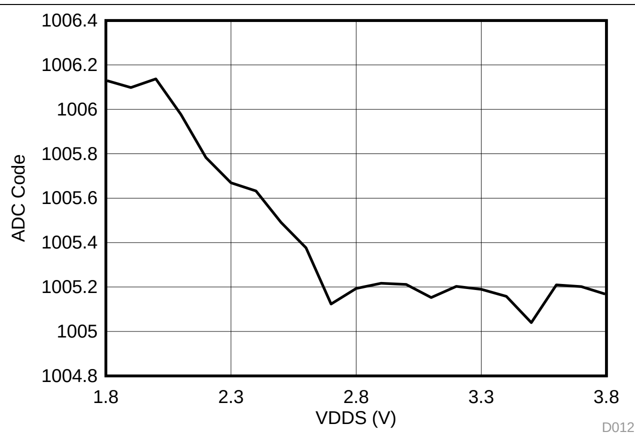

Figure 5-8. SoC ADC Output vs Supply Voltage (Fixed Input, Internal Reference, No Scaling)

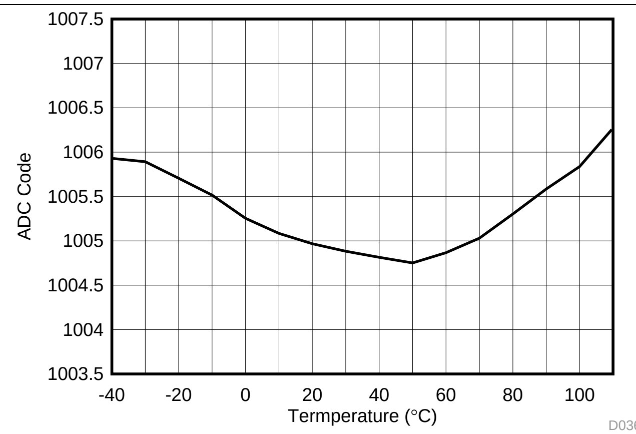

Figure 5-9. SoC ADC Output vs Temperature (Fixed Input, Internal Reference, No Scaling)

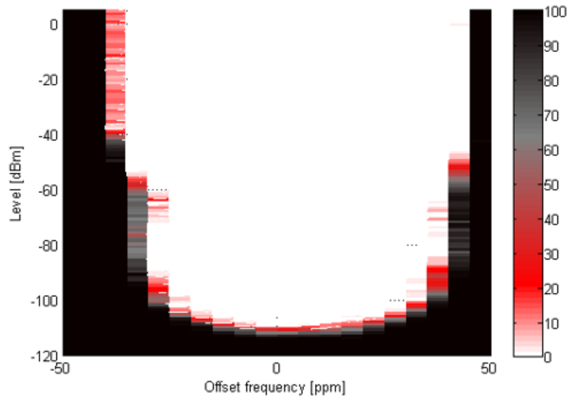

Figure 5-10. RX, (50-kbps) Packet Error Rate (PER) vs Input RF Level vs Frequency Offset, 868 MHz

5.23 Typical Characteristics – Sub-1 GHz

Unless otherwise stated, all performance figures represent an average over six typical parts at room temperature and with the internal DC/DC converter enabled.

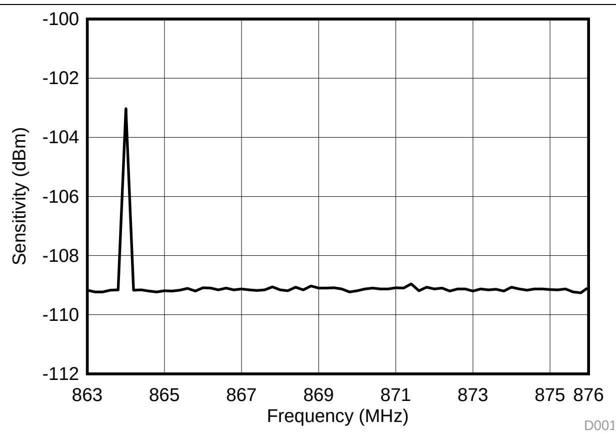

Figure 5-11. RX (50 kbps) Sensitivity vs Frequency 863 MHz to 876 MHz

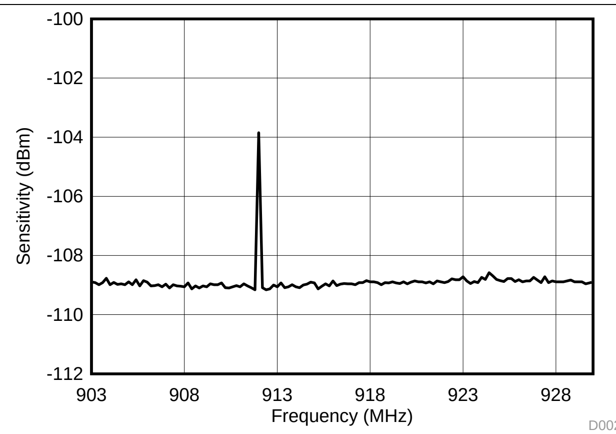

Figure 5-12. RX (50 kbps) Sensitivity vs Frequency 902 MHz to 928 MHz

Unless otherwise stated, all performance figures represent an average over six typical parts at room temperature and with the internal DC/DC converter enabled.

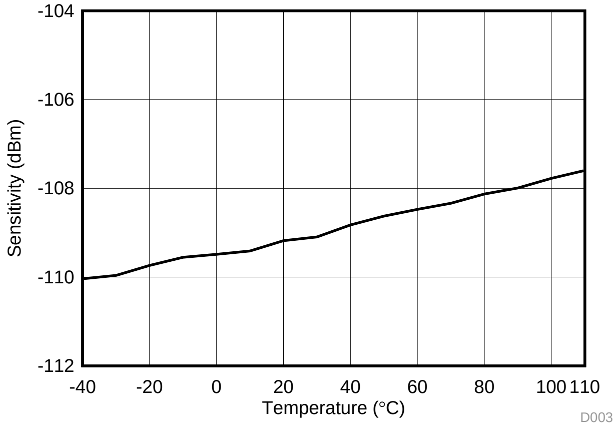

Figure 5-13. RX (50 kbps) Sensitivity vs Temperature 868 MHz

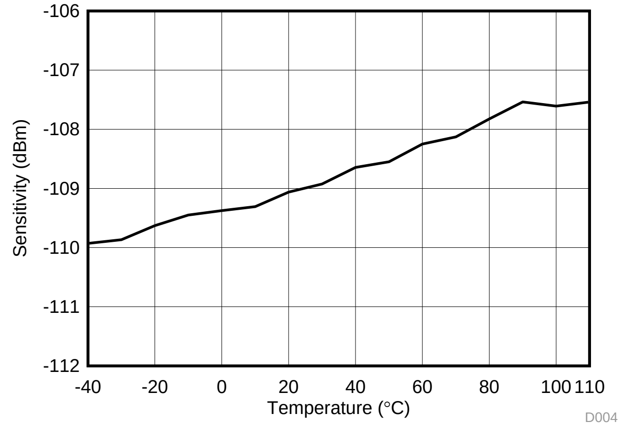

Figure 5-14. RX (50 kbps) Sensitivity vs Temperature 915 MHz

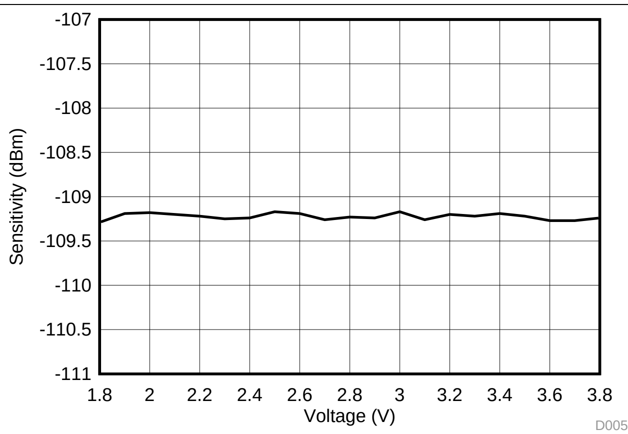

Figure 5-15. RX (50 kbps) Sensitivity vs Voltage 868 MHz

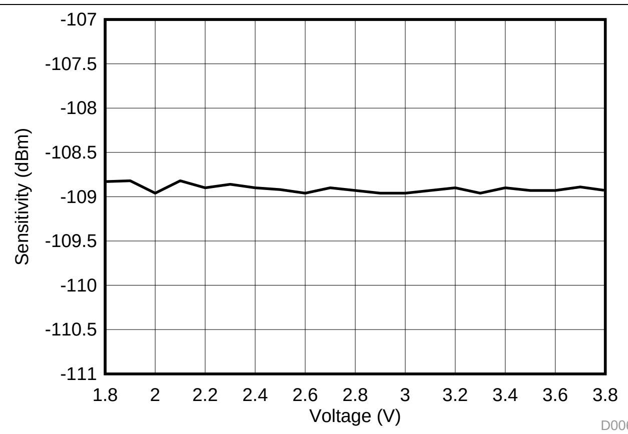

Figure 5-16. RX (50 kbps) Sensitivity vs Voltage 915 MHz

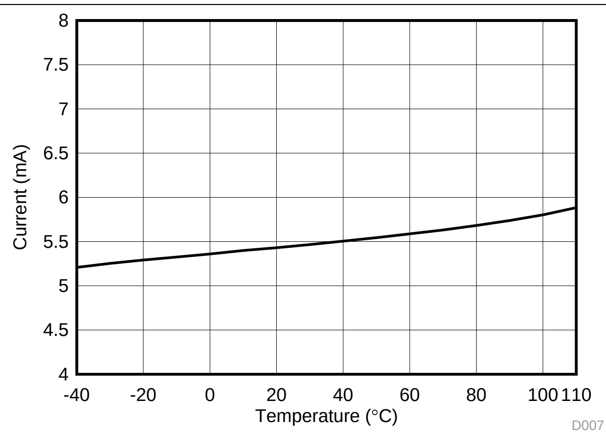

Figure 5-17. RX (50 kbps) Current vs Temperature at 868 MHz

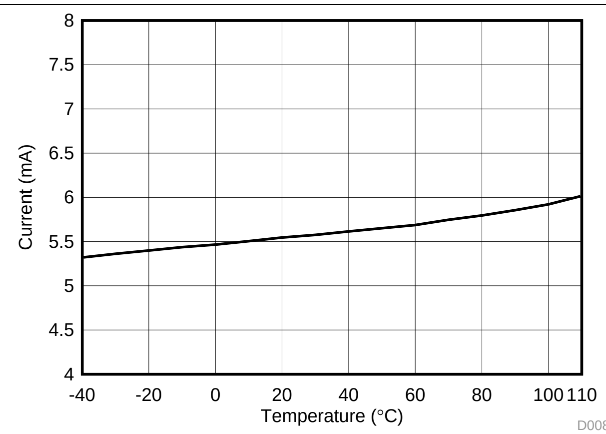

Figure 5-18. RX (50 kbps) Current vs Temperature at 915 MHz

Unless otherwise stated, all performance figures represent an average over six typical parts at room temperature and with the internal DC/DC converter enabled.

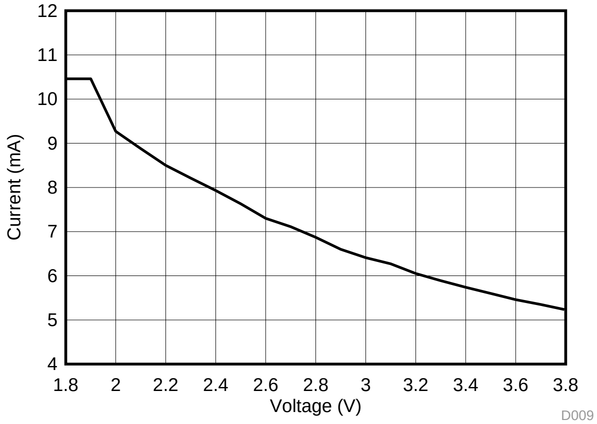

Figure 5-19. RX (50 kbps) Current vs Voltage at 868 MHz

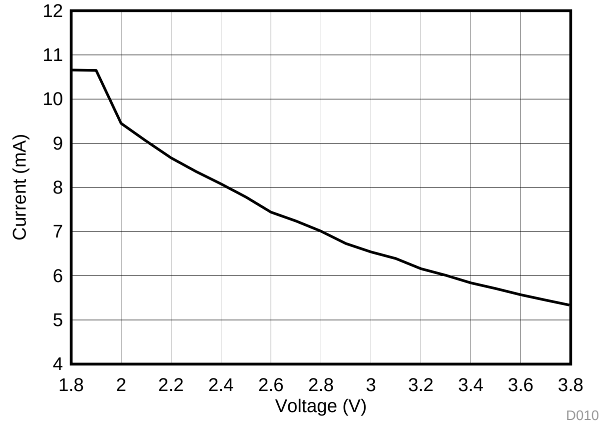

Figure 5-20. RX (50 kbps) Current vs Voltage at 915 MHz

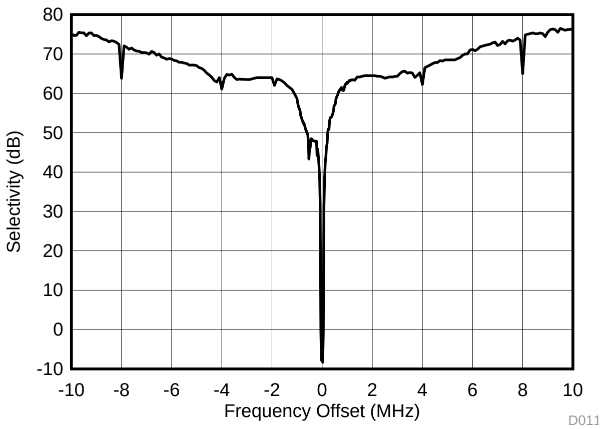

Figure 5-21. RX (50 kbps) Selectivity With Wanted Signal at 868 MHz, 3 dB Above Sensitivity Limit

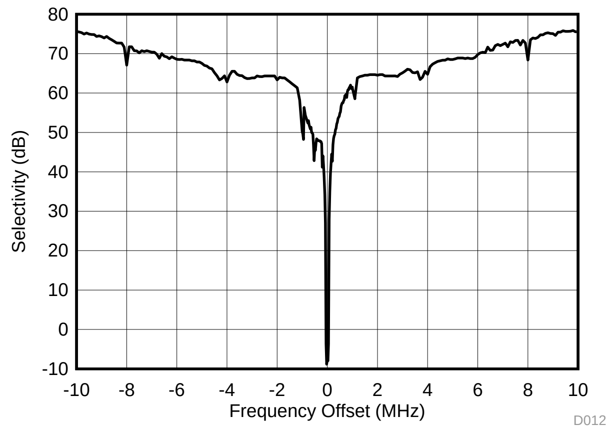

Figure 5-22. RX (50 kbps) Selectivity With Wanted Signal at 915 MHz, 3 dB Above Sensitivity Limit

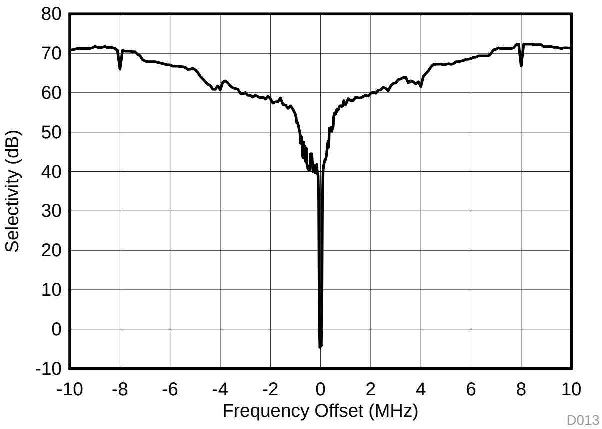

Figure 5-23. RX (50 kbps) Selectivity With Wanted Signal at 868 MHz, –96 dBm

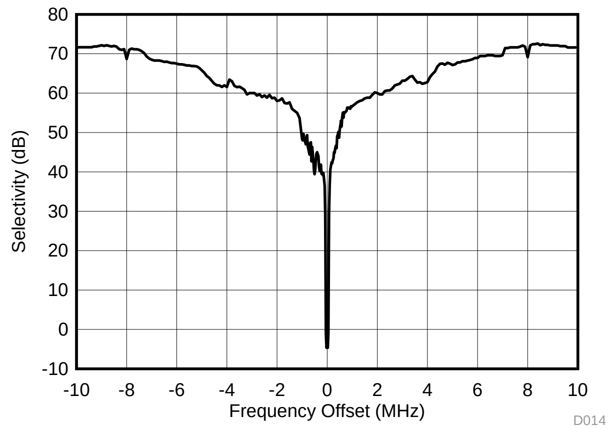

Figure 5-24. RX (50 kbps) Selectivity With Wanted Signal at 915 MHz, –96 dBm

Unless otherwise stated, all performance figures represent an average over six typical parts at room temperature and with the internal DC/DC converter enabled.

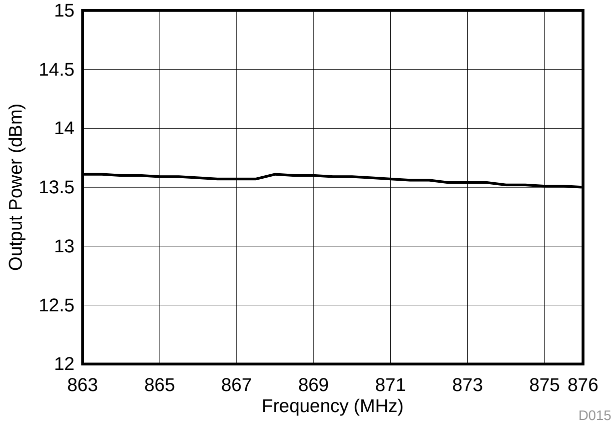

Figure 5-25. TX Maximum Output Power, 863 MHz to 876 MHz

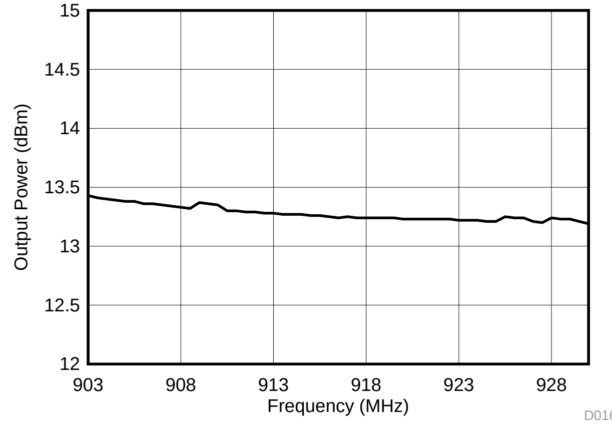

Figure 5-26. TX Maximum Output Power, 902 MHz to 928 MHz

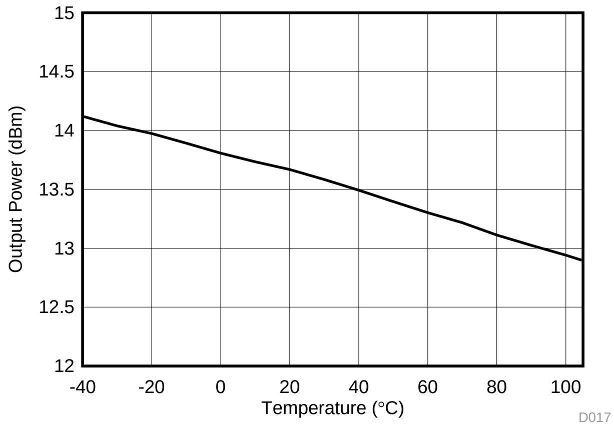

Figure 5-27. TX Maximum Output Power vs Temperature, 868 MHz

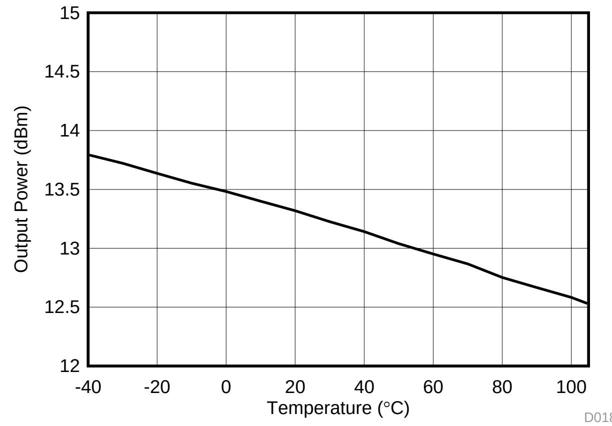

Figure 5-28. TX Maximum Output Power vs Temperature, 915 MHz

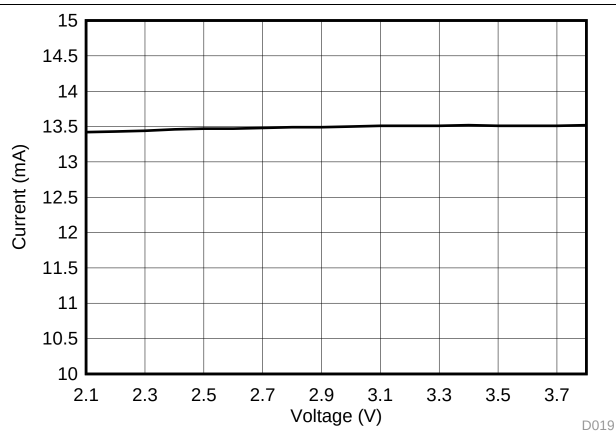

Figure 5-29. TX Maximum Output Power vs VDDS, 868 MHz

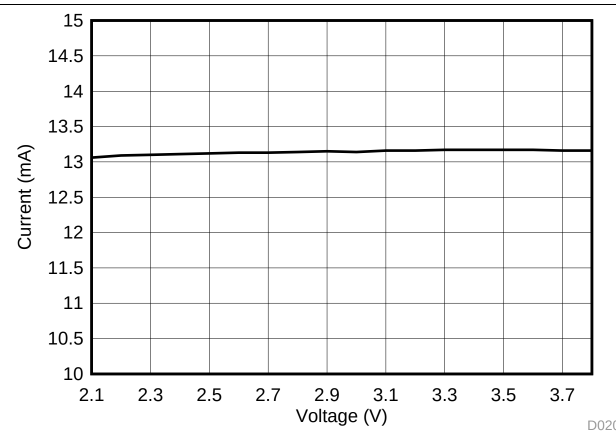

Figure 5-30. TX Maximum Output Power vs VDDS, 915 MHz

Unless otherwise stated, all performance figures represent an average over six typical parts at room temperature and with the internal DC/DC converter enabled.

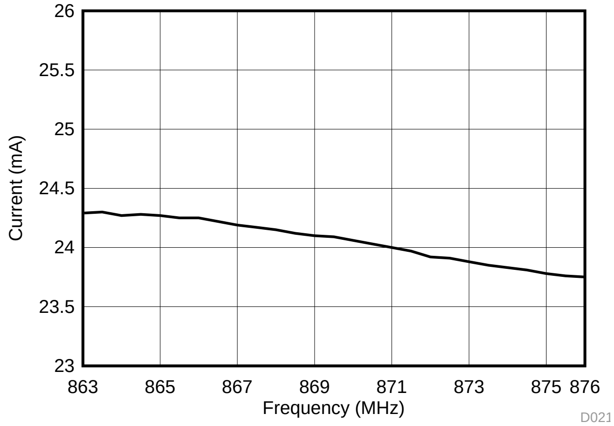

Figure 5-31. TX Current With Maximum Output Power, 863 MHz to 876 MHz

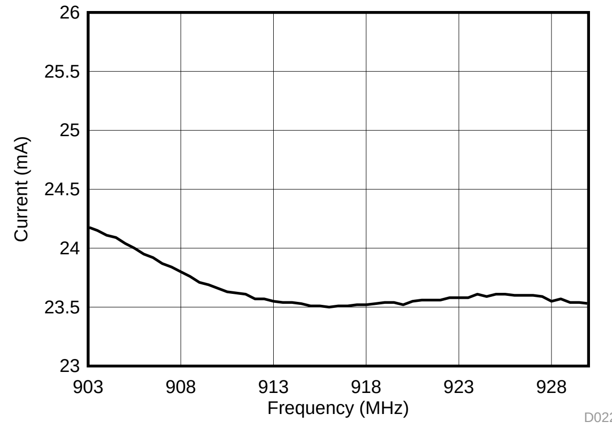

Figure 5-32. TX Current With Maximum Output Power, 902 MHz to 928 MHz

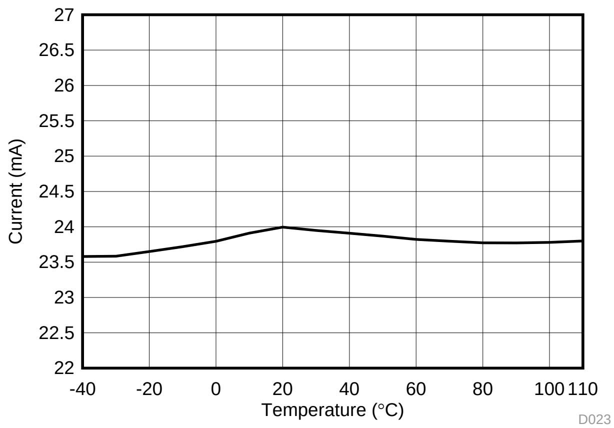

Figure 5-33. TX Current With Maximum Output Power vs Temperature, 868 MHz

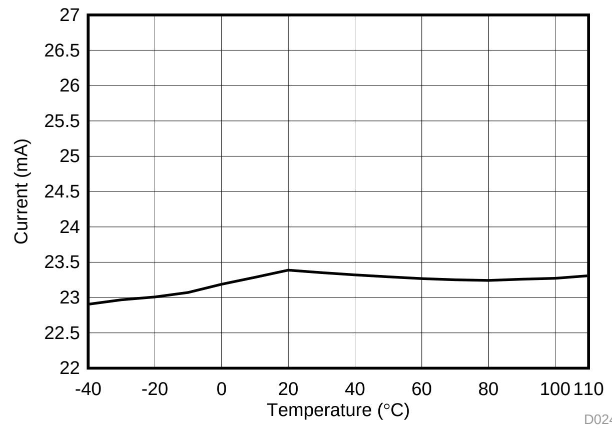

Figure 5-34. TX Current With Maximum Output Power vs Temperature, 915 MHz

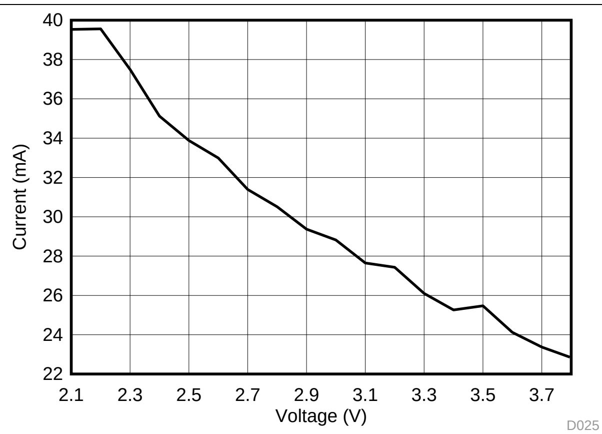

Figure 5-35. TX Current With Maximum Output Power vs Voltage, 868 MHz

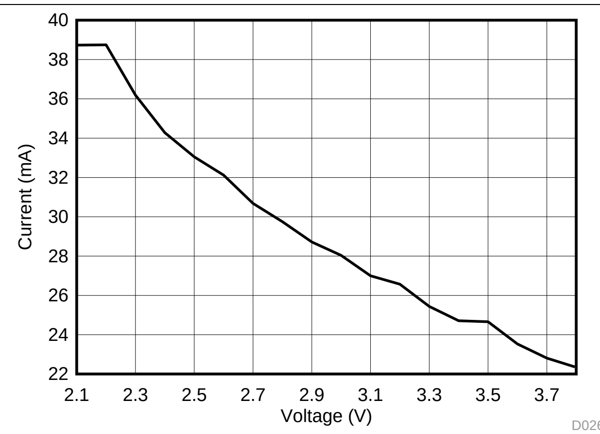

Figure 5-36. TX Current With Maximum Output Power vs Voltage, 915 MHz

Unless otherwise stated, all performance figures represent an average over six typical parts at room temperature and with the internal DC/DC converter enabled.

5.24 Typical Characteristics – 2.4 GHz

Unless otherwise stated, all performance figures represent an average over six typical parts at room temperature and with the internal DC/DC converter enabled.

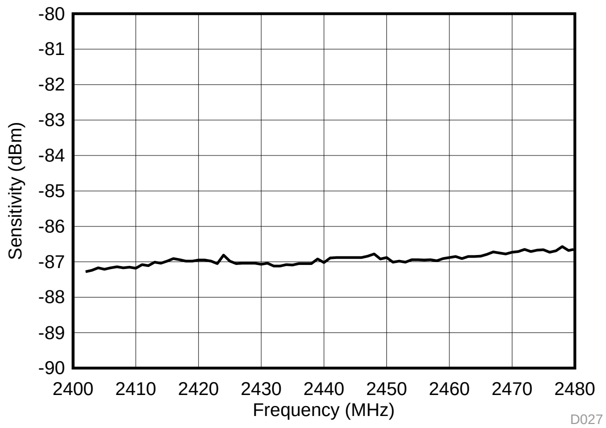

Figure 5-37. RX Bluetooth low energy Sensitivity vs Frequency 2402 MHz to 2480 MHz

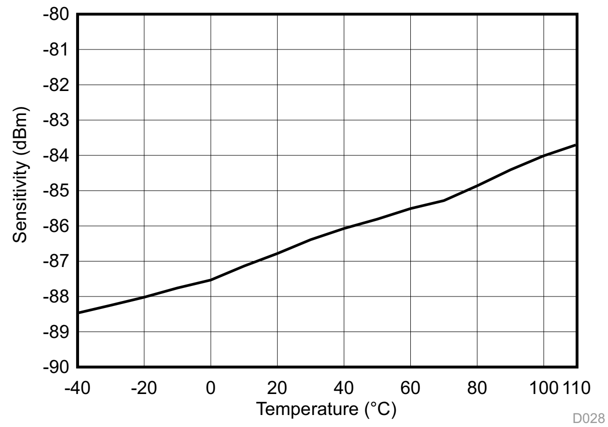

Figure 5-38. RX Bluetooth low energy Sensitivity vs Temperature 2440 MHz

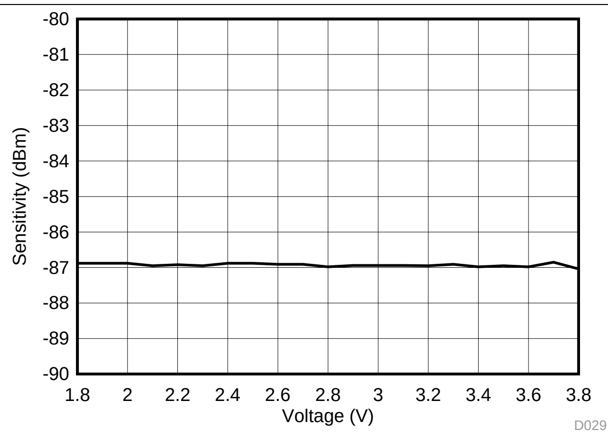

Figure 5-39. RX Bluetooth low energy Sensitivity vs Voltage, 2440 MHz

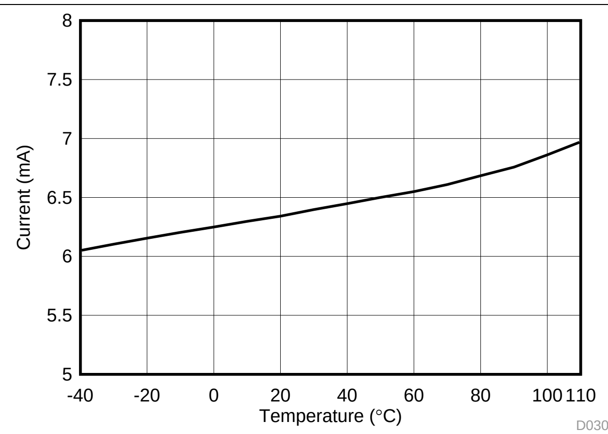

Figure 5-40. RX Bluetooth low energy Current vs Temperature at 2440 MHz

Unless otherwise stated, all performance figures represent an average over six typical parts at room temperature and with the internal DC/DC converter enabled.

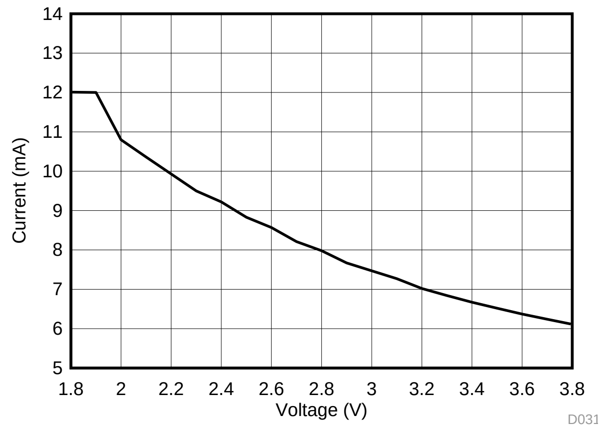

Figure 5-41. RX Bluetooth low energy Current vs Voltage at 2440 MHz

Figure 5-42. RX Bluetooth low energy Selectivity vs Frequency Offset

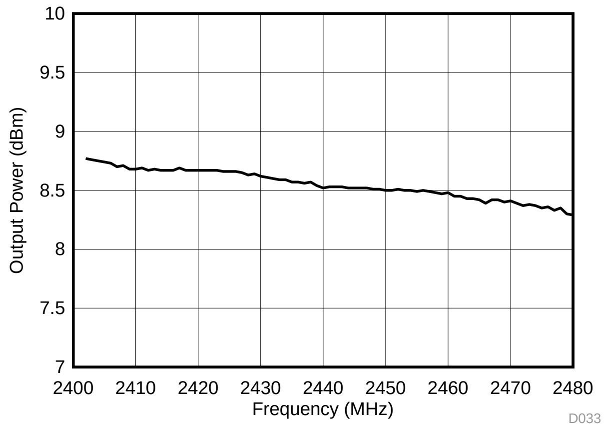

Figure 5-43. TX Bluetooth low energy Maximum Output Power, 2402 MHz to 2480 MHz

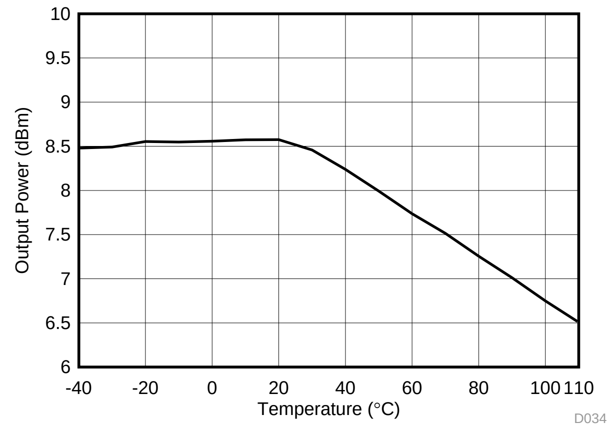

Figure 5-44. TX Bluetooth low energy Maximum Output Power vs Temperature, 2440 MHz

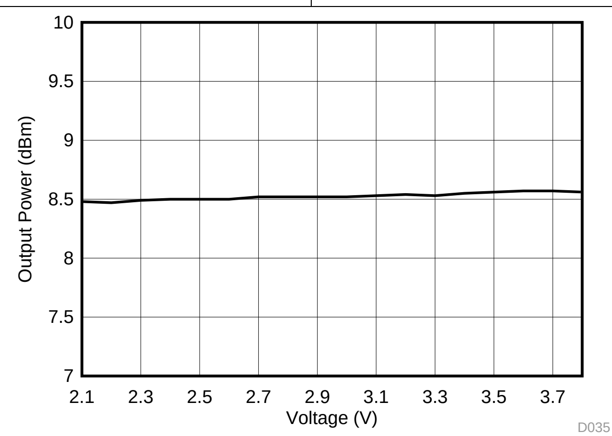

Figure 5-45. TX Bluetooth low energy Maximum Output Power vs VDDS, 2440 MHz

6 Detailed Description

6.1 Overview

Section 1.4 shows a block diagram of the core modules of the CC13xx product family.

6.2 Main CPU

The CC1350 SimpleLink Wireless MCU contains an ARM Cortex-M3 (CM3) 32-bit CPU, which runs the application and the higher layers of the protocol stack.

The CM3 processor provides a high-performance, low-cost platform that meets the system requirements of minimal memory implementation and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

The CM3 features include the following:

- 32-bit ARM Cortex-M3 architecture optimized for small-footprint embedded applications
- Outstanding processing performance combined with fast interrupt handling
- ARM Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit ARM core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for microcontroller-class applications:
  - Single-cycle multiply instruction and hardware divide
  - Atomic bit manipulation (bit-banding), delivering maximum memory use and streamlined peripheral control
  - Unaligned data access, enabling data to be efficiently packed into memory
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system, and memories
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- Deterministic, high-performance interrupt handling for time-critical applications
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial wire trace reduces the number of pins required for debugging and tracing
- Migration from the ARM7™ processor family for better performance and power efficiency
- Optimized for single-cycle flash memory use
- Ultra-low power consumption with integrated sleep modes
- 1.25 DMIPS per MHz

6.3 RF Core

The RF core is a highly flexible and capable radio system that interfaces the analog RF and baseband circuits, handles data to and from the system side, and assembles the information bits in a given packet structure.

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU and leaving more resources for the user application. The RF core offers a high-level, command-based API to the main CPU.

The RF core supports a wide range of modulation formats, frequency bands, and accelerator features, which include the following:

- Wide range of data rates:
  - From 625 bps (offering long range and high robustness) to as high as 4 Mbps
- Wide range of modulation formats:
  - Multilevel (G) FSK and MSK
  - On-Off Keying (OOK) with optimized shaping to minimize adjacent channel leakage
  - Coding-gain support for long range
- Dedicated packet handling accelerators:
  - Forward error correction
  - Data whitening
  - 802.15.4g mode-switch support
  - Automatic CRC
- Automatic listen-before-talk (LBT) and clear channel assist (CCA)
- Digital RSSI
- Highly configurable channel filtering, supporting channel spacing schemes from 40 kHz to 4 MHz
- High degree of flexibility, offering a future-proof solution

The RF core interfaces a highly flexible radio, with a high-performance synthesizer that can support a wide range of frequency bands.

6.4 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in standby mode. The peripherals in this domain may be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously; thereby significantly reducing power consumption and offloading the main CM3 CPU.

A PC-based development tool called *Sensor Controller Studio* is used to write, test, and debug code for the Sensor Controller. The tool produces C driver source code, which the System CPU application uses to control and exchange data with the Sensor Controller. Typical use cases may be (but are not limited to) the following:

- Analog sensors using integrated ADC
- Digital sensors using GPIOs with bit-banged I^2C or SPI
- Capacitive sensing
- Waveform generation
- Pulse counting
- Key scan
- Quadrature decoder for polling rotational sensors

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the device from any state in which the comparator is active. A configurable internal reference can be used with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller takes care of baseline tracking, hysteresis, filtering, and other related functions.
- The ADC is a 12-bit, 200-ksamples/s ADC with 8 inputs and a built-in voltage reference. The ADC can be triggered by many different sources, including timers, I/O pins, software, the analog comparator, and the RTC.
- The analog modules can be connected to up to eight different GPIOs (see Table 6-1).

The peripherals in the Sensor Controller can also be controlled from the main application processor.

Table 6-1. GPIOs Connected to the Sensor Controller(1)

ANALOG CAPABLE	CC13x0		
	7 × 7 RGZ DIO NUMBER	5 × 5 RHB DIO NUMBER	4 × 4 RSM DIO NUMBER
Y	30	14	
Y	29	13	
Y	28	12	
Y	27	11	9
Y	26	9	8
Y	25	10	7
Y	24	8	6
Y	23	7	5
N	7	4	2
N	6	3	1
N	5	2	0
N	4	1	
N	3	0	
N	2		
N	1		
N	0		

(1) Depending on the package size, up to 15 pins can be connected to the Sensor Controller. Up to eight of these pins can be connected to analog modules.

6.5 Memory

The flash memory provides nonvolatile storage for code and data. The flash memory is in-system programmable.

The SRAM (static RAM) is split into two 4-KB blocks and two 6-KB blocks and can be used to store data and execute code. Retention of the RAM contents in standby mode can be enabled or disabled individually for each block to minimize power consumption. In addition, if flash cache is disabled, the 8-KB cache can be used as general-purpose RAM.

The ROM provides preprogrammed, embedded TI-RTOS kernel and Driverlib. The ROM also contains a bootloader that can be used to reprogram the device using SPI or UART.

6.6 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface.

6.7 Power Management

To minimize power consumption, the CC1350 device supports a number of power modes and power-management features (see Table 6-2).

Table 6-2. Power Modes

MODE	SOFTWARE-CONFIGURABLE POWER MODES				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	On	Off	Off
Radio	Available	Available	Off	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Current	1.2 mA + 25.5 µA/MHz	570 µA	0.6 µA	185 nA	0.1 µA
Wake-up Time to CPU Active (1)	–	14 µs	174 µs	1015 µs	1015 µs
Register Retention	Full	Full	Partial	No	No
SRAM Retention	Full	Full	Full	No	No
High-Speed Clock	XOSC_HF or RCOSC_HF	XOSC_HF or RCOSC_HF	Off	Off	Off
Low-Speed Clock	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Sensor Controller	Available	Available	Available	Off	Off
Wake-up on RTC	Available	Available	Available	Off	Off
Wake-up on Pin Edge	Available	Available	Available	Available	Off
Wake-up on Reset Pin	Available	Available	Available	Available	Available
Brown Out Detector (BOD)	Active	Active	Duty Cycled	Off	N/A
Power On Reset (POR)	Active	Active	Active	Active	N/A

(1) Not including RTOS overhead.

In active mode, the application CM3 CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see Table 6-2).

In idle mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event returns the processor to active mode.

In standby mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or Sensor Controller event is required to return the device to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In shutdown mode, the device is entirely turned off (including the AON domain and Sensor Controller), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or POR by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independent of the main CPU. This means that the main CPU does not have to wake up, for example to execute an ADC sample or poll a digital sensor over SPI, thus saving both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio lets the user configure the Sensor Controller and choose which peripherals are controlled and which conditions wake up the main CPU.

6.8 Clock Systems

The CC1350 device supports two external and two internal clock sources.

A 24-MHz external crystal is required as the frequency reference for the radio. This signal is doubled internally to create a 48-MHz clock.

The 32.768-kHz crystal is optional. The low-speed crystal oscillator is designed for use with a 32.768-kHz watch-type crystal.

The internal high-speed RC oscillator (48-MHz) can be used as a clock source for the CPU subsystem.

The internal low-speed RC oscillator (32-kHz) can be used as a reference if the low-power crystal oscillator is not used.

The 32-kHz clock source can be used as external clocking reference through GPIO.

6.9 General Peripherals and Modules

The I/O controller controls the digital I/O pins and contains multiplexer circuitry to assign a set of peripherals to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in **bold** in Section 4.

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and TI's synchronous serial interfaces. The SSIs support both SPI master and slave up to 4 MHz.

The UART implements a universal asynchronous receiver and transmitter function. The UART supports flexible baud-rate generation up to a maximum of 3 Mbps.

Timer 0 is a general-purpose timer module (GPTM) that provides two 16-bit timers. The GPTM can be configured to operate as a single 32-bit timer, dual 16-bit timers, or as a PWM module.

Timer 1, Timer 2, and Timer 3 are also GPTMs; each timer is functionally equivalent to Timer 0.

In addition to these four timers, a separate timer in the RF core handles timing for RF protocols; the RF timer can be synchronized to the RTC.

The I2S interface is used to handle digital audio (for more information, see the *CC13x0, CC26x0 SimpleLink™ Wireless MCU Technical Reference Manual*).

The I^2C interface is used to communicate with devices compatible with the I^2C standard. The I^2C interface can handle 100-kHz and 400-kHz operation, and can serve as both I^2C master and I^2C slave.

The TRNG module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.

The watchdog timer is used to regain control if the system fails due to a software error after an external device fails to respond as expected. The watchdog timer can generate an interrupt or a reset when a predefined time-out value is reached.

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the CM3 CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the µDMA controller follow (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits

The AON domain contains circuitry that is always enabled, except when in shutdown mode (where the digital supply is off). This circuitry includes the following:

- The RTC can be used to wake the device from any state where it is active. The RTC contains three compare registers and one capture register. With software support, the RTC can be used for clock and calendar operation. The RTC is clocked from the 32-kHz RC oscillator or crystal. The RTC can also be compensated to tick at the correct frequency even when the internal 32-kHz RC oscillator is used instead of a crystal.
- The battery monitor and temperature sensor are accessible by software and provide a battery status indication as well as a coarse temperature measure.

6.10 Voltage Supply Domains

The CC1350 device can interface to two or three different voltage domains depending on the package type. On-chip level converters ensure correct operation as long as the signal voltage on each input/output pin is set with respect to the corresponding supply pin (VDDS, VDDS2, or VDDS3). Table 6-3 lists the pin-to-VDDS mapping.

Table 6-3. Pin Function to VDDS Mapping Table

	Package		
	VQFN 7 × 7 (RGZ)	**VQFN 5 × 5 (RHB)**	**VQFN 4 × 4 (RSM)**
VDDS(1)	DIO 23–30 Reset_N	DIO 7–14 Reset_N	DIO 5–9 Reset_N
VDDS2	DIO 1–11	DIO 0–6 JTAG_TCKC JTAG_TMSC	DIO 0–4 JTAG_TCKC JTAG_TMSC
VDDS3	DIO 12–22 JTAG_TCKC JTAG_TMSC	NA	NA

(1) The VDDS_DCDC pin must always be connected to the same voltage as the VDDS pin.

6.11 System Architecture

Depending on the product configuration, the CC1350 device can function as a wireless network processor (WNP – a device running the wireless protocol stack, with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the ARM CM3 core inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

7 Application, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

Few external components are required for the operation of the CC1350 device. Figure 7-1 shows a typical application circuit.

The board layout greatly influences the RF performance of the CC1350 device.

On the Texas Instruments CC1350_7XD-Dual Band reference design, the optimal differential impedance seen from the RF pins into the balun and filter and antenna is 44 + j15.

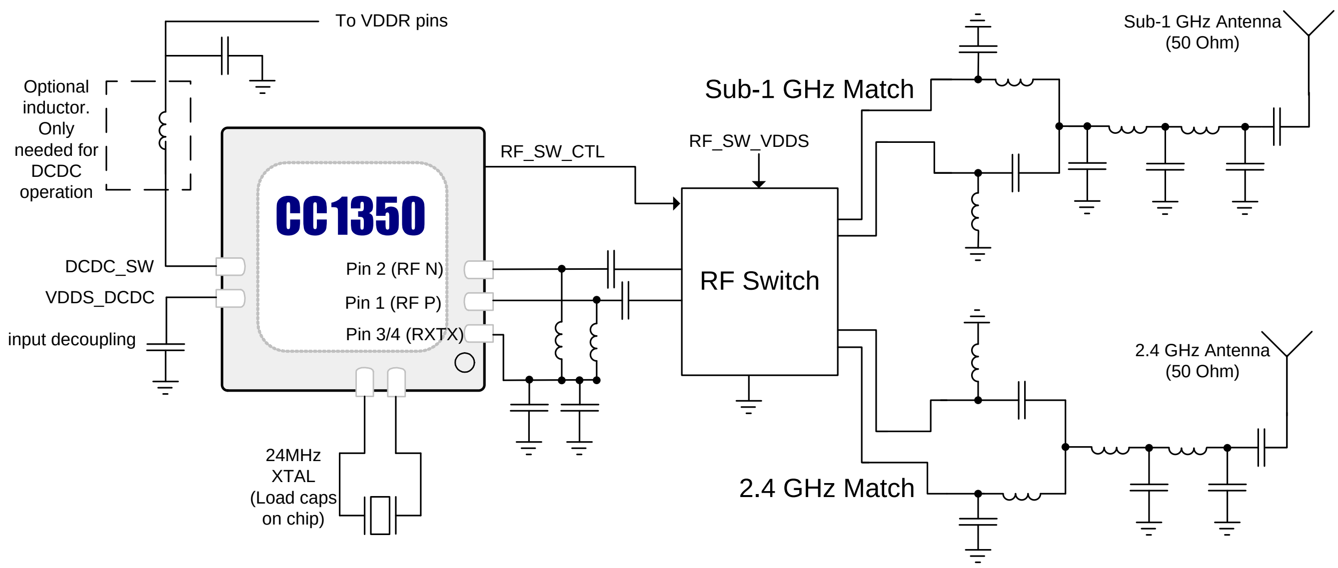

Figure 7-1 does not show decoupling capacitors for power pins. For a complete reference design, see the product folder on www.ti.com.

Figure 7-1. CC1350 Application Circuits

7.2 TI Design or Reference Design

The TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jumpstart your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

Humidity and Temperature Sensor Node for Sub-1 GHz Star Networks Enabling 10+ Year Coin Cell Battery Life

This reference design uses TI's nano-power system timer, boost converter, SimpleLink™ ultra-low-power Sub-1GHzwireless MCU platform, and humidity-sensing technologies to demonstrate an ultra-low-power method to duty-cycle sensor end nodes leading to extremely long battery life. The TI Design includes techniques for system design, detailed test results, and information to get the design operating running quickly.

SimpleLink™ Sub-1 GHz Sensor to Cloud Gateway Reference Design for TI-RTOS Systems

This reference design demonstrates how to connect sensors to the cloud over a long-range Sub-1 GHz wireless network, suitable for industrial settings such as building control and asset tracking. The solution is based on a TI-RTOS gateway. This design provides a complete end-to-end solution for creating a Sub-1 GHz sensor network with an Internet of Things (IoT) gateway solution and cloud connectivity. The gateway solution is based on the low-power, SimpleLink™ Wi-Fi® CC3220 wireless microcontroller (MCU), which hosts the gateway application and the SimpleLink Sub-1 GHz CC1310/CC1312R or the multi-band CC1350/ CC1352R wireless MCU as the MAC Co-Processor. The reference design also includes sensor node example applications running on the SimpleLink Sub-1 GHz CC1312R/CC1310 and multi-band CC1352R/CC1350 wireless MCUs.

Low-Power Wireless M-Bus Communications Module Reference Design

This reference design explains how to use the TI wireless M-Bus stack for CC1310 and CC1350 wireless MCUs and integrate it into a smart meter or data-collector product. This software stack is compatible with the Open Metering System (OMS) v3.0.1 specification. This design offers ready-to-use binary images for any of the wireless M-Bus S-, T-, or C-modes at 868 MHz with unidirectional (meter) or bidirectional configurations (both meter and data collector).

Low-Power Water Flow Measurement With Inductive Sensing Reference Design

This reference design demonstrates a highly-integrated solution for this application using an inductive sensing technique enabled by the CC1310/CC1350 SimpleLink™ Wireless MCU and FemtoFET™ MOSFET. This reference design also provides the platform for integration of wireless communications such as wireless M-Bus, Sigfox™, or a proprietary protocol.

Heat Cost Allocator with wM-Bus at 868 MHz Reference Design

This reference design implements a heat cost allocator system following the EN834 standard with the ‘two-sensor measurement method’. The solution achieves better than 0.5 degrees Celsius accuracy across a range of +20 to +85°C. Two analog temperature sensors are available as matched pairs to eliminate the need for calibration during manufacturing and lowering OEM system cost. The CC1310 wireless MCU provides a single-chip solution for heat measurement (control of the two temperature sensors) and RF communications (example code using 868 MHz wM-Bus S, T and C-modes “Meter” device).

Sub-1 GHz Sensor to Cloud Industrial IoT Gateway Reference Design for Linux Systems

This reference design demonstrates how to connect sensors to the cloud over a long-range Sub-1 GHz wireless network, suitable for industrial settings such as building control and asset tracking. This design provides a complete end-to-end solution for creating a Sub-1 GHz sensor network with an Internet of Things (IoT) gateway solution and cloud connectivity. The gateway solution is based on the low-power, SimpleLink™ Wi-Fi® CC3220 wireless microcontroller (MCU), which hosts the gateway application and the SimpleLink Sub-1 GHz CC1312R/CC1310 or the multi-band CC1352R/CC1350 wireless MCU as the MAC Co-Processor.

Commissioning Sensors in a Sub-1 GHz Network Over Bluetooth® low energy Reference Design

This TI Design reference design demonstrates how to easily commission a Sub-1 GHz sensor node over Bluetooth® low energy, which enables quick connectivity with a smartphone or tablet device. The design is powered by the SimpleLink™ dual-band CC1350 wireless microcontroller (MCU), which is the sensor node being commissioned. There is an added option to emulate a sensor network concentrator using a SimpleLink dual-band CC1350 or Sub-1 GHz CC1310 devices for a complete user experience.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed in the following.

8.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, CC1350 is in production; therefore, no prefix/identification is assigned).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RGZ*).

For orderable part numbers of *CC1350* devices in the *RSM (4-mm × 4-mm), RHB (5-mm × 5-mm), or RGZ (7-mm × 7-mm)* package types, see the *Package Option Addendum* of this document, the TI website (www.ti.com), or contact your TI sales representative.

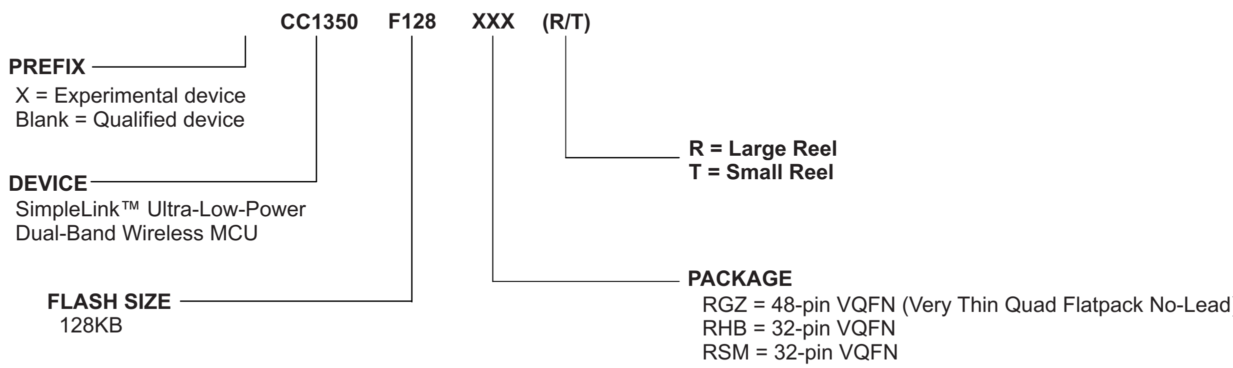

Figure 8-1. Device Nomenclature

8.2 Tools and Software

Development Kit:

Simplelink™ Dual-Band CC1350 Wireless MCU LaunchPad™ Development Kit

The CC1350 LaunchPad™ development kit combines a Bluetooth Smart radio with a Sub-1 GHz radio for the ultimate combination of easy mobile phone integration with long-range connectivity including a 32-bit Arm Cortex-M3 processor on a single chip. The CC1350 device is a wireless MCU targeting low power, long-range wireless applications.

The CC1350 device contains a 32-bit Arm Cortex-M3 processor that runs at 48 MHz as the main processor and a rich peripheral feature set that includes a unique ultra-low-power sensor controller. This sensor controller is great for interfacing external sensors and for collecting analog and digital data autonomously while the rest of the system is in sleep mode.

Software:

SimpleLink™ CC13x0 SDK

The SimpleLink™ Sub-1 GHz CC13x0 software development kit (SDK) provides a comprehensive Sub-1 GHz software package for the Sub-1 GHz CC1310 and Dual-band CC1350 wireless MCUs and includes the following:

- TI 15.4-Stack - IEEE 802.15.4e/g-based star topology networking solution for Sub-1 GHz ISM bands (433 MHz, 868 MHz and 915 MHz).
- Support for proprietary solutions - proprietary RF examples for Sub-1 GHz based on the RF driver and EasyLink Abstraction Layer.
- Bluetooth Low Energy – Stack including support for all Bluetooth core specification 4.2 features as well as a BLE micro-stack to support customers using the Dual-Band CC1350 wireless MCU.

The SimpleLink CC13x0 SDK is part of the TI SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit www.ti.com/simplelink.

Software Tools:

SmartRF™ Studio 7

SmartRF™ Studio is a PC application that helps designers of radio systems to easily evaluate the RF-IC at an early stage in the design process.

- Test functions for transmitting and receiving radio packets, continuous wave transmit and receive
- Evaluate RF performance on custom boards by wiring it to a supported evaluation board or debugger
- Can also be used without any hardware, but then only to generate, edit and export radio configuration settings
- Can be used in combination with several development kits for Texas Instruments' CC1350 RF-ICs

Sensor Controller Studio

Sensor Controller Studio provides a development environment for the CC1350 Sensor Controller. The Sensor Controller is a proprietary, power-optimized CPU inside the CC1350 , which can perform simple background tasks autonomously and independent of the System CPU state.

- Allows for Sensor Controller task algorithms to be implemented using a C-like programming language
- Outputs a Sensor Controller Interface driver, which incorporates the generated Sensor Controller machine code and associated definitions
- Allows for rapid development by using the integrated Sensor Controller task testing and debugging functionality. This allows for live visualization of sensor data and algorithm verification.

IDEs and Compilers:

Code Composer Studio™ IDE

- An integrated development environment (IDE) with project management tools and editor
- Code Composer Studio (CCS) 6.1 and later has built-in support for the CC1350 device family
- Best support for XDS debuggers; XDS100v3, XDS110 and XDS200
- High integration with TI-RTOS with support for TI-RTOS Object View

Code Composer Studio™ Cloud IDE

Code Composer Studio™ (CCS) Cloud is a web-based IDE that allows you to create, edit, and build CCS and Energia projects. After you have successfully built your project, you can download and run on your connected LaunchPad™ development kit. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.

CCS UniFlash

CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

IAR Embedded Workbench® for Arm

- Integrated development environment with project management tools and editor
- IAR EWARM 7.30.3 and later has built-in support for the CC1350 device family
- Broad debugger support, supporting XDS100v3, XDS200, IAR I-jet® and SEGGER J-Link™
- Integrated development environment with project management tools and editor
- RTOS plugin available for TI-RTOS

For a complete listing of development-support tools for the CC1350 platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

8.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com (**CC1350**). In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the CC1350, related peripherals, and other technical collateral is listed in the following.

Errata

CC1350 SimpleLink™ Wireless MCU Silicon Errata

Technical Reference Manual

CC13xx, CC26xx SimpleLink™ Wireless MCU Technical Reference Manual

Reference Guide

CC26xx/CC13xx Power Management Software Developer's Reference Guide

8.4 Texas Instruments Low-Power RF Website

TI's Low-Power RF website has all the latest products, application and design notes, FAQ section, news and events updates. Go to www.ti.com/longrange.

8.5 Additional Information

Texas Instruments offers a wide selection of cost-effective, low-power RF solutions for proprietary and standard-based wireless applications for use in industrial and consumer applications. The selection includes RF transceivers, RF transmitters, RF front ends, and Systems-on-Chips as well as various software solutions for the Sub-1 GHz and 2.4-GHz frequency bands.

In addition, Texas Instruments provides a large selection of support collateral such as development tools, technical documentation, reference designs, application expertise, customer support, third-party and university programs.

Other than providing technical support forums, videos, and blogs, the Low-Power RF E2E Online Community also presents the opportunity to interact with engineers from all over the world.

With a broad selection of product solutions, end-application possibilities, and a range of technical support, Texas Instruments offers the broadest low-power RF portfolio.

8.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.7 Trademarks

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CoreMark is a registered trademark of Embedded Microprocessor Benchmark Consortium.
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Wi-SUN is a trademark of Wi-SUN Alliance, Inc.
Zigbee is a registered trademark of Zigbee Alliance.
All other trademarks are the property of their respective owners.

8.8 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.10 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

9.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CC1350F128RGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1350 F128
CC1350F128RGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1350 F128
CC1350F128RGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1350 F128
CC1350F128RGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1350 F128
CC1350F128RHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1350 F128
CC1350F128RHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1350 F128
CC1350F128RHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1350 F128
CC1350F128RHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1350 F128
CC1350F128RSMR	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1350 F128
CC1350F128RSMR.B	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1350 F128
CC1350F128RSMT	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1350 F128
CC1350F128RSMT.B	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1350 F128
CC1350F128RSMTG4	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1350 F128
CC1350F128RSMTG4.B	Active	Production	VQFN (RSM) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1350 F128

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

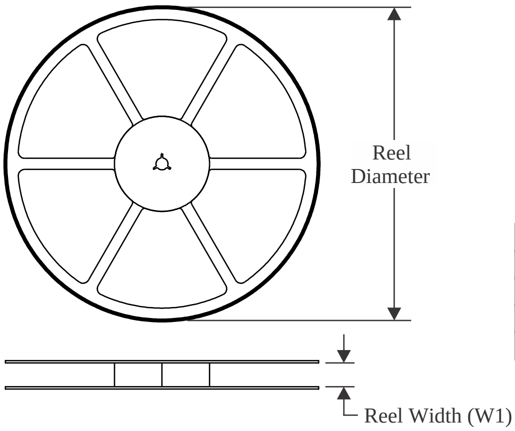
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

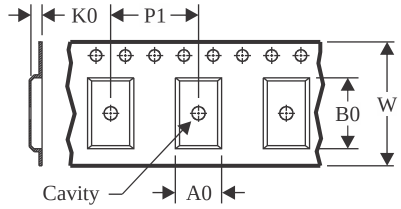
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

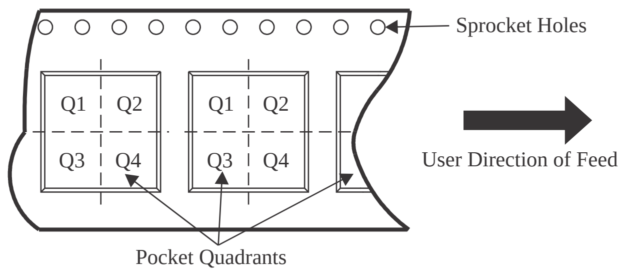


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

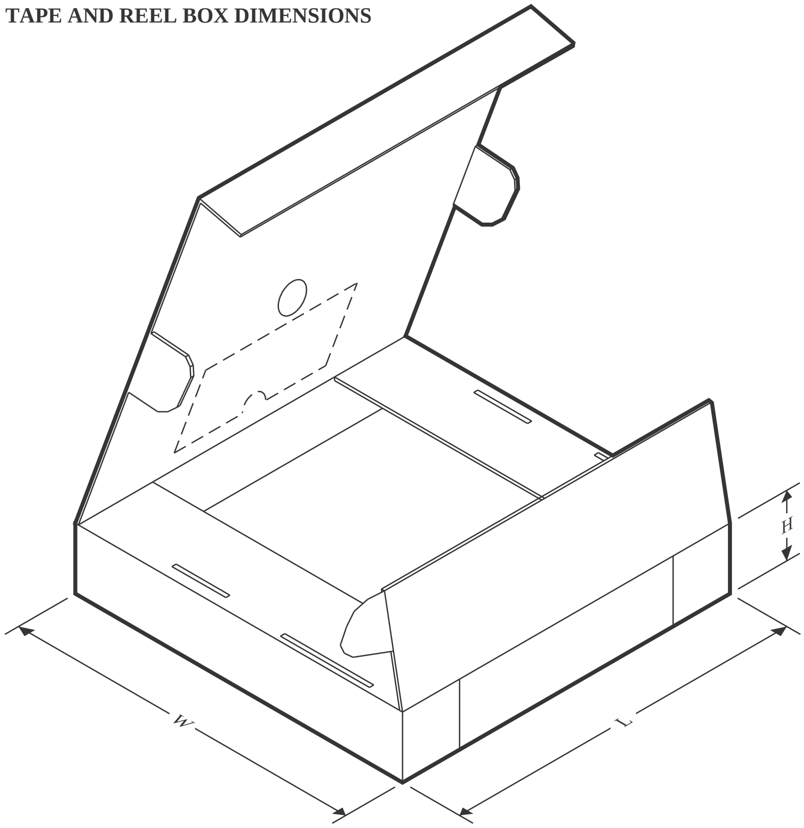
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC1350F128RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1350F128RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1350F128RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC1350F128RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC1350F128RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC1350F128RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC1350F128RSMTG4	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

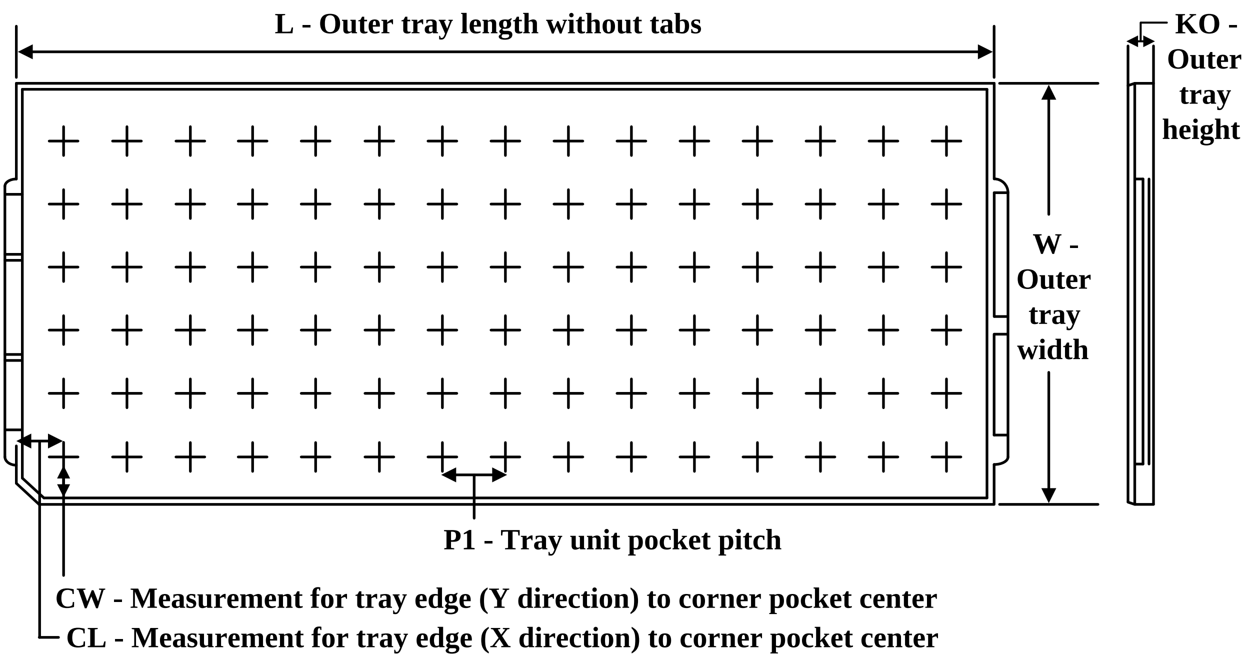
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC1350F128RGZR	VQFN	RGZ	48	2500	367.0	367.0	35.0
CC1350F128RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
CC1350F128RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
CC1350F128RHBT	VQFN	RHB	32	250	210.0	185.0	35.0
CC1350F128RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
CC1350F128RSMT	VQFN	RSM	32	250	210.0	185.0	35.0
CC1350F128RSMTG4	VQFN	RSM	32	250	210.0	185.0	35.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
CC1350F128RGZR	RGZ	VQFN	48	2500	26 x 10	150	315	135.9	7620	11.8	10	10.35
CC1350F128RGZR	RGZ	VQFN	48	2500	26 x 10	150	315	135.9	7620	11.8	10	10.35
CC1350F128RGZR.B	RGZ	VQFN	48	2500	26 x 10	150	315	135.9	7620	11.8	10	10.35
CC1350F128RGZR.B	RGZ	VQFN	48	2500	26 x 10	150	315	135.9	7620	11.8	10	10.35
CC1350F128RGZT	RGZ	VQFN	48	250	26 x 10	150	315	135.9	7620	11.8	10	10.35
CC1350F128RGZT.B	RGZ	VQFN	48	250	26 x 10	150	315	135.9	7620	11.8	10	10.35
CC1350F128RHBR	RHB	VQFN	32	3000	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC1350F128RHBR.B	RHB	VQFN	32	3000	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC1350F128RHBT	RHB	VQFN	32	250	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC1350F128RHBT.B	RHB	VQFN	32	250	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC1350F128RSMR	RSM	VQFN	32	3000	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC1350F128RSMR	RSM	VQFN	32	3000	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC1350F128RSMR.B	RSM	VQFN	32	3000	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC1350F128RSMR.B	RSM	VQFN	32	3000	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC1350F128RSMT	RSM	VQFN	32	250	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC1350F128RSMT	RSM	VQFN	32	250	14 x 35	150	315	135.9	7620	8.8	7.9	8.15
CC1350F128RSMT.B	RSM	VQFN	32	250	14 x 35	150	315	135.9	7620	8.8	7.9	8.15

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
CC1350F128RSMT.B	RSM	VQFN	32	250	14 x 35	150	315	135.9	7620	8.8	7.9	8.15

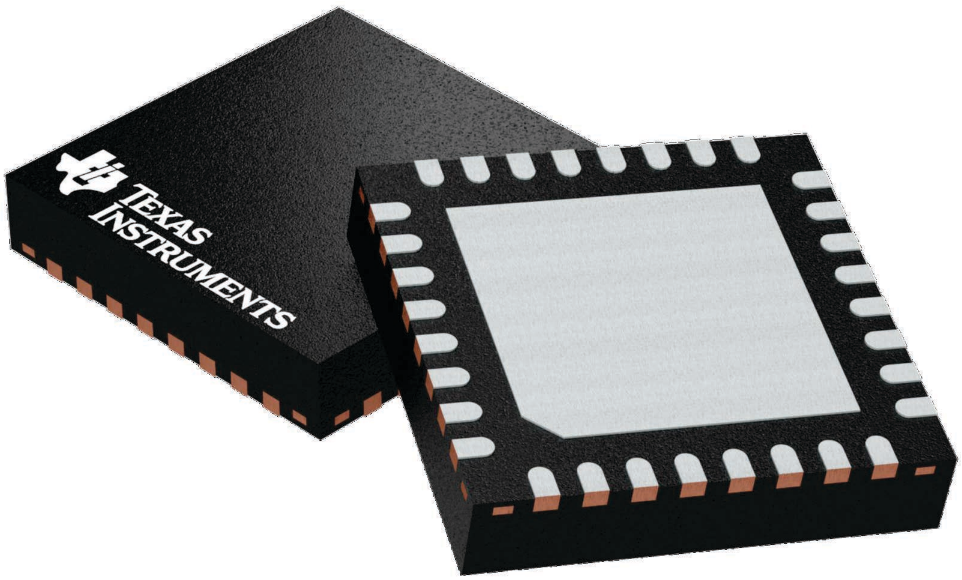
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



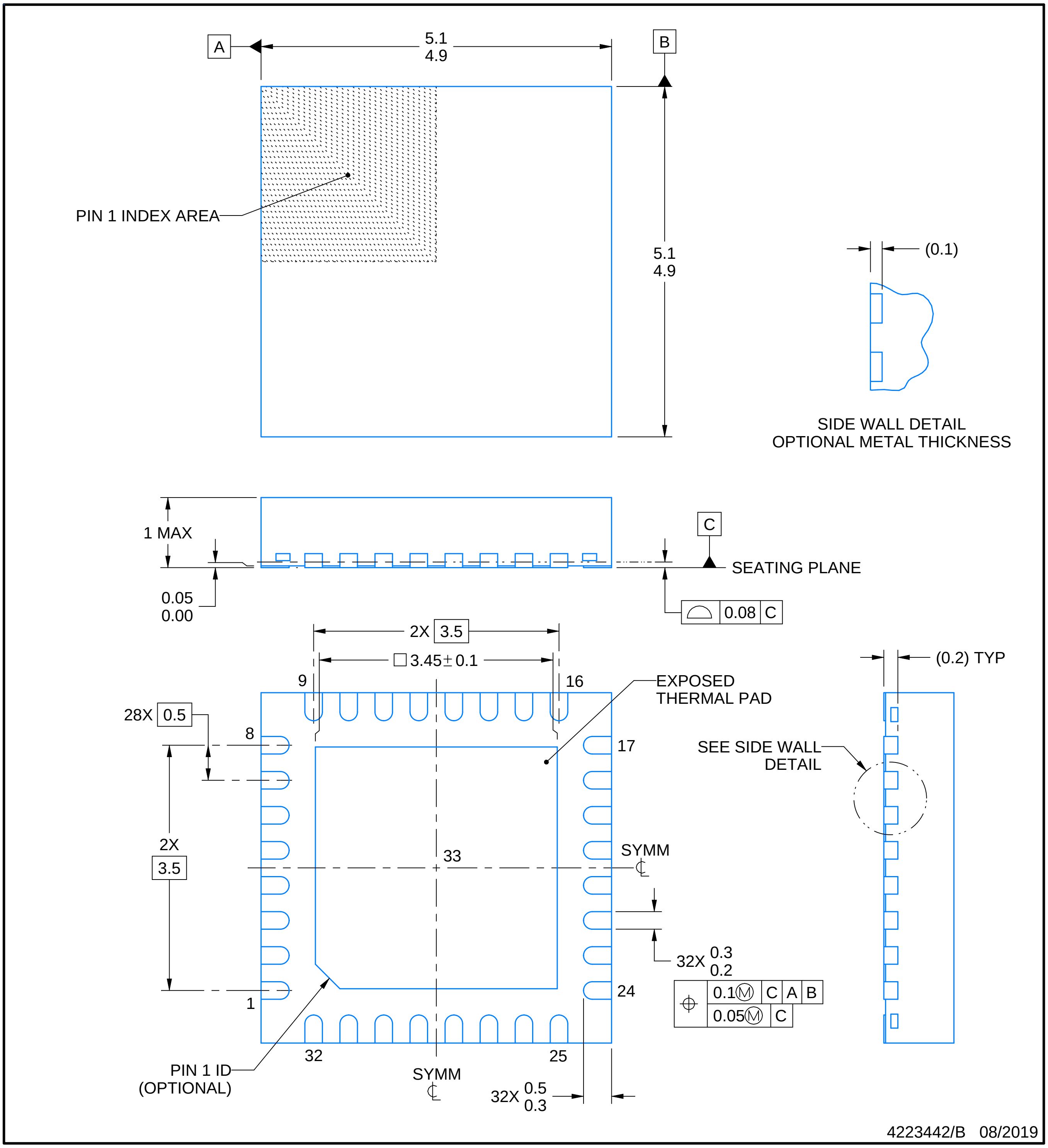
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

PACKAGE OUTLINE

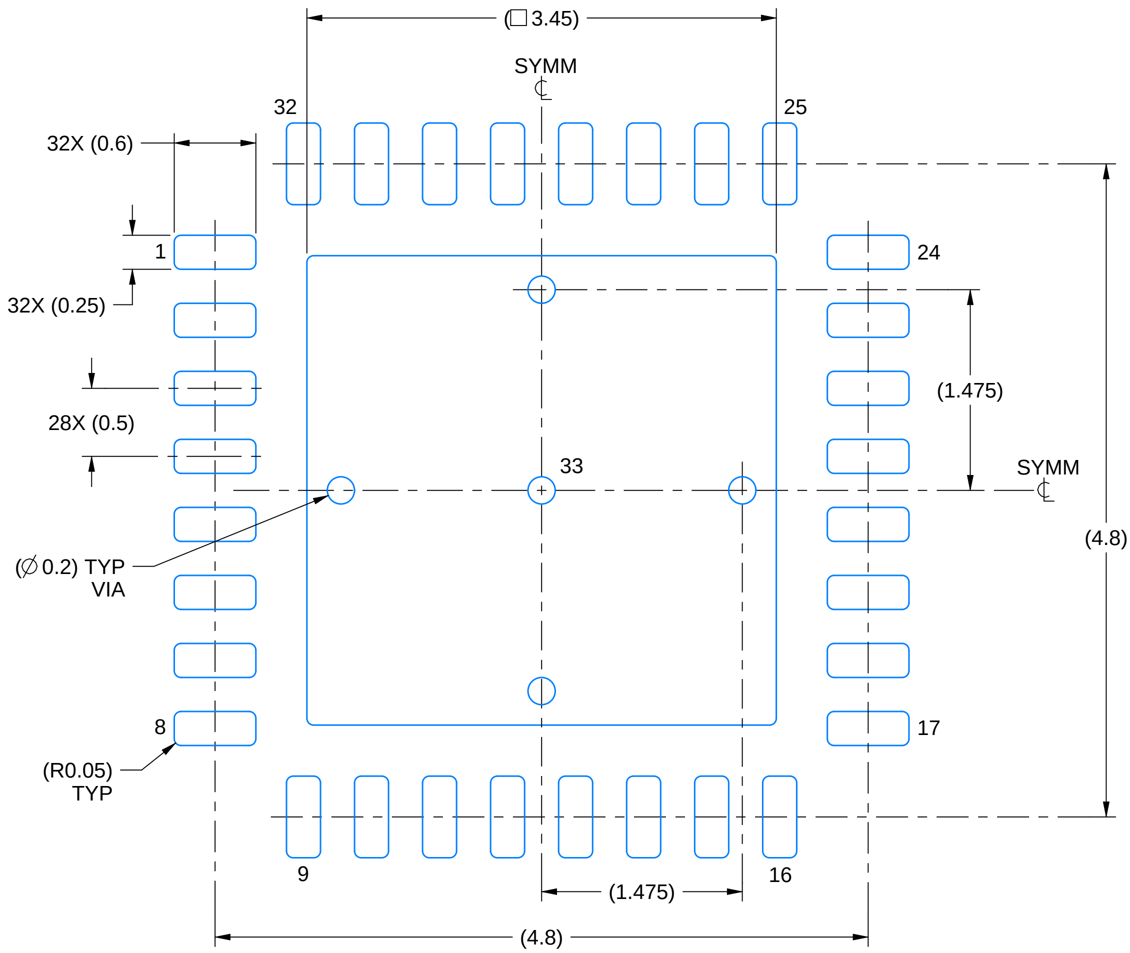
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

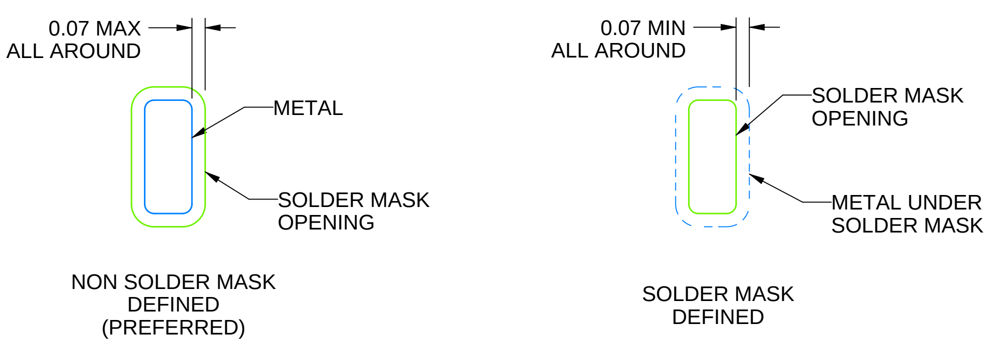


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

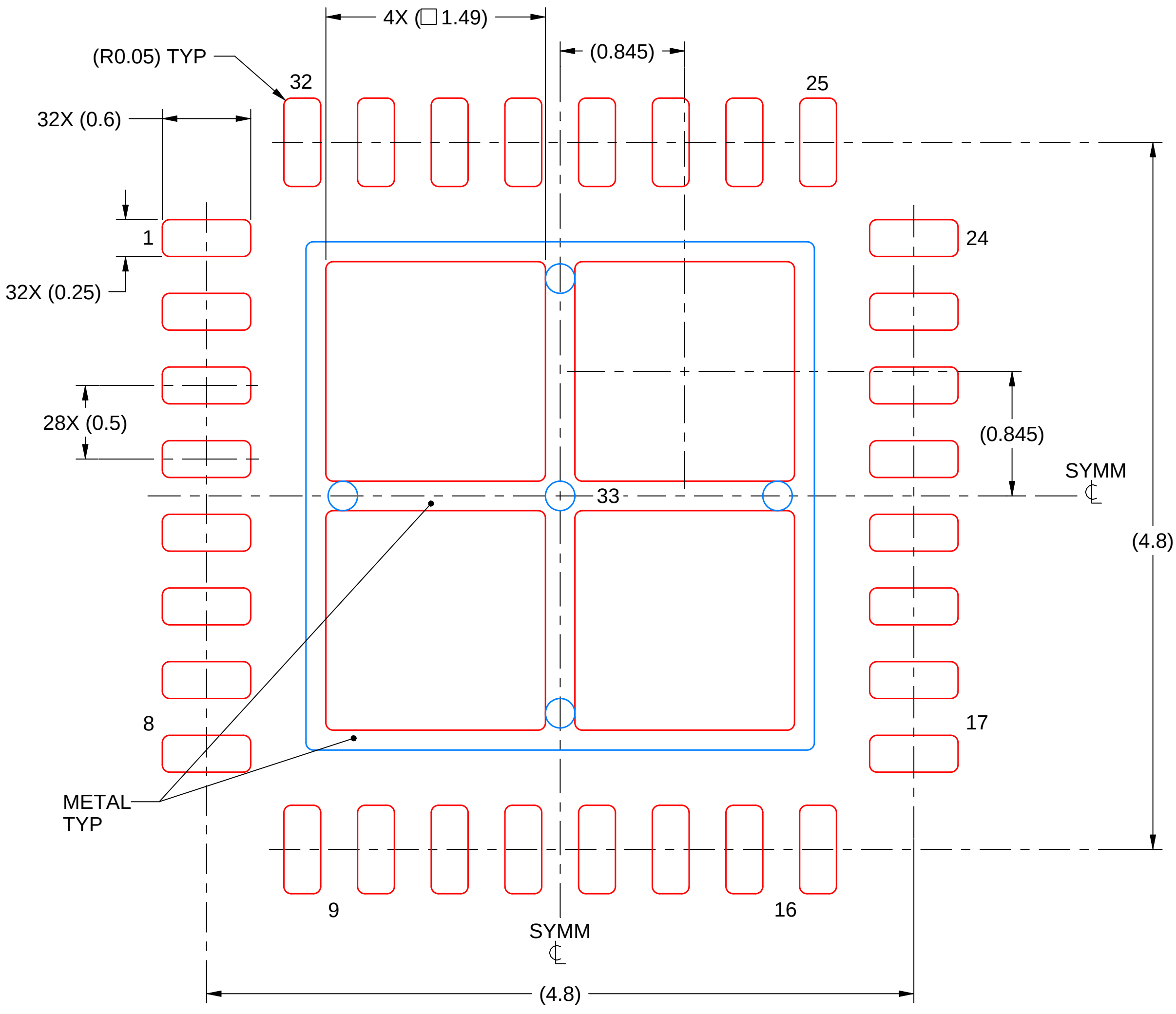


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

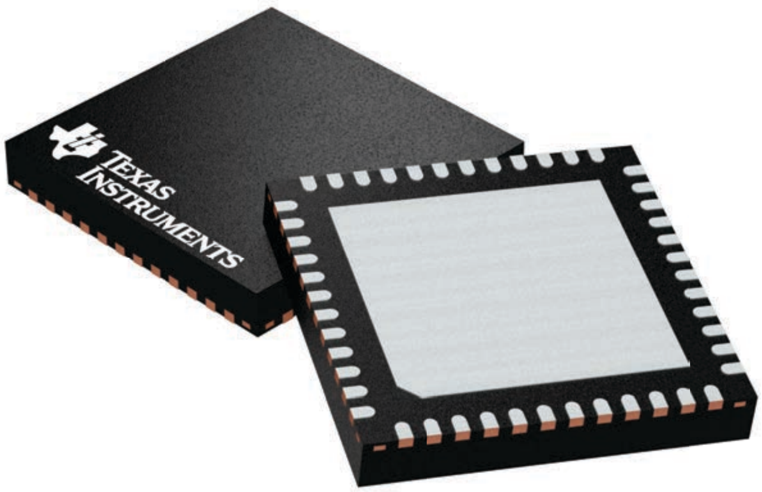
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RGZ 48

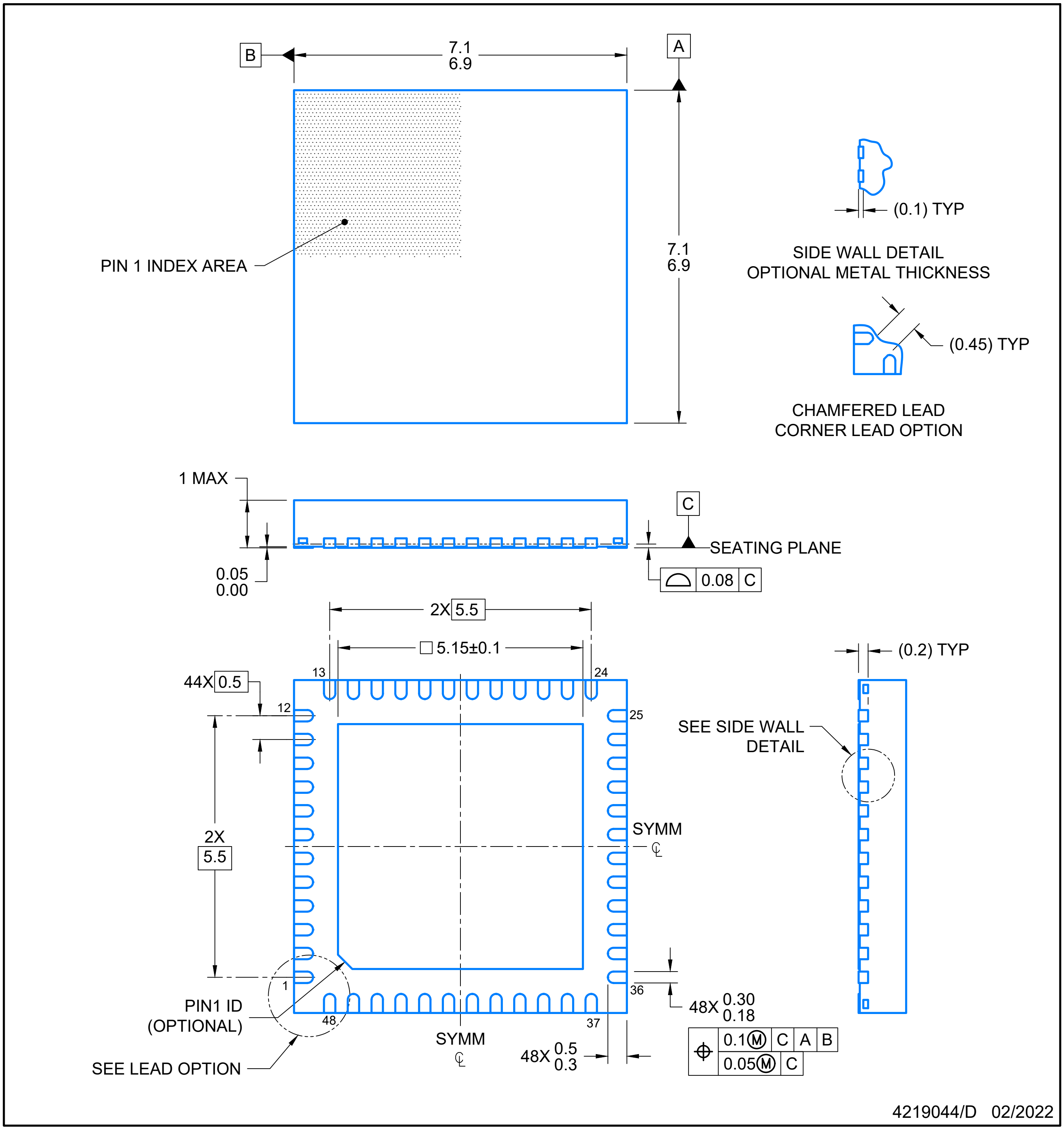
VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD

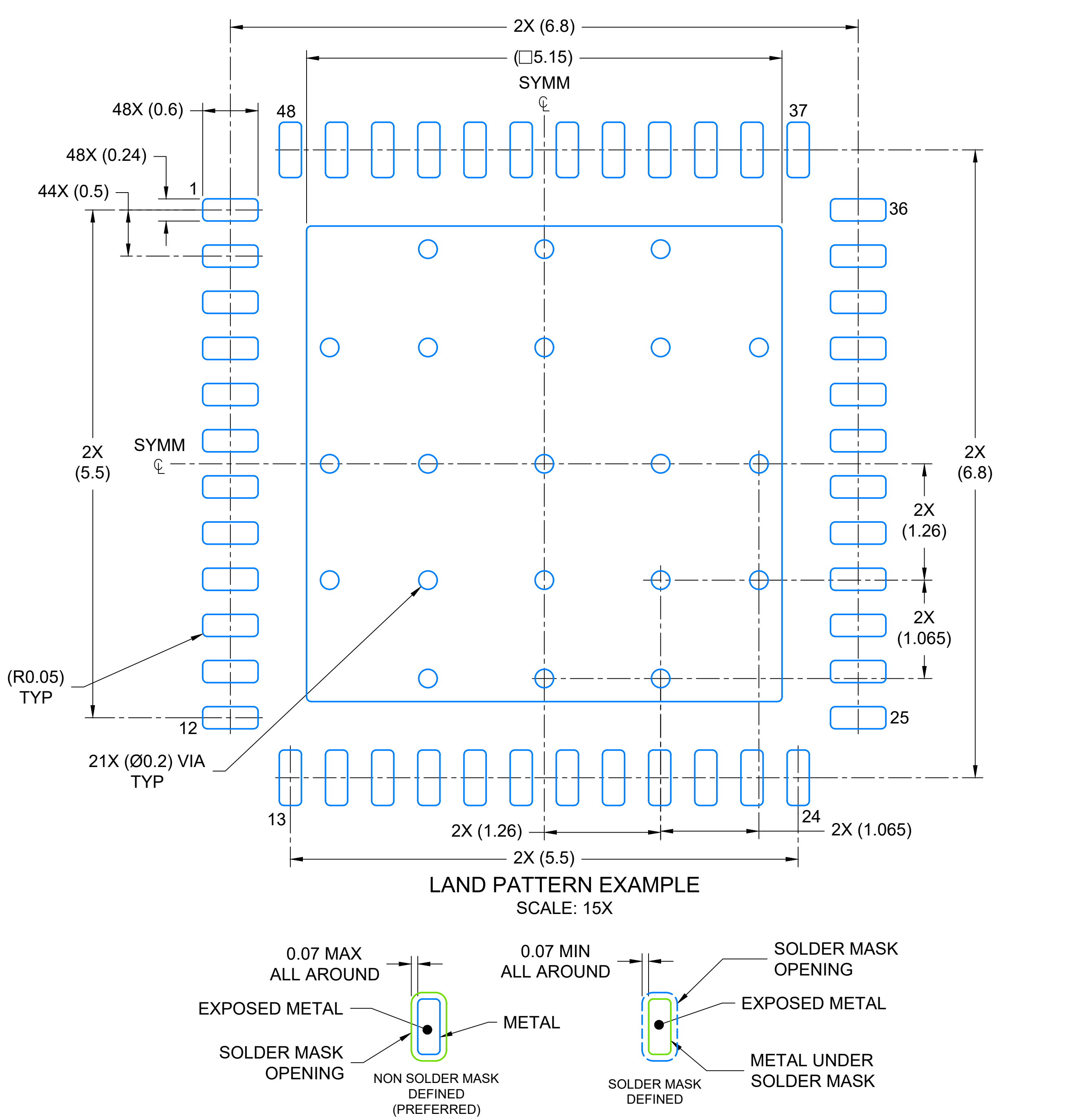


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



NOTES:

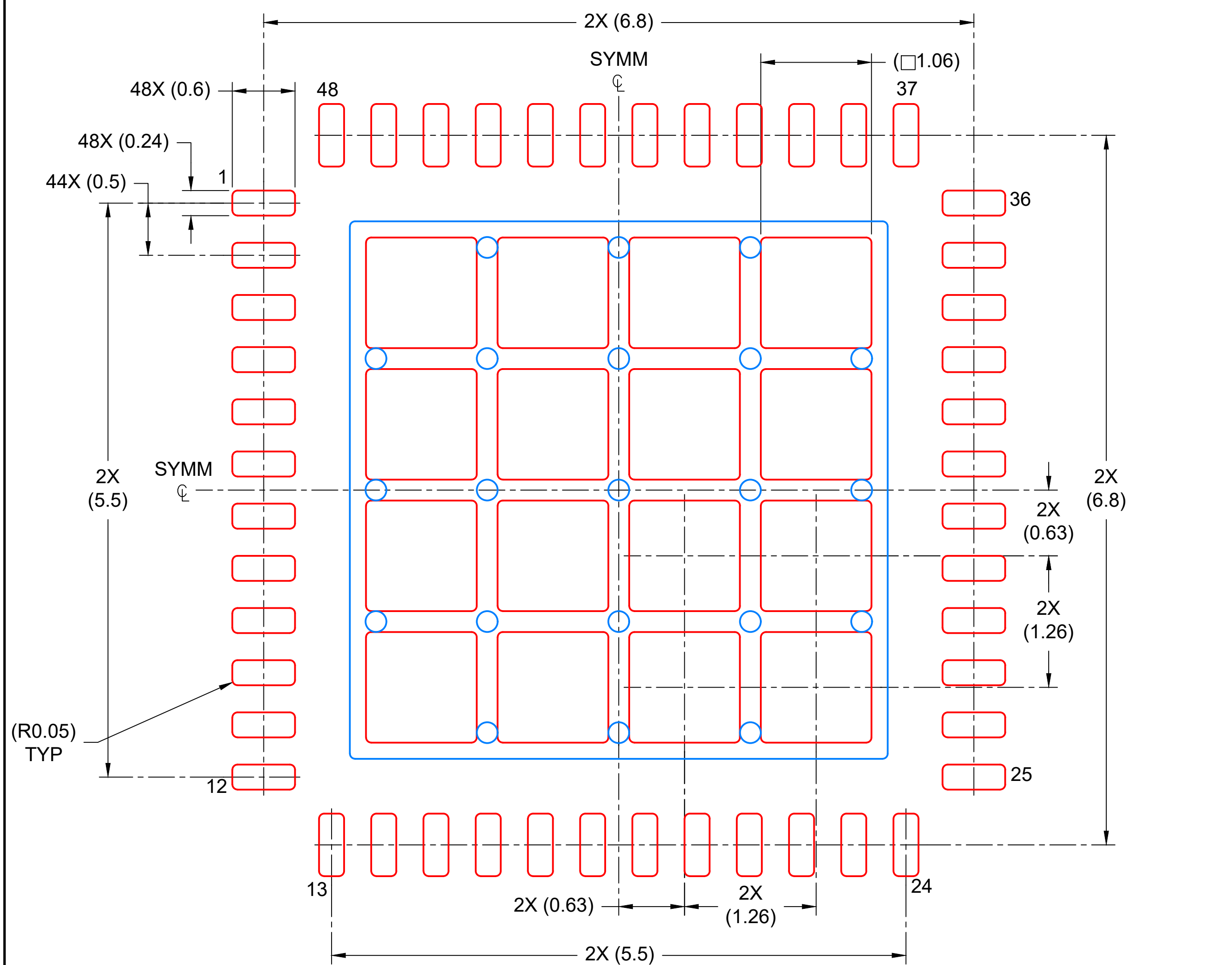
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



4219044/D 02/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/D 02/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

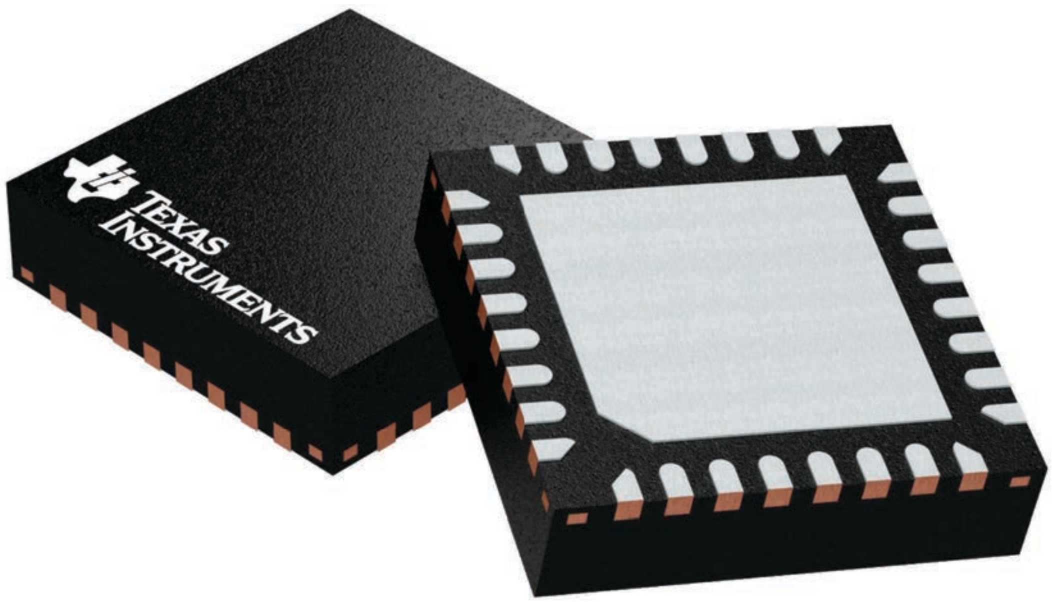
RSM 32

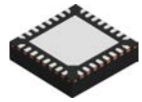
VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

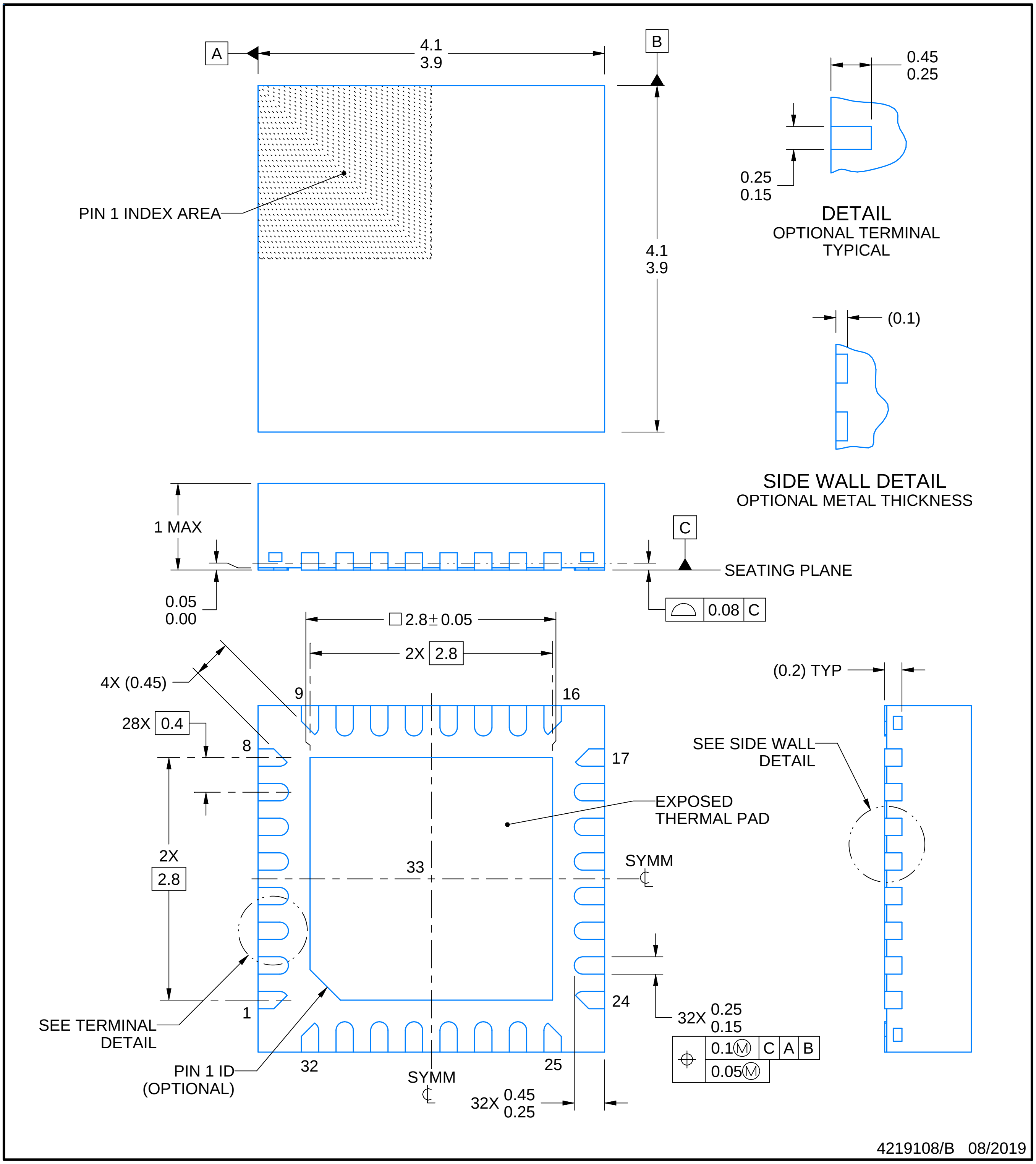




PACKAGE OUTLINE

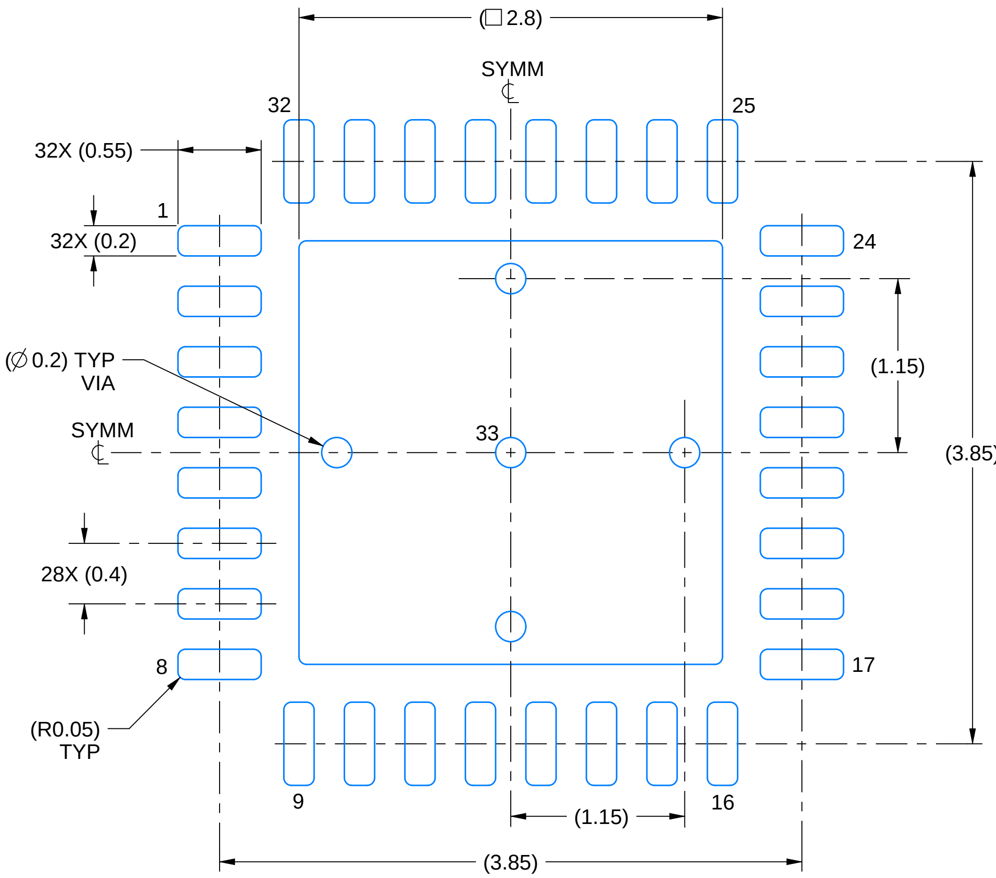
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

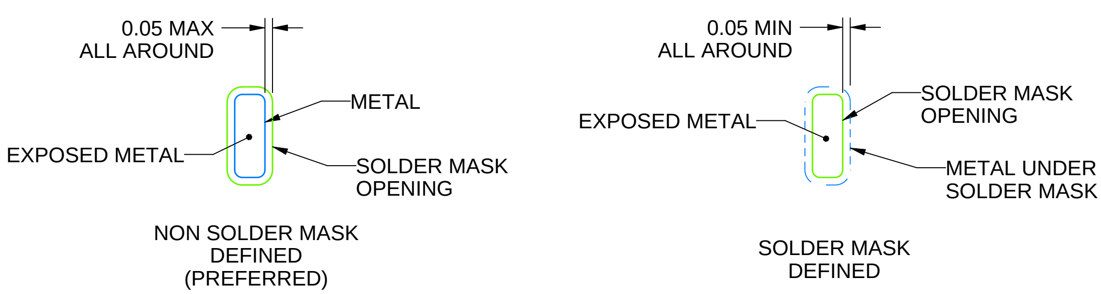


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

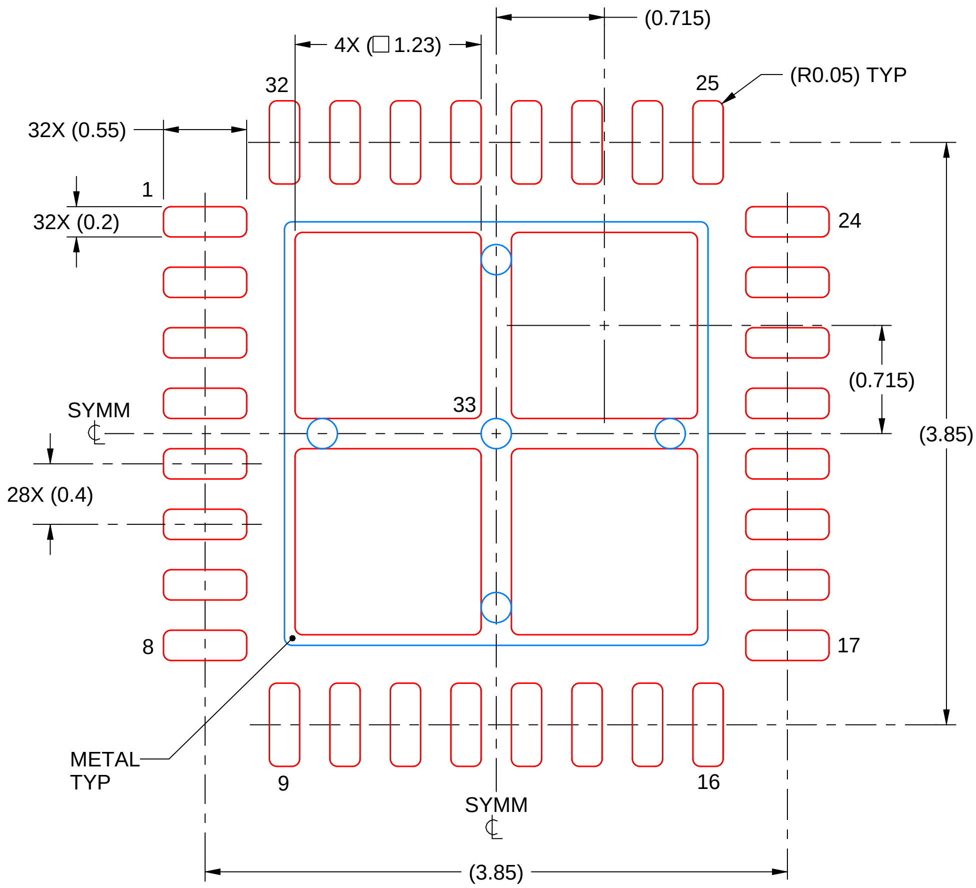


SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219108/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.