AMC0x36-Q1 Automotive, Precision, ±1V Input, Basic and Reinforced Isolated Delta-Sigma Modulators With External Clock

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Linear input voltage range: ±1V
- High input impedance: 2.4GΩ (typical)
- Supply voltage range:
  - High-side (AVDD): 3.0V to 5.5V
  - Low-side (DVDD): 2.7V to 5.5V
- Low DC errors:
  - Offset error: ±0.9mV (maximum)
  - Offset drift: 6.5µV/°C (maximum)
  - Gain error: ±0.25% (maximum)
  - Gain drift: ±35ppm/°C (maximum)
- High CMTI: 150V/ns (minimum)
- Missing high-side supply detection
- Low EMI: Meets CISPR-11 and CISPR-25 standards
- Isolation ratings:
  - AMC0236-Q1: Basic isolation
  - AMC0336-Q1: Reinforced Isolation
- Safety-related certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL1577

2 Applications

- Traction inverters
- Onboard chargers
- DC/DC converters

3 Description

The AMC0x36-Q1 is a precision, galvanically isolated delta-sigma (ΔΣ) modulator with a ±1V, high impedance input and external clock. The high-impedance input is optimized for connection to high-impedance resistive dividers or other voltage signal sources with high output resistance.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels. The isolation barrier is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation up to $5kV_{RMS}$ (DWV package) and basic isolation up to $3kV_{RMS}$ (D package) (60s).

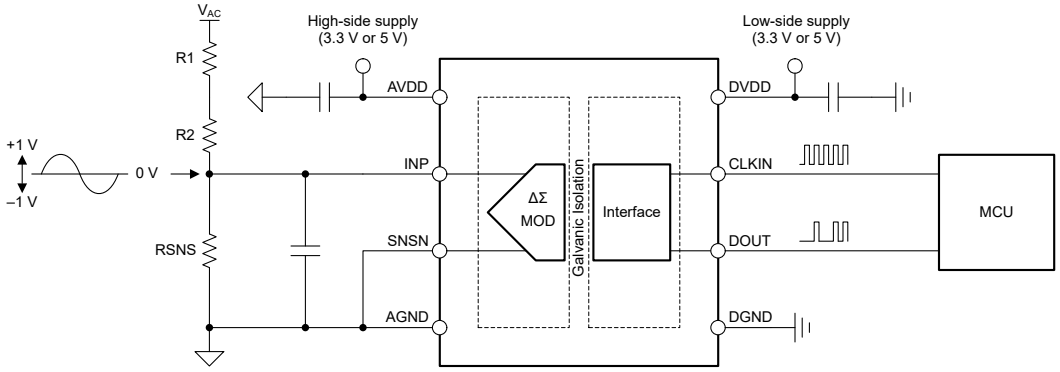
The output bitstream of the AMC0x36-Q1 is synchronized to an external clock. Combined with a sinc3, OSR 256 filter, the device achieves 14.8 effective bits of resolution or 89dB of dynamic range, at a 39kSPS sample rate.

The AMC0x36-Q1 devices come in 8-pin, wide-and narrow-body SOIC packages, and are fully specified over the temperature range from –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AMC0236-Q1 (3)	D (SOIC, 8)	4.9mm × 6mm
AMC0336-Q1	DWV (SOIC, 8)	5.85mm × 11.5mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information* section.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Product Preview, not Production Data.



Typical Application

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4 Device Comparison Table

PARAMETER	AMC0236-Q1 (1)	AMC0336-Q1
Isolation rating per VDE 0884-17	Basic	Reinforced
Package	Narrow-body SOIC (D)	Wide-body SOIC (DWV)

(1) Product Preview, not Advance Information.

5 Pin Configuration and Functions

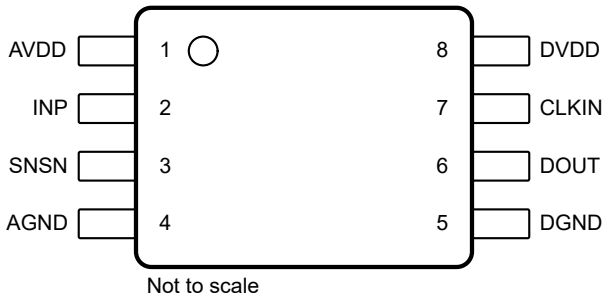


Figure 5-1. DWV and D Package, 8-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	AVDD	High-side power	Analog (high-side) power supply(1)
2	INP	Analog input	Noninverting analog input. Connect a 10nF filter capacitor from INP to SNSN.
3	SNSN	Analog input	AGND sense pin and inverting input to the modulator. Connect to AGND.
4	AGND	High-side ground	Analog (high-side) ground
5	DGND	Low-side ground	Digital (low-side) ground
6	DOUT	Digital output	Modulator data output
7	CLKIN	Digital input	Modulator clock input with internal pulldown resistor (typical value: 1.5MΩ)
8	DVDD	Low-side power	Digital (low-side) power supply(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power-supply voltage	High-side AVDD to AGND	–0.3	6.5	V
	Low-side DVDD to DGND	–0.3	6.5	
Analog input voltage	INP, SNSN to AGND	AGND – 3	AVDD + 0.5	V
Digital input voltage	CLKIN to DGND	DGND – 0.5	DVDD+ 0.5	V
Digital output voltage	DOUT to DGND	DGND – 0.5	DVDD + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1), HBM ESD classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
AVDD	Hgh-side power supply	AVDD to AGND	3	5.0	5.5	V
DVDD	Low-side power supply	DVDD to DGND	2.7	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Input voltage before clipping output	$V_{IN} = V_{INP} – V_{SNSN}$		±1.25		V
V_{FSR}	Specified linear differential input voltage	$V_{IN} = V_{INP} – V_{SNSN}$	–1		1	V
DIGITAL I/O						
V_{IO}	Digital input/output voltage		0		DVDD	V
f_{CLKIN}	Input clock frequency		5	10	11	MHz
t_{HIGH}	Input clock high time		40	50	110	ns
t_{LOW}	Input clock low time		40	50	110	ns
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–40		125	°C

6.4 Thermal Information (D Package)

THERMAL METRIC(1)		D (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Thermal Information (DWV Package)

THERMAL METRIC(1)		DWV (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.6 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	AVDD = DVDD = 5.5V	67	mW
P_{D1}	Maximum power dissipation (high-side)	AVDD = 5.5V	39	mW
P_{D2}	Maximum power dissipation (low-side)	DVDD = 5.5V	28	mW

6.7 Insulation Specifications (Basic Isolation)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 4	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 4	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the insulation	≥ 15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	1130	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	800	V_{RMS}
		At DC voltage	1130	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production test)	4250	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s	≤ 5	
		Method b2, at routine test (100% production)(7), $V_{pd(ini)} = V_{IOTM} = V_{pd(m)}$, $t_{ini} = t_m$ = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5V_{PP} at 1MHz	≅1.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production test)	3000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

6.8 Insulation Specifications (Reinforced Isolation)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 6000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2120	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V_{RMS}
		At DC voltage	2120	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production test)	7000	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	7700	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = 1.2 \times V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	
		Method b2, at routine test (100% production)(7) $V_{pd(ini)} = V_{pd(m)} = 1.2 \times V_{IOTM}$, $t_{ini} = t_m$ = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5V_{PP} at 1MHz	≅1.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

6.9 Safety-Related Certifications (Basic Isolation)

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN 61010-1 (VDE 0411-1) Clause : 6.4.3 ; 6.7.1.3 ; 6.7.2.1 ; 6.7.2.2 ; 6.7.3.4.2 ; 6.8.3.1	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Basic insulation	Single protection
Certificate number: Pending	File number: Pending

6.10 Safety-Related Certifications (Reinforced Isolation)

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: Pending	File number: Pending

6.11 Safety Limiting Values (D Package)

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 116.5°C/W, VDDx = 5.5V, T_J = 150°C, T_A = 25°C			195	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 116.5°C/W, T_J = 150°C, T_A = 25°C			1070	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

6.12 Safety Limiting Values (DWV Package)

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 102.8°C/W, VDDx = 5.5V, T_J = 150°C, T_A = 25°C			220	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 102.8°C/W, T_J = 150°C, T_A = 25°C			1210	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

6.13 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0V to 5.5V, DVDD = 2.7V to 5.5V, V_{INP} = –1V to +1V, and SNSN = AGND; typical specifications are at T_A = 25°C, AVDD = 5V, DVDD = 3.3V, and f_{CLKIN} = 10MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
C_{IN}	Input capacitance	f_{CLKIN} = 10MHz		2		pF
R_{IN}	Input resistance	INP pin to AGND, SNSN = AGND	0.05	2.4		GΩ
I_{IB}	Input bias current(1)	INP pin, INP = AGND	–10	±3	10	nA
CMTI	Common-mode transient immunity		150			V/ns
DC ACCURACY						
E_O	Offset error(1)	T_A = 25°C, INP = AGND	–0.9	±0.1	0.9	mV
TCE_O	Offset error temperature drift(3)			3	6.5	µV/°C
E_G	Gain error(1)	Initial, at T_A = 25°C, V_{INP} = 1V or V_{INP} = –1V	–0.25	±0.02	0.25	%
TCE_G	Gain error temperature drift(4)		–35	±10	35	ppm/°C
INL	Integral nonlinearity(2)	Resolution: 16 bits	–6	±1	6	LSB
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
PSRR	Power-supply rejection ratio	AVDD DC PSRR, IN = AGND, AVDD from 3.3V to 5V with ±10% variation around nominal		–83		dB
		AVDD AC PSRR, IN = AGND, AVDD with10kHz / 100mV ripple		–63		
AC ACCURACY						
SNR	Signal-to-noise ratio	V_{IN} = $2V_{PP}$, f_{IN} = 1kHz	84.5	89		dB
SINAD	Signal-to-noise + distortion	V_{IN} = $2V_{PP}$, f_{IN} = 1kHz	77	88		dB
THD	Total harmonic distortion(5)	V_{IN} = $2V_{PP}$, f_{IN} = 1kHz		–91	–80	dB
DIGITAL INPUT (CMOS Logic With Schmitt-Trigger)						
I_{IN}	Input current	DGND ≤ V_{IN} ≤ DVDD			7	µA
C_{IN}	Input capacitance			4		pF
V_{IH}	High-level input voltage		0.7 x DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 x DVDD	V
DIGITAL OUTPUT (CMOS)						
C_{LOAD}	Output load capacitance	f_{CLKIN} = 10MHz		15	30	pF
V_{OH}	High-level output voltage	I_{OH} = –4mA	DVDD – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4mA			0.4	V
POWER SUPPLY						
I_{AVDD}	High-side supply current			5.3	7	mA
I_{DVDD}	Low-side supply current	C_{LOAD} = 15pF		3.6	5	mA
$AVDD_{UV}$	High-side undervoltage detection threshold	AVDD rising	2.4	2.6	2.8	V
		AVDD falling	1.9	2.05	2.2	
$DVDD_{UV}$	Low-side undervoltage detection threshold	DVDD rising	2.3	2.5	2.7	V
		DVDD falling	1.9	2.05	2.2	

(1) The typical value includes one sigma statistical variation.
(2) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.
(3) Offset error drift is calculated using the box method, as described by the following equation:
$TCE_O = (value_{MAX} - value_{MIN}) / TempRange$
(4) Gain error drift is calculated using the box method, as described by the following equation:
TCE_G (ppm) = $((value_{MAX} - value_{MIN}) / (value \times TempRange)) \times 10^6$
(5) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.

6.14 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_H	DOUT hold time after rising edge of CLKIN	C_{LOAD} = 15pF	10			ns
t_D	Rising edge of CLKIN to DOUT valid delay	C_{LOAD} = 15pF			35	ns
t_r	DOUT rise time	10% to 90%, 2.7V ≤ DVDD ≤ 3.6V, C_{LOAD} = 15pF		2.5	6	ns
		10% to 90%, 4.5V ≤ DVDD ≤ 5.5V, C_{LOAD} = 15pF		3.2	6	
t_f	DOUT fall time	10% to 90%, 2.7V ≤ DVDD ≤ 3.6V, C_{LOAD} = 15pF		2.2	6	ns
		10% to 90%, 4.5V ≤ DVDD ≤ 5.5V, C_{LOAD} = 15pF		2.9	6	
t_{START}	Device start-up time	AVDD step from 0 to 3.0V with DVDD ≥ 2.7V to bitstream valid, 0.1% settling		30		µs

6.15 Timing Diagrams

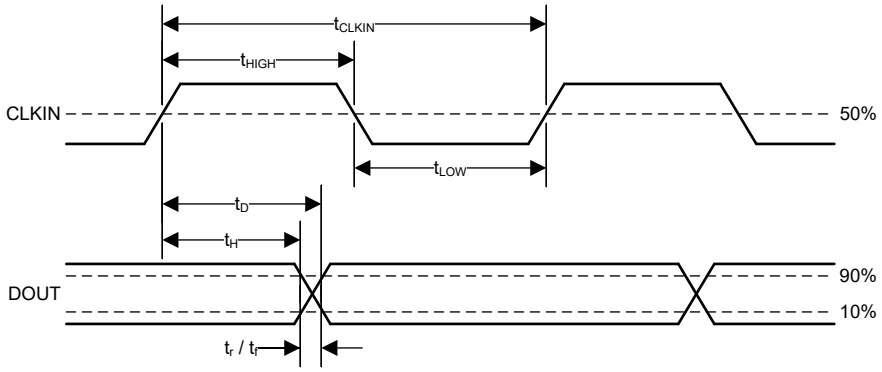


Figure 6-1. Digital Interface Timing

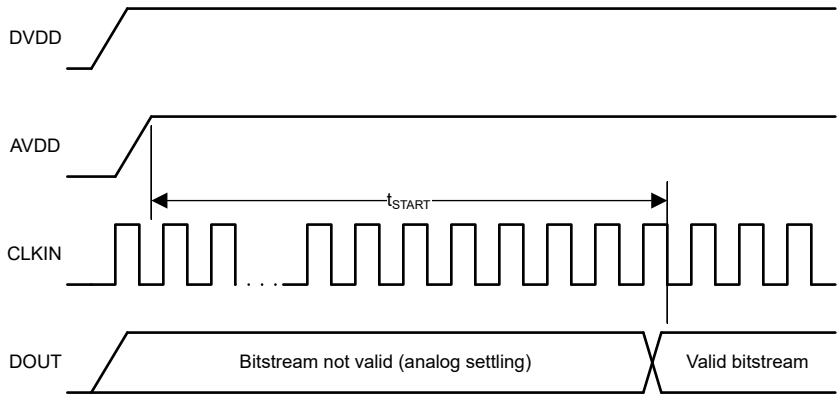


Figure 6-2. Device Start-Up Timing

6.16 Insulation Characteristics Curves

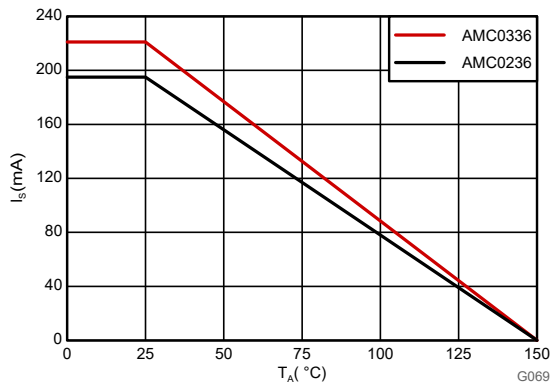


Figure 6-3. Thermal Derating Curve for Safety-Limiting Current per VDE

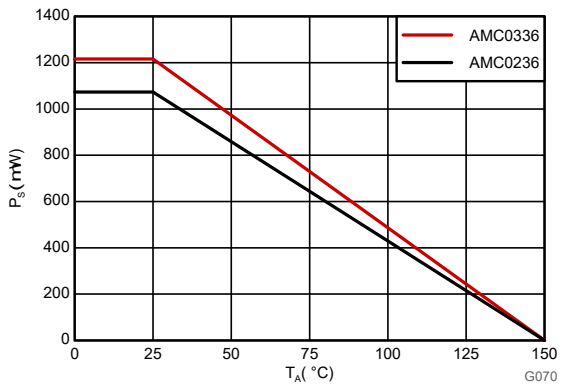
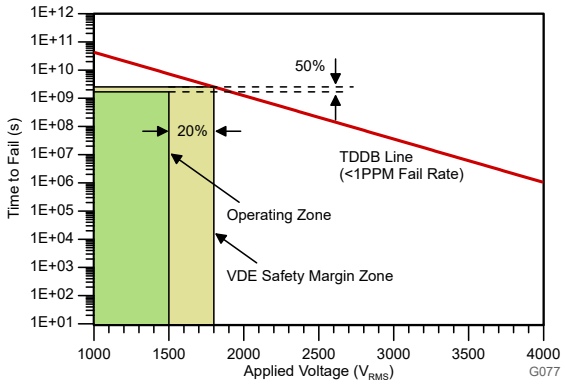


Figure 6-4. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 1500V_{RMS}, projected operating lifetime ≥50 years

Figure 6-5. Isolation Capacitor Lifetime Projection

6.17 Typical Characteristics

at AVDD = 5V, DVDD = 3.3V, V_{INP} = –1V to 1V, SNSN = AGND, f_{CLKIN} = 10MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

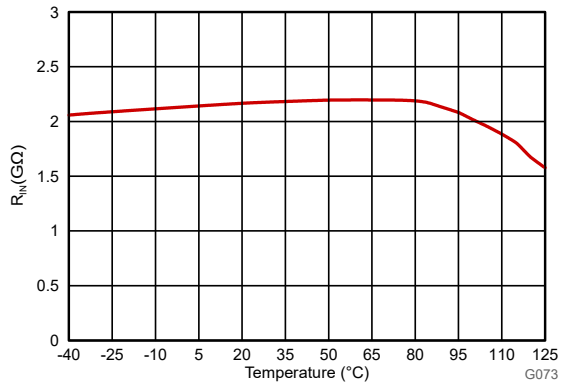


Figure 6-6. Input Resistance vs Temperature

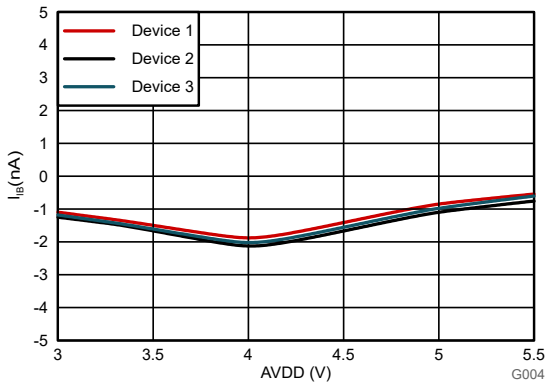


Figure 6-7. Input Bias Current vs High-Side Supply Voltage (INP Pin)

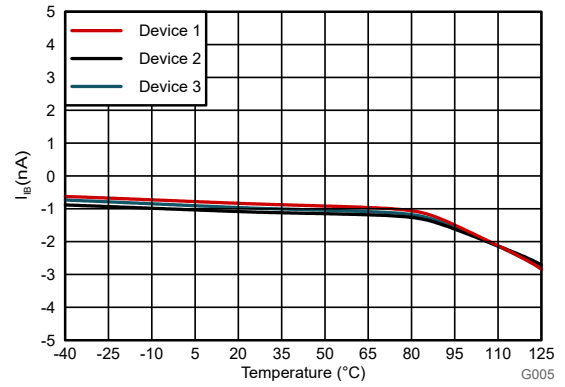


Figure 6-8. Input Bias Current vs Temperature (INP Pin)

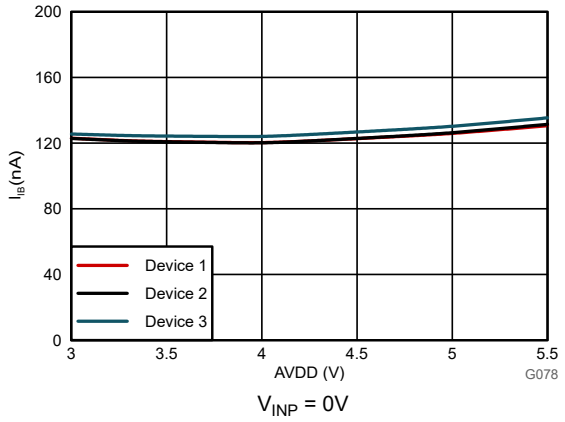


Figure 6-9. Input Bias Current vs High-Side Supply Voltage (SNSN Pin)

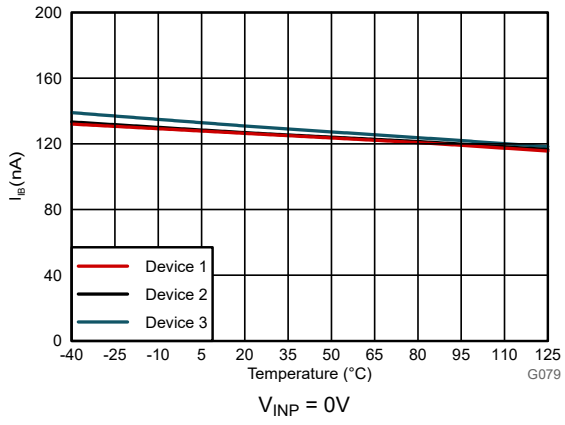


Figure 6-10. Input Bias Current vs Temperature (SNSN Pin)

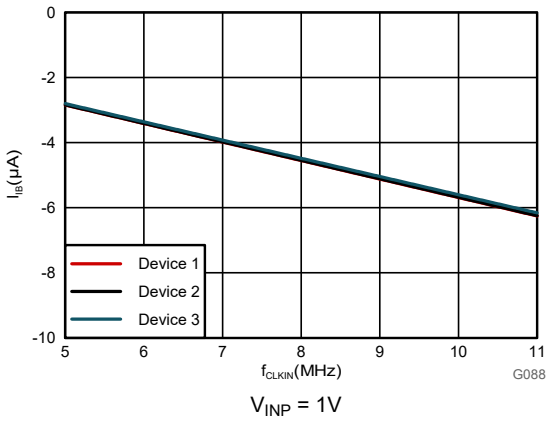


Figure 6-11. Input Bias Current vs Clock Frequency (SNSN Pin)

6.17 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V, V_{INP} = –1V to 1V, SNSN = AGND, f_{CLKIN} = 10MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

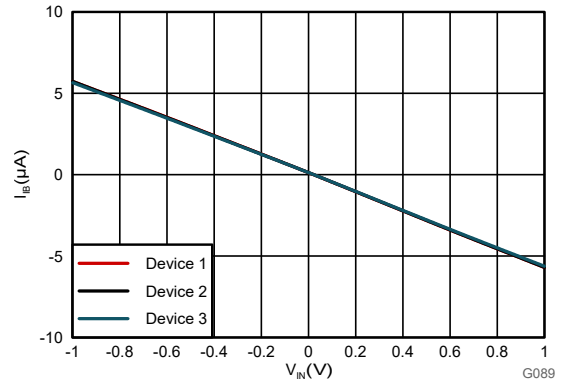
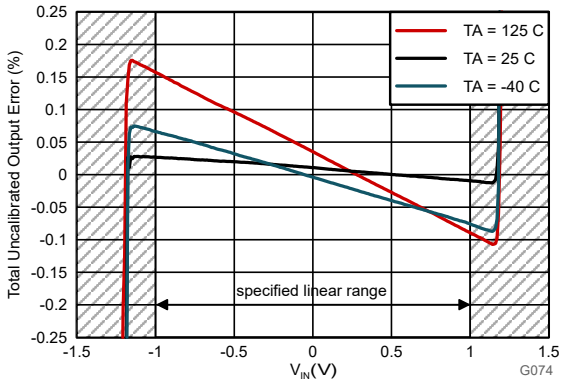


Figure 6-12. Input Bias Current vs Input Voltage (SNSN Pin)



Total uncalibrated output error (in %) is defined as:
(Output Code / 2^{16}) – (V_{IN} + 1.25V) / 2.5V) × 100,
where V_{IN} = (V_{INP} – V_{SNSN})

Figure 6-13. Total Uncalibrated Output Error vs Input Voltage

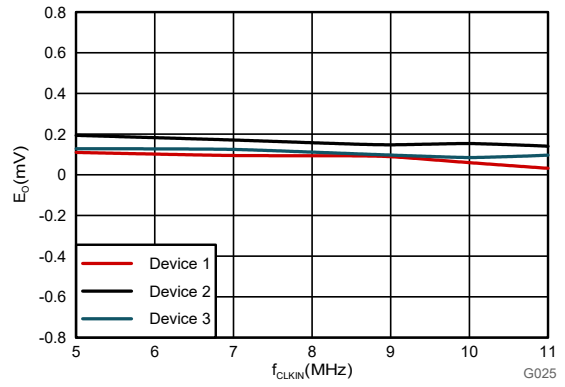


Figure 6-14. Offset Error vs Clock Frequency

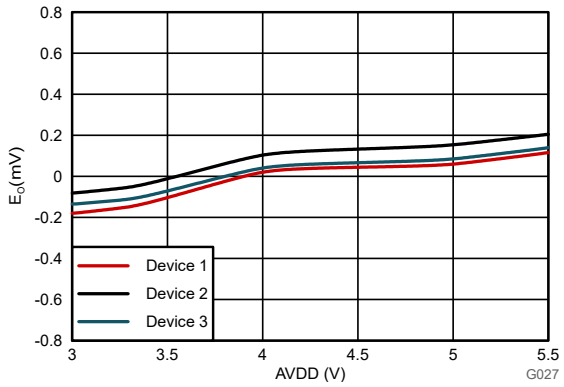


Figure 6-15. Offset Error vs High-Side Supply Voltage

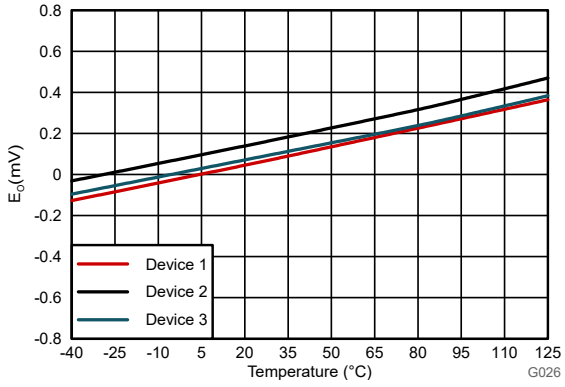


Figure 6-16. Offset Error vs Temperature

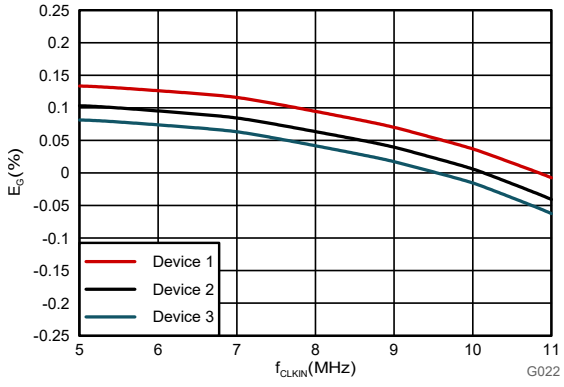


Figure 6-17. Gain Error vs Clock Frequency

6.17 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V, V_{INP} = –1V to 1V, SNSN = AGND, f_{CLKIN} = 10MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

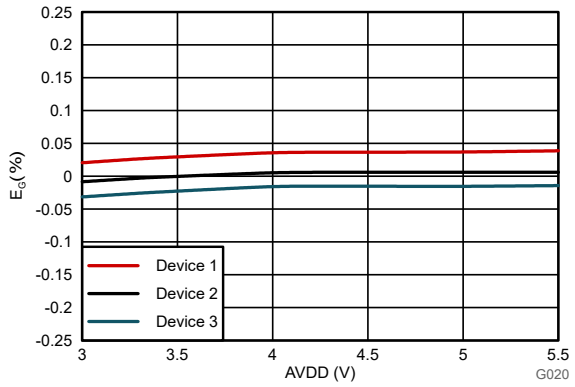


Figure 6-18. Gain Error vs High-Side Supply Voltage

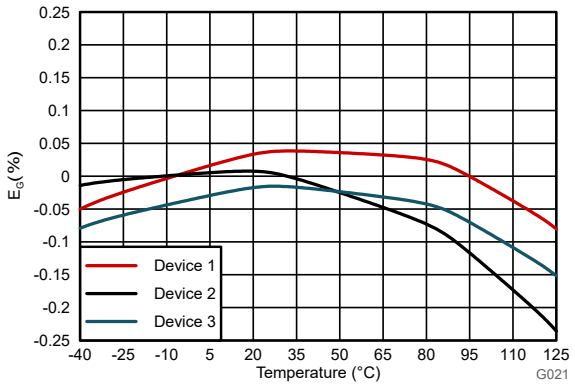


Figure 6-19. Gain Error vs Temperature

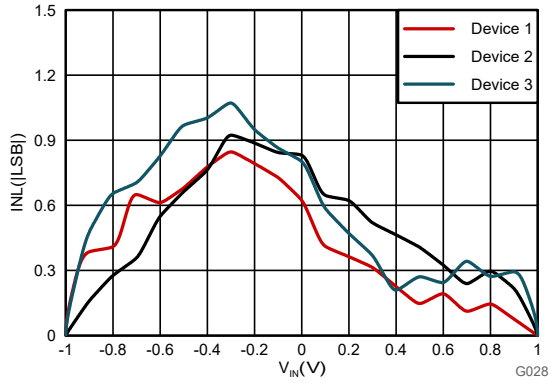


Figure 6-20. Integral Nonlinearity vs Input Voltage

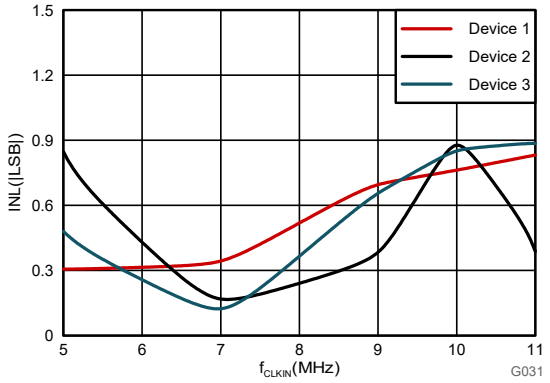


Figure 6-21. Integral Nonlinearity vs Clock Frequency

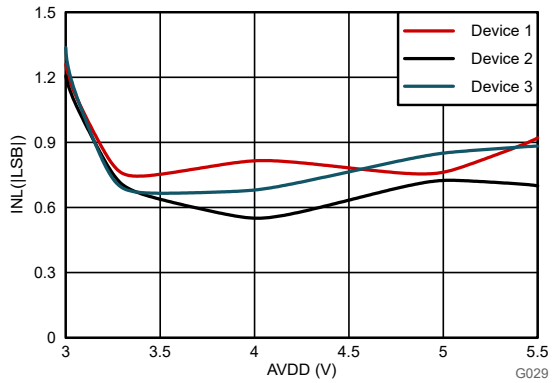


Figure 6-22. Integral Nonlinearity vs Supply Voltage

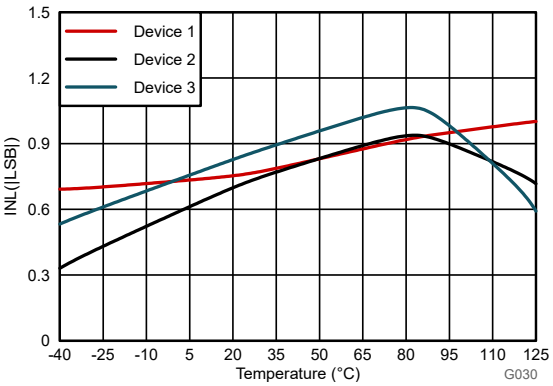


Figure 6-23. Integral Nonlinearity vs Temperature

6.17 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V, V_{INP} = –1V to 1V, SNSN = AGND, f_{CLKIN} = 10MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

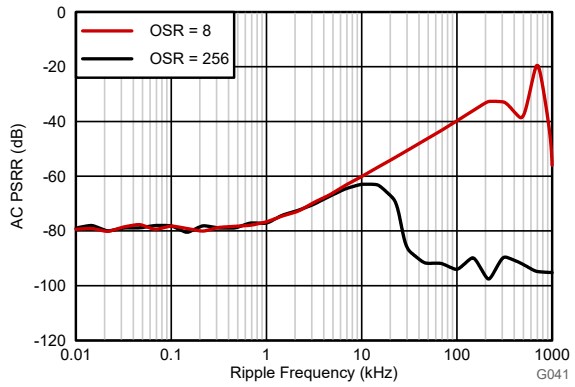


Figure 6-24. Power-Supply Rejection Ratio vs Ripple Frequency

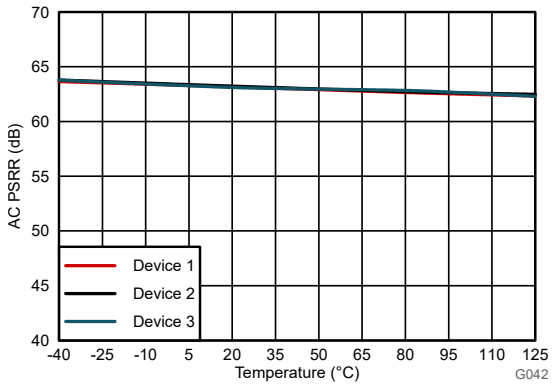


Figure 6-25. AC Power-Supply Rejection Ratio vs Temperature

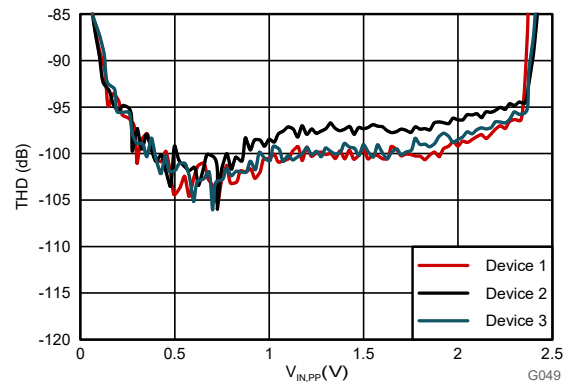


Figure 6-26. Total Harmonic Distortion vs Input Signal Amplitude

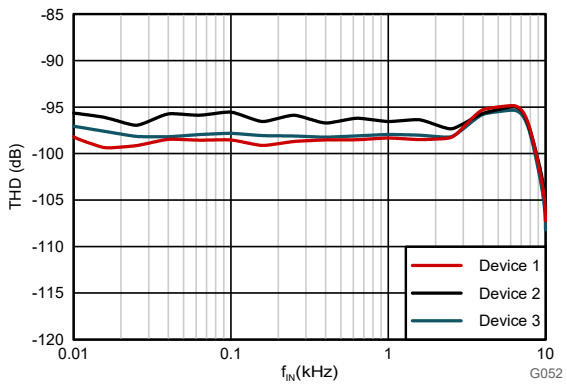


Figure 6-27. Total Harmonic Distortion vs Input Signal Frequency

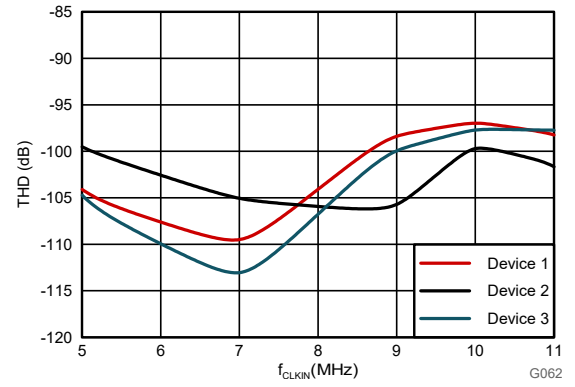


Figure 6-28. Total Harmonic Distortion vs Clock Frequency

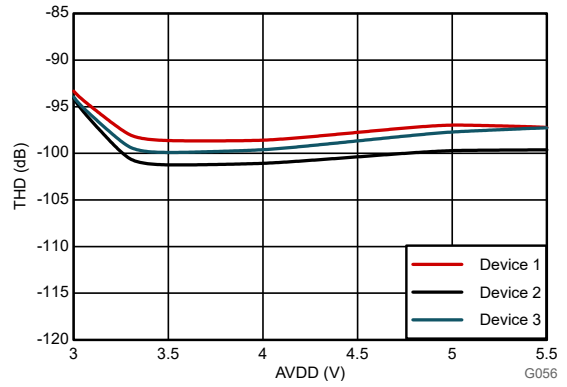


Figure 6-29. Total Harmonic Distortion vs High-Side Supply Voltage

6.17 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V, V_{INP} = –1V to 1V, SNSN = AGND, f_{CLKIN} = 10MHz, and $sinc^3$ filter with OSR = 256 (unless otherwise noted)

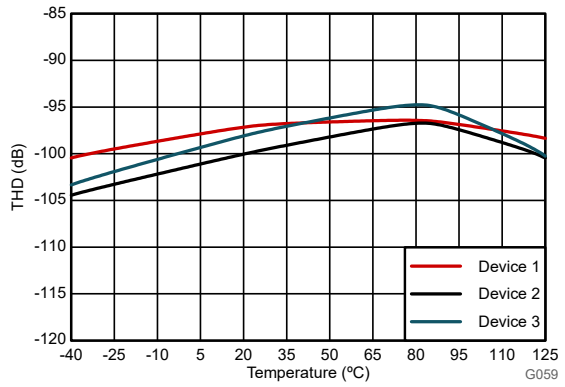


Figure 6-30. Total Harmonic Distortion vs Temperature

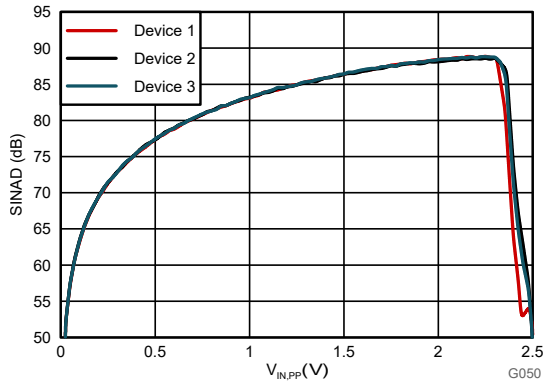


Figure 6-31. Signal-to-Noise + Distortion vs Input Signal Amplitude

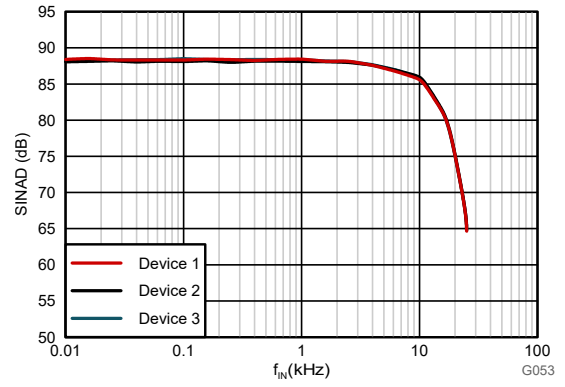


Figure 6-32. Signal-to-Noise + Distortion vs Input Signal Frequency

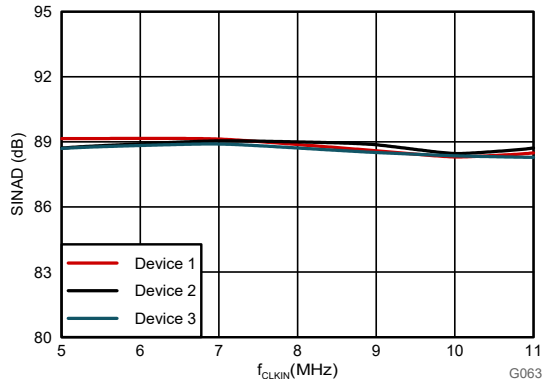


Figure 6-33. Signal-to-Noise + Distortion vs Clock Frequency

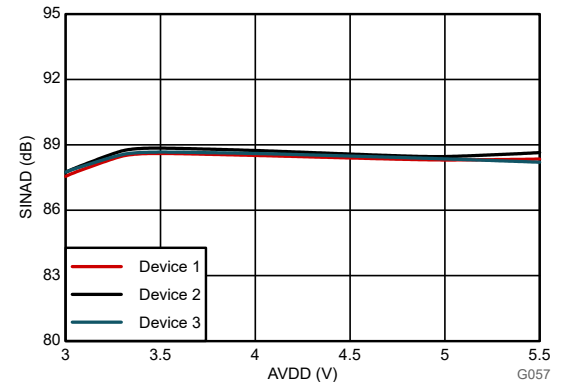


Figure 6-34. Signal-to-Noise + Distortion vs High-Side Supply Voltage

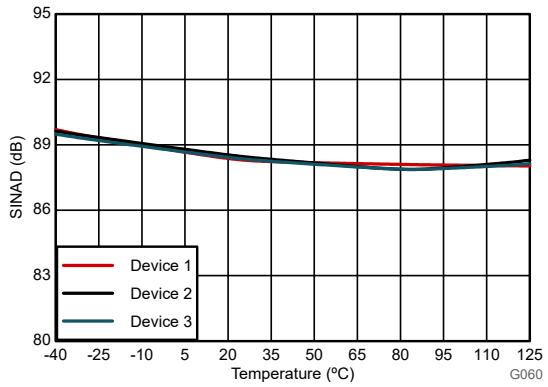


Figure 6-35. Signal-to-Noise + Distortion vs Temperature

6.17 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V, V_{INP} = –1V to 1V, SNSN = AGND, f_{CLKIN} = 10MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

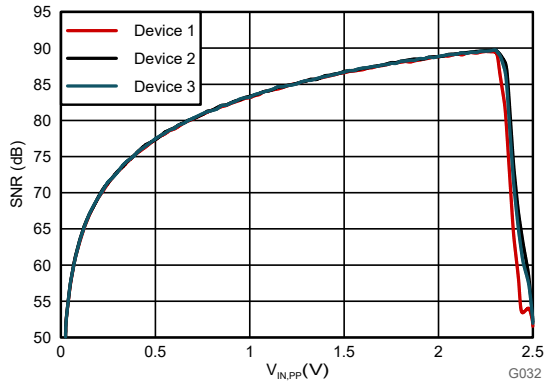


Figure 6-36. Signal-to-Noise Ratio vs Input Signal Amplitude

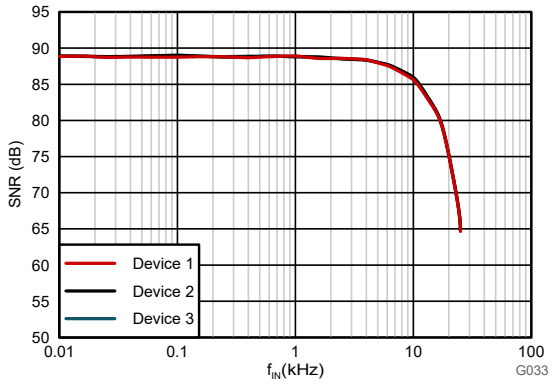


Figure 6-37. Signal-to-Noise Ratio vs Input Signal Frequency

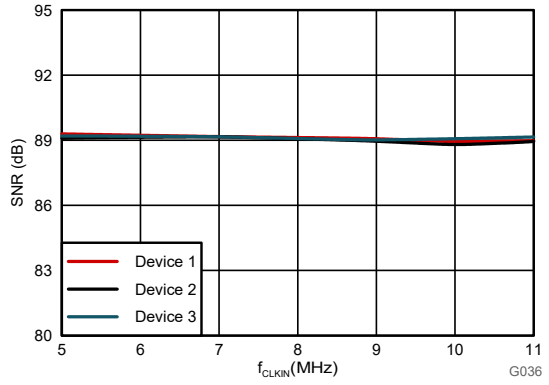


Figure 6-38. Signal-to-Noise Ratio vs Clock Frequency

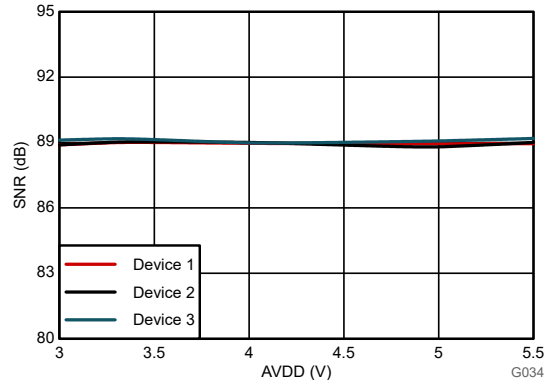


Figure 6-39. Signal-to-Noise Ratio vs High-Side Supply Voltage

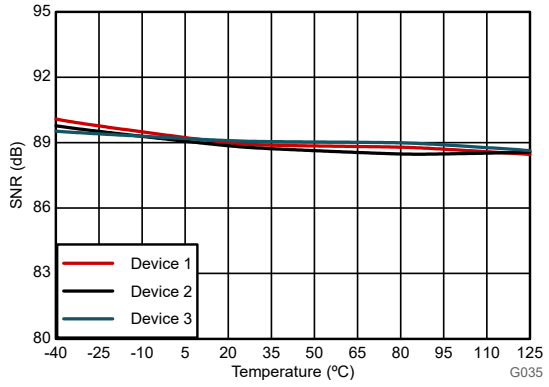
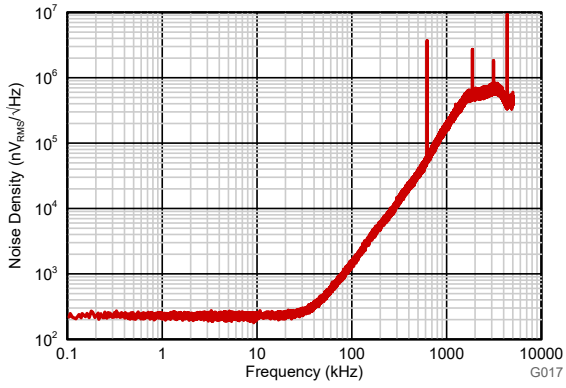


Figure 6-40. Signal-to-Noise Ratio vs Temperature

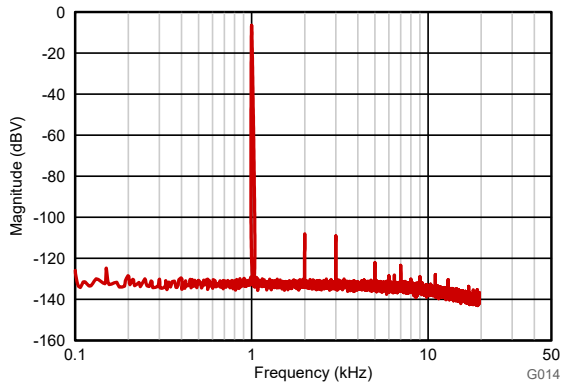


sinc^3, OSR = 1, frequency bin-width equals 1Hz

Figure 6-41. Noise Density With Both Inputs Shorted to AGND

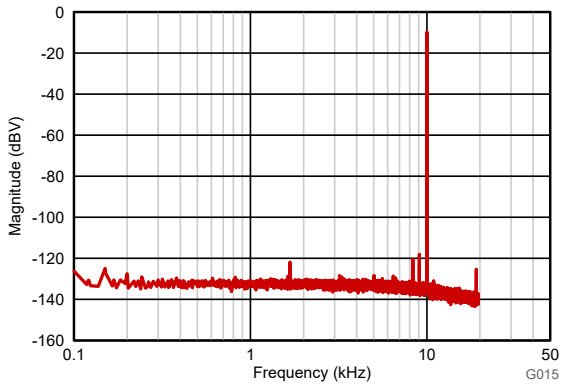
6.17 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V, V_{INP} = –1V to 1V, SNSN = AGND, f_{CLKIN} = 10MHz, and $sinc^3$ filter with OSR = 256 (unless otherwise noted)



$sinc^3$, OSR = 256, V_{INP} = $2V_{PP}$

Figure 6-42. Frequency Spectrum With 1kHz Input Signal



$sinc^3$, OSR = 256, V_{INP} = $2V_{PP}$

Figure 6-43. Frequency Spectrum With 10kHz Input Signal

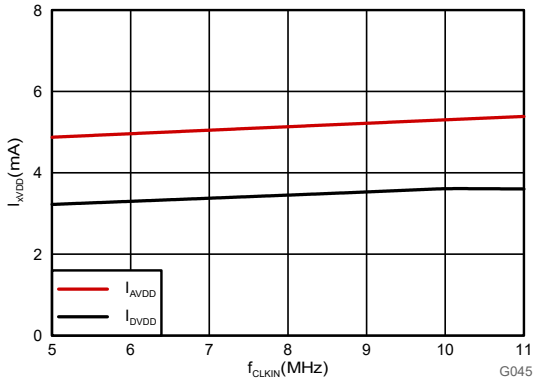


Figure 6-44. Supply Current vs Clock Frequency

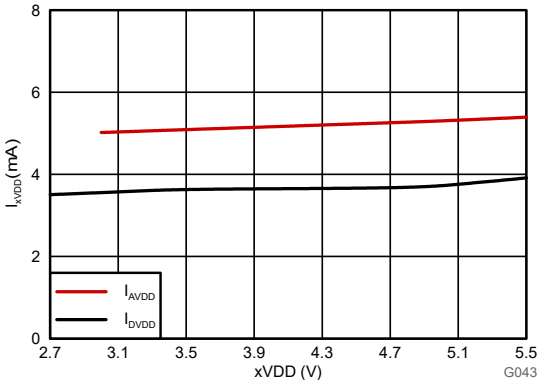


Figure 6-45. Supply Current vs Supply Voltage

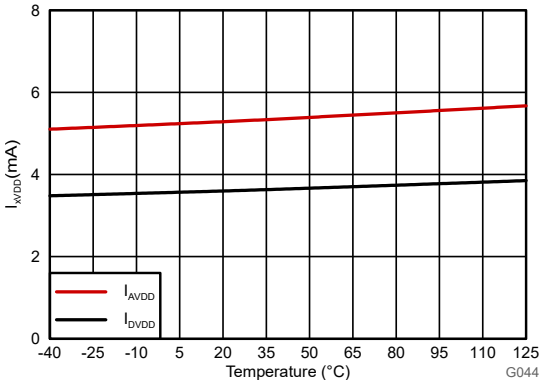


Figure 6-46. Supply Current vs Temperature

7 Detailed Description

7.1 Overview

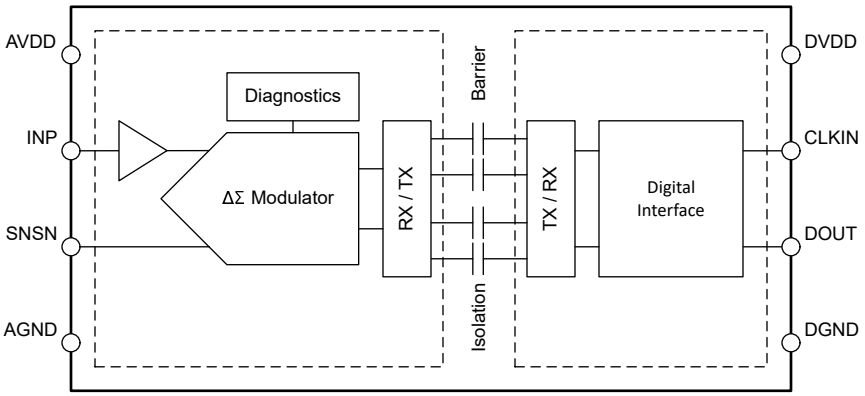
The AMC0x36-Q1 is a single-channel, second-order, CMOS, delta-sigma (ΔΣ) modulator with a high impedance input, designed for high resolution voltage measurements. The isolated output of the converter (DOUT) provides a stream of digital ones and zeros synchronous to the external clock applied to the CLKIN pin. The time average of this serial output is proportional to the analog input voltage.

The modulator shifts the quantization noise to high frequencies; therefore, use a digital low-pass digital filter, such as a Sinc filter at the device output to increase overall performance. This filter also converts the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). Use a microcontroller (µC) or field-programmable gate array (FPGA) to implement the filter.

The overall performance (speed and resolution) depends on the selection of an appropriate oversampling ratio (OSR) and filter type. A higher OSR results in higher resolution while operating at a lower refresh rate. A lower OSR results in lower resolution, but provides data at a higher refresh rate. This system allows flexibility with the digital filter design and is capable of analog-to-digital conversion results with a dynamic range exceeding 89dB with OSR = 256.

The silicon-dioxide (SiO_2) based capacitive isolation barrier supports a high level of magnetic field immunity; see the *ISO72x Digital Isolator Magnetic-Field Immunity* application note. The AMC0x36-Q1 uses an on-off keying (OOK) modulation scheme to transmit data across the isolation barrier. This modulation and the isolation barrier characteristics, result in high reliability in noisy environments and high common-mode transient immunity.

7.2 Functional Block Diagram

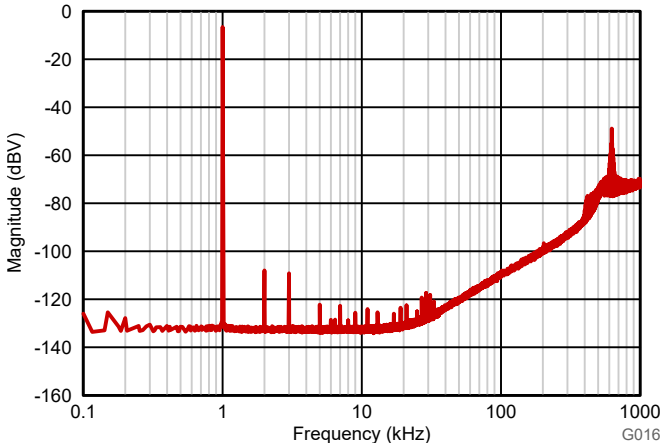


7.3 Feature Description

7.3.1 Analog Input

The high-impedance input buffer on the INP pin feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

For reduced offset and offset drift, the input buffer is chopper-stabilized with the chopping frequency set at $f_{CLKIN}/16$. Figure 7-1 shows the spur at 625kHz that is generated by the chopping frequency for a modulator clock of 10MHz.



sinc^3 filter, OSR = 1, f_{CLKIN} = 10MHz, f_{IN} = 1kHz

Figure 7-1. Quantization Noise Shaping

There are two restrictions on the analog input signal. First, if the input voltage exceeds the value specified in the *Absolute Maximum Ratings* table, limit the input current to 10mA. This limitation is caused by the device input electrostatic discharge (ESD) diodes turning on. Second, linearity and noise performance are specified only when the input voltage is within the linear full-scale range (V_{FSR}). V_{FSR} is specified in the *Recommended Operating Conditions* table.

7.3.2 Modulator

Figure 7-2 conceptualizes the second-order, switched-capacitor, feed-forward ΔΣ modulator implemented in the AMC0x36-Q1. The output V_5 of the 1-bit, digital-to-analog converter (DAC) is subtracted from the input voltage V_{IN} = (V_{INP} – V_{SNSN}). This subtraction provides an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage. The result of the second integration is an output voltage V_3 that is summed with V_{IN} and the V_2 output. V_{IN} is the input signal and V_2 is the first integrator. Depending on the value of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage V_5. Thus, causing the integrators to progress in the opposite direction and forcing the integrator output value to track the average value of the input.

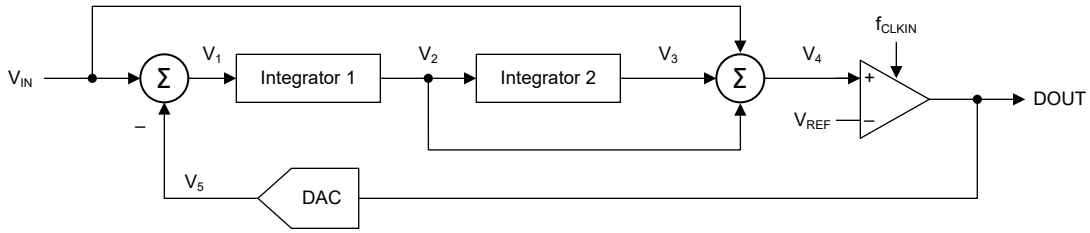


Figure 7-2. Block Diagram of the Second-Order Modulator

7.3.3 Isolation Channel Signal Transmission

As shown in Figure 7-3, the AMC0x36-Q1 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) is illustrated in the *Functional Block Diagram* . TX transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one*. However, TX does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC0x36-Q1 is 480MHz.

The AMC0x36-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and the lowest level of radiated emissions. The high-frequency carrier and RX/TX buffer switching cause these emissions.

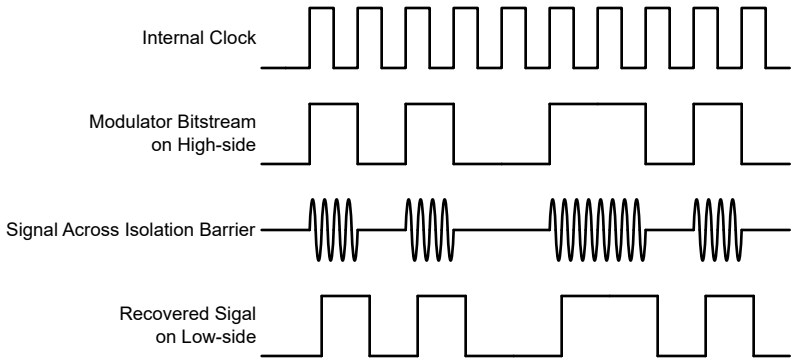


Figure 7-3. OOK-Based Modulation Scheme

7.3.4 Digital Output

An input signal of 0V ideally produces a stream of ones and zeros that are high 50% of the time. An input of 1V produces a stream of ones and zeros that are high 90.0% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 58982. An input of –1V produces a stream of ones and zeros that are high 10.0% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 6554. These input voltages are also the specified linear range of the AMC0x36-Q1. If the input voltage value exceeds this range, the output of the modulator shows increasing nonlinear behavior as the quantization noise increases. The modulator output clips with a constant stream of zeros at an input ≤–1.25V. The modulator output also clips with a constant stream of ones at an input ≥1.25V. In this case, however, the AMC0x36-Q1 generates a single 1 or 0 every 128 clock cycles to indicate proper device function. A single 1 is generated if the input is at negative full-scale and a 0 is generated if the input is at positive full scale. See the *Output Behavior in Case of a Full-Scale Input* section for more details. Figure 7-4 shows the input voltage versus the output modulator signal.

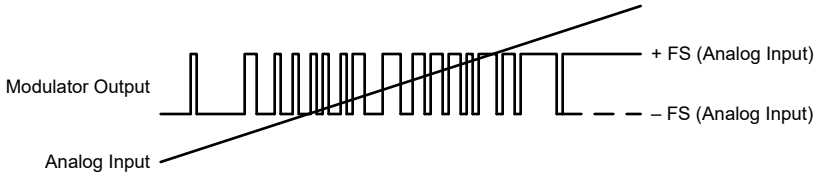


Figure 7-4. Modulator Output vs Analog Input

The following equation calculates the density of ones in the output bitstream for any input voltage V_{IN} = (V_{INP} – V_{SNSN}) value. The only exception is a full-scale input signal. See the *Output Behavior in Case of a Full-Scale Input* section.

$$\rho = (|V_{Clipping}| + V_{IN}) / (2 \times V_{Clipping}) \quad (1)$$

7.3.4.1 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC0x36-Q1, the device generates a single one or zero every 128 bits at DOUT. Figure 7-5 shows a timing diagram of this process. A single 1 or 0 is generated depending on the actual polarity of the signal being sensed. A full-scale signal is defined as $|V_{INP} – V_{SNSN}| \geq |V_{Clipping}|$. In this way, differentiating between a missing AVDD and a full-scale input signal is possible on the system level. See the *Diagnosing Delta-Sigma Modulator Bitstream Using C2000™ Configurable Logic Block (CLB)* application note for code examples of diagnosing the digital bitstream.

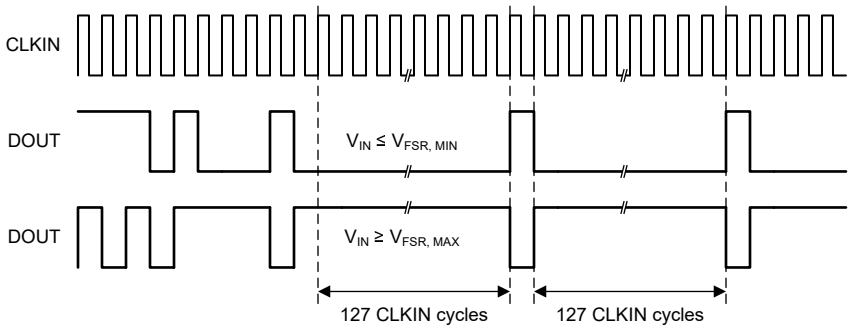


Figure 7-5. Full-Scale Output of the AMC0x36-Q1

7.3.4.2 Output Behavior in Case of a Missing High-Side Supply

If the high-side supply (AVDD) is missing, the device provides a constant bitstream of logic 0's at the output, and DOUT is permanently low. Figure 7-6 shows a timing diagram of this process. A one is not generated every 128 clock pulses, which differentiates this condition from a valid negative fullscale input. This feature helps identify high-side power-supply problems on the board. See the *Diagnosing Delta-Sigma Modulator Bitstream Using C2000™ Configurable Logic Block (CLB)* application note for code examples of diagnosing the digital bitstream.

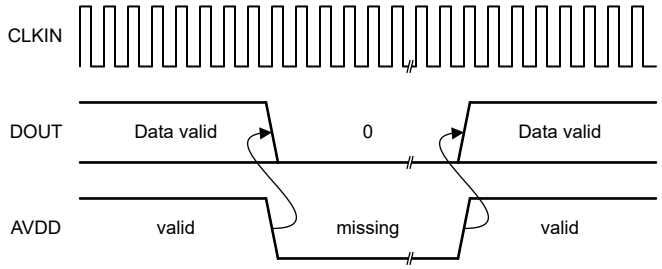


Figure 7-6. Output of the AMC0x36-Q1 in Case of a Missing High-Side Supply

7.4 Device Functional Modes

The AMC0x36-Q1 operates in one of the following states:

- OFF-state: The low-side of the device (DVDD) is below the $DVDD_{UV}$ threshold. The device is not responsive. DOUT is Hi-Z state. Internally, DOUT and CLKIN are clamped to DVDD and DGND by ESD protection diodes.
- Missing high-side supply: The low-side of the device (DVDD) is supplied and within the limits listed in the *Recommended Operating Conditions* . The high-side supply (AVDD) is below the $AVDD_{UV}$ threshold. The device outputs a constant bitstream of logic 0's, as described in the *Output Behavior in Case of a Missing High-Side Supply* section.
- Analog input overrange (positive full-scale input): AVDD and DVDD are within the recommended operating conditions. However, the analog input voltage $V_{IN} = (V_{INP} – V_{SNSN})$ is above the maximum clipping voltage ($V_{Clipping, MAX}$). The device outputs a logic 0 every 128 clock cycles, as described in the *Output Behavior in Case of a Full-Scale Input* section.
- Analog input underrange (negative full-scale input): AVDD and DVDD are within the recommended operating conditions. However, the analog input voltage $V_{IN} = (V_{INP} – V_{SNSN})$ is below the minimum clipping voltage ($V_{Clipping, MIN}$). The device outputs a logic 1 every 128 clock cycles, as described in the *Output Behavior in Case of a Full-Scale Input* section.
- Normal operation: AVDD, DVDD, and V_{IN} are within the recommended operating conditions. The device outputs a digital bitstream, as explained in the *Digital Output* section.

Table 7-1 lists the operational modes.

Table 7-1. Device Operational Modes

OPERATINAL MODE	AVDD	DVDD	V_{IN}	DEVICE RESPONSE
OFF	Don't care	$V_{DVDD} < DVDD_{UV}$	Don't care	DOUT is Hi-Z state. Internally, DOUT and CLKIN are clamped to DVDD and DGND by ESD protection diodes.
Missing high-side supply	$V_{AVDD} < AVDD_{UV}$	Valid(1)	Don't care	The device outputs a constant bitstream of logic 0's, as described in the *Output Behavior in Case of a Missing High-Side Supply* section.
Input overrange	Valid(1)	Valid(1)	$V_{IN} > V_{Clipping, MAX}$	The device outputs a logic 0 every 128 clock cycles, as described in the *Output Behavior in Case of a Full-Scale Input* section.
Input underrange	Valid(1)	Valid(1)	$V_{IN} < V_{Clipping, MIN}$	The device outputs a logic 1 every 128 clock cycles, as described in the *Output Behavior in Case of a Full-Scale Input* section.
Normal operation	Valid(1)	Valid(1)	Valid(1)	Normal operation

(1) *Valid* denotes the value is within the recommended operating conditions.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

AC-line powered power supplies are divided into two or more voltage domains that are galvanically isolated from each other. For example, the high-voltage domain includes the AC grid, DC-Link, and the power stage for power-factor-correction (PFC). The low-voltage domain includes the system controller and human interface. The PFC controller must measure the value of the AC line voltage while remaining galvanically isolated from the AC mains for safety reasons. With the high-impedance input and galvanically isolated output, the AMC0x36-Q1 enables this measurement.

8.2 Typical Application

Figure 8-1 illustrates a simplified schematic of a circuit that senses the line voltages of a three-phase AC system. All three voltages are measured against neutral. Thus allowing the three AMC0x36-Q1 devices to share a common isolated power supply on the input side.

The AC line voltage on phase L1 is divided down to a ±1V level across the bottom resistor (RSNS) of a high-impedance resistive divider. The voltage across RSNS is sensed by the AMC0x36-Q1 (*device 1*). On the opposite side of the isolation barrier *device 1* outputs a serial bitstream that represents the L1-to-neutral voltage. In the same way, *device 2* and *device 3* sense the L2 and L3 line voltages, respectively. A common AVDD supply is generated from the low-voltage side by an isolated DC/DC converter circuit. A low-cost solution is based on the push-pull driver SN6501-Q1 and a transformer that supports the desired isolation voltage ratings.

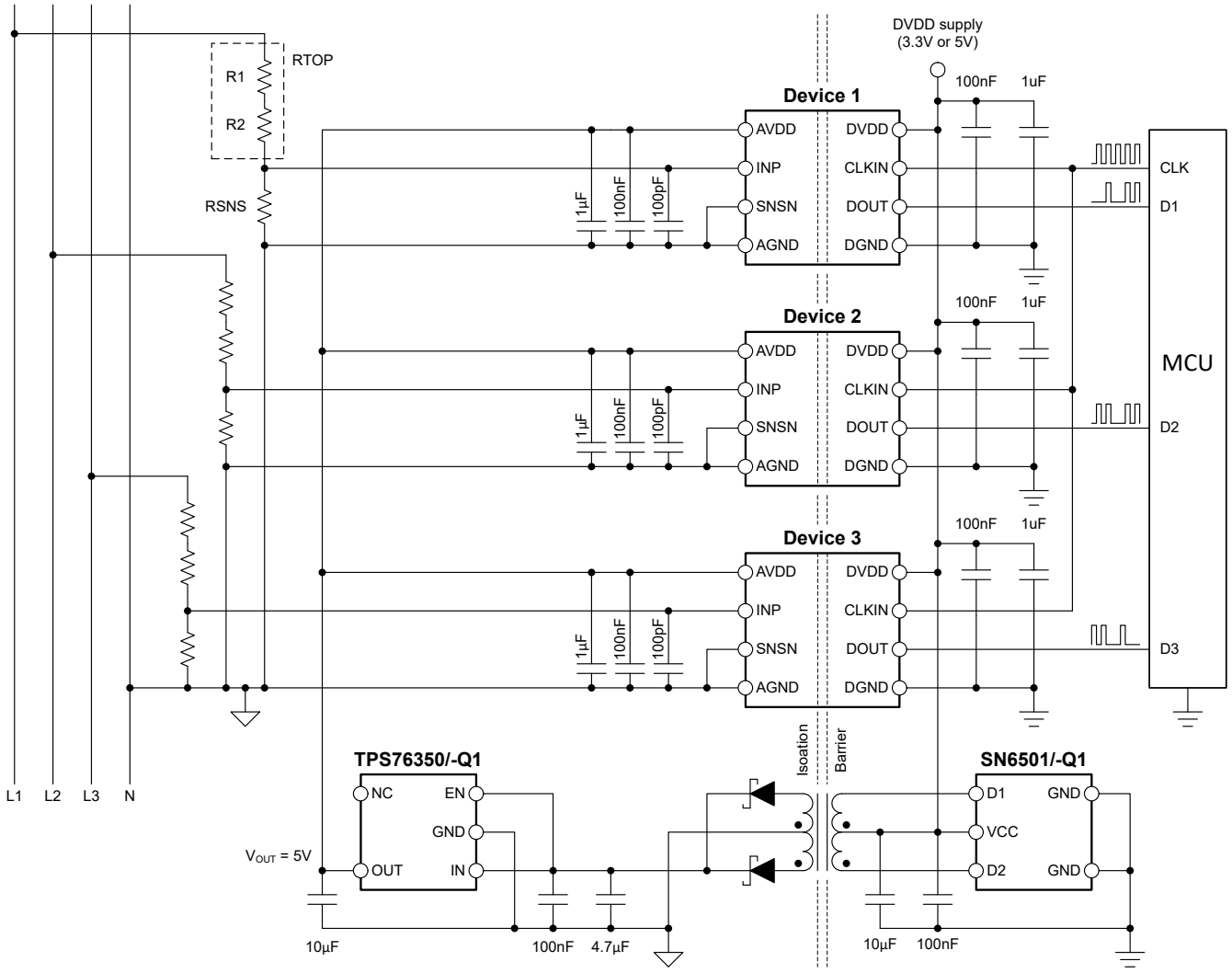


Figure 8-1. Using the AMC0x36-Q1 in a Typical Application

8.2.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

Table 8-1. Design Requirements

PARAMETER	VALUE
System input voltage (phase to neutral)	$230V_{RMS}$ ±10%, 50Hz
High-side supply voltage	5V
Low-side supply voltage	3.3V
Maximum resistor operating voltage	125V
Voltage drop across the sense resistor (RSNS) for a linear response	±1V (maximum)
Current through the resistive divider, I_{CROSS}	200µA (maximum)

8.2.2 Detailed Design Procedure

The peak input voltage is 230V × √2 × 1.1 = 360V. The 200µA maximum cross-current requirement determines that the total impedance of the resistive divider is 1.8MΩ. The impedance of the resistive divider is dominated by the top resistors (illustrated exemplary as R1 and R2 in the *Typical Application*). The maximum allowed voltage drop per unit resistor is specified as 125V. Therefore, the minimum number of unit resistors in the top portion of the resistive divider is 360V / 125V ≅ 3. The calculated unit value is 1.8MΩ / 3 = 600kΩ and the next closest value from the E96 series is 604kΩ.

Size RSNS such that the voltage drop at the maximum input voltage (360V) equals the linear full-scale input voltage (V_{FSR}) of the AMC0x36-Q1. RSNS is calculated as RSNS = V_{FSR} / (V_{Peak} – V_{FSR}) × R_{TOP}. R_{TOP} is the total value of the top resistor string (3 × 604kΩ = 1.812MΩ). The resulting value for RSNS is 5.05kΩ. The next closest value from the E96 series is 4.99kΩ.

Table 8-2 summarizes the design of the resistive divider.

Table 8-2. Resistor Value Examples

PARAMETER	VALUE
Unit resistor value, R_{TOP}	604kΩ
Number of unit resistors in R_{TOP}	3
Sense resistor value, RSNS	4.99kΩ
Total resistance value (R_{TOP} + RSNS)	1.817MΩ
Resulting current through resistive divider, I_{CROSS}	198.1µA
Resulting full-scale voltage drop across sense resistor RSNS	989mV
Peak power dissipated in R_{TOP} unit resistor	23.7mW
Total peak power dissipated in resistive divider	71.3mW

8.2.2.1 Input Filter Design

Place an RC filter in front of the device to improve signal-to-noise performance of the signal path. Input noise with a frequency close to the ΔΣ modulator sampling frequency (typically 10MHz) is folded back into the low-frequency range by the modulator. The purpose of the RC filter is to attenuate high-frequency noise below the desired noise level of the measurement. In practice, a cutoff frequency that is two orders of magnitude lower than the modulator frequency yields good results.

Most voltage-sensing applications use high-impedance resistive dividers in front of the isolated modulator to scale down the input voltage. In this case, a single capacitor, as shown in Figure 8-2, is sufficient to filter the input signal. For (R1 + R2) >> RSNS, the cutoff frequency of the input filter is 1 / (2 × π × RSNS × C5). For example, RSNS = 10kΩ and C5 = 100pF results in a cutoff frequency of 160kHz.

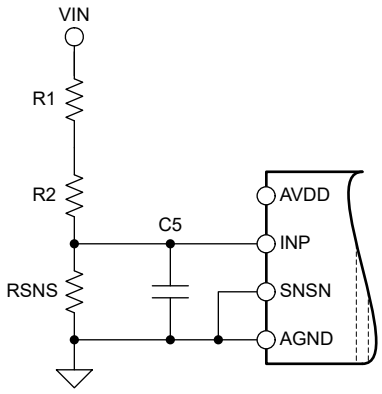


Figure 8-2. Input Filter

8.2.2.2 Bitstream Filtering

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word, that is proportional to the input voltage. Equation 2 represents a sinc^3-type filter, which is a very simple filter built with minimal effort and hardware.

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \quad (2)$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All characterization in this document is also done with a sinc^3 filter. This filter has an oversampling ratio (OSR) of 256 and an output word width of 16 bits.

The *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note provides an example code. This example code implements a sinc^3 filter in an FPGA. This application note is available for download at www.ti.com.

For modulator output bitstream filtering, a device from TI's C2000 or Sitara microcontroller families is recommended. These families support multichannel dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel. One path provides high-accuracy results for the control loop and the other provides a fast-response path for overcurrent detection.

A *delta sigma modulator filter calculator* is available for download at www.ti.com. This calculator aids in filter design and selecting the right OSR and filter order to achieve the desired output resolution and filter response time.

8.2.3 Application Curve

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. The following figure shows the ENOB of the AMC0x36-Q1 with different oversampling ratios.

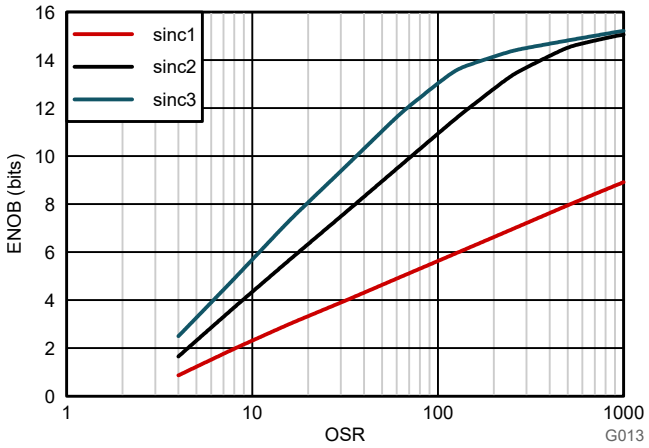


Figure 8-3. Measured Effective Number of Bits vs Oversampling Ratio

8.3 Best Design Practices

Do not leave the analog input (INP pin) of the AMC0x36-Q1 unconnected when the device is powered up. If the device input is left floating, the output of the device is not valid.

Do not connect protection diodes to the input (INP pin) of the AMC0x36-Q1. Diode leakage current potentially introduces significant measurement error especially at high temperatures. The input pin is protected against high voltages by the ESD protection circuit and the high impedance of the external resistive divider.

8.4 Power Supply Recommendations

In a typical application, the high-side power supply (AVDD) for the AMC0x36-Q1 is generated from the low-side supply (DVDD) by an isolated DC/DC converter. A low-cost option is based on the push-pull driver SN6501-Q1 and a transformer that supports the desired isolation voltage ratings.

The AMC0x36-Q1 does not require any specific power-up sequencing. The high-side power supply (AVDD) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1µF capacitor (C2). The low-side power supply (DVDD) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. Figure 8-4 shows a decoupling diagram for the AMC0x36-Q1.

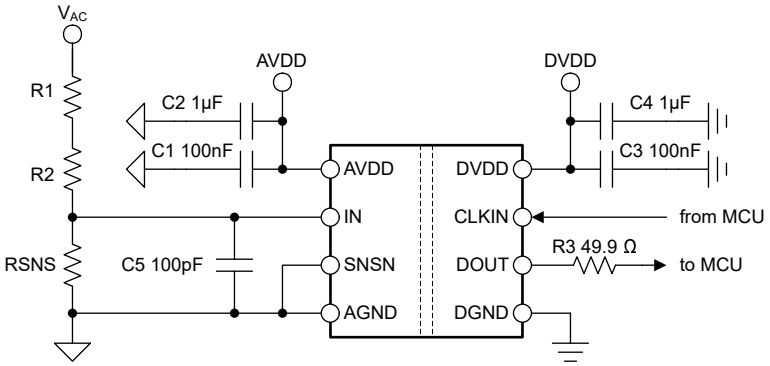


Figure 8-4. Decoupling of the AMC0x36-Q1

Make sure capacitors provide adequate *effective* capacitance under the applicable DC bias conditions experienced in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of the nominal capacitance under real-world conditions. Consider this factor when selecting these capacitors. This issue is especially acute in low-profile capacitors, where the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

8.5 Layout

8.5.1 Layout Guidelines

The *Layout Example* section provides a layout recommendation detailing the critical placement of the decoupling and filter capacitors. Place decoupling and filter capacitors as close as possible to the AMC0x36-Q1 input pins.

8.5.2 Layout Example

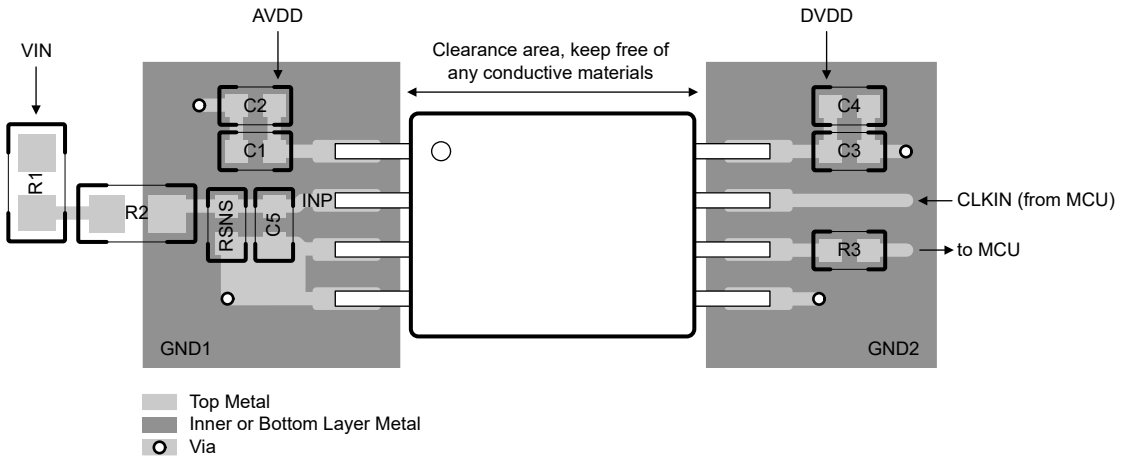


Figure 8-5. Recommended Layout of the AMC0x36-Q1

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Isolation Glossary* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application note
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application note
- Texas Instruments, *Diagnosing Delta-Sigma Modulator Bitstream Using C2000™ Configurable Logic Block (CLB)* application note
- Texas Instruments, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note
- Texas Instruments, *Delta Sigma Modulator Filter Calculator* design tool

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC0236QDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C0236Q
AMC0336QDWVRQ1	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC0336Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF AMC0236-Q1, AMC0336-Q1 :

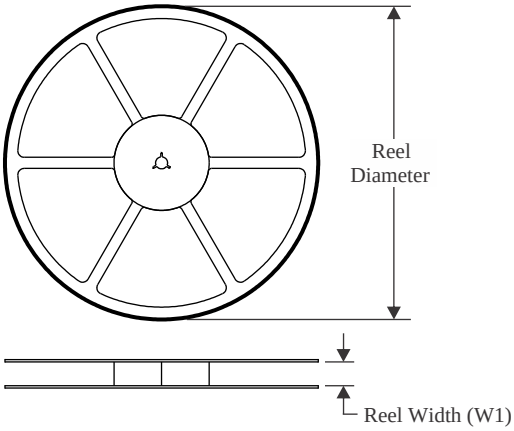
- Catalog : AMC0236, AMC0336

NOTE: Qualified Version Definitions:

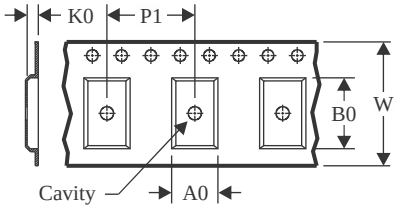
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

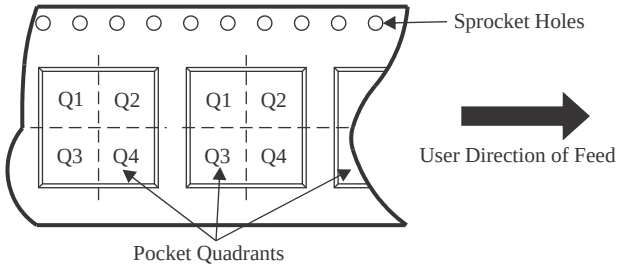


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

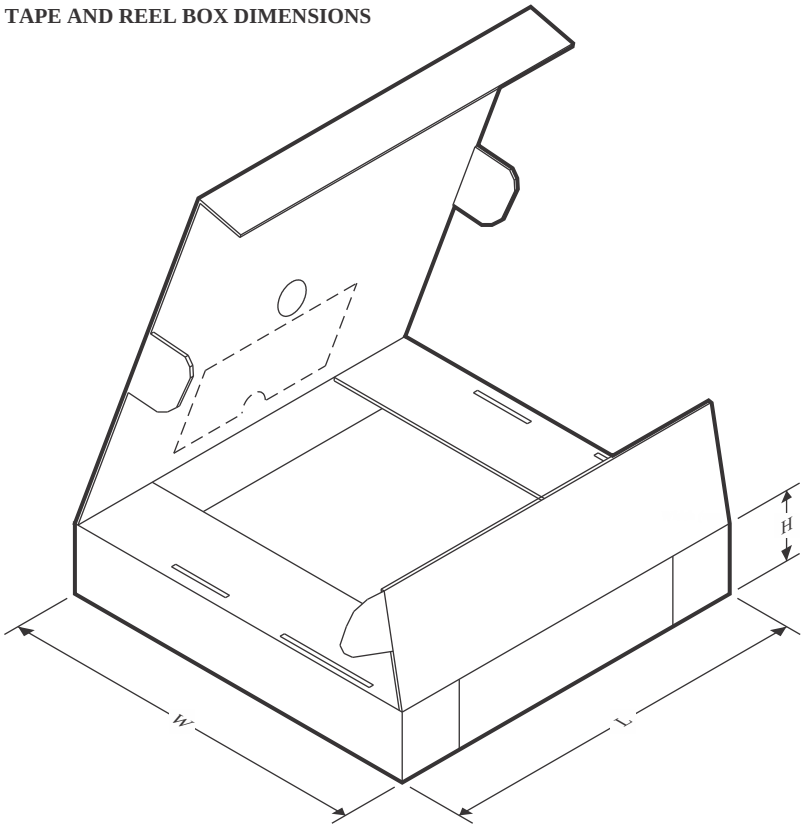
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

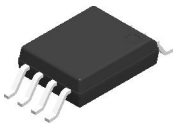
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC0236QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
AMC0336QDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

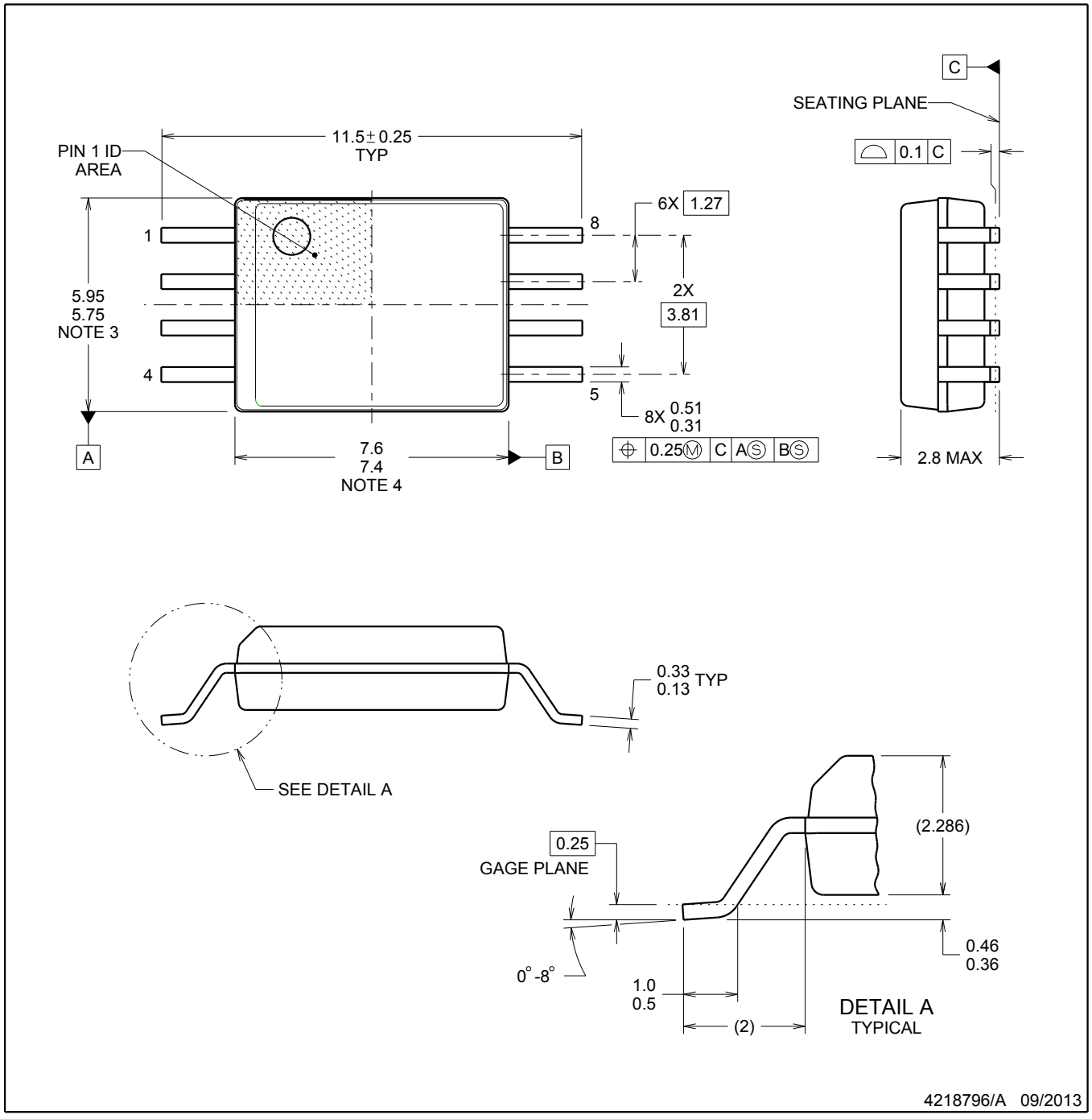
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC0236QDRQ1	SOIC	D	8	3000	353.0	353.0	32.0
AMC0336QDWVRQ1	SOIC	DWV	8	1000	353.0	353.0	32.0



DWV0008A

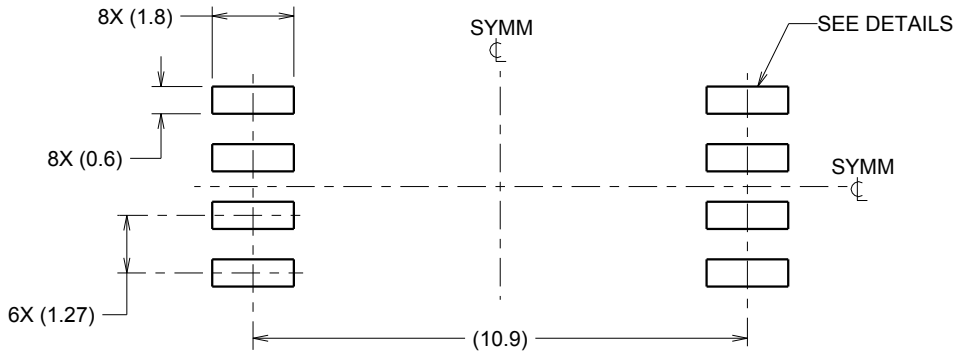
SOIC - 2.8 mm max height

SOIC

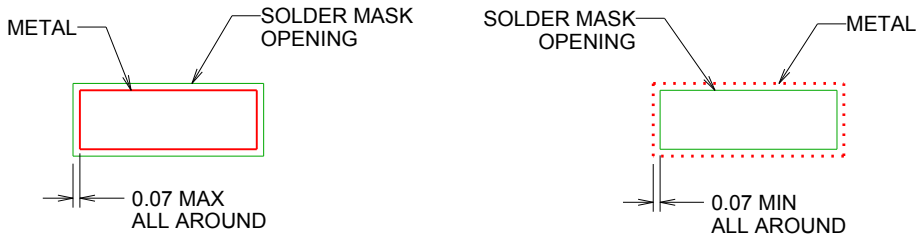


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

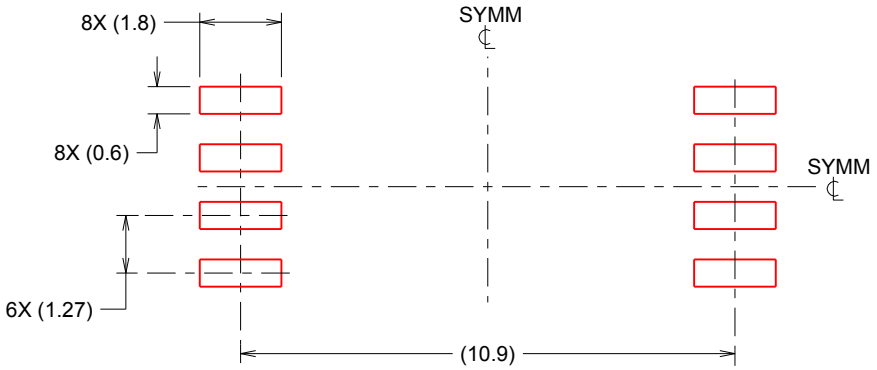
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC

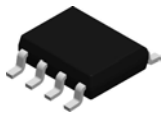


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

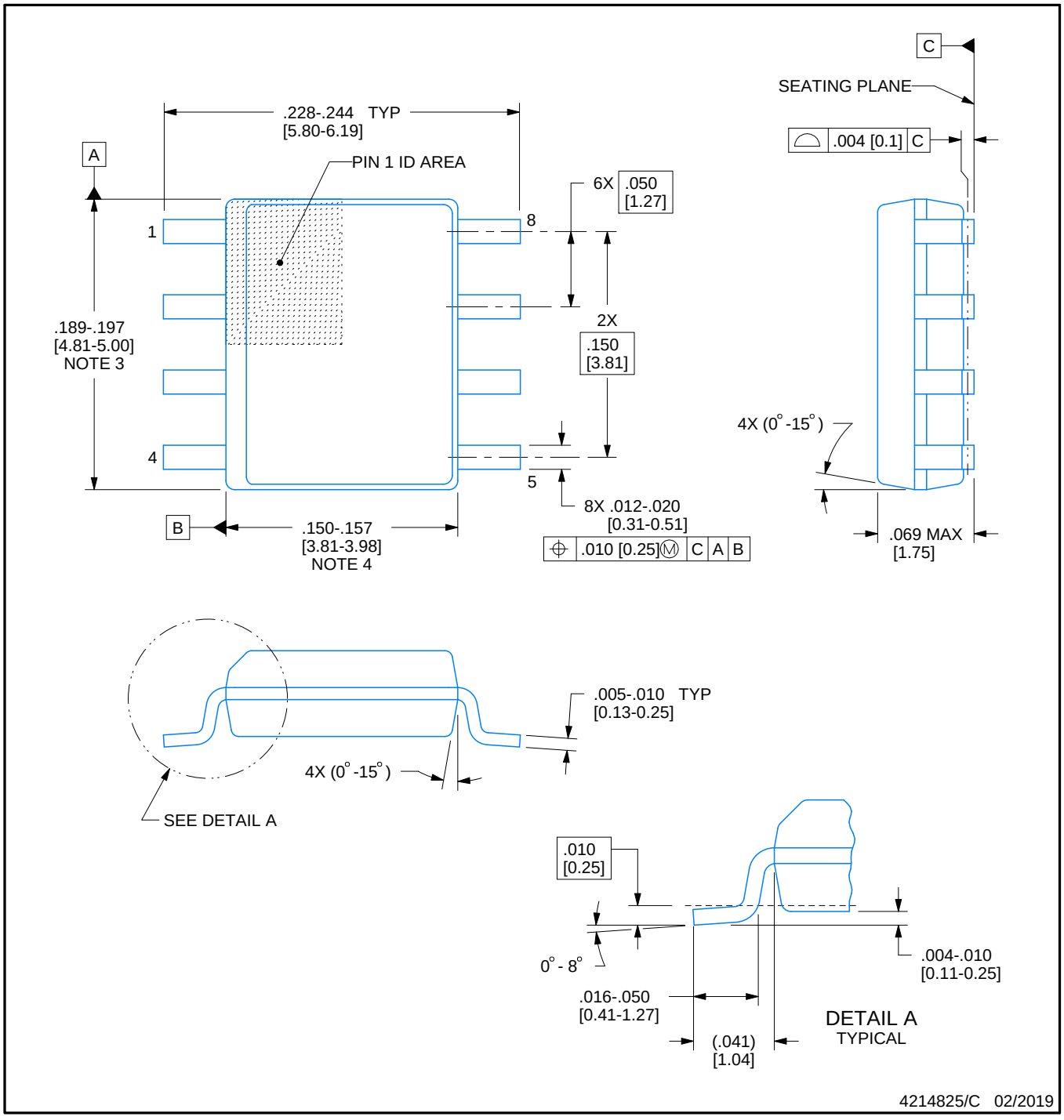


PACKAGE OUTLINE

D0008A

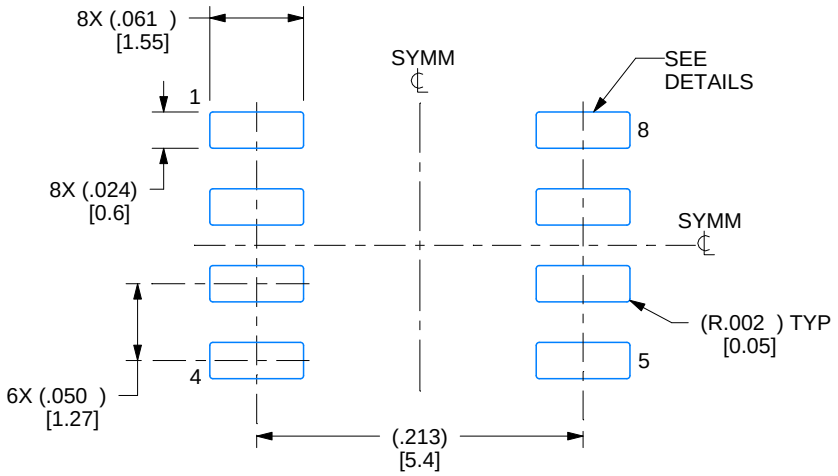
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

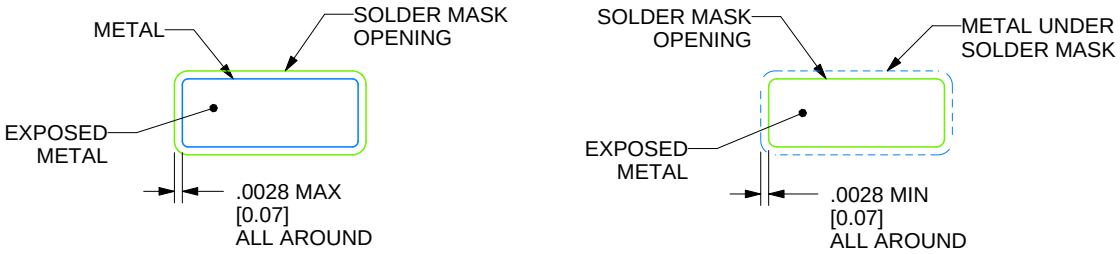


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

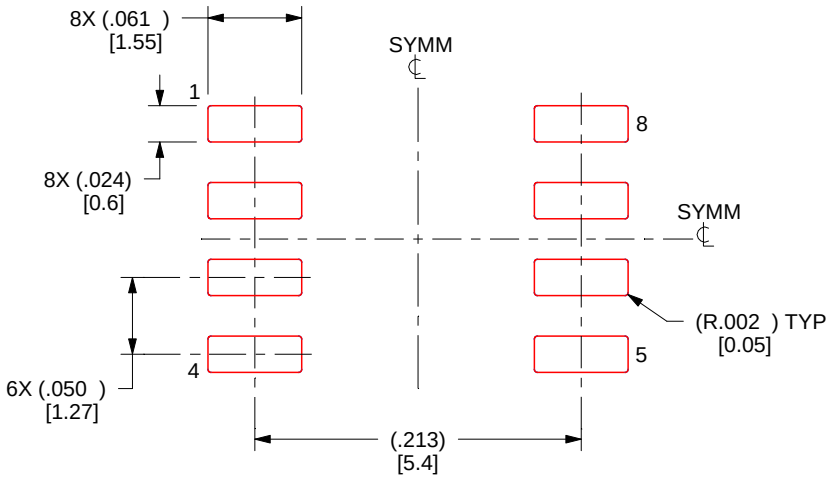
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025