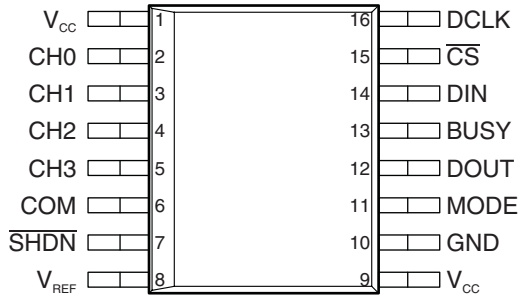
12-BIT 4-CHANNEL SERIAL-OUTPUT SAMPLING ANALOG-TO-DIGITAL CONVERTER

Check for Samples: ADS7841-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Single Supply: 2.7 V To 5 V**
- **Four-Channel Single-Ended Or Two-Channel Differential Input**
- **Up To 200-kHz Conversion Rate**
- **±2 LSB Max INL and DNL**
- **No Missing Codes**
- **71-dB Typ SINAD**
- **Serial Interface**
- **Alternate Source For MAX1247**

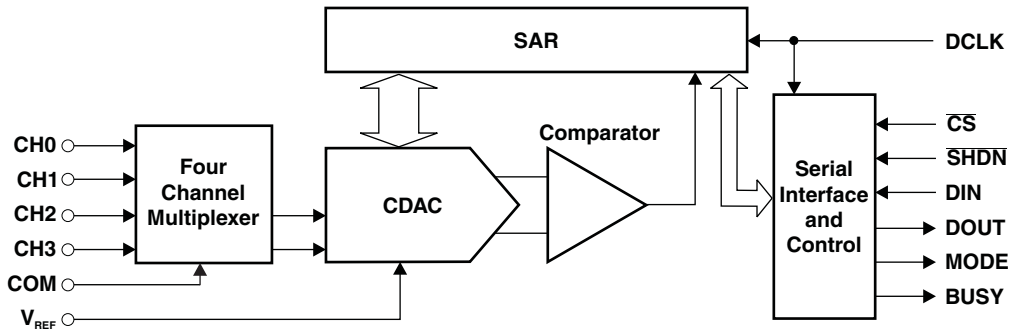
DBQ PACKAGE
(TOP VIEW)



DESCRIPTION

The ADS7841 is a 4-channel 12-bit sampling analog-to-digital converter (ADC) with a synchronous serial interface. The resolution is programmable to either 8 bits or 12 bits. Typical power dissipation is 2 mW at a 200-kHz throughput rate and a 5-V supply. The reference voltage (V_{REF}) can be varied between 100 mV and V_{CC}, providing a corresponding input voltage range of 0 V to V_{REF}. The device includes a shutdown mode that reduces power dissipation to under 15 µW. The ADS7841 is specified down to 2.7-V operation.

Low power, high speed, and on-board multiplexer make the ADS7841 ideal for battery-operated systems. The serial interface also provides low-cost isolation for remote data acquisition. The ADS7841 is available in a SSOP-16 package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	ADS7841EIDBQRQ1	S7841E
–40°C to 125°C	ADS7841ESQDBQRQ1	S7841S

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
V_{CC}	1		Power supply
CH0	2	I	Analog input channel 0
CH1	3	I	Analog input channel 1
CH2	4	I	Analog input channel 2
CH3	5	I	Analog input channel 3
COM	6	I	Ground reference for analog inputs. Sets zero code voltage in single-ended mode. Connect this pin to ground or ground reference point.
$\overline{SHDN}$	7	I	Shutdown. When low, the device enters a very low power shutdown mode.
V_{REF}	8	I	Voltage reference
V_{CC}	9		Power supply
GND	10		Ground
MODE	11	I	Conversion mode. When low, the device always performs a 12-bit conversion. When high, the resolution is set by the MODE bit in the CONTROL byte.
DOUT	12	O	Serial data output. Data is shifted on the falling edge of DCLK. This output is high-impedance when $\overline{CS}$ is high.
BUSY	13	O	Busy output. This output is high-impedance when $\overline{CS}$ is high.
DIN	14	I	Serial data input. If $\overline{CS}$ is low, data is latched on rising edge of DCLK.
$\overline{CS}$	15	I	Chip select input. Controls conversion timing and enables the serial input/output register.
DCLK	16	I	External clock input. This clock runs the SAR conversion process and synchronizes serial data I/O.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage		–0.3 V to 6 V
V_{IN}	Input voltage	Analog inputs to GND	–0.3 V to (V_{CC} + 0.3 V)
		Digital inputs to GND	–0.3 V to 6 V
P_D	Power dissipation		250 mW
T_J	Maximum virtual-junction temperature		150°C
T_A	Operating free-air temperature range	ADS7841EIDBQRQ1	–40°C to 85°C
		ADS7841ESQDBQRQ1	–40°C to 125°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE RATINGS

			RATING
ESD	Electrostatic discharge rating	Human-Body Model (HBM)	2000 V
		Machine Model (MM)	150 V
		Charged-Device Model (CDM)	1000 V

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CC}	Supply voltage		V_{CC} = 5 V (nom)	4.75	5.25	V
			V_{CC} = 2.7 V (nom)	2.7	3.6	
V_{REF}	Reference voltage, V_{REF} terminal			0.1	V_{CC}	V
V_{IN}	Input voltage, analog inputs	Differential, full-scale		0	V_{REF}	V
		Positive input		–0.2	V_{CC} + 0.2	
		Negative input	V_{CC} = 5 V (nom)	–0.2	1.25	
			V_{CC} = 2.7 V (nom)	–0.2	0.2	
V_{IH}	High-level input voltage, digital inputs	| I_{IH} | ≤ 5 µA	V_{CC} = 5 V (nom)	3	5.5	V
			V_{CC} = 2.7 V (nom)	0.7 V_{CC}	5.5	
V_{IL}	Low-level input voltage, digital inputs	| I_{IL} | ≤ 5 µA	V_{CC} = 5 V (nom)	–0.3	0.8	V
			V_{CC} = 2.7 V (nom)	–0.3	0.8	
T_A	Operating free-air temperature	ADS7841EIDBQRQ1		–40	85	°C
		ADS7841ESQDBQRQ1		–40	125	

ELECTRICAL CHARACTERISTICS

V_{CC} = 5 V, V_{REF} = 5 V, f_{SAMPLE} = 200 kHz, f_{CLK} = 16 × f_{SAMPLE} = 3.2 MHz, over operating temperature –40°C to 125°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Input							
C_I	Input capacitance				25		pF
I_{leak}	Leakage current					200	nA
System Performance							
	Resolution				12		bits
	No missing codes	ADS7841EIDBQRQ1		12			bits
		ADS7841ESQDBQRQ1		11			
INL	Integral linearity error					±2	LSB(1)
DNL	Differential linearity error				±0.8		LSB
	Offset error					±3	LSB
	Offset error match				0.15	1	LSB
	Gain error					±4	LSB
	Gain error match				0.1	1	LSB
V_n	Noise				30		μV_{rms}
PSRR	Power-supply ripple rejection				70		dB
Sampling Dynamics							
t_{conv}	Conversion time					12	CLK cycles
t_{acq}	Acquisition time			3			CLK cycles
	Throughput rate					200	kHz
t_{settle}	Multiplexer settling time				500		ns
t_d	Aperture delay				30		ns
t_{jitter}	Aperture jitter				100		ps
Dynamic Characteristics							
THD	Total harmonic distortion(2)		V_{IN} = 5 V_{p-p} at 10 kHz		–78	–72	dB
SINAD	Signal to noise + distortion ratio		V_{IN} = 5 V_{p-p} at 10 kHz	68	71		dB
	Spurious-free dynamic range		V_{IN} = 5 V_{p-p} at 10 kHz	72	79		dB
	Channel-to-channel isolation		V_{IN} = 5 V_{p-p} at 50 kHz		120		dB
Reference Input							
R_I	Resistance		DCLK static		5		GΩ
I_I	Input current				40	100	μA
			f_{SAMPLE} = 12.5 kHz		2.5		
			DCLK static		0.001	3	
Digital Input/Output							
V_{OH}	High-level output voltage		I_{OH} = –250 μA	3.5			V
V_{OL}	Low-level output voltage		I_{OL} = 250 μA			0.4	V
Power Supply							
I_Q	Quiescent current				550	900	μA
			f_{SAMPLE} = 12.5 kHz		300		
			Power-down mode(3), $\overline{CS}$ = V_{CC}			3	

(1) LSB = least significant bit. With V_{REF} = 5 V, one LSB is 1.22 mV.
(2) First five harmonics of the test frequency
(3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7 V, V_{REF} = 2.5 V, f_{SAMPLE} = 125 kHz, f_{CLK} = 16 × f_{SAMPLE} = 2 MHz, over operating temperature –40°C to 85°C (unless otherwise noted)

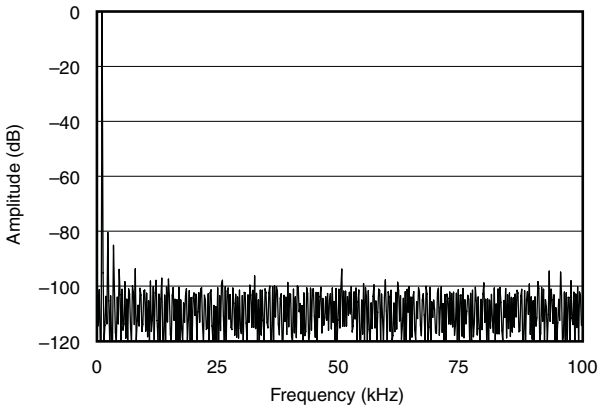
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Input						
C_I	Input capacitance			25		pF
I_{leak}	Leakage current			±1		µA
System Performance						
	Resolution			12		bits
	No missing codes		12			bits
INL	Integral linearity error				±2	LSB(1)
DNL	Differential linearity error			±0.8		LSB
	Offset error				±3	LSB
	Offset error match			0.15	1	LSB
	Gain error				±4	LSB
	Gain error match			0.1	1	LSB
V_n	Noise			30		μV_{rms}
PSRR	Power-supply ripple rejection			70		dB
Sampling Dynamics						
t_{conv}	Conversion time				12	CLK cycles
t_{acq}	Acquisition time		3			CLK cycles
	Throughput rate				125	kHz
t_{settle}	Multiplexer settling time			500		ns
t_d	Aperture delay			30		ns
t_{jitter}	Aperture jitter			100		ps
Dynamic Characteristics						
THD	Total harmonic distortion(2)	V_{IN} = 2.5 V_{p-p} at 10 kHz		–77	–72	dB
SINAD	Signal to noise + distortion ratio	V_{IN} = 2.5 V_{p-p} at 10 kHz	68	71		dB
	Spurious-free dynamic range	V_{IN} = 2.5 V_{p-p} at 10 kHz	72	78		dB
	Channel-to-channel isolation	V_{IN} = 2.5 V_{p-p} at 50 kHz		100		dB
Reference Input						
R_I	Resistance	DCLK static		5		GΩ
I_I	Input current			13	40	µA
		f_{SAMPLE} = 12.5 kHz		2.5		
		DCLK static		0.001	3	
Digital Input/Output						
V_{OH}	High-level output voltage	I_{OH} = –250 µA	0.8 V_{CC}			V
V_{OL}	Low-level output voltage	I_{OL} = 250 µA			0.4	V
Power Supply						
I_Q	Quiescent current			280	650	µA
		f_{SAMPLE} = 12.5 kHz		220		
		Power-down mode(3), $\overline{CS}$ = V_{CC}			3	

(1) LSB = least significant bit. With V_{REF} = 2.5 V, one LSB is 0.61 mV.
(2) First five harmonics of the test frequency
(3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND

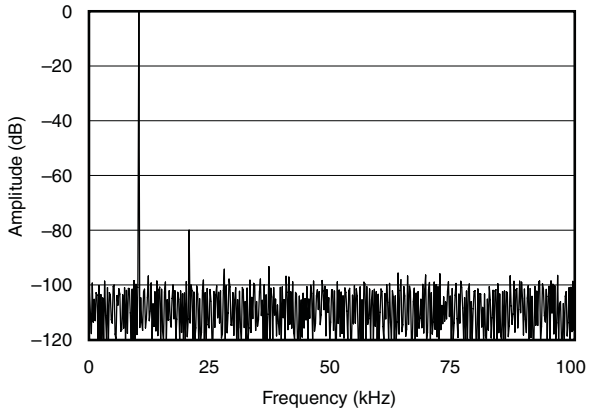
TYPICAL CHARACTERISTICS, V_{CC} = 5 V

V_{CC} = 5 V, T_A = 25°C, V_{REF} = 5 V, f_{SAMPLE} = 200 kHz, f_{CLK} = 16 × f_{SAMPLE} = 3.2 MHz (unless otherwise noted)

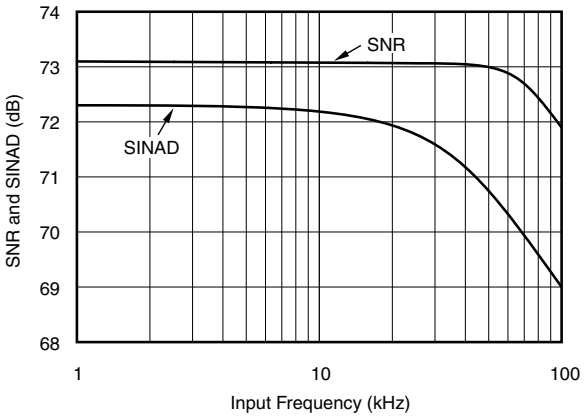
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1,123Hz, –0.2dB)



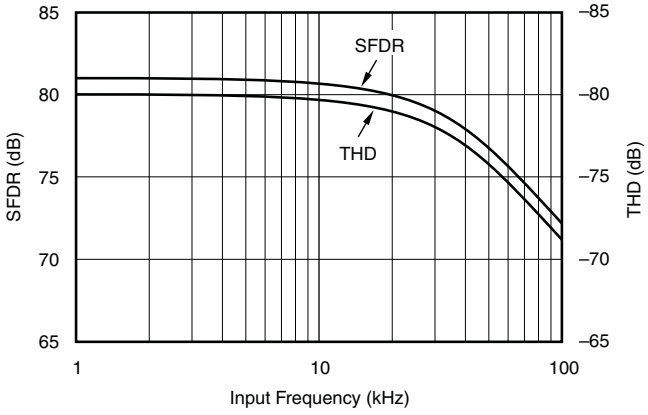
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 10.3kHz, –0.2dB)



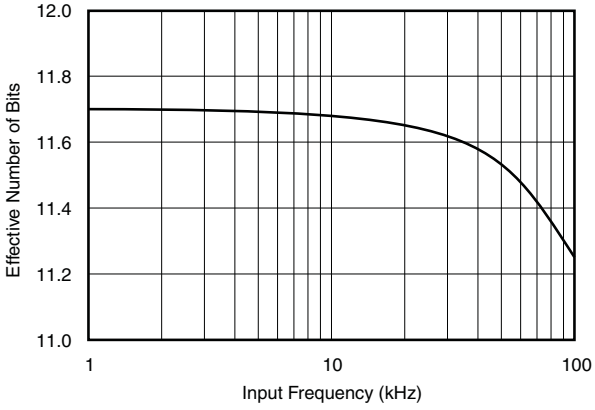
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-(NOISE+DISTORTION) vs INPUT FREQUENCY



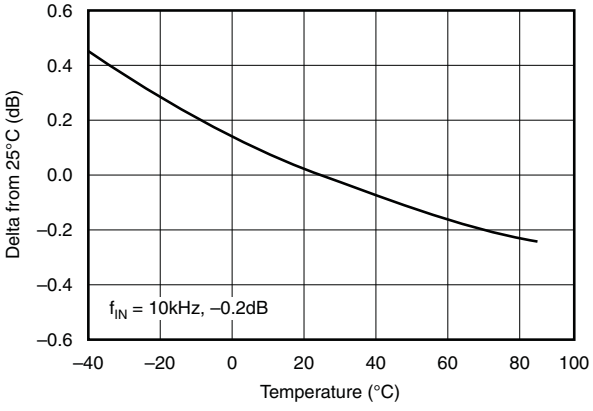
SPURIOUS-FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY



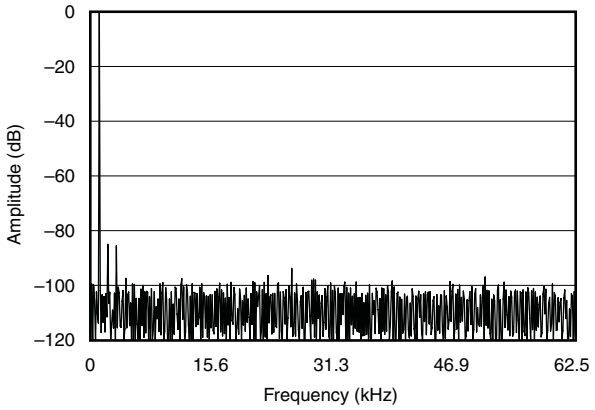
CHANGE IN SIGNAL-TO-(NOISE+DISTORTION) vs TEMPERATURE



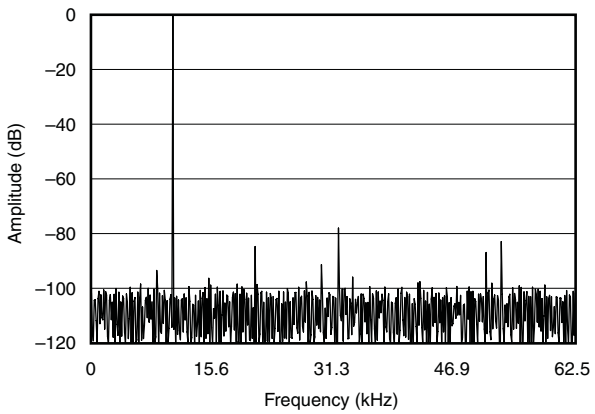
TYPICAL CHARACTERISTICS, V_{CC} = 2.7 V

V_{CC} = 2.7 V, T_A = 25°C, V_{REF} = 2.5 V, f_{SAMPLE} = 125 kHz, f_{CLK} = 16 × f_{SAMPLE} = 2 MHz (unless otherwise noted)

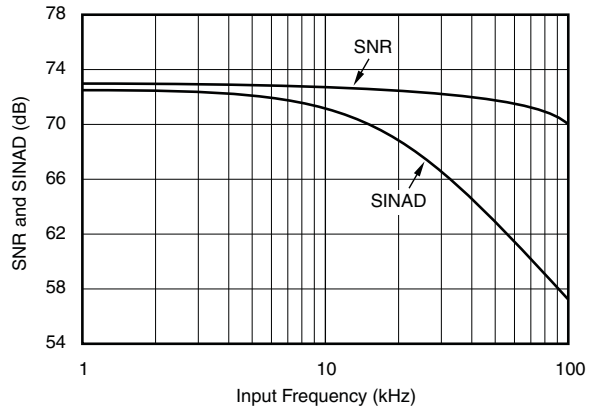
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1,129Hz, –0.2dB)



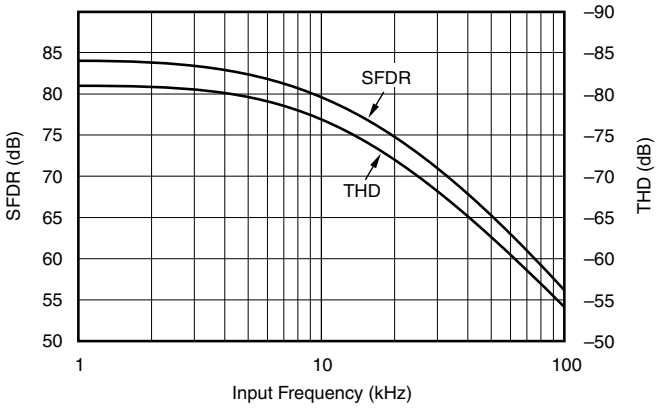
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 10.6kHz, –0.2dB)



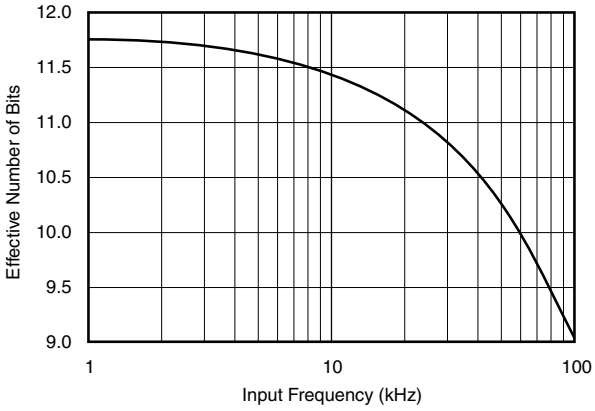
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE+DISTORTION) vs INPUT FREQUENCY



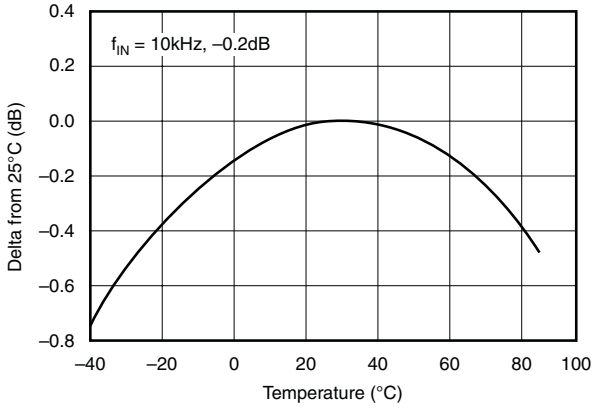
SPURIOUS-FREE DYNAMIC RANGE AND TOTAL
HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



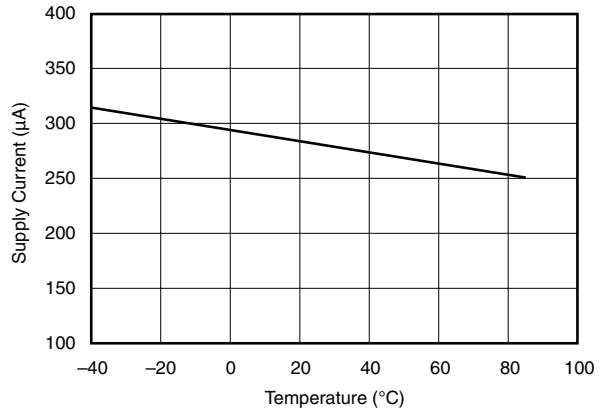
CHANGE IN SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



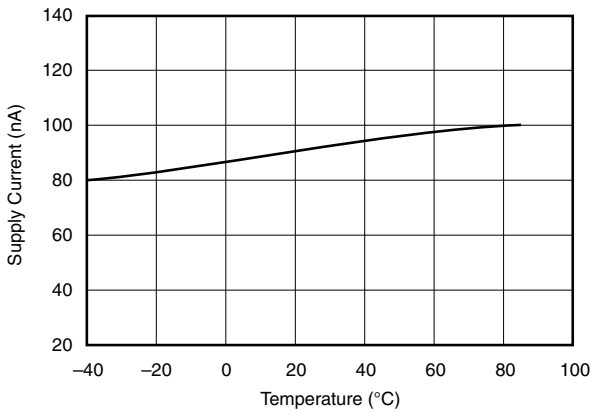
TYPICAL CHARACTERISTICS, V_{CC} = 2.7 V (continued)

V_{CC} = 2.7 V, T_A = 25°C, V_{REF} = 2.5 V, f_{SAMPLE} = 125 kHz, f_{CLK} = 16 × f_{SAMPLE} = 2 MHz (unless otherwise noted)

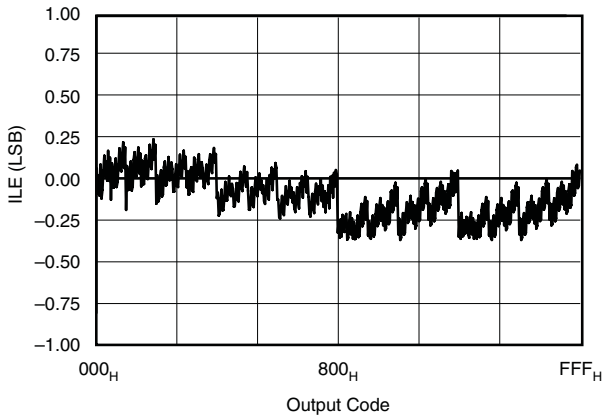
SUPPLY CURRENT vs TEMPERATURE



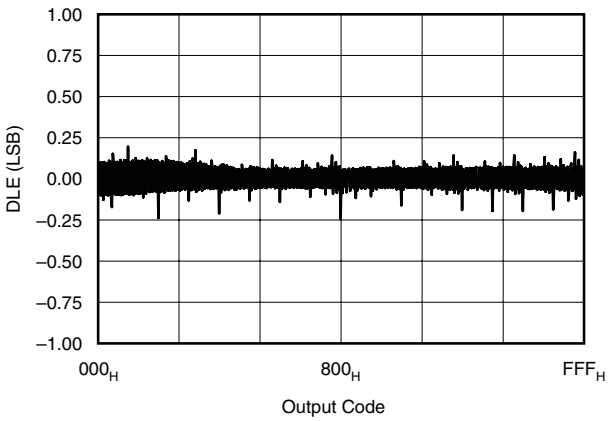
POWER DOWN SUPPLY CURRENT vs TEMPERATURE



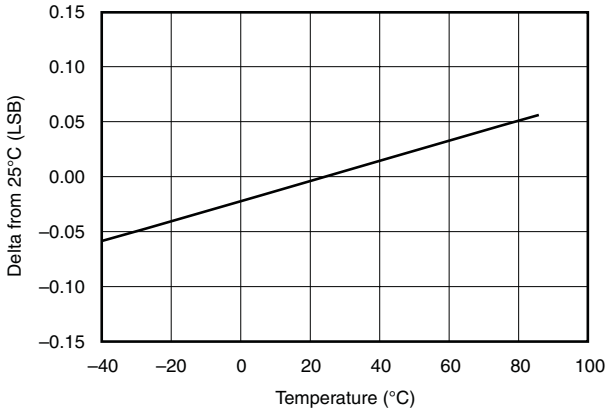
INTEGRAL LINEARITY ERROR vs CODE



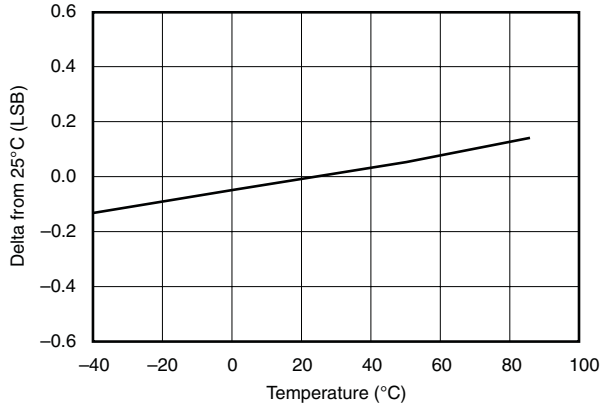
DIFFERENTIAL LINEARITY ERROR vs CODE



CHANGE IN GAIN vs TEMPERATURE



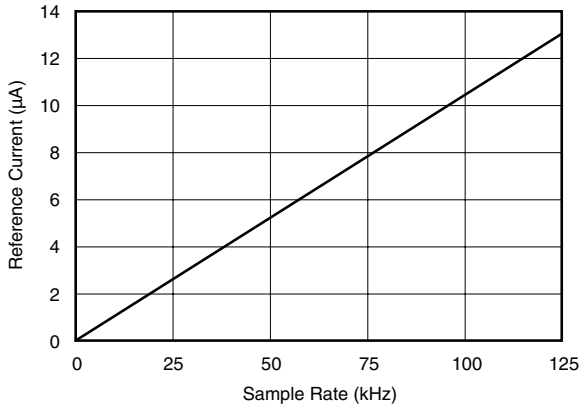
CHANGE IN OFFSET vs TEMPERATURE



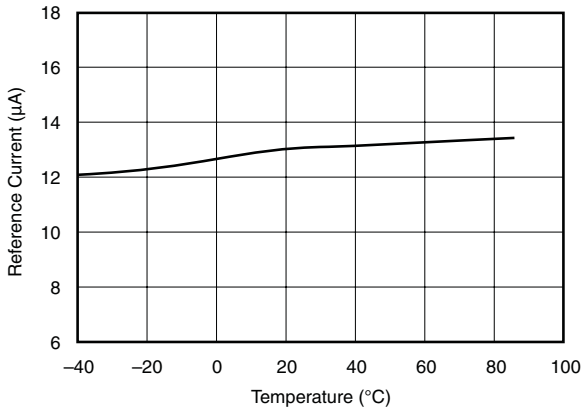
TYPICAL CHARACTERISTICS, V_{CC} = 2.7 V (continued)

V_{CC} = 2.7 V, T_A = 25°C, V_{REF} = 2.5 V, f_{SAMPLE} = 125 kHz, f_{CLK} = 16 × f_{SAMPLE} = 2 MHz (unless otherwise noted)

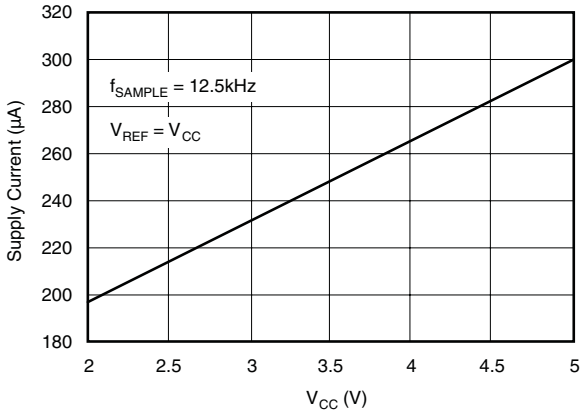
REFERENCE CURRENT vs SAMPLE RATE



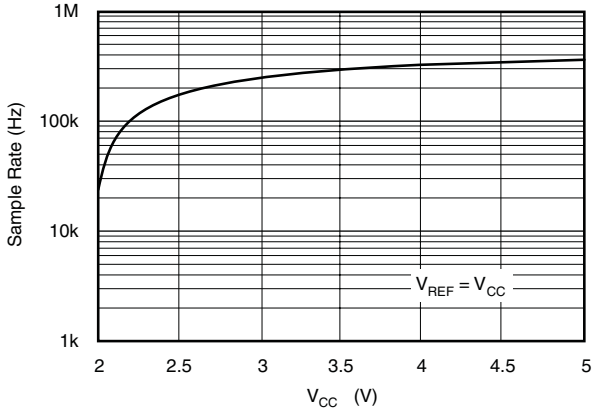
REFERENCE CURRENT vs TEMPERATURE



SUPPLY CURRENT vs V_{CC}



MAXIMUM SAMPLE RATE vs V_{CC}



APPLICATION INFORMATION

The ADS7841 is a classic successive approximation register (SAR) ADC. The architecture is based on capacitive redistribution that inherently includes a sample-and-hold function. The converter is fabricated on a 0.6-µs CMOS process.

The basic operation of the ADS7841 is shown in Figure 1. The device requires an external reference and an external clock. It operates from a single supply of 2.7 V to 5.25 V. The external reference can be any voltage between 100 mV and V_{CC}. The value of the reference voltage directly sets the input range of the converter. The average reference input current depends on the conversion rate of the ADS7841.

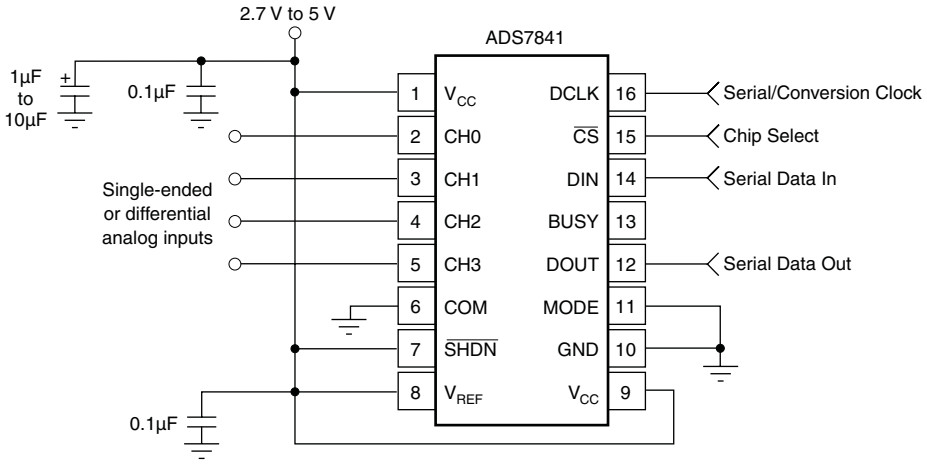


Figure 1. Basic Operation of the ADS7841

The analog input to the converter is differential and is provided via a four-channel multiplexer. The input can be provided in reference to a voltage on the COM pin (which is generally ground) or differentially by using two of the four input channels (CH0-CH3). The particular configuration is selectable via the digital interface.

Analog Input

Figure 2 shows a block diagram of the input multiplexer on the ADS7841. The differential input of the converter is derived from one of the four inputs in reference to the COM pin or two of the four inputs. Table 1 and Table 2 show the relationship between the A2, A1, A0, and SGL/DIF control bits and the configuration of the analog multiplexer. The control bits are provided serially via the DIN pin, see the Digital Interface section of this data sheet for more details.

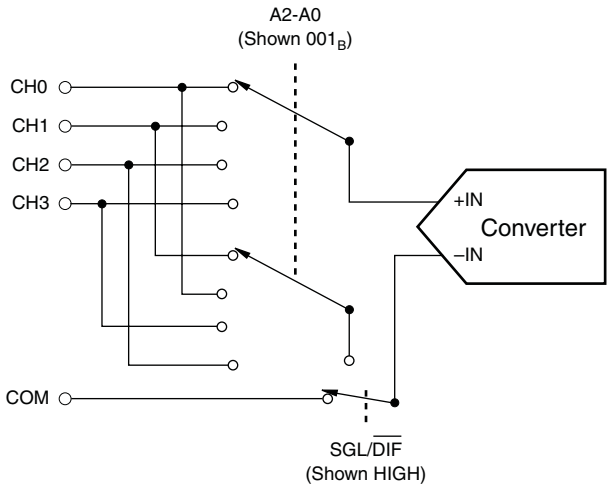


Figure 2. Simplified Diagram of the Analog Input

Table 1. Single-Ended Channel Selection (SGL/$\overline{DIF}$ high)

A2	A1	A0	CH0	CH1	CH2	CH3	COM
0	0	1	+IN				–IN
1	0	1		+IN			–IN
0	1	0			+IN		–IN
1	1	0				+IN	–IN

Table 2. Differential Channel Control (SGL/$\overline{DIF}$ low)

A2	A1	A0	CH0	CH1	CH2	CH3	COM
0	0	1	+IN	–IN			
1	0	1	–IN	+IN			
0	1	0			+IN	–IN	
1	1	0			–IN	+IN	

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs (as shown in Figure 2) is captured on the internal capacitor array. The voltage on the –IN input is limited between –0.2 V and 1.25 V, allowing the input to reject small signals that are common to both the +IN and –IN input. The +IN input has a range of –0.2 V to V_{CC} + 0.2 V.

The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25 pF). After the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

Reference Input

The external reference sets the analog input range. The ADS7841 operates with a reference in the range of 100 mV to V_{CC}. Keep in mind that the analog input is the difference between the +IN input and the –IN input, see Figure 2. For example, in the single-ended mode, a 1.25-V reference, and with the COM pin grounded, the selected input channel (CH0-CH3) digitizes a signal in the range of 0 V to 1.25 V. If the COM pin is connected to 0.5 V, the input range on the selected channel is 0.5 V to 1.75 V.

There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. Any offset or gain error inherent in the ADC appears to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2 LSBs with a 2.5-V reference, then it is typically 10 LSBs with a 0.5-V reference. In each case, the actual offset of the device is the same, 1.22 mV.

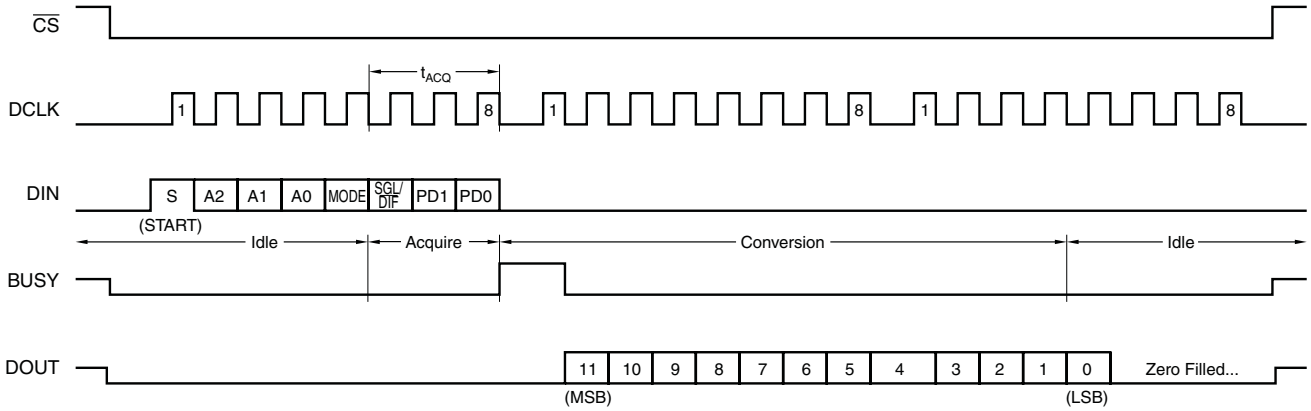
Likewise, the noise or uncertainty of the digitized output increases with lower LSB size. With a reference voltage of 100 mV, the LSB size is 24 μV. This level is below the internal noise of the device. As a result, the digital output code is not stable and varies around a mean value by a number of LSBs. The distribution of output codes is gaussian, and the noise can be reduced by simply averaging consecutive conversion results or applying a digital filter.

With a lower reference voltage, care should be taken to provide a clean layout including adequate bypassing, a clean (low-noise, low-ripple) power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter is also more sensitive to nearby digital signals and electromagnetic interference.

The voltage into the V_{REF} input is not buffered and directly drives the Capacitor Digital-to-Analog Converter (CDAC) portion of the ADS7841. Typically, the input current is 13 μA with a 2.5-V reference. This value varies by microamps depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period does not reduce overall current drain from the reference.

Digital Interface

Figure 3 shows the typical operation of the ADS7841's digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface (note that the digital inputs are over-voltage tolerant up to 5.5 V, regardless of V_{CC}). Each communication between the processor and the converter consists of eight clock cycles. One complete conversion can be accomplished with three serial communications, for a total of 24 clock cycles on the DCLK input.



A. 24 clock cycles per conversion, 8-bit bus interface. No DCLK delay required with dedicated serial port.

Figure 3. Conversion Timing

The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer appropriately, it enters the acquisition (sample) mode. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample-and-hold goes into the hold mode. The next twelve clock cycles accomplish the actual Analog-to-Digital conversion. A thirteenth clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT is low). These are ignored by the converter.

Control Byte

Also shown in Figure 3 is the placement and order of the control bits within the control byte. Table 3 and Table 4 give detailed information about these bits. The first bit, the 'S' bit, must always be high and indicates the start of the control byte. The ADS7841 ignores inputs on the DIN pin until the start bit is detected. The next three bits (A2-A0) select the active input channel or channels of the input multiplexer (see Table 1, Table 2, and Figure 2).

Table 3. Order of Control Bits in Control Byte

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
S	A2	A1	A0	MODE	SGL/$\overline{\text{DIF}}$	PD1	PD0

Table 4. Descriptions of Control Bits Within Control Byte

BIT	NAME	DESCRIPTION
7	S	Start bit. Control byte starts with first high bit on DIN. A new control byte can start every 15th clock cycle in 12-bit conversion mode or every 11th clock cycle in 8-bit conversion mode.
6-4	A2-A0	Channel select bits. Along with the SGL/DIF bit, these bits control the setting of the multiplexer input, see Table 1 and Table 2.
3	MODE	12-bit/8-bit conversion select bit. If the MODE pin is high, this bit controls the number of bits for the next conversion: 12-bits (low) or 8-bits (high). If the MODE pin is low, this bit has no function and the conversion is always 12 bits.
2	SGL/$\overline{\text{DIF}}$	Single-ended/differential select bit. Along with bits A2-A0, this bit controls the setting of the multiplexer input, see Table 1 and Table 2.
1-0	PD1-PD0	Power-down mode select bits. See Table 5 for details.

The MODE bit and the MODE pin work together to determine the number of bits for a given conversion. If the MODE pin is low, the converter always performs a 12-bit conversion regardless of the state of the MODE bit. If the MODE pin is high, then the MODE bit determines the number of bits for each conversion, either 12 bits (low) or 8 bits (high).

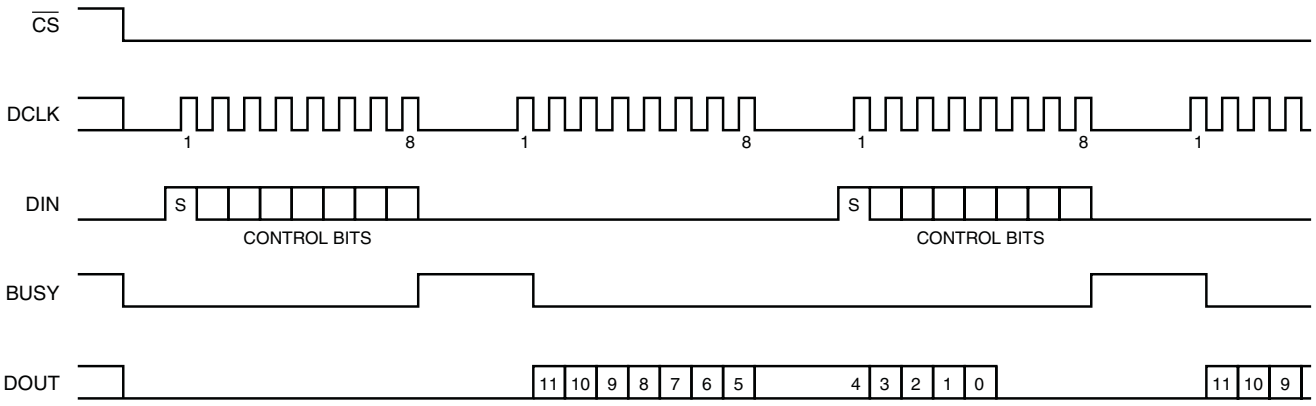
The SGL/DIF bit controls the multiplexer input mode: either single-ended (high) or differential (low). In single-ended mode, the selected input channel is referenced to the COM pin. In differential mode, the two selected inputs provide a differential input. See Table 1, Table 2, and Figure 2 for more information. The last two bits (PD1-PD0) select the powerdown mode, as shown in Table 5. If both inputs are high, the device is always powered up. If both inputs are low, the device enters a power-down mode between conversions. When a new conversion is initiated, the device resumes normal operation instantly—no delay is needed to allow the device to power up and the very first conversion is valid.

Table 5. Power-Down Selection

PD1	PD0	DESCRIPTION
0	0	Power-down between conversions. When each conversion is finished, the converter enters a low power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid.
0	1	Reserved
1	0	Reserved
1	1	No power-down between conversions, device always powered.

16 Clock Cycles Per Conversion

The control bits for conversion n+1 can be overlapped with conversion 'n' to allow for a conversion every 16 clock cycles, as shown in Figure 4. This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer between the processor and the converter. This is possible provided that each conversion completes within 1.6ms of starting. Otherwise, the signal that has been captured on the input sample-and-hold may droop enough to affect the conversion result. In addition, the ADS7841 is fully powered while other serial communications are taking place.



A. 16 clock cycles per conversion, 8-bit bus interface. No DCLK delay required with dedicated serial port.

Figure 4. Conversion Timing

Digital Timing

Figure 5, Table 6, and Table 7 provide detailed timing for the digital interface of the ADS7841.

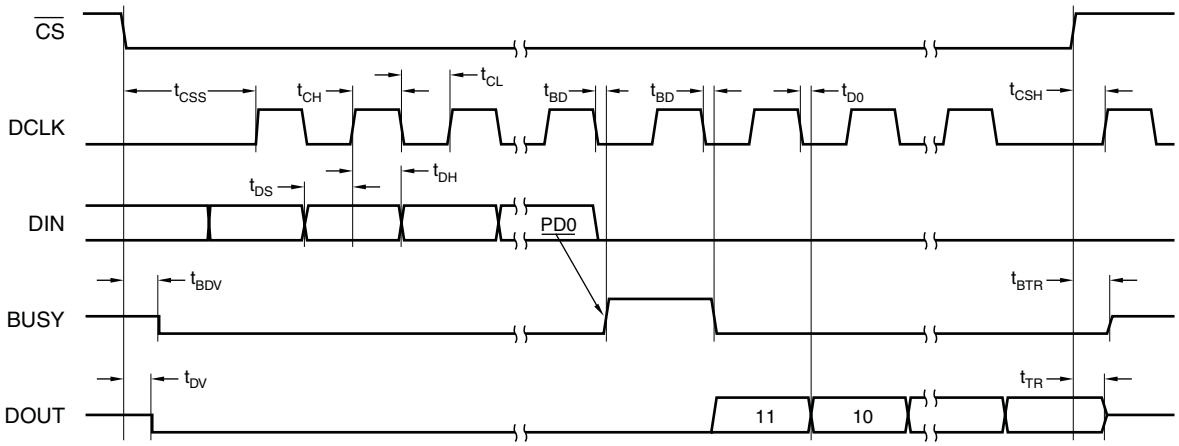


Figure 5. Detailed Timing Diagram

Table 6. Timing Specifications, V_{CC} = 2.7 V to 3.6 V, T_A = –40°C to 85°C, C_{LOAD} = 50 pF

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{ACQ}	Acquisition time	1500		ns
t_{DS}	DIN valid prior to DCLK rising	100		ns
t_{DH}	DIN hold after DCLK high	10		ns
t_{DO}	DCLK falling to DOUT valid		200	ns
t_{DV}	$\overline{CS}$ falling to DOUT enabled		200	ns
t_{TR}	$\overline{CS}$ rising to DOUT disabled		200	ns
t_{CSS}	$\overline{CS}$ falling to first DCLK rising	100		ns
t_{CSH}	$\overline{CS}$ rising to DCLK ignored	0		ns
t_{CH}	DCLK high	200		ns
t_{CL}	DCLK low	200		ns
t_{BD}	DCLK falling to BUSY rising		200	ns
t_{BDV}	$\overline{CS}$ falling to BUSY enabled		200	ns
t_{BTR}	$\overline{CS}$ rising to BUSY disabled		200	ns

Table 7. Timing Specifications, V_{CC} = 4.75 V to 5.25 V, T_A = –40°C to 85°C, C_{LOAD} = 50 pF

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{ACQ}	Acquisition time	900		ns
t_{DS}	DIN valid prior to DCLK rising	50		ns
t_{DH}	DIN hold after DCLK high	10		ns
t_{DO}	DCLK falling to DOUT valid		100	ns
t_{DV}	$\overline{CS}$ falling to DOUT enabled		70	ns
t_{TR}	$\overline{CS}$ rising to DOUT disabled		70	ns
t_{CSS}	$\overline{CS}$ falling to first DCLK rising	50		ns
t_{CSH}	$\overline{CS}$ rising to DCLK ignored	0		ns
t_{CH}	DCLK high	150		ns
t_{CL}	DCLK low	150		ns
t_{BD}	DCLK falling to BUSY rising		100	ns
t_{BDV}	$\overline{CS}$ falling to BUSY enabled		70	ns
t_{BTR}	$\overline{CS}$ rising to BUSY disabled		70	ns

15 Clock Cycles Per Conversion

Figure 6 provides the fastest way to clock the ADS7841. This method does not work with the serial interface of most microcontrollers and digital signal processors as they are generally not capable of providing 15 clock cycles per serial transfer. However, this method could be used with field programmable gate arrays (FPGAs) or application specific integrated circuits (ASICs). Note that this effectively increases the maximum conversion rate of the converter beyond the values given in the specification tables, which assume 16 clock cycles per conversion.

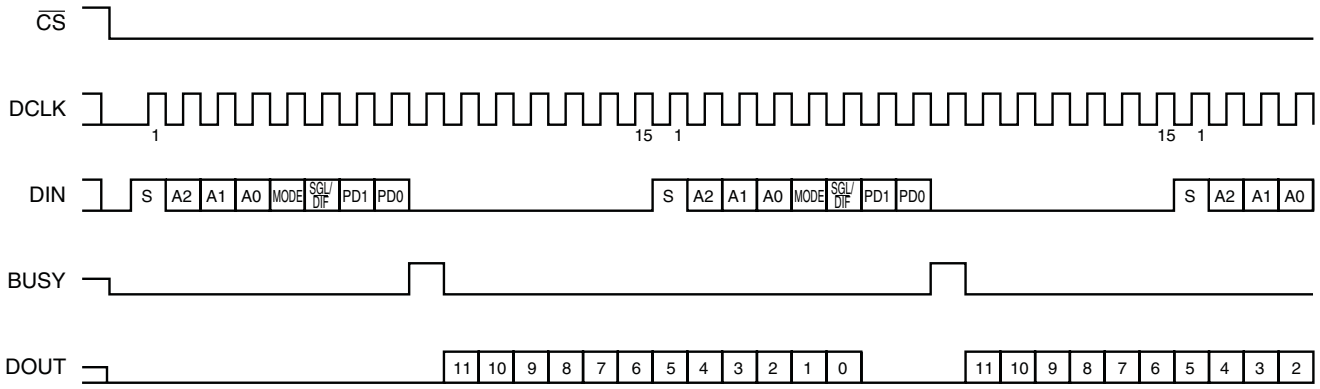
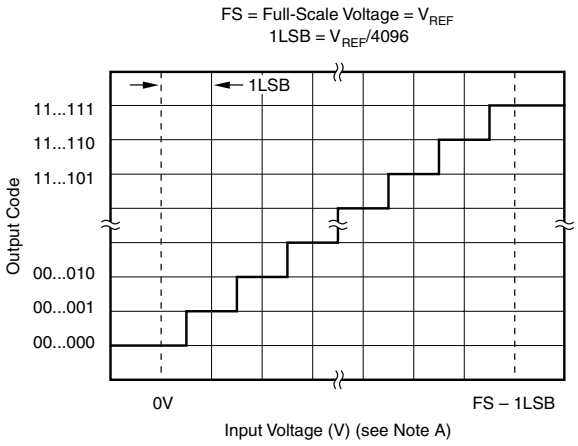


Figure 6. Maximum Conversion Rate, 15 Clock Cycles Per Conversion

Data Format

The ADS7841 output data is in straight binary format, as shown in Figure 7. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.



A. Voltage at converter input, after multiplexer: +IN – (–IN). See Figure 2.

Figure 7. Ideal Input Voltages and Output Codes

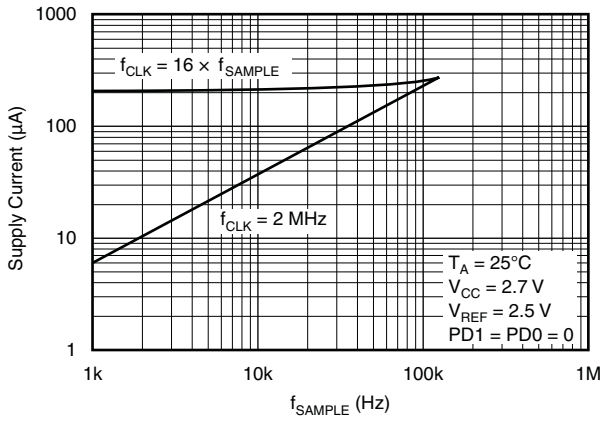
8-Bit Conversion

The ADS7841 provides an 8-bit conversion mode that can be used when faster throughput is needed and the digital result is not as critical. By switching to the 8-bit mode, a conversion is complete four clock cycles earlier. This could be used in conjunction with serial interfaces that provide a 12-bit transfer or two conversions could be accomplished with three 8-bit transfers. Not only does this shorten each conversion by four bits (25% faster throughput), but each conversion can actually occur at a faster clock rate. This is because the internal settling time of the ADS7841 is not as critical, settling to better than 8 bits is all that is needed. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide a 2x increase in conversion rate.

Power Dissipation

There are three power modes for the ADS7841: full power (PD1-PD0 = 11b), auto power-down (PD1-PD0 = 00b), and shutdown (SHDN low). The affects of these modes varies depending on how the ADS7841 is being operated. For example, at full conversion rate and 16 clocks per conversion, there is very little difference between full power mode and auto power-down. Likewise, if the device has entered auto power-down, a shutdown (SHDN low) does not lower power dissipation.

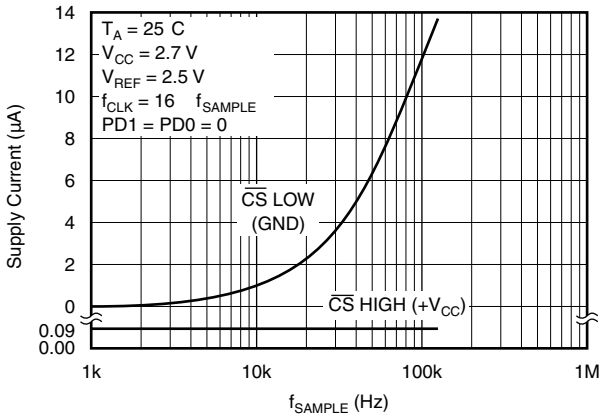
When operating at full-speed and 16-clocks per conversion (see Figure 4), the ADS7841 spends most of its time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Thus, the difference between full power mode and auto power-down is negligible. If the conversion rate is decreased by simply slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion, but conversion are simply done less often, then the difference between the two modes is dramatic. Figure 8 shows the difference between reducing the DCLK frequency ("scaling" DCLK to match the conversion rate) or maintaining DCLK at the highest frequency and reducing the number of conversion per second. In the later case, the converter spends an increasing percentage of its time in power-down mode (assuming the auto power-down mode is active).



A. Directly scaling the frequency of DCLK with sample rate or keeping DCLK at the maximum possible frequency

Figure 8. Supply Current vs Sample Rate

If DCLK is active and $\overline{CS}$ is low while the ADS7841 is in auto power-down mode, the device continues to dissipate some power in the digital logic. The power can be reduced to a minimum by keeping $\overline{CS}$ high. The differences in supply current for these two cases are shown in Figure 9.



A. Varied with state of $\overline{CS}$

Figure 9. Supply Current vs Sample Rate

Operating the ADS7841 in auto power-down mode results in the lowest power dissipation, and there is no conversion time "penalty" on power-up. The very first conversion is valid. $\overline{\text{SHDN}}$ can be used to force an immediate power-down.

PCB Layout

For optimum performance, care should be taken with the physical layout of the ADS7841 circuitry. This is particularly true if the reference voltage is low and/or the conversion rate is high.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the ADS7841 should be clean and well bypassed. A 0.1-µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1-µF to 10-µF capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply.

The reference should be similarly bypassed with a 0.1-µF capacitor. Again, a series resistor and large capacitor can be used to low-pass filter the reference voltage. If the reference voltage originates from an op amp, make sure that it can drive the bypass capacitor without oscillation (the series resistor can help in this case). The ADS7841 draws very little current from the reference on average, but it does place larger demands on the reference circuitry over short periods of time (on each rising edge of DCLK during a conversion).

The ADS7841 architecture offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply appears directly in the digital results. While high-frequency noise can be filtered out as discussed in the previous paragraph, voltage variation due to line frequency (50 Hz or 60 Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this is the "analog" ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power supply entry point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.

REVISION HISTORY

Changes from Revision B (September, 2011) to Revision C	Page
• Deleted package column from Ordering Information table; changed top-side marking of ADS7841EIDBQRQ1 from ADS7841E to S7841E and changed top-side marking for ADS7841ESQDBQRQ1 from ADS7841S to S7841S.	2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS7841EIDBQRQ1	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-	S7841E
ADS7841EIDBQRQ1.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	S7841E
ADS7841ESQDBQRQ1	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	S7841S
ADS7841ESQDBQRQ1.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	S7841S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF ADS7841-Q1 :

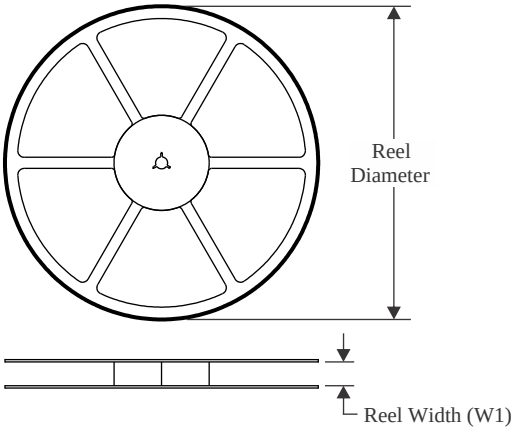
- Catalog : ADS7841

NOTE: Qualified Version Definitions:

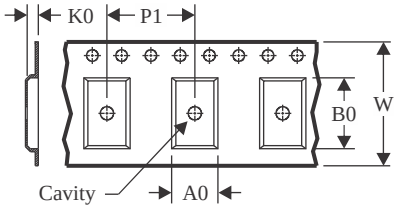
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

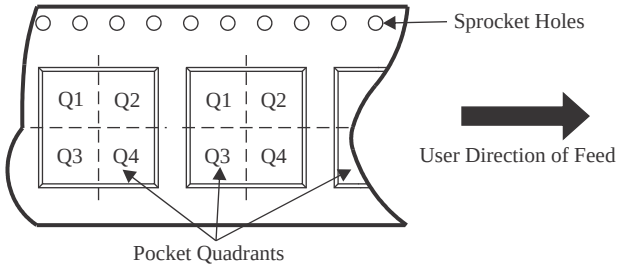


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

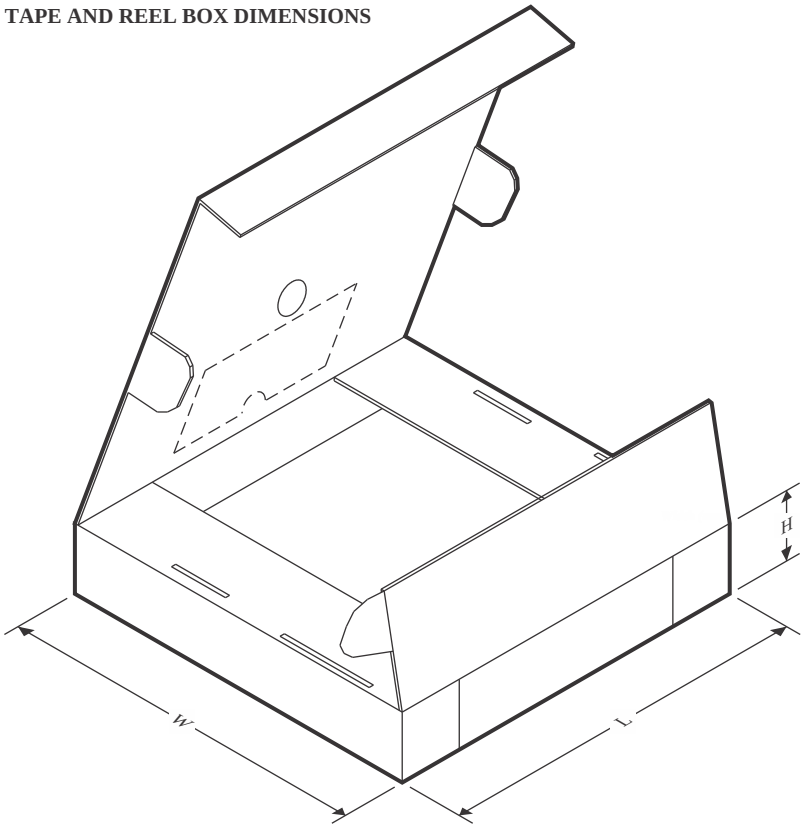
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

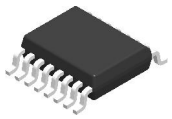
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7841EIDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ADS7841ESQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7841EIDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0
ADS7841ESQDBQRQ1	SSOP	DBQ	16	2500	353.0	353.0	32.0

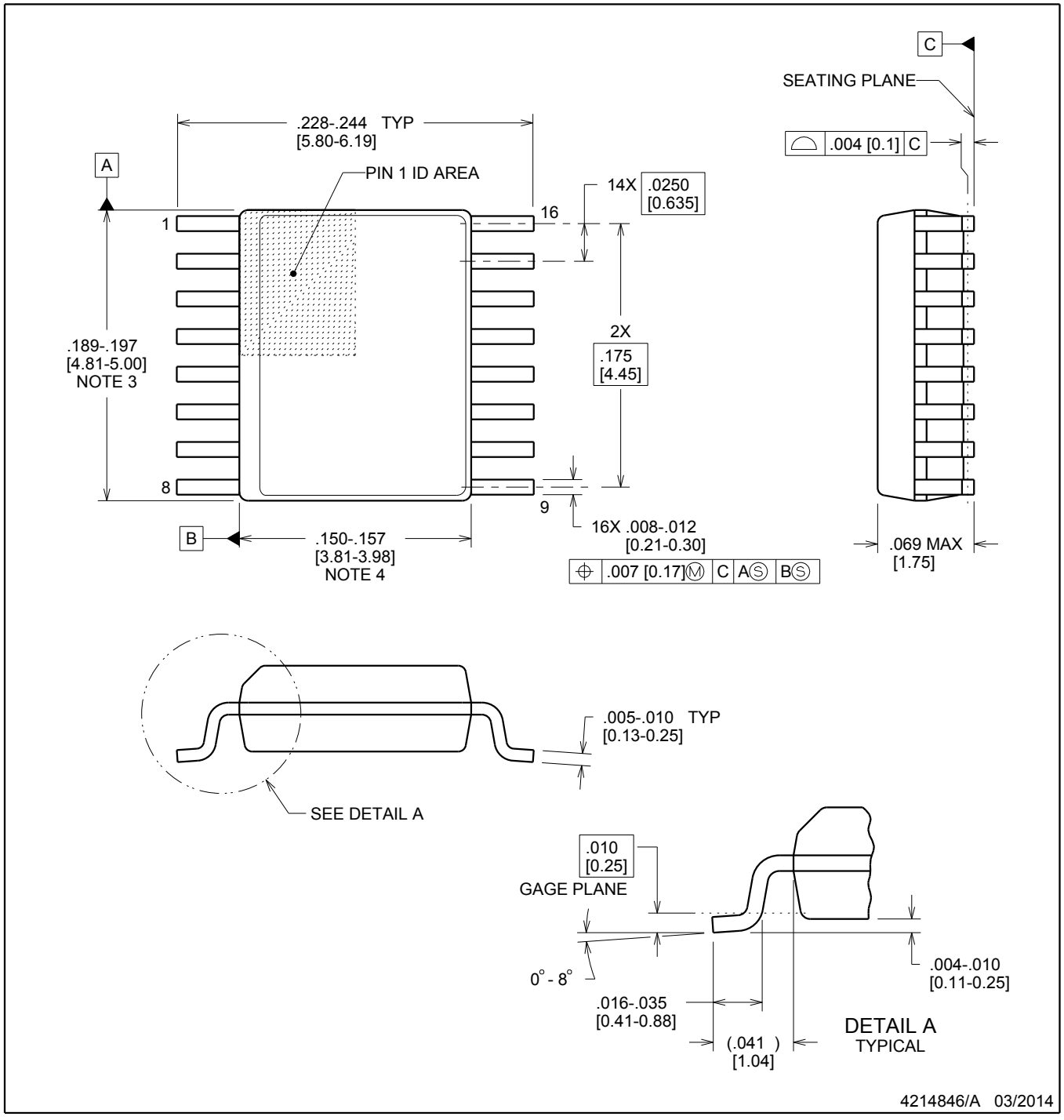


PACKAGE OUTLINE

DBQ0016A

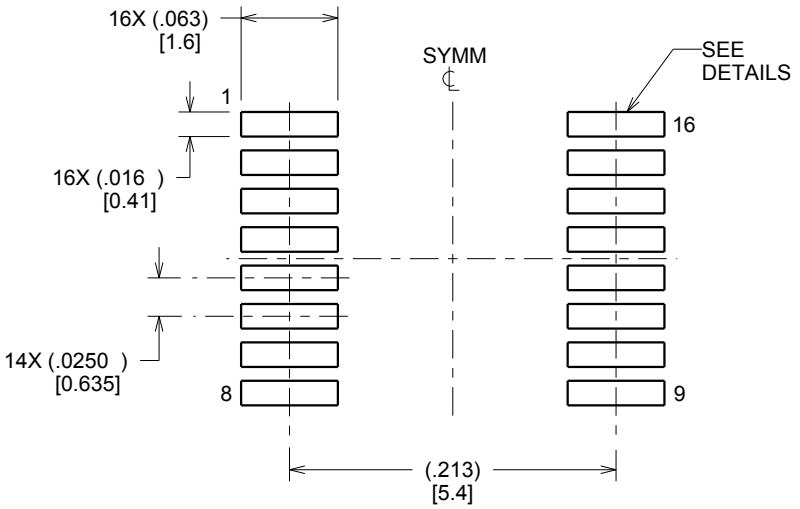
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

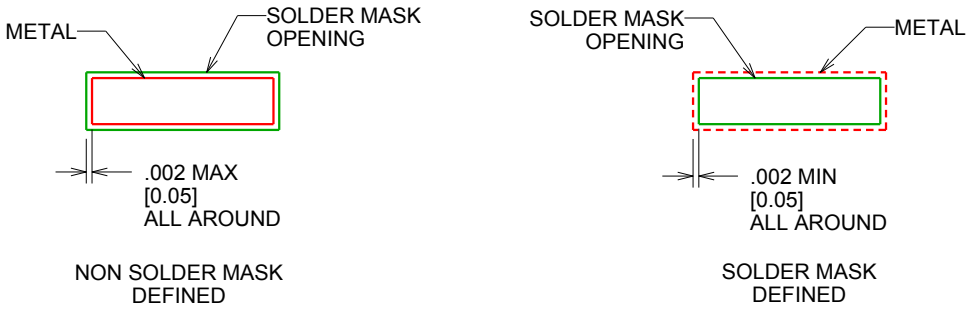


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

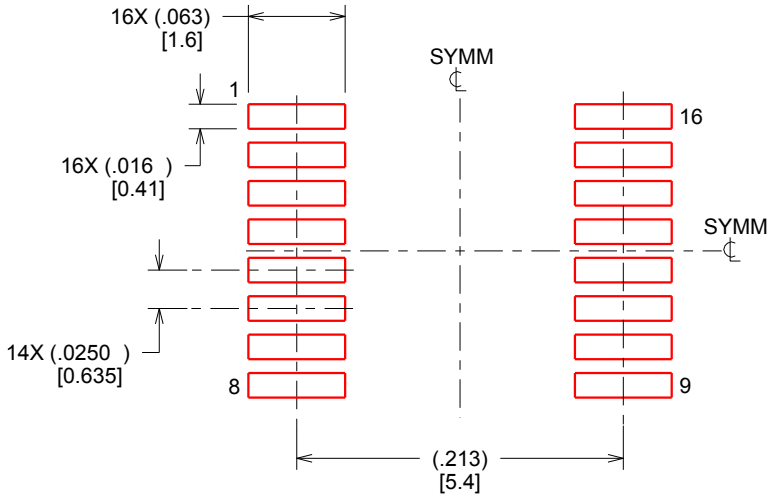
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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