

## ADS556x 16-Bit, 40 and 80 MSPS ADCs With DDR LVDS and CMOS Outputs

### 1 Features

- 16-Bit Resolution
- Maximum Sample Rate:
  - ADS5562: 80 MSPS
  - ADS5560: 40 MSPS
- Total Power:
  - 865 mW at 80 MSPS
  - 674 mW at 40 MSPS
- No Missing Codes
- High SNR: 84 dBFS (3 MHz IF)
- SFDR: 85 dBc (3 MHz IF)
- Low-Frequency Noise Suppression Mode
- Programmable Fine Gain, 1-dB steps Until 6-dB Maximum Gain
- Double Data-Rate (DDR) LVDS and Parallel CMOS Output Options
- Internal and External Reference Support
- 3.3-V Analog and Digital Supply
- Pin-for-Pin With ADS5547 Family
- 48-VQFN Package (7.00 mm × 7.00 mm)

### 2 Applications

- Medical Imaging, MRI
- Wireless Communications Infrastructure
- Software Defined Radio
- Test and Measurement Instrumentation
- High Definition Video

### 3 Description

The ADS556x is a high-performance 16-bit family of ADCs with sampling rates up to 80 MSPS. The device supports very-high SNR for input frequencies in the first Nyquist zone. The device includes a low-frequency noise suppression mode that improves the noise from DC to about 1 MHz.

In addition to high performance, the device offers several flexible features such as output interface (either Double Data Rate [DDR] LVDS or parallel CMOS) and fine gain in 1-dB steps until 6-dB maximum gain.

Innovative techniques, such as DDR LVDS and an internal reference that does not require external decoupling capacitors, have been used to achieve significant savings in pin count. This innovation results in a compact 7-mm × 7-mm 48-pin VQFN package.

The device can be put in an external reference mode, where the VCM pin behaves as the external reference input. For applications where power is important, the ADS556x device offers power down modes and automatic power scaling at lower sample rates.

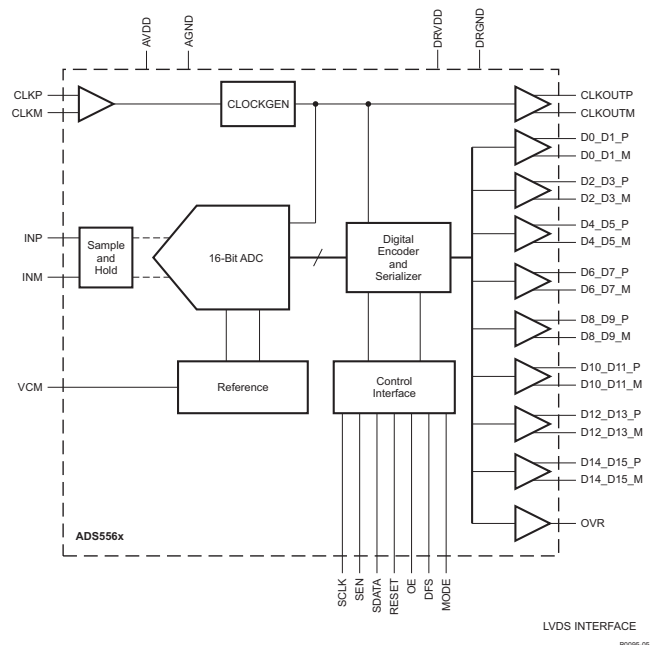
The device is specified over the industrial temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE   | BODY SIZE (NOM)   |
|-------------|-----------|-------------------|
| ADS5560     | VQFN (48) | 7.00 mm × 7.00 mm |
| ADS5562     |           |                   |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Block Diagram



LVDS INTERFACE  
80055-05



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

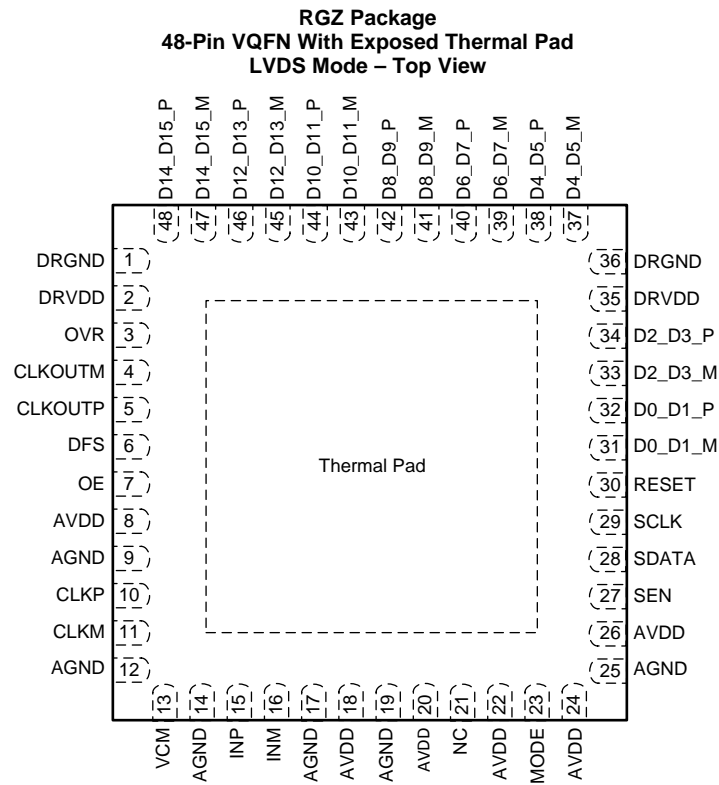
| Changes from Revision A (May 2012) to Revision B  | Page |
|---|------|
| <ul style="list-style-type: none"> <li>Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ....</li> </ul> | 1    |

| Changes from Original (May 2008) to Revision A   | Page  |
|--|---|
| <ul style="list-style-type: none"> <li>Changed Programmable Fine Gain in FEATURES .....</li> <li>Added maximum gain to end of second paragraph of DESCRIPTION .....</li> <li>Changed Voltage between AVDD to DRVDD to Voltage between AVDD and DRVDD in ABS MAX RATINGS .....</li> <li>Added Voltage applied to analog input pins, INP, INM in ABS MAX RATINGS .....</li> <li>Added Voltage applied to analog input pins, CLKP, CLKM, MODE in ABS MAX RATINGS .....</li> <li>Added Voltage applied to analog input pins, RESET, SCLK, SDATA, SEN, OE, DFS in ABS MAX RATINGS .....</li> <li>Changed boundary between DEFAULT SPEED mode and LOW SPEED mode from 30 MSPS to 25 MSPS in RECOMMENDED OPERATING CONDITIONS .....</li> <li>Changed <math>t_{ho}</math> to <math>t_h</math> in header row of <a href="#">Timing Characteristics at Lower Sampling Frequencies</a> .....</li> <li>Added text to Note regarding RESET pulse requirement in <a href="#">Figure 1</a> .....</li> <li>Added 32k Point FFT to TYPICAL CHARACTERISTICS section conditions .....</li> <li>Changed <a href="#">Figure 48</a> .....</li> <li>Added text to end of Programmable Fine Gain section .....</li> <li>Added (Serial Interface Mode) to <a href="#">Table 1</a> title .....</li> <li>Changed LOW SPEED mode boundary from 30 MSPS to 25 MSPS in Low Sampling Frequency Operation section .....</li> </ul> | 1<br>1<br>8<br>8<br>8<br>8<br>9<br>16<br>16<br>19<br>28<br>29<br>29<br>29 |

- Added text to Clock Input section..... 30
- Changed Clock Input section paragraphs and 4 illustrations ..... 30
- Added (of width greater than 10ns) in USING SERIAL INTERFACE PROGRAMMING ONLY section ..... 36
- Added to Priority last row in [Table 3](#) ..... 36
- Changed Parallel Interface Control description for SCLK Control Pin, (SCLK = 0, 3dB gain; SCLK = DRVDD, 1 dB gain) in [Table 4](#)..... 37
- Changed first paragraph in SERIAL INTERFACE section ..... 38
- Added text to [Table 9](#) Note..... 39
- Changed  $F_s > 30$  MSPS to  $F_s > 25$  MSPS in <LOW SPEED> ..... 41

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## 5 Pin Configuration and Functions

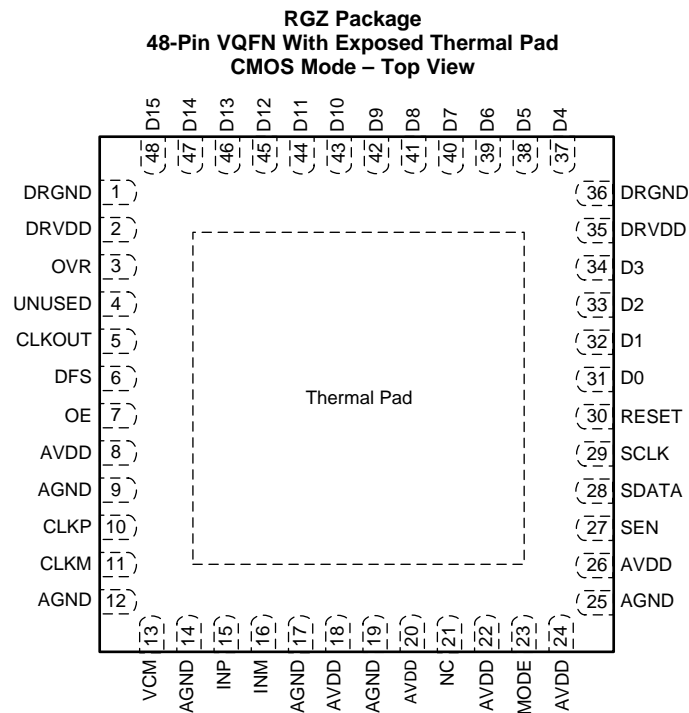


**Pin Functions - LVDS Mode**

| PIN                   |           | I/O | DESCRIPTION  |
|-----------------------|-----------|-----|--|
| NO.                   | NAME      |     |  |
| 9, 12, 14, 17, 19, 25 | AGND      | I   | Analog ground  |
| 8, 18, 20, 22, 24, 26 | AVDD      | I   | Analog power supply  |
| 4                     | CLKOUTM   | O   | Differential output clock, complement                        |
| 5                     | CLKOUTP   | O   | Differential output clock, true                              |
| 10                    | CLKP      | I   | Differential clock input                                     |
| 11                    | CLKM      |     |  |
| 31                    | D0_D1_M   | O   | Differential output data D0 and D1 multiplexed, complement.  |
| 32                    | D0_D1_P   | O   | Differential output data D0 and D1 multiplexed, true         |
| 43                    | D10_D11_M | O   | Differential output data D10 and D11 multiplexed, complement |
| 44                    | D10_D11_P | O   | Differential output data D10 and D11 multiplexed, true       |
| 45                    | D12_D13_M | O   | Differential output data D12 and D13 multiplexed, complement |
| 46                    | D12_D13_P | O   | Differential output data D12 and D13 multiplexed, true       |
| 47                    | D14_D15_M | O   | Differential output data D14 and D15 multiplexed, complement |
| 48                    | D14_D15_P | O   | Differential output data D14 and D15 multiplexed, true       |
| 33                    | D2_D3_M   | O   | Differential output data D2 and D3 multiplexed, complement   |
| 34                    | D2_D3_P   | O   | Differential output data D2 and D3 multiplexed, true         |
| 37                    | D4_D5_M   | O   | Differential output data D4 and D5 multiplexed, complement   |
| 38                    | D4_D5_P   | O   | Differential output data D4 and D5 multiplexed, true         |

**Pin Functions - LVDS Mode (continued)**

| PIN   |         | I/O | DESCRIPTION   |
|-------|---------|-----|---|
| NO.   | NAME    |     |   |
| 39    | D6_D7_M | O   | Differential output data D6 and D7 multiplexed, complement  |
| 40    | D6_D7_P | O   | Differential output data D6 and D7 multiplexed, true  |
| 41    | D8_D9_M | O   | Differential output data D8 and D9 multiplexed, complement  |
| 42    | D8_D9_P | O   | Differential output data D8 and D9 multiplexed, true  |
| 6     | DFS     | I   | Data Format Select input.<br>This pin sets the DATA FORMAT (2s complement or Offset binary) and the LVDS/CMOS output mode type. See <a href="#">Table 7</a> for detailed information.<br>The pin has an internal 100-kΩ pulldown resistor to DRGND.   |
| 1, 36 | DRGND   | I   | Digital and output buffer ground  |
| 2, 35 | DRVDD   | I   | Digital and output buffer supply  |
| 15    | INP     | I   | Differential analog input   |
| 16    | INM     |     |   |
| 23    | MODE    | I   | Mode select input.<br>This pin selects the Internal or External reference mode. See <a href="#">Table 8</a> for detailed information.<br>The pin has an internal 100-kΩ pulldown resistor to AGND.  |
| 21    | NC      | —   | Do not connect  |
| 7     | OE      | I   | Output buffer enable input, active high.<br>The pin has an internal 100-kΩ pullup resistor to DRVDD.  |
| 3     | OVR     | O   | Out-of-range indicator, CMOS level signal   |
| 30    | RESET   | I   | Serial interface reset input.<br>When using the serial interface, the user should apply a high-going pulse on this pin to reset the internal registers.<br>When the serial interface is not used, the user should tie RESET permanently high. (SCLK, SDATA and SEN can be used as parallel pin controls).<br>The pin has an internal 100-kΩ pulldown resistor to DRGND. |
| 29    | SCLK    | I   | This pin functions as serial interface clock input when RESET is low.<br>It functions as LOW SPEED MODE control when RESET is tied high. See <a href="#">Table 4</a> for detailed information.<br>The pin has an internal 100-kΩ pulldown resistor to DRGND.  |
| 28    | SDATA   | I   | This pin functions as serial interface data input when RESET is low.<br>It functions as STANDBY control pin when RESET is tied high.<br>See <a href="#">Table 5</a> for detailed information.<br>The pin has an internal 100-kΩ pulldown resistor to DRGND.   |
| 27    | SEN     | I   | This pin functions as serial interface enable input when RESET is low.<br>It functions as CLKOUT edge programmability when RESET is tied high. See <a href="#">Table 6</a> for detailed information.<br>The pin has an internal 100-kΩ pullup resistor to DRVDD.  |
| 13    | VCM     | I/O | Internal reference mode – Common-mode voltage output.<br>External reference mode – Reference input. The voltage forced on this pin sets the internal reference.   |
| —     | PAD     | —   | Connect the PAD to the ground plane. See the <a href="#">Exposed Thermal Pad</a> section.   |



### Pin Functions - CMOS Mode

| PIN                   |        | I/O | DESCRIPTION              |
|-----------------------|--------|-----|--------------------------|
| NO.                   | NAME   |     |                          |
| 9, 12, 14, 17, 19, 25 | AGND   | I   | Analog ground            |
| 8, 18, 20, 22, 24, 26 | AVDD   | I   | Analog power supply      |
| 5                     | CLKOUT | O   | CMOS output clock        |
| 10                    | CLKP   | I   | Differential clock input |
| 11                    | CLKM   |     |                          |
| 31                    | D0     | O   | CMOS output data D0      |
| 32                    | D1     | O   | CMOS output data D1      |
| 43                    | D10    | O   | CMOS output data D10     |
| 44                    | D11    | O   | CMOS output data D11     |
| 45                    | D12    | O   | CMOS output data D12     |
| 46                    | D13    | O   | CMOS output data D13     |
| 47                    | D14    | O   | CMOS output data D14     |
| 48                    | D15    | O   | CMOS output data D15     |
| 33                    | D2     | O   | CMOS output data D2      |
| 34                    | D3     | O   | CMOS output data D3      |
| 37                    | D4     | O   | CMOS output data D4      |
| 38                    | D5     | O   | CMOS output data D5      |
| 39                    | D6     | O   | CMOS output data D6      |
| 40                    | D7     | O   | CMOS output data D7      |
| 41                    | D8     | O   | CMOS output data D8      |
| 42                    | D9     | O   | CMOS output data D9      |

**Pin Functions - CMOS Mode (continued)**

| PIN   |        | I/O | DESCRIPTION   |
|-------|--------|-----|---|
| NO.   | NAME   |     |   |
| 6     | DFS    | I   | Data Format Select input.<br>This pin sets the DATA FORMAT (2s complement or Offset binary) and the LVDS/CMOS output mode type. See <a href="#">Table 7</a> for detailed information.<br>The pin has an internal 100-k $\Omega$ pulldown resistor to DRGND.   |
| 1, 36 | DRGND  | I   | Digital and output buffer ground  |
| 2, 35 | DRVDD  | I   | Digital and output buffer supply  |
| 15    | INP    | I   | Differential analog input   |
| 16    | INM    |     |   |
| 23    | MODE   | I   | Mode select input.<br>This pin selects the Internal or External reference mode. See <a href="#">Table 8</a> for detailed information.<br>The pin has an internal 100-k $\Omega$ pulldown resistor to AGND.  |
| 21    | NC     | —   | Do not connect  |
| 7     | OE     | I   | Output buffer enable input, active high.<br>The pin has an internal 100-k $\Omega$ pullup resistor to DRVDD.  |
| 3     | OVR    | O   | Out-of-range indicator, CMOS level signal   |
| 30    | RESET  | I   | Serial interface reset input.<br>When using the serial interface, the user should apply a high-going pulse on this pin to reset the internal registers.<br>When the serial interface is not used, the user should tie RESET permanently high. (SCLK, SDATA and SEN can be used as parallel pin controls).<br>The pin has an internal 100-k $\Omega$ pulldown resistor to DRGND. |
| 29    | SCLK   | I   | This pin functions as serial interface clock input when RESET is low.<br>It functions as LOW SPEED MODE control when RESET is tied high. See <a href="#">Table 4</a> for detailed information.<br>The pin has an internal 100-k $\Omega$ pulldown resistor to DRGND.  |
| 28    | SDATA  | I   | This pin functions as serial interface data input when RESET is low.<br>It functions as STANDBY control pin when RESET is tied high.<br>See <a href="#">Table 5</a> for detailed information.<br>The pin has an internal 100-k $\Omega$ pulldown resistor to DRGND.   |
| 27    | SEN    | I   | This pin functions as serial interface enable input when RESET is low.<br>It functions as CLKOUT edge programmability when RESET is tied high. See <a href="#">Table 6</a> for detailed information.<br>The pin has an internal 100-k $\Omega$ pullup resistor to DRVDD.  |
| 4     | UNUSED | —   | Unused pin in CMOS mode   |
| 13    | VCM    | I/O | Internal reference mode – Common-mode voltage output.<br>External reference mode – Reference input. The voltage forced on this pin sets the internal references.  |
| —     | PAD    | —   | Connect the PAD to the ground plane. See the <a href="#">Exposed Thermal Pad</a> section.   |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|   |  | MIN  | MAX                | UNIT |
|---|--|------|--------------------|------|
| Supply voltage  | AVDD   | -0.3 | 3.9                | V    |
|   | DRVDD  | -0.3 | 3.9                | V    |
| Voltage between AGND and DRGND                          |  | -0.3 | 0.3                | V    |
| Voltage between AVDD and DRVDD                          |  | -0.3 | 3.3                | V    |
| Voltage applied to VCM pin (in external reference mode) |  | -0.3 | 1.8                | V    |
| Voltage applied to analog input pins                    | INP, INM   | -0.3 | (3.6, AVDD + 0.3)  | V    |
|   | CLKP, CLKM <sup>(2)</sup> , MODE                       | -0.3 | (3.6, AVDD + 0.3)  |      |
|   | RESET, SCLK, SDATA, SEN, OE, DFS                       | -0.3 | (3.6, DRVDD + 0.3) | V    |
| T <sub>A</sub>  | Operating free-air temperature                         | -40  | 85                 | °C   |
| T <sub>jmax</sub>                                       | Operating junction temperature                         |      | 125                | °C   |
|   | Lead temperature 1,6 mm (1/16") from the case for 10 s |      | 220                | °C   |
| T <sub>STG</sub>  | Storage temperature                                    | -65  | 150                | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) When AVDD is turned off, TI recommends switching off the input clock (or ensure the voltage on CLKP, CLKM is <|0.3 V|). This prevents the ESD protection diodes at the clock input pins from turning on.

### 6.2 ESD Ratings

|  |   | VALUE | UNIT |
|--|---|-------|------|
| V <sub>(ESD)</sub>   | Electrostatic discharge   |       |      |
|  | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> | 2000  | V    |
| Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | 500   |       |      |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|   |   | MIN                           | NOM  | MAX | UNIT            |      |
|---|---|-------------------------------|------|-----|-----------------|------|
| <b>SUPPLIES AND REFERENCES</b>  |   |                               |      |     |                 |      |
| AVDD  | Analog supply voltage   | 3                             | 3.3  | 3.6 | V               |      |
| DRVDD   | Digital supply voltage  | 3                             | 3.3  | 3.6 | V               |      |
| <b>ANALOG INPUTS</b>  |   |                               |      |     |                 |      |
| Differential input voltage range (with default fine gain=1 dB)                                    |   | 3.56                          |      |     | V <sub>PP</sub> |      |
| Input common-mode voltage   |   | 1.5 ±0.1                      |      |     | V               |      |
| Voltage applied on VCM in external reference mode   |   | 1.5 ±0.05                     |      |     | V               |      |
| <b>CLOCK INPUT</b>  |   |                               |      |     |                 |      |
| Sample rate   | ADS5562   | DEFAULT SPEED mode            | > 25 |     | 80              | MSPS |
|   |   | LOW SPEED mode <sup>(1)</sup> | 1    |     | 25              | MSPS |
|   | ADS5560   | DEFAULT SPEED mode            | > 25 |     | 40              | MSPS |
|   |   | LOW SPEED mode                | 1    |     | 25              | MSPS |
| Clock amplitude, ac-coupled, differential (V <sub>CLKP</sub> – V <sub>CLKM</sub> ) <sup>(2)</sup> |   | 0.4                           |      |     | V <sub>PP</sub> |      |
| Clock duty cycle  |   | 45%                           | 50%  | 55% |                 |      |
| <b>DIGITAL OUTPUTS</b>  |   |                               |      |     |                 |      |
| C <sub>L</sub>  | Maximum external load capacitance from each output pin to DRGND (LVDS and CMOS modes) | 5                             |      |     | pF              |      |
| R <sub>L</sub>  | Differential external load resistance between the LVDS output pairs (LVDS mode)       | 100                           |      |     | Ω               |      |
| Operating free-air temperature  |   | –40                           |      |     | 85              | °C   |

 (1) See the [Low Sampling Frequency Operation](#) section for details.

(2) Supported clock waveform formats: sine wave, LVPECL, LVDS, and LVCMOS

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | ADS5560<br>ADS5562 | UNIT |
|-------------------------------|--|--------------------|------|
|                               |  | RGZ (VQFN)         |      |
|                               |  | 48 PINS            |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 27.6               | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 12.4               | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 4.4                | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.2                | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 4.4                | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 0.9                | °C/W |

 (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling rate = Maximum Rated, sine wave input clock, 1.5-V<sub>PP</sub> clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, internal reference mode, DDR LVDS interface, *default fine gain (1 dB)*. Minimum and maximum values are across the full temperature range T<sub>MIN</sub> = –40°C to T<sub>MAX</sub> = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = Maximum Rated, unless otherwise noted.

| PARAMETER  |   | TEST CONDITIONS   | MIN     | TYP     | MAX  | UNIT            |
|--|---|---|---------|---------|------|-----------------|
| Resolution   |   |   |         | 16      |      | bits            |
| <b>ANALOG INPUT</b>  |   |   |         |         |      |                 |
| Differential input voltage range <sup>(1)</sup>  |   |   |         | 3.56    |      | V <sub>PP</sub> |
| Differential input capacitance   |   |   |         | 5       |      | pF              |
| Analog input bandwidth   |   |   |         | 300     |      | MHz             |
| Analog input common-mode current (per input pin)   |   |   |         | 6.6     |      | µA/MSPS         |
| VCM  | Common-mode output voltage                            | Internal reference mode   |         | 1.5     |      | V               |
| VCM output current capability  |   | Internal reference mode   |         | ±4      |      | mA              |
| <b>DC ACCURACY</b>   |   |   |         |         |      |                 |
| No Missing Codes   |   | 0-dB gain   |         | Assured |      |                 |
| DNL  | Differential non-linearity                            |   | –0.95   | 0.5     | 3    | LSB             |
| INL  | Integral non-linearity                                |   | –8.5    | ±3      | 8.5  | LSB             |
| Offset error   |   |   | –25     | ±10     | 25   | mV              |
| Offset error temperature coefficient   |   |   |         | 0.005   |      | mV/°C           |
| Variation of offset error across AVDD supply   |   |   |         | 1.5     |      | mV/V            |
| There are two sources of gain error: i) internal reference inaccuracy and ii) channel gain error |   |   |         |         |      |                 |
| E <sub>GREF</sub>  | Gain error due to internal reference inaccuracy alone |   | –2.5    | ±1      | 2.5  | % full scale    |
| E <sub>CHAN</sub>  | Channel gain error alone                              |   | –2.5    | ±1      | 2.5  | % full scale    |
| Channel gain error temperature coefficient   |   |   |         | 0.01    |      | Δ%/°C           |
| <b>POWER SUPPLY</b>  |   |   |         |         |      |                 |
| IAVDD  | Analog supply current                                 | ADS5560   |         | 210     | 250  | mA              |
|  |   | ADS5562   |         | 160     | 190  |                 |
| IDRVDD   | Digital supply current                                | LVDS mode<br>C <sub>L</sub> = 5 pF, I <sub>O</sub> = 3.5 mA, R <sub>L</sub> = 100 Ω | ADS5560 | 52      |      | mA              |
|  |   |   | ADS5562 | 44      |      |                 |
|  |   | CMOS mode<br>C <sub>L</sub> = 5 pF, F <sub>IN</sub> = 3 MHz                         | ADS5560 | 60      |      | mA              |
|  |   |   | ADS5562 | 37      |      |                 |
| Total power  |   | LVDS mode   | ADS5560 | 865     | 1100 | mW              |
|  |   |   | ADS5562 | 674     | 810  |                 |
| Standby power  |   | STANDBY mode with clock running   | ADS5560 | 155     |      | mW              |
|  |   |   | ADS5562 | 135     |      |                 |
| Clock stop power   |   |   |         | 125     | 150  | mW              |

(1) The full-scale voltage range is a function of the fine gain settings. See [Table 1](#).

## 6.6 AC Electrical Characteristics for ADS5560 $F_s = 40$ MSPS

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling rate = Maximum Rated, sine wave input clock, 1.5-V<sub>pp</sub> clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, internal reference mode, DDR LVDS interface, 0 dB fine gain<sup>(1)</sup>. Minimum and maximum values are across the full temperature range T<sub>MIN</sub> = -40°C to T<sub>MAX</sub> = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = Maximum Rated, *default fine gain (1 dB)*, unless otherwise noted.

| PARAMETER                                     | TEST CONDITIONS                          |                          | MIN  | TYP  | MAX | UNIT |
|---|--|--------------------------|------|------|-----|------|
| SNR<br>Signal to noise ratio                  | LVDS interface                           | F <sub>IN</sub> = 3 MHz  |      | 84.3 |     | dBFS |
|   |  | F <sub>IN</sub> = 10 MHz | 80   | 84   |     |      |
|   |  | F <sub>IN</sub> = 25 MHz |      | 82.5 |     |      |
|   |  | F <sub>IN</sub> = 30 MHz |      | 81.8 |     |      |
|   | CMOS interface                           | F <sub>IN</sub> = 3 MHz  |      | 83.5 |     | dBFS |
|   |  | F <sub>IN</sub> = 10 MHz | 78   | 83.1 |     |      |
|   |  | F <sub>IN</sub> = 25 MHz |      | 81.8 |     |      |
|   |  | F <sub>IN</sub> = 30 MHz |      | 81.6 |     |      |
| RMS output noise                              | Inputs tied to common-mode               |                          |      | 1.42 |     | LSB  |
| SINAD<br>Signal to noise and distortion ratio | LVDS interface                           | F <sub>IN</sub> = 3 MHz  |      | 83.2 |     | dBFS |
|   |  | F <sub>IN</sub> = 10 MHz | 76   | 83   |     |      |
|   |  | F <sub>IN</sub> = 25 MHz |      | 79   |     |      |
|   |  | F <sub>IN</sub> = 30 MHz |      | 77   |     |      |
|   | CMOS interface                           | F <sub>IN</sub> = 3 MHz  |      | 82   |     | dBFS |
|   |  | F <sub>IN</sub> = 10 MHz | 75   | 81.4 |     |      |
|   |  | F <sub>IN</sub> = 25 MHz |      | 79.3 |     |      |
|   |  | F <sub>IN</sub> = 30 MHz |      | 78   |     |      |
| ENOB<br>Effective number of bits              | LVDS interface, F <sub>IN</sub> = 10 MHz |                          | 12.4 | 13.5 |     | bits |
| SFDR<br>Spurious free dynamic range           | F <sub>IN</sub> = 3 MHz                  |                          |      | 90   |     | dBc  |
|   | F <sub>IN</sub> = 10 MHz                 |                          | 78   | 88   |     |      |
|   | F <sub>IN</sub> = 25 MHz                 |                          |      | 83   |     |      |
|   | F <sub>IN</sub> = 30 MHz                 |                          |      | 79   |     |      |
| HD2<br>Second harmonic                        | F <sub>IN</sub> = 3 MHz                  |                          |      | 94   |     | dBc  |
|   | F <sub>IN</sub> = 10 MHz                 |                          | 78   | 92   |     |      |
|   | F <sub>IN</sub> = 25 MHz                 |                          |      | 90   |     |      |
|   | F <sub>IN</sub> = 30 MHz                 |                          |      | 88   |     |      |

(1) After reset, the device is initialized to 1-dB fine gain setting. For SFDR and SNR performance across fine gains, see the [Typical Characteristics](#) section.

## 6.7 AC Electrical Characteristics for ADS5562, $F_s = 80$ MSPS

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling rate = Maximum Rated, sine wave input clock, 1.5-V<sub>pp</sub> clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, internal reference mode, DDR LVDS interface, 0 dB fine gain<sup>(1)</sup>. Minimum and maximum values are across the full temperature range T<sub>MIN</sub> = –40°C to T<sub>MAX</sub> = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = Maximum Rated, *default fine gain (1 dB)*, unless otherwise noted.

| PARAMETER                                     | TEST CONDITIONS                          | MIN                      | TYP  | MAX  | UNIT |
|---|--|--------------------------|------|------|------|
| SNR<br>Signal to noise ratio                  | LVDS interface                           | F <sub>IN</sub> = 3 MHz  |      | 84   | dBFS |
|   |  | F <sub>IN</sub> = 10 MHz | 79   | 83.8 |      |
|   |  | F <sub>IN</sub> = 25 MHz |      | 83.2 |      |
|   |  | F <sub>IN</sub> = 30 MHz |      | 82.8 |      |
|   | CMOS interface                           | F <sub>IN</sub> = 3 MHz  |      | 81.7 | dBFS |
|   |  | F <sub>IN</sub> = 10 MHz | 77   | 81.4 |      |
|   |  | F <sub>IN</sub> = 25 MHz |      | 80.7 |      |
|   |  | F <sub>IN</sub> = 30 MHz |      | 80.4 |      |
| RMS output noise                              | Inputs tied to common-mode               |                          | 1.42 |      | LSB  |
| SINAD<br>Signal to noise and distortion ratio | LVDS interface                           | F <sub>IN</sub> = 3 MHz  |      | 80.5 | dBFS |
|   |  | F <sub>IN</sub> = 10 MHz | 75   | 80.5 |      |
|   |  | F <sub>IN</sub> = 25 MHz |      | 79.5 |      |
|   |  | F <sub>IN</sub> = 30 MHz |      | 79   |      |
|   | CMOS interface                           | F <sub>IN</sub> = 3 MHz  |      | 80.5 | dBFS |
|   |  | F <sub>IN</sub> = 10 MHz | 73.5 | 80.2 |      |
|   |  | F <sub>IN</sub> = 25 MHz |      | 79.3 |      |
|   |  | F <sub>IN</sub> = 30 MHz |      | 77.9 |      |
| ENOB<br>Effective number of bits              | LVDS interface, F <sub>IN</sub> = 10 MHz | 12.2                     | 13.1 |      | bits |
| SFDR<br>Spurious free dynamic range           | F <sub>IN</sub> = 3 MHz                  |                          | 85   | dBc  |      |
|   | F <sub>IN</sub> = 10 MHz                 | 77                       | 85   |      |      |
|   | F <sub>IN</sub> = 25 MHz                 |                          | 83   |      |      |
|   | F <sub>IN</sub> = 30 MHz                 |                          | 80   |      |      |
| HD2<br>Second harmonic                        | F <sub>IN</sub> = 3 MHz                  |                          | 90   | dBc  |      |
|   | F <sub>IN</sub> = 10 MHz                 | 77                       | 89   |      |      |
|   | F <sub>IN</sub> = 25 MHz                 |                          | 88   |      |      |
|   | F <sub>IN</sub> = 30 MHz                 |                          | 88   |      |      |

(1) After reset, the device is initialized to 1-dB fine gain setting. For SFDR and SNR performance across fine gains, see the [Typical Characteristics](#) section.

## 6.8 Electrical Characteristics for ADS5562

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling rate = Maximum Rated, sine wave input clock, 1.5-V<sub>PP</sub> clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0 dB fine gain<sup>(1)</sup>, internal reference mode, DDR LVDS interface. Minimum and maximum values are across the full temperature range T<sub>MIN</sub> = –40°C to T<sub>MAX</sub> = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = Maximum Rated, default fine gain (1 dB), unless otherwise noted.

| PARAMETER                                     | TEST CONDITIONS  | MIN  | TYP | MAX | UNIT            |
|---|--|------|-----|-----|-----------------|
| HD3<br>Third harmonic                         | F <sub>IN</sub> = 3 MHz  |      | 85  |     | dBc             |
|   | F <sub>IN</sub> = 10 MHz   | 77   | 85  |     |                 |
|   | F <sub>IN</sub> = 25 MHz   |      | 83  |     |                 |
|   | F <sub>IN</sub> = 30 MHz   |      | 80  |     |                 |
| Worst harmonic<br>other than HD2, HD3         | F <sub>IN</sub> = 3 MHz  |      | 104 |     | dBc             |
|   | F <sub>IN</sub> = 10 MHz   |      | 102 |     |                 |
|   | F <sub>IN</sub> = 25 MHz   |      | 100 |     |                 |
|   | F <sub>IN</sub> = 30 MHz   |      | 100 |     |                 |
| THD<br>Total harmonic distortion              | F <sub>IN</sub> = 3 MHz  |      | 84  |     | dBc             |
|   | F <sub>IN</sub> = 10 MHz   | 75.5 | 83  |     |                 |
|   | F <sub>IN</sub> = 25 MHz   |      | 82  |     |                 |
|   | F <sub>IN</sub> = 30 MHz   |      | 80  |     |                 |
| IMD<br>Two-tone intermodulation<br>distortion | F <sub>IN1</sub> = 5 MHz, F <sub>IN2</sub> = 10 MHz, each tone –7 dBFS |      | 92  |     | dBFS            |
| Voltage overload recovery time                | Recovery to 1% for 6-dB overload                                       |      | 1   |     | clock<br>cycles |

(1) After reset, the device is initialized to 1-dB fine gain setting. For SFDR and SNR performance across fine gains, see the [Typical Characteristics](#) section.

## 6.9 Electrical Characteristics for ADS5560

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling rate = Maximum Rated, sine wave input clock, 1.5-V<sub>PP</sub> clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, internal reference mode, DDR LVDS interface, 0 dB fine gain<sup>(1)</sup>. Minimum and maximum values are across the full temperature range T<sub>MIN</sub> = –40°C to T<sub>MAX</sub> = 85°C, AVDD = DRVDD = 3.3 V, sampling rate = Maximum Rated, default fine gain (1 dB), unless otherwise noted.

| PARAMETER                                     | TEST CONDITIONS  | MIN  | TYP | MAX | UNIT            |
|---|--|------|-----|-----|-----------------|
| HD3<br>Third harmonic                         | F <sub>IN</sub> = 3 MHz  |      | 90  |     | dBc             |
|   | F <sub>IN</sub> = 10 MHz   | 78   | 88  |     |                 |
|   | F <sub>IN</sub> = 25 MHz   |      | 83  |     |                 |
|   | F <sub>IN</sub> = 30 MHz   |      | 79  |     |                 |
| Worst harmonic<br>other than HD2, HD3         | F <sub>IN</sub> = 3 MHz  |      | 104 |     | dBc             |
|   | F <sub>IN</sub> = 10 MHz   |      | 102 |     |                 |
|   | F <sub>IN</sub> = 25 MHz   |      | 101 |     |                 |
|   | F <sub>IN</sub> = 30 MHz   |      | 101 |     |                 |
| THD<br>Total harmonic distortion              | F <sub>IN</sub> = 3 MHz  |      | 88  |     | dBc             |
|   | F <sub>IN</sub> = 10 MHz   | 76.5 | 86  |     |                 |
|   | F <sub>IN</sub> = 25 MHz   |      | 81  |     |                 |
|   | F <sub>IN</sub> = 30 MHz   |      | 78  |     |                 |
| IMD<br>Two-tone intermodulation<br>distortion | F <sub>IN1</sub> = 5 MHz, F <sub>IN2</sub> = 10 MHz, each tone –7 dBFS |      | 98  |     | dBFS            |
| Voltage overload recovery time                | Recovery to 1% for 6-dB overload                                       |      | 1   |     | clock<br>cycles |

(1) After reset, the device is initialized to 1-dB fine gain setting. For SFDR and SNR performance across fine gains, see the [Typical Characteristics](#) section.

## 6.10 Digital Characteristics

DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1,  $AVDD = 3\text{ V}$  to  $3.6\text{ V}$ ,  $I_O = 3.5\text{ mA}$ ,  $R_L = 100\ \Omega$  <sup>(1)(2)</sup>

| PARAMETER                             | TEST CONDITIONS  | MIN | TYP   | MAX | UNIT          |
|---------------------------------------|--|-----|-------|-----|---------------|
| <b>DIGITAL INPUTS</b>                 |  |     |       |     |               |
| High-level input voltage              |  | 2.4 |       |     | V             |
| Low-level input voltage               |  |     |       | 0.8 | V             |
| High-level input current              |  |     | 33    |     | $\mu\text{A}$ |
| Low-level input current               |  |     | -33   |     | $\mu\text{A}$ |
| Input capacitance                     |  |     | 4     |     | pF            |
| <b>DIGITAL OUTPUTS – CMOS MODE</b>    |  |     |       |     |               |
| High-level output voltage             |  |     | DRVDD |     | V             |
| Low-level output voltage              |  |     | 0     |     | V             |
| Output capacitance                    | Capacitance inside the device from each output pin to ground |     | 4     |     | pF            |
| <b>DIGITAL OUTPUTS – LVDS MODE</b>    |  |     |       |     |               |
| High-level output voltage, $V_{ODH}$  |  |     | 350   |     | mV            |
| Low-level output voltage, $V_{ODL}$   |  |     | -350  |     | mV            |
| Output common-mode voltage, $V_{OCM}$ |  |     | 1.2   |     | V             |
| Output capacitance                    | Capacitance inside the device from each output pin to ground |     | 4     |     | pF            |

(1) All LVDS and CMOS specifications are characterized, but not tested at production.

(2)  $I_O$  refers to the LVDS buffer current setting;  $R_L$  is the differential load resistance between the LVDS output pair.

## 6.11 Timing Characteristics for LVDS and CMOS Modes

Typical values are at  $25^\circ\text{C}$ ,  $AVDD = 3.3\text{ V}$ ,  $DRVDD = 3$  to  $3.6\text{ V}$ , Sampling frequency = 80 MSPS, sine wave input clock, 50% clock duty cycle,  $1.5\text{-}V_{PP}$  clock amplitude,  $C_L = 5\text{ pF}$  <sup>(1)</sup>, no internal termination,  $I_O = 3.5\text{ mA}$ ,  $R_L = 100\ \Omega$  <sup>(2)</sup> Minimum and maximum values are across the full temperature range  $T_{MIN} = -40^\circ\text{C}$  to  $T_{MAX} = 85^\circ\text{C}$ ,  $AVDD = DRVDD = 3$  to  $3.6\text{ V}$ , unless otherwise noted. <sup>(3)</sup>

|                                     |                                | MIN   | NOM | MAX  | UNIT         |               |    |
|-------------------------------------|--------------------------------|---|-----|------|--------------|---------------|----|
| $t_a$                               | Aperture delay                 | 0.5   | 1.2 | 2    | ns           |               |    |
| $t_j$                               | Aperture jitter                | Sampling frequency = 80 MSPS  |     | 90   | fs rms       |               |    |
|                                     |                                | Sampling frequency = 40 MSPS  |     | 135  | fs rms       |               |    |
|                                     | Wake-up time                   | Time to data stable <sup>(4)</sup> after coming out of STANDBY mode       |     | 60   | 200          | $\mu\text{s}$ |    |
|                                     |                                | Time to valid data after stopping and restarting the input clock          |     | 80   |              | $\mu\text{s}$ |    |
|                                     | Latency                        |   | 16  |      | Clock cycles |               |    |
| <b>DDR LVDS MODE <sup>(5)</sup></b> |                                |   |     |      |              |               |    |
|                                     | LVDS bit clock duty cycle      | 47%   | 50% | 53%  |              |               |    |
| $t_{su}$                            | Data setup time <sup>(6)</sup> | Data valid <sup>(7)</sup> to zero-crossing of CLKOUTP                     |     | 2    | 3            | ns            |    |
| $t_h$                               | Data hold time <sup>(6)</sup>  | Zero-crossing of CLKOUTP to data becoming invalid <sup>(7)</sup>          |     | 2    | 3            | ns            |    |
| $t_{PDI}$                           | Clock propagation delay        | Input clock rising edge cross-over to output clock rising edge cross-over |     | 9.5  | 11           | 12.5          | ns |
| $t_r$                               | Data rise time                 | Rise time measured from $-100\text{ mV}$ to $100\text{ mV}$               |     | 0.15 | 0.22         | 0.3           | ns |
| $t_f$                               | Data fall time                 | Fall time measured from $100\text{ mV}$ to $-100\text{ mV}$               |     | 0.15 | 0.22         | 0.3           | ns |
| $t_r$                               | Output clock rise time         | Rise time measured from $-100\text{ mV}$ to $100\text{ mV}$               |     | 0.15 | 0.22         | 0.3           | ns |

(1)  $C_L$  is the effective external single-ended load capacitance between each output pin and ground.

(2)  $I_O$  refers to the LVDS buffer current setting;  $R_L$  is the differential load resistance between the LVDS output pair.

(3) Timing parameters are ensured by design and characterization and not tested in production.

(4) Data stable is defined as the point at which the SNR is within 2 dB of the normal value.

(5) Measurements are done with a transmission line of  $100\text{-}\Omega$  characteristic impedance between the device and the load.

(6) Setup and hold time specifications take into account the effect of jitter on the output data and clock.

(7) Data valid refers to logic high of  $100\text{ mV}$  and logic low of  $-100\text{ mV}$ .

## Timing Characteristics for LVDS and CMOS Modes (continued)

Typical values are at 25°C, AVDD = 3.3 V, DRVDD = 3 to 3.6 V, Sampling frequency = 80 MSPS, sine wave input clock, 50% clock duty cycle, 1.5-V<sub>PP</sub> clock amplitude, C<sub>L</sub> = 5 pF<sup>(1)</sup>, no internal termination, I<sub>O</sub> = 3.5 mA, R<sub>L</sub> = 100 Ω<sup>(2)</sup> Minimum and maximum values are across the full temperature range T<sub>MIN</sub> = -40°C to T<sub>MAX</sub> = 85°C, AVDD = DRVDD = 3 to 3.6 V, unless otherwise noted.<sup>(3)</sup>

|                           |                                  |   | MIN  | NOM  | MAX | UNIT |
|---------------------------|----------------------------------|---|------|------|-----|------|
| t <sub>f</sub>            | Output clock fall time           | Fall time measured from 100 mV to -100 mV                         | 0.15 | 0.22 | 0.3 | ns   |
| t <sub>OE</sub>           | Output enable (OE) to data delay | Time to data valid after OE becomes active                        | 700  |      |     | ns   |
| <b>PARALLEL CMOS MODE</b> |                                  |   |      |      |     |      |
|                           | CMOS output clock duty cycle     |   | 50%  |      |     |      |
| t <sub>su</sub>           | Data setup time                  | Data valid <sup>(8)</sup> to 50% of CLKOUT rising edge            | 6.5  | 8    |     | ns   |
| t <sub>h</sub>            | Data hold time                   | 50% of CLKOUT rising edge to data becoming invalid <sup>(8)</sup> | 2    | 3    |     | ns   |
| t <sub>PDI</sub>          | Clock propagation delay          | Input clock rising edge cross-over to 50% of CLKOUT rising edge   | 6.3  | 7.8  | 9.3 | ns   |
| t <sub>r</sub>            | Data rise time                   | Rise time measured from 20% to 80% of DRVDD                       | 1    | 1.5  | 2   | ns   |
| t <sub>f</sub>            | Data fall time                   | Fall time measured from 80% to 20% of DRVDD                       | 1    | 1.5  | 2   | ns   |
| t <sub>r</sub>            | Output clock rise time           | Rise time measured from 20% to 80% of DRVDD                       | 0.7  | 1    | 1.2 | ns   |
| t <sub>f</sub>            | Output clock fall time           | Fall time measured from 80% to 20% of DRVDD                       | 1.2  | 1.5  | 1.8 | ns   |
| t <sub>OE</sub>           | Output enable (OE) to data delay | Time to data valid after OE becomes active                        | 200  |      |     | ns   |

(8) Data valid refers to logic high of 2.6 V and logic low of 0.66 V.

### 6.12 Serial Interface Timing Characteristics

Typical values at 25°C, minimum and maximum values across the full temperature range T<sub>MIN</sub> = -40°C to T<sub>MAX</sub> = 85°C, AVDD = DRVDD = 3.3 V (unless otherwise noted)

|                    |                        |  | MIN  | NOM | MAX | UNIT |
|--------------------|------------------------|--|------|-----|-----|------|
| f <sub>SCLK</sub>  | SCLK frequency         |  | > DC |     | 20  | MHz  |
| t <sub>LOADS</sub> | SEN to SCLK setup time |  | 25   |     |     | ns   |
| t <sub>LOADH</sub> | SCLK to SEN hold time  |  | 25   |     |     | ns   |
| t <sub>DSU</sub>   | SDATA setup time       |  | 25   |     |     | ns   |
| t <sub>DH</sub>    | SDATA hold time        |  | 25   |     |     | ns   |

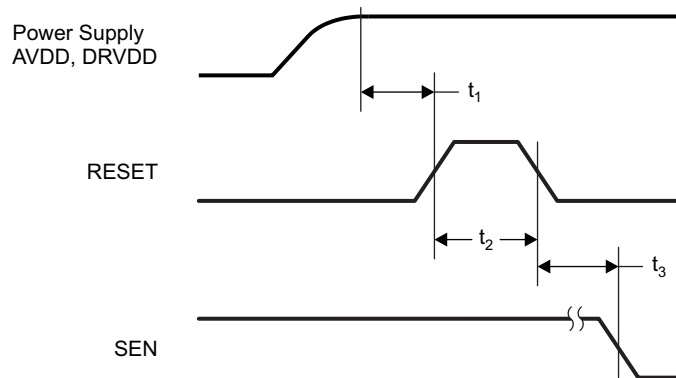
### 6.13 Reset Timing

Typical values at 25°C, minimum and maximum values across the full temperature range T<sub>MIN</sub> = -40°C to T<sub>MAX</sub> = 85°C, AVDD = DRVDD = 3.3 V (unless otherwise noted)

|                 |                      |   | MIN | NOM | MAX | UNIT |
|-----------------|----------------------|---|-----|-----|-----|------|
| t <sub>1</sub>  | Power-on delay       | Delay from power-up of AVDD and DRVDD to RESET pulse active | 5   |     |     | ms   |
| t <sub>2</sub>  | Reset pulse width    | Pulse width of active RESET signal                          | 10  |     |     | ns   |
|                 |                      |   |     |     | 1   | μs   |
| t <sub>3</sub>  | Register write delay | Delay from RESET disable to SEN active                      | 25  |     |     | ns   |
| t <sub>PO</sub> | Power-up time        | Delay from power-up of AVDD and DRVDD to output stable      |     | 6.5 |     | ms   |

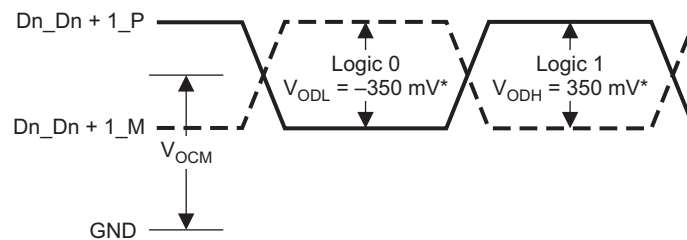
### 6.14 Timing Characteristics at Lower Sampling Frequencies

| SAMPLING FREQUENCY (MSPS) | t <sub>su</sub> , SETUP TIME (ns) |      |     | t <sub>h</sub> , HOLD TIME (ns) |     |     | t <sub>pDI</sub> , CLOCK PROPAGATION DELAY (ns) |      |      |
|---------------------------|-----------------------------------|------|-----|---------------------------------|-----|-----|---|------|------|
|                           | MIN                               | TYP  | MAX | MIN                             | TYP | MAX | MIN   | TYP  | MAX  |
| <b>DDR LVDS</b>           |                                   |      |     |                                 |     |     |   |      |      |
| 65                        | 2.7                               | 3.7  |     | 2.7                             | 3.7 |     | 11.5  | 13   | 14.5 |
| 40                        | 5                                 | 6    |     | 5                               | 6   |     | 16.5  | 18   | 19.5 |
| 20                        | 8                                 | 11   |     | 8                               | 11  |     | 30.5  | 32   | 33.5 |
| <b>PARALLEL CMOS</b>      |                                   |      |     |                                 |     |     |   |      |      |
| 65                        | 8                                 | 9.5  |     | 3                               | 4   |     | 7   | 8.5  | 10   |
| 40                        | 14                                | 15.5 |     | 6.5                             | 7.5 |     | 8   | 9.5  | 11   |
| 20                        | 14                                |      |     | 6.5                             |     |     | 5   | 10.5 | 15   |



NOTE: A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset. If the pulse is greater than 1 μs, the device could enter the parallel configuration mode briefly then return back to serial interface mode. For parallel interface operation, RESET must be tied permanently HIGH.

Figure 1. Reset Timing Diagram

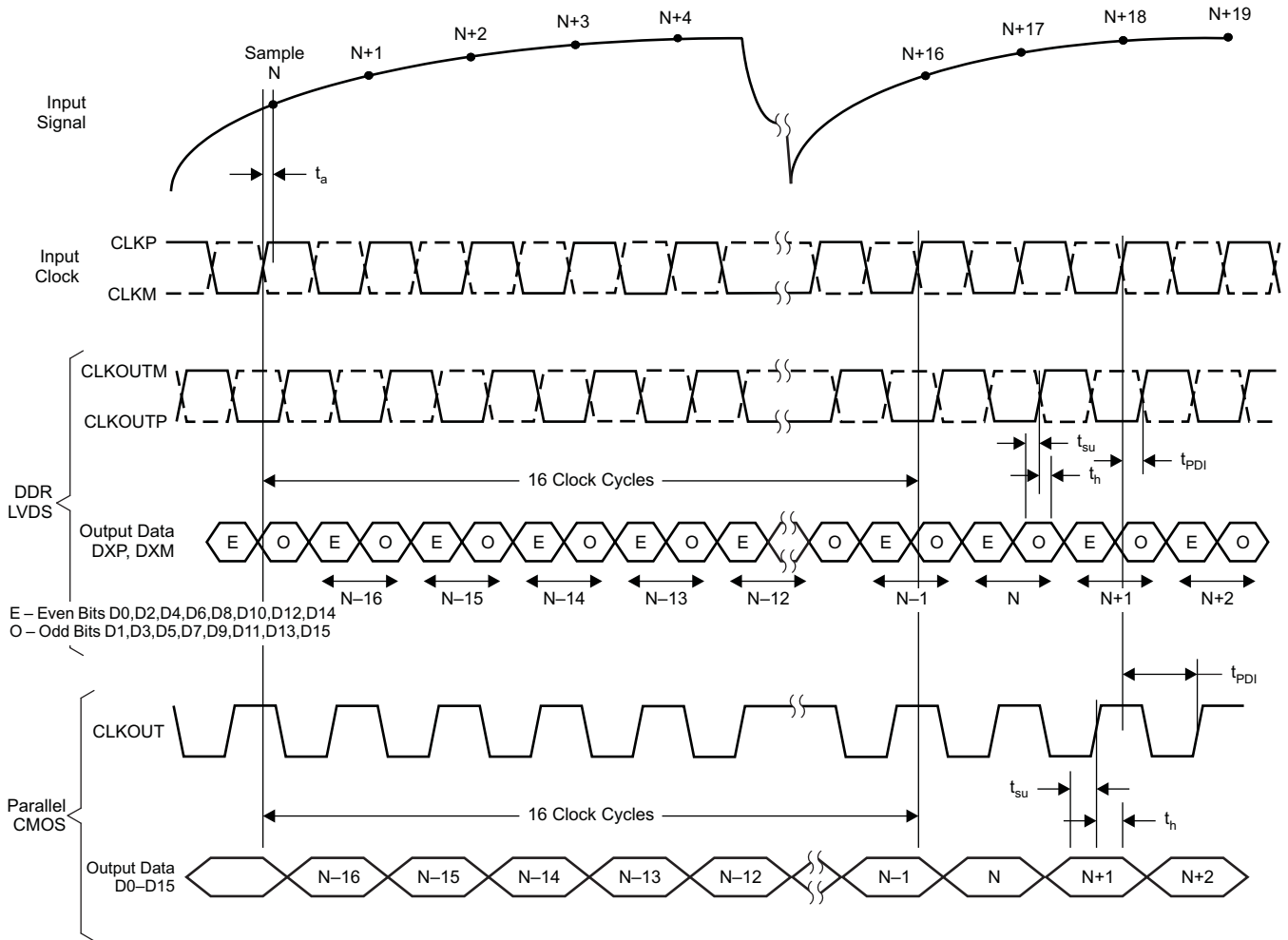


\* With external 100-Ω termination

T0334-01

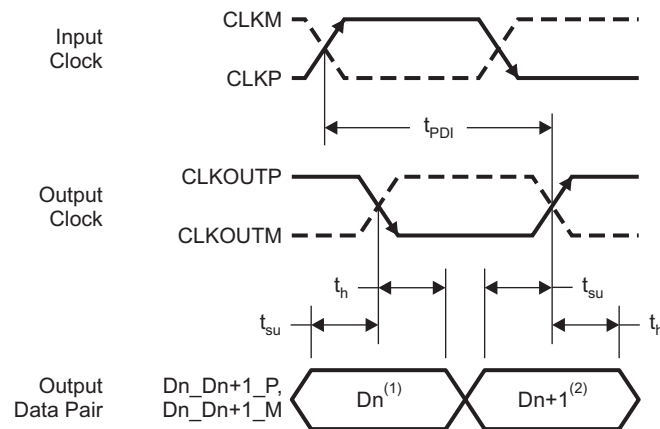
Figure 2. LVDS Output Voltage Levels





T0105-08

Figure 3. Latency

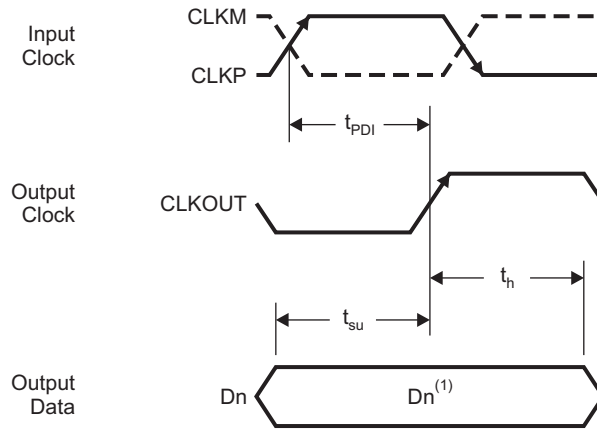


<sup>(1)</sup> Dn – Bits D0, D2, D4, D6, D8, D10, D12, D14

<sup>(2)</sup> Dn+1 – Bits D1, D3, D5, D7, D9, D11, D13, D15

T0106-06

Figure 4. LVDS Mode Timing



<sup>(1)</sup>Dn – Bits D0–D15

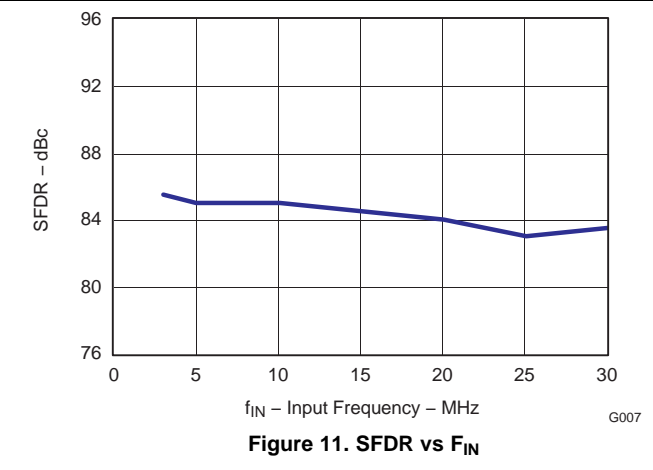
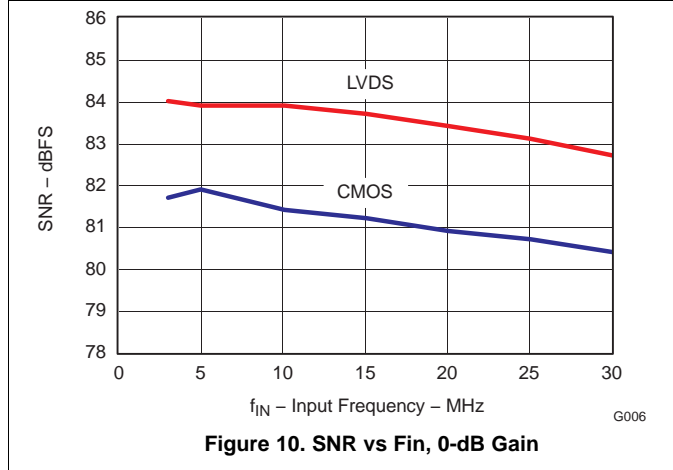
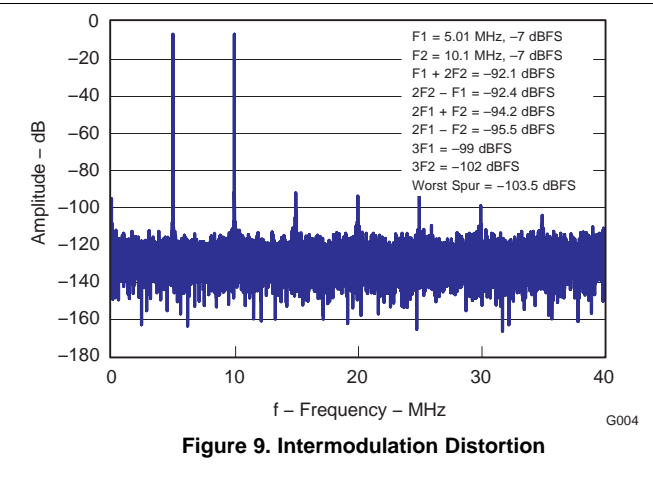
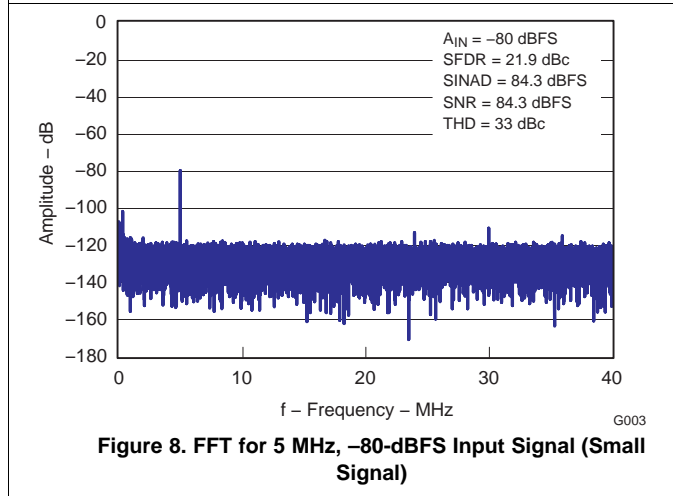
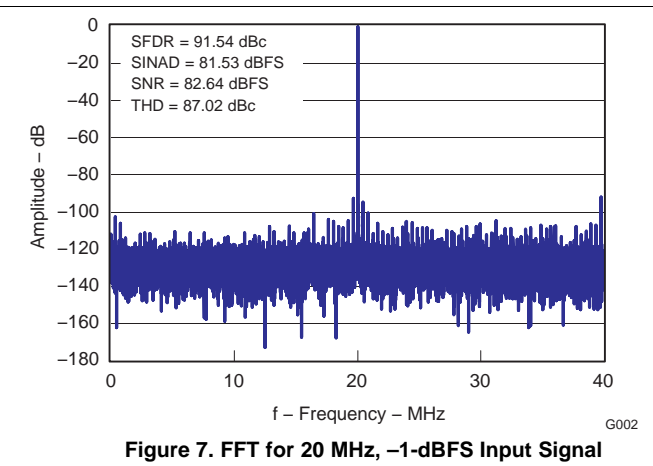
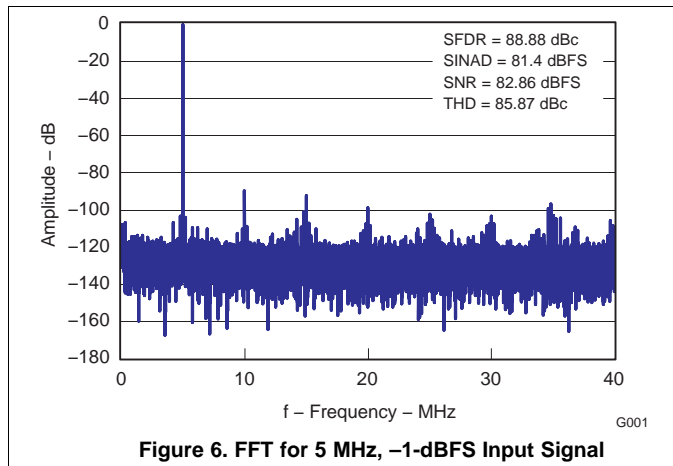
T0107-04

**Figure 5. CMOS Mode Timing**

## 6.15 Typical Characteristics

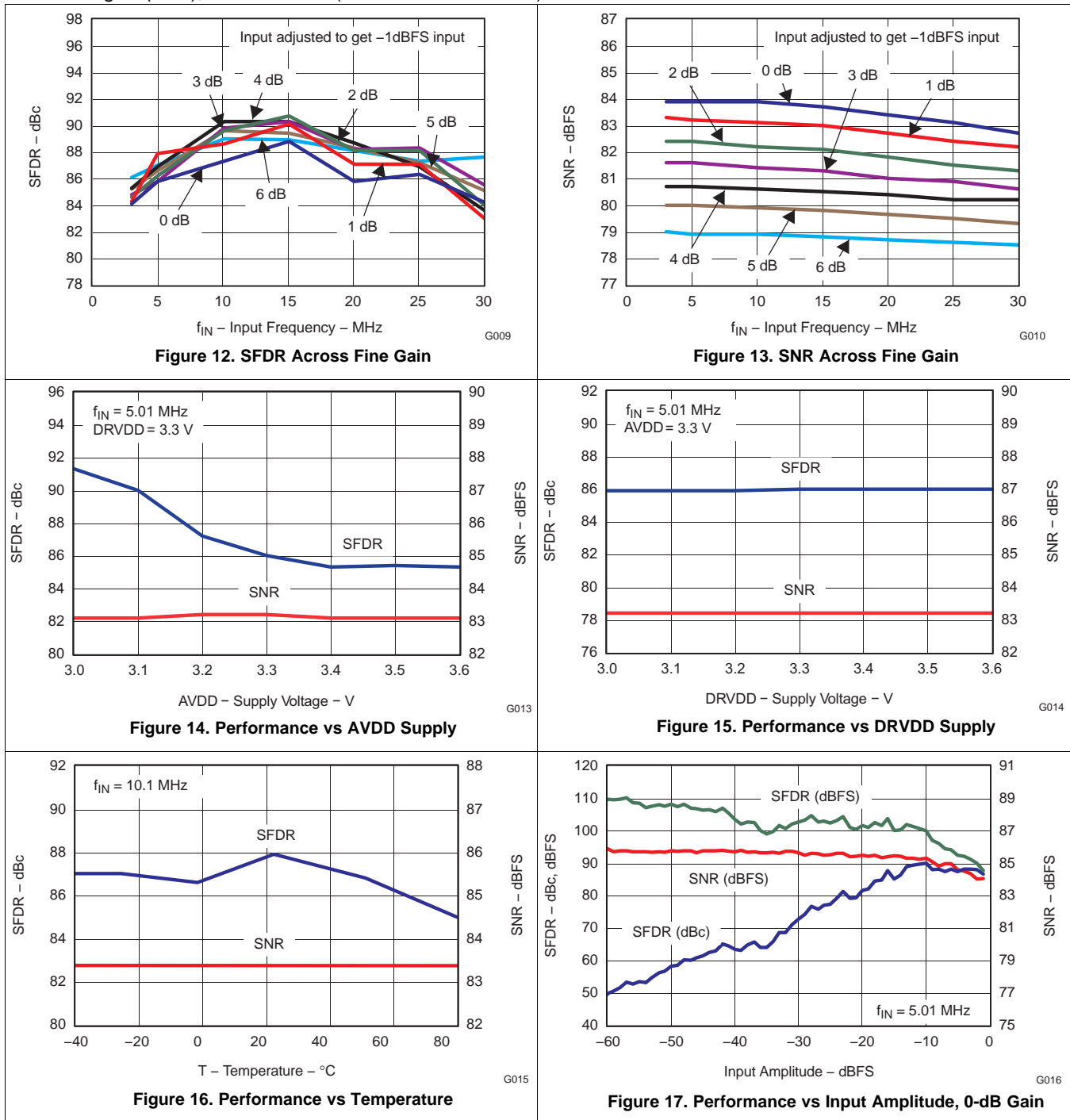
### 6.15.1 ADS5562 – 80 MSPS

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Maximum Rated, sine wave input clock, 1.5-V<sub>PP</sub> clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, internal reference mode, DDR LVDS interface, default fine gain (1 dB), 32k Point FFT (unless otherwise noted)



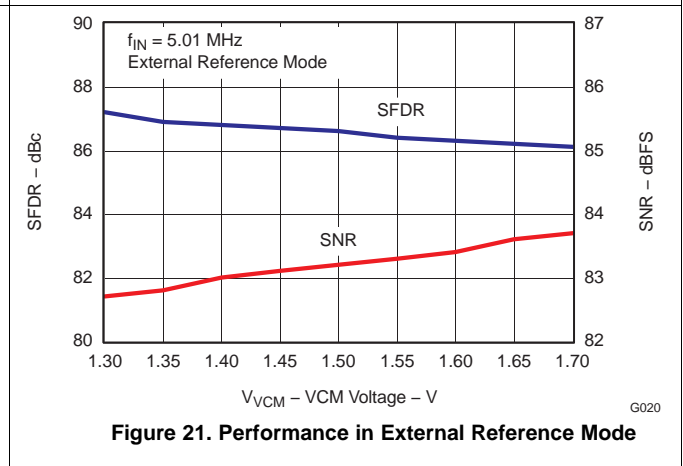
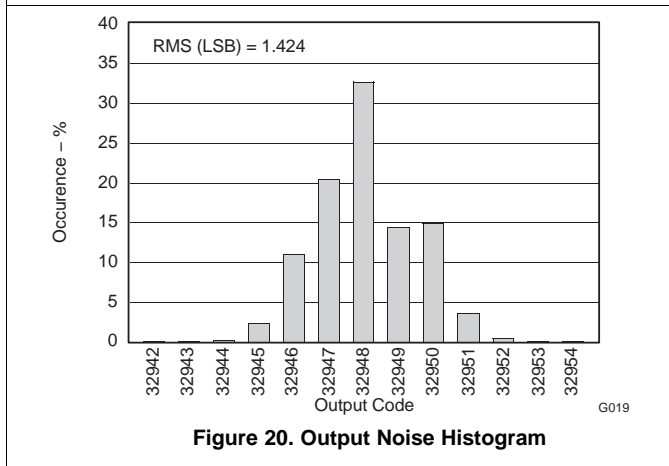
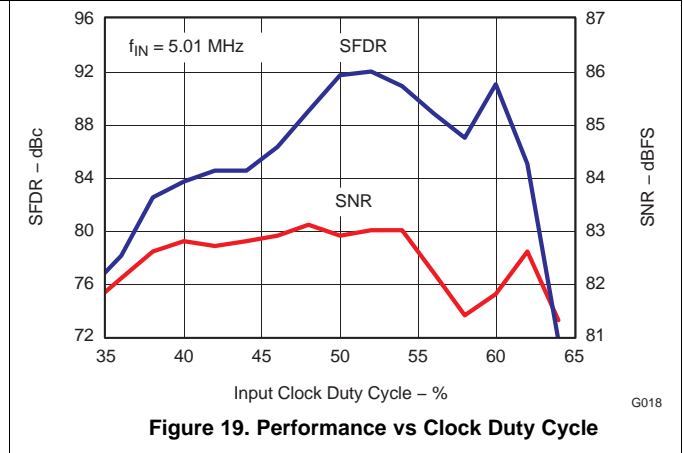
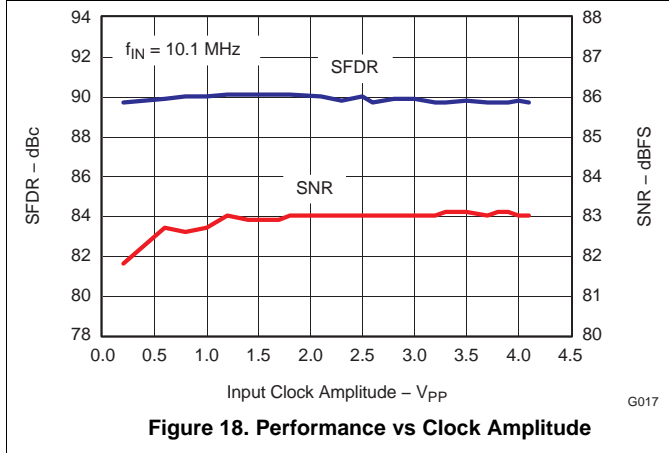
**ADS5562 – 80 MSPS (continued)**

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Maximum Rated, sine wave input clock, 1.5-V<sub>PP</sub> clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, internal reference mode, DDR LVDS interface, default fine gain (1 dB), 32k Point FFT (unless otherwise noted)



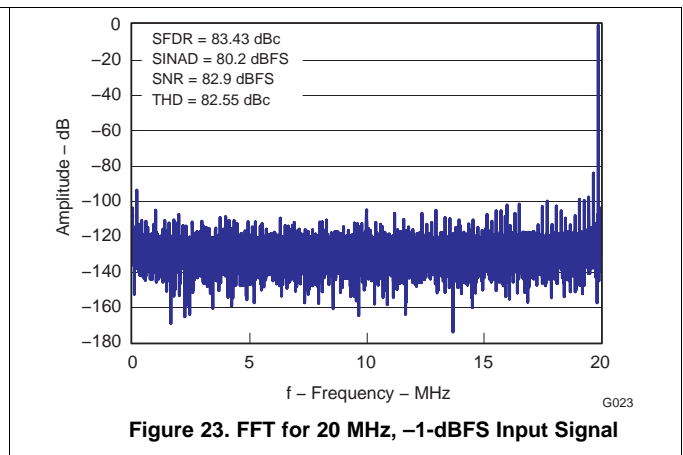
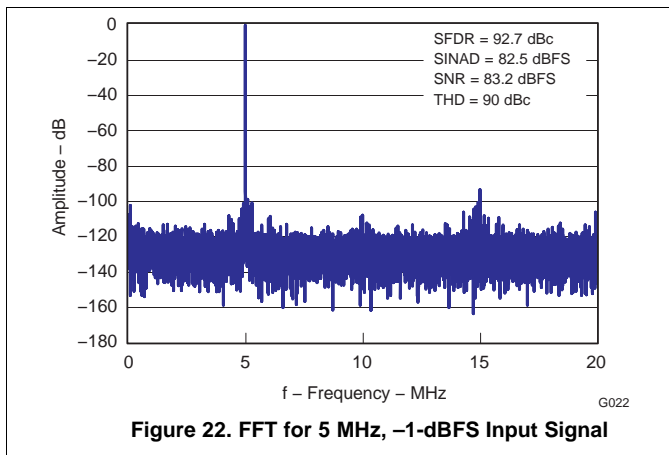
ADS5562 – 80 MSPS (continued)

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Maximum Rated, sine wave input clock, 1.5-V<sub>PP</sub> clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, internal reference mode, DDR LVDS interface, default fine gain (1 dB), 32k Point FFT (unless otherwise noted)



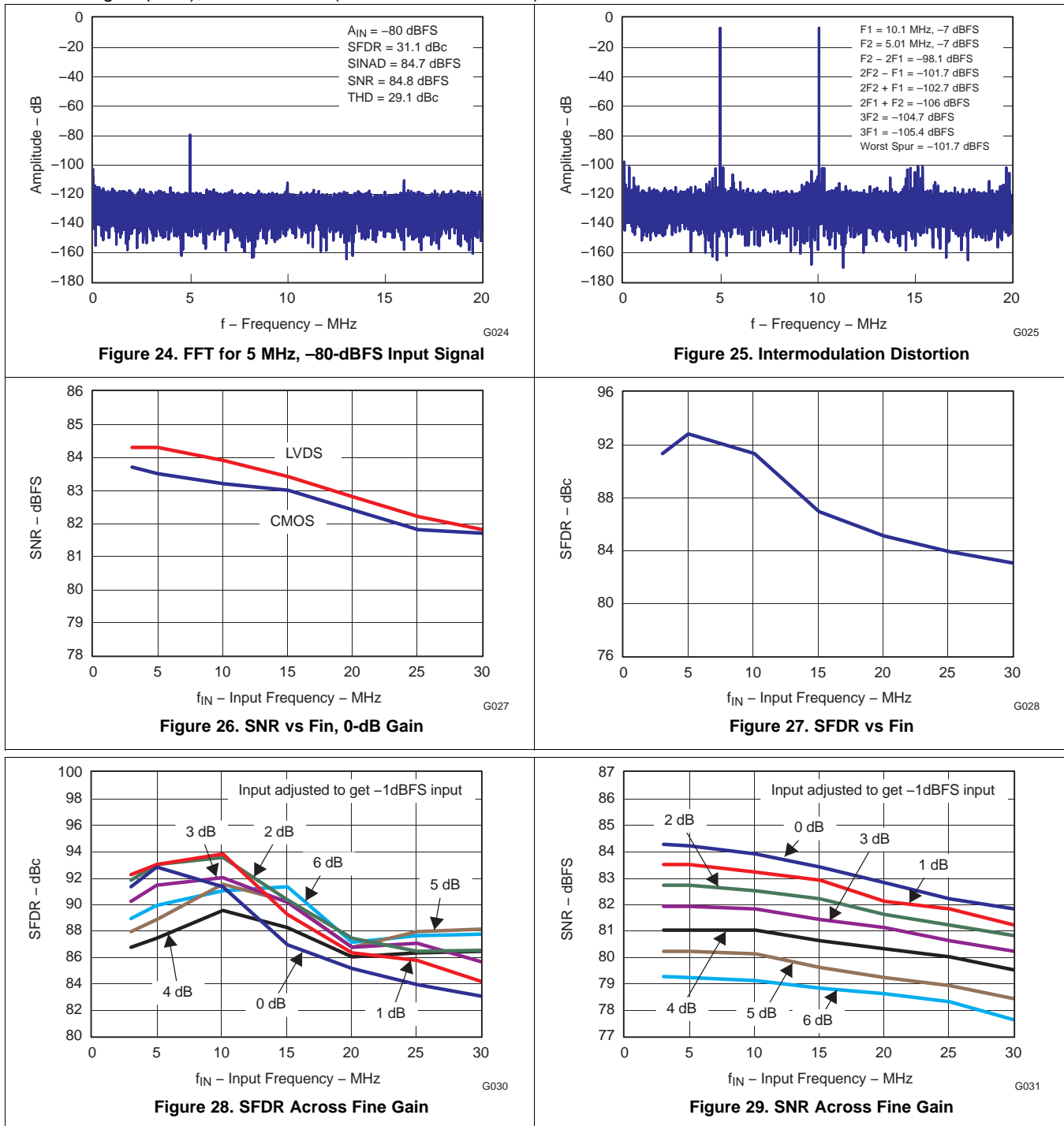
6.15.2 ADS5560 – 40 MSPS

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Maximum Rated, sine wave input clock, 1.5-V<sub>PP</sub> clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, internal reference mode, DDR LVDS interface, default fine gain (1 dB), 32k Point FFT (unless otherwise noted)



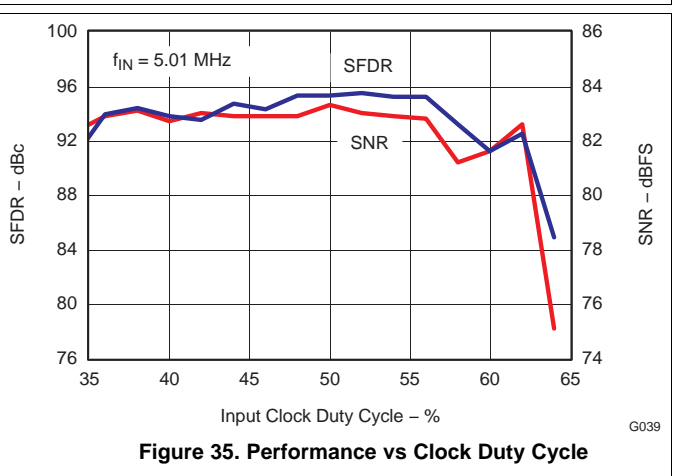
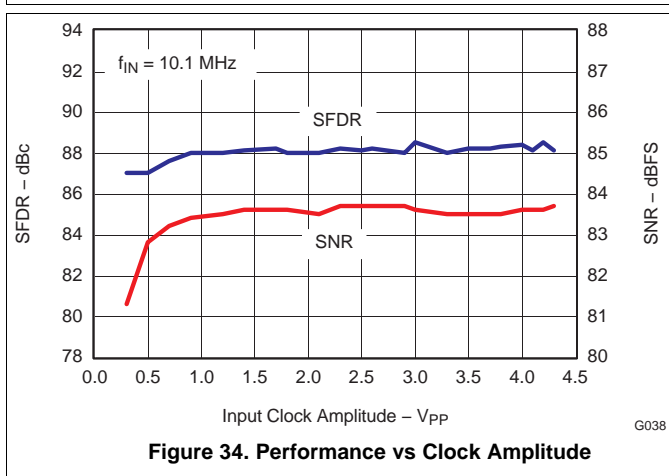
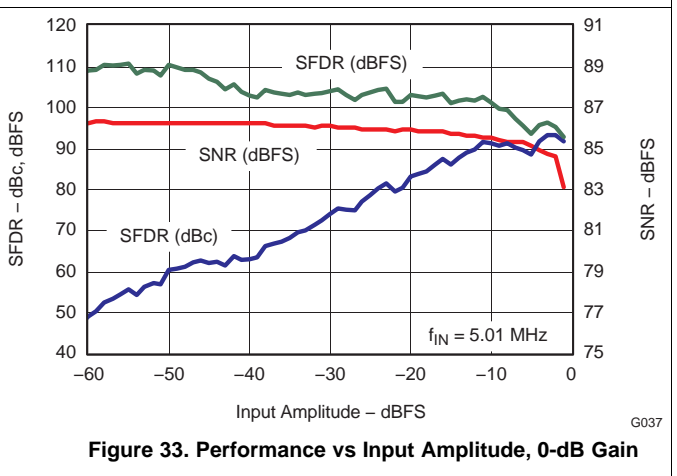
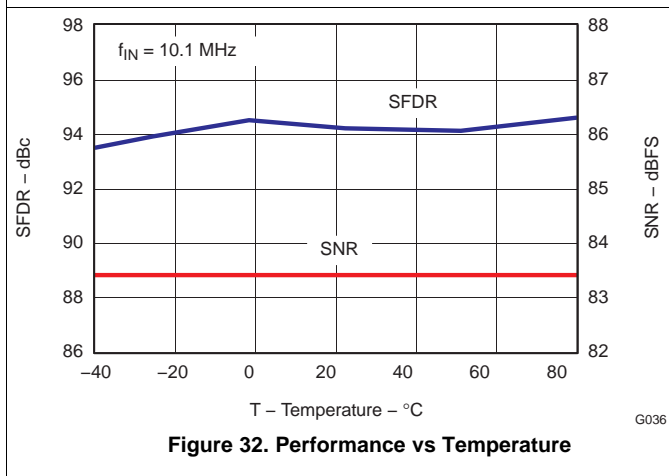
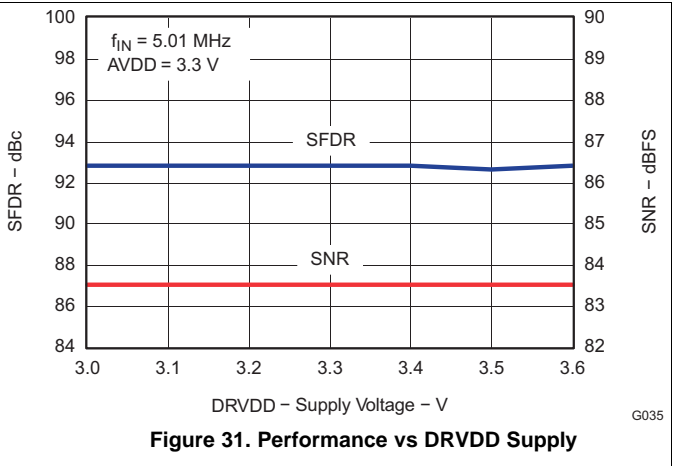
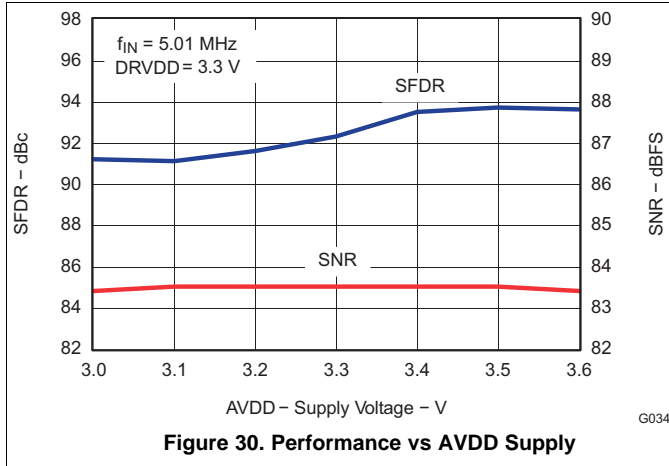
**ADS5560 – 40 MSPS (continued)**

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Maximum Rated, sine wave input clock, 1.5-V<sub>PP</sub> clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, internal reference mode, DDR LVDS interface, default fine gain (1 dB), 32k Point FFT (unless otherwise noted)



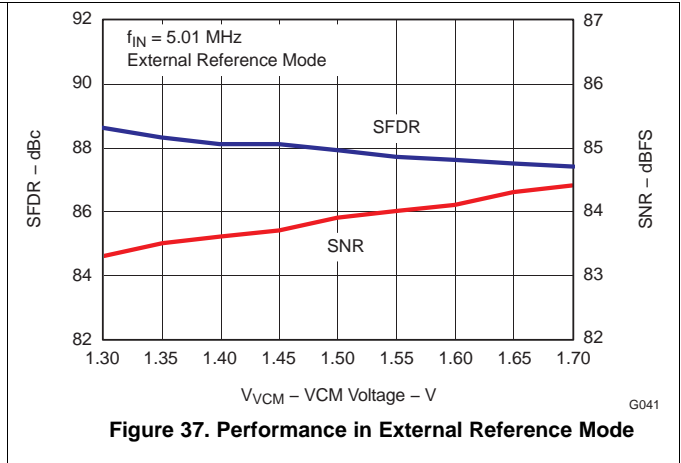
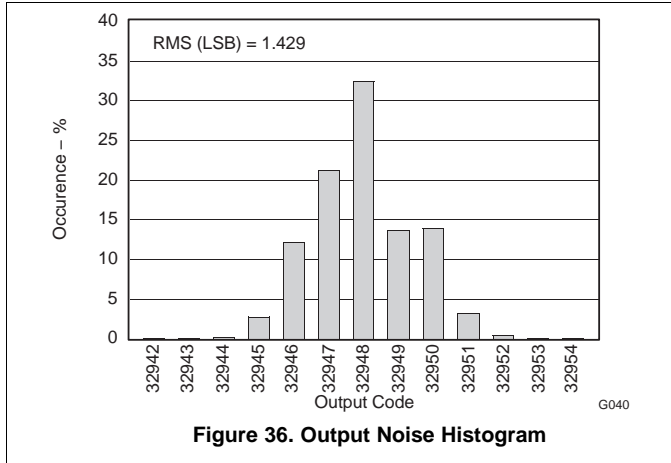
ADS5560 – 40 MSPS (continued)

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Maximum Rated, sine wave input clock, 1.5-V<sub>PP</sub> clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, internal reference mode, DDR LVDS interface, default fine gain (1 dB), 32k Point FFT (unless otherwise noted)



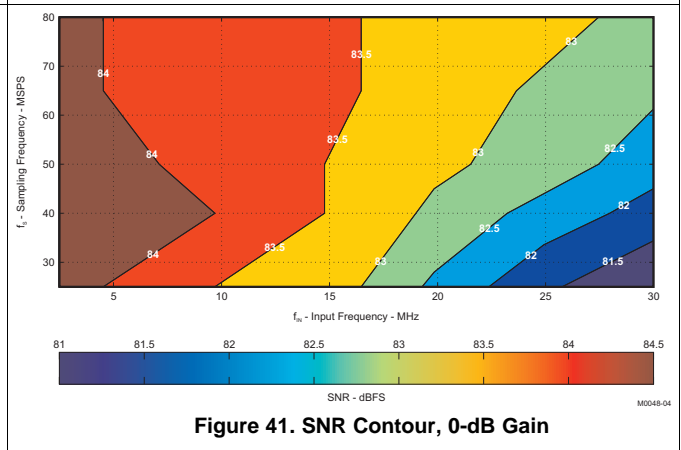
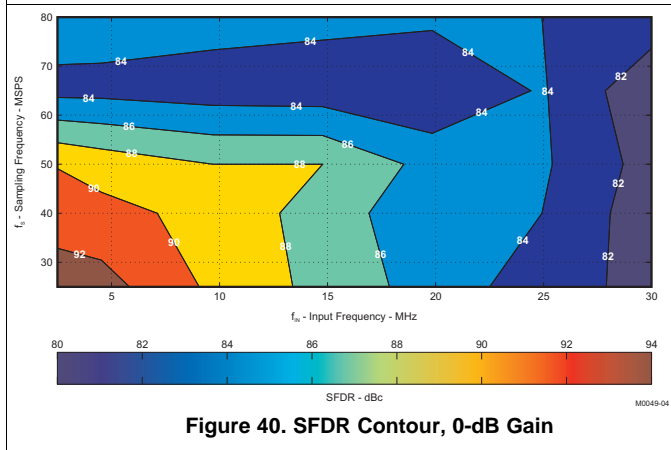
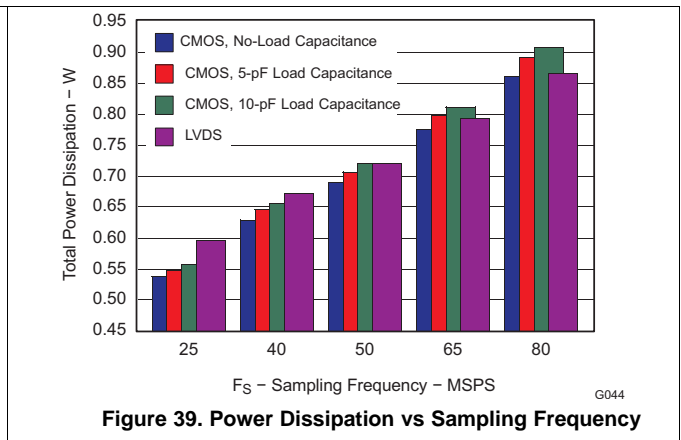
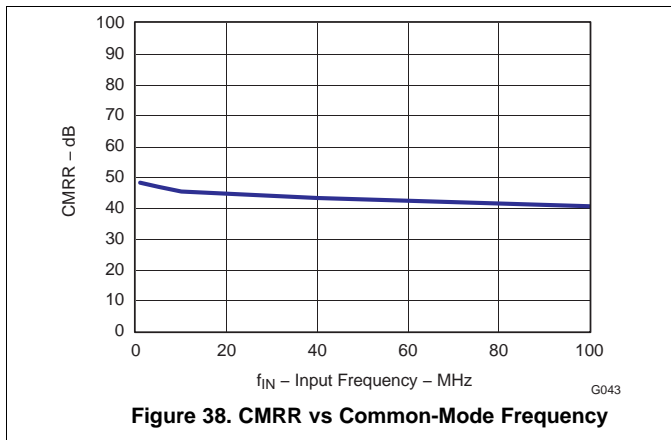
**ADS5560 – 40 MSPS (continued)**

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Maximum Rated, sine wave input clock, 1.5-V<sub>PP</sub> clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, internal reference mode, DDR LVDS interface, default fine gain (1 dB), 32k Point FFT (unless otherwise noted)



**6.15.3 Valid Up to Max Clock Rate (ADS5562 or ADS5560)**

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, sampling frequency = Maximum Rated, sine wave input clock, 1.5-V<sub>PP</sub> clock amplitude, 50% clock duty cycle, -1-dBFS differential analog input, internal reference mode, DDR LVDS interface, default fine gain (1 dB), 32k Point FFT (unless otherwise noted)



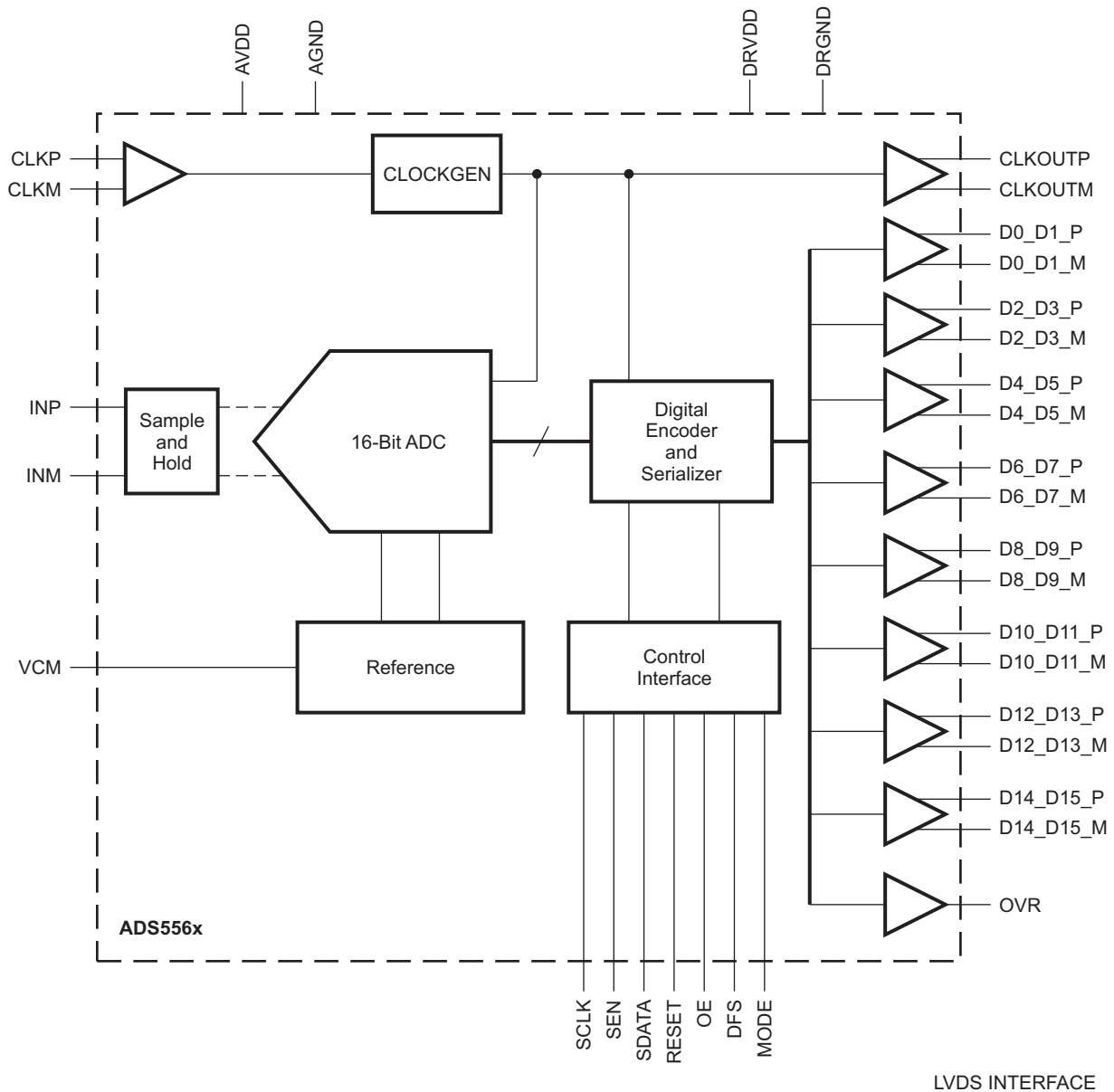


## 7 Detailed Description

### 7.1 Overview

The ADS556x device is a high-performance 16-bit ADC family with sampling rates up to 80 MSPS. The device is based on switched capacitor technology and runs off a single 3.3-V supply. When the signal is captured by the input sample and hold, the input sample is sequentially converted by a series of small resolution stages. At every clock edge, the sample propagates through the pipeline resulting in a data latency of 16 clock cycles. The output is available as 16-bit data, in DDR LVDS or parallel CMOS and coded in either offset binary or binary 2s-complement format.

### 7.2 Functional Block Diagram

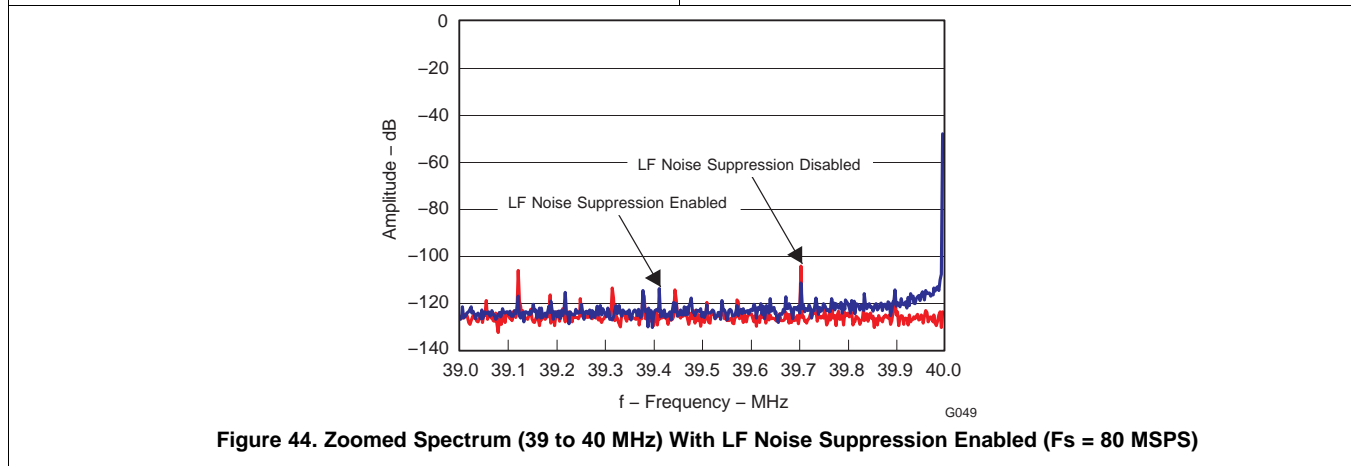
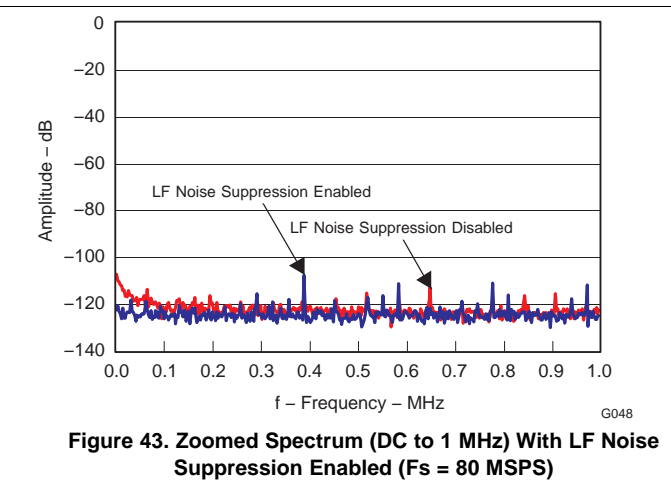
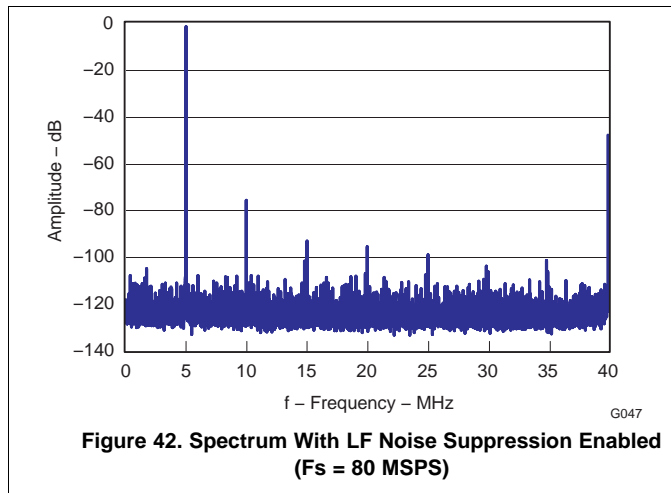


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## 7.3 Feature Description

### 7.3.1 Low-Frequency Noise Suppression

The low-frequency noise suppression mode is specifically useful in applications where good noise performance is desired in the low-frequency band of DC to 1 MHz. Setting this mode shifts the low-frequency noise of the ADS556x device to approximately  $(F_s / 2)$ , thereby moving the noise floor around DC to a much lower value. The <LF NOISE SUPPRESSION> register bit enables this mode. As Figure 43 shows, when the mode is enabled, the noise floor from DC to 1 MHz improves significantly. The low-frequency noise components get shifted to the region around  $F_s / 2$  (Figure 44).



## Feature Description (continued)

### 7.3.2 Analog Input Circuit

The analog input consists of a switched-capacitor based differential sample and hold architecture as shown in Figure 45.

This differential topology results in good AC performance even for high input frequencies at high sampling rates. The INP and INM pins must be externally biased around a common-mode voltage of 1.5 V (VCM). For a full-scale differential input, each input pin (INP and INM) must swing symmetrically between  $V_{CM} + 0.9\text{ V}$  and  $V_{CM} - 0.9\text{ V}$ , resulting in a 3.6-V<sub>PP</sub> differential input swing.

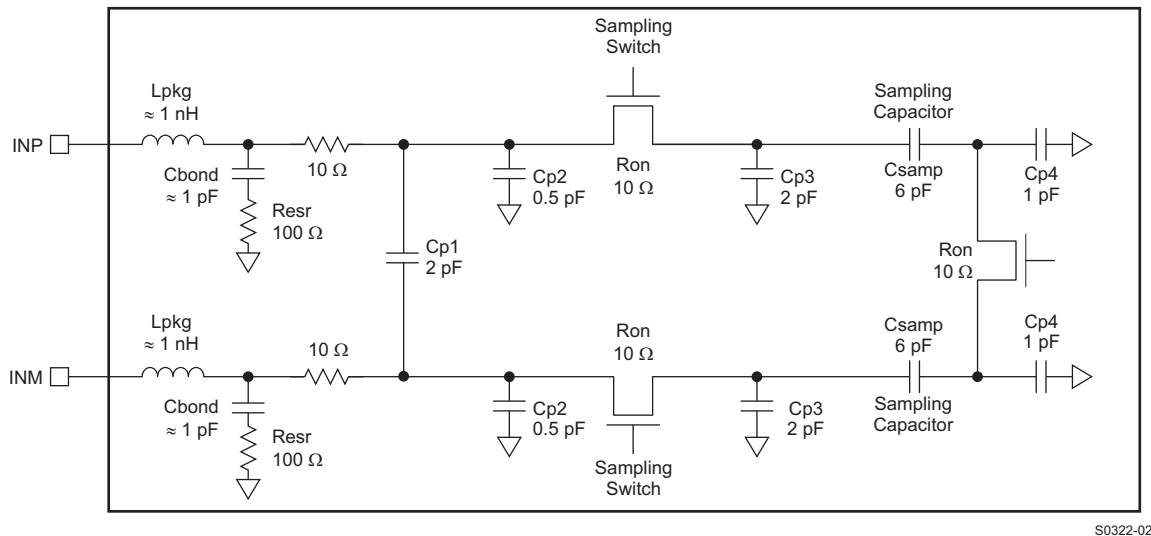


Figure 45. Input Stage

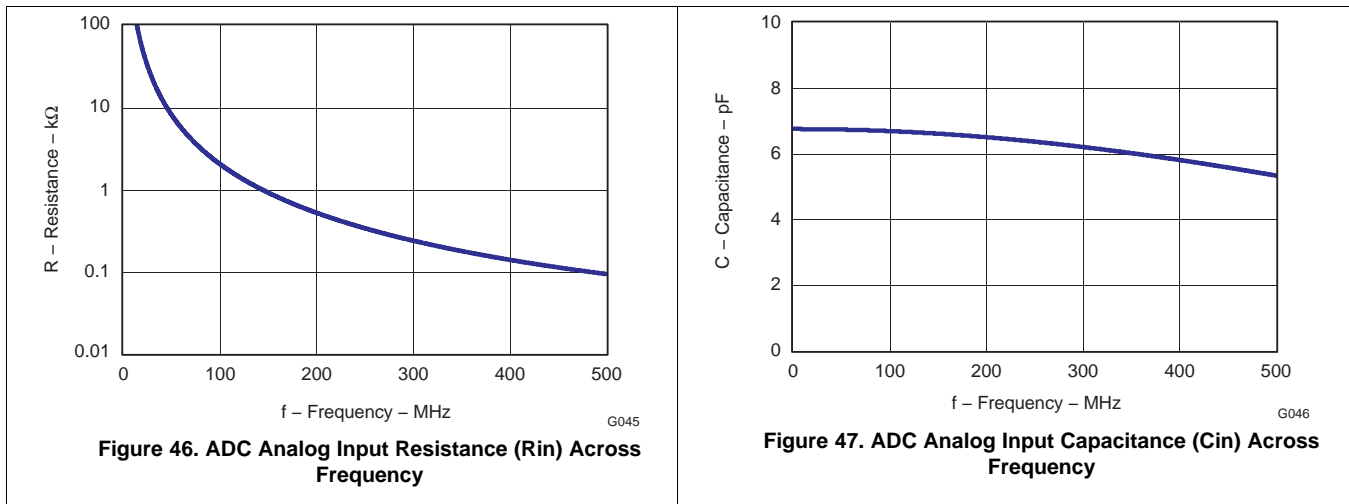
#### 7.3.2.1 Drive Circuit Recommendations

For optimum performance, the analog inputs must be driven differentially which improves the common-mode noise immunity and even-order harmonic rejection. A resistor in series with each input pin (about 15 Ω) is recommended to damp out ringing caused by package parasitics. Low impedance (< 50 Ω) is required for the common-mode switching currents which can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM).

The device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the glitches caused by the opening and closing of the sampling capacitors. The filtering of the glitches can be improved further using an external R-C-R filter.

In addition to the previously listed requirements, the drive circuit may must be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While doing this, the ADC input impedance (Zin = Rin || Cin) looking into the ADC input pins.

Feature Description (continued)



7.3.2.2 Example Driving Circuit

Figure 48 shows an example input configuration using RF transformers. In this example, an external R-C-R filter using a 22-pF capacitor has been used. Together with the series inductor (39 nH), this combination forms a filter and absorbs the sampling glitches. Because of the relatively large capacitor (22 pF) in the R-C-R and the 15-Ω resistors in series with each input pin, this drive circuit has low bandwidth and is suited for low input frequencies.

The drive circuit has been terminated by 50 Ω near the ADC side. The termination is accomplished by a 25-Ω resistor from each input to the 1.5-V common-mode (VCM) from the device. This allows the analog inputs to be biased around the required common-mode voltage.

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back to back helps minimize this mismatch and good performance is obtained for high frequency input signals. An additional termination resistor pair may be required between the two transformers (enclosed by the dashed lines in Figure 48). The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side must be chosen to get an effective 50 Ω (in the case of 50-Ω source impedance).

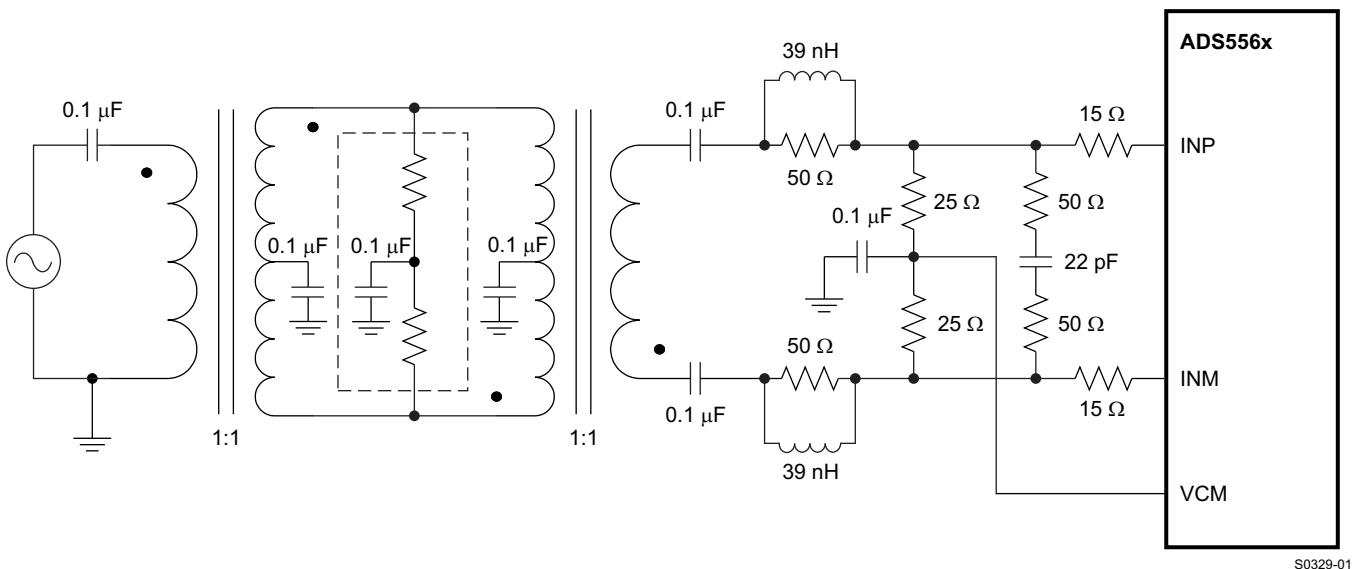


Figure 48. Drive Circuit Using RF Transformers

## Feature Description (continued)

### 7.3.2.3 Input Common-Mode

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1- $\mu$ F low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. Each input pin of the ADC sinks a common-mode current in the order of 6 $\mu$ A/MSPS (about 1mA at 80 MSPS) from the external drive circuit.

### 7.3.2.4 Programmable Fine Gain

ADS556x has programmable fine gain from 0 dB to 6dB in steps of 1 dB. The corresponding full-scale input range varies from 3.6  $V_{PP}$  down to 2  $V_{PP}$ . The fine gain is useful, when lower full-scale input ranges are used to get SFDR improvement (See [Figure 11](#) and [Figure 27](#)). This is accompanied by corresponding degradation in SNR (see [Figure 12](#) and [Figure 28](#)). The gain can be programmed using the register bits **GAIN** ([Table 14](#)).

After reset, the device is initialized to 1 dB fine gain when configured as Serial Interface Mode. The gain of the device in Parallel Mode will depend on the voltage applied on the SCLK pin. See [Table 4](#) for details.

**Table 1. Full-scale Input Range Across Gains (Serial Interface Mode)**

| GAIN (dB)              | CORRESPONDING FULL-SCALE INPUT RANGE ( $V_{PP}$ ) |
|------------------------|---|
| 0                      | 3.56 <sup>(1)</sup>                               |
| 1, default after reset | 3.56  |
| 2                      | 3.2   |
| 3                      | 2.85  |
| 4                      | 2.55  |
| 5                      | 2.27  |
| 6                      | 2   |

(1) With 0 dB gain, the full-scale input range continues to be 3.56  $V_{PP}$ . This means that the output code range will be 58409 LSBs (or 1 dB below 65536).

## 7.4 Device Functional Modes

### 7.4.1 Low Sampling Frequency Operation

For best performance at high sampling frequencies, the ADS556x device uses a clock generator circuit to derive internal timing for the ADC. The clock generator operates from 80 MSPS down to 25 MSPS in the DEFAULT SPEED mode. The ADC enters this mode after applying reset (with serial interface configuration) or by tying SCLK pin to low (with parallel configuration).

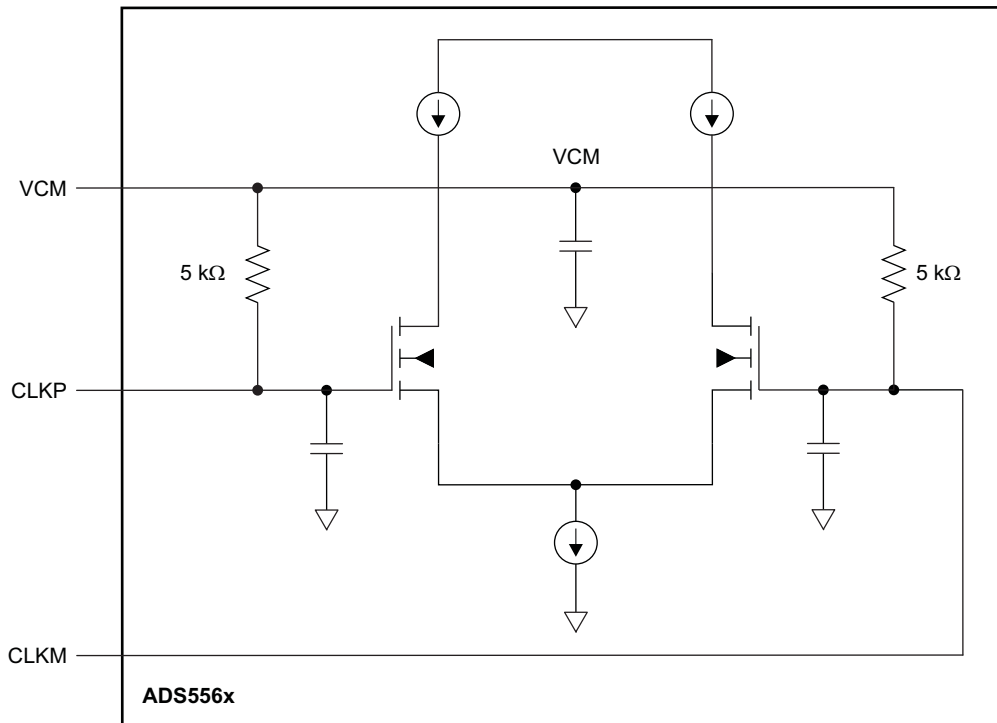
For low sampling frequencies (below 25 MSPS), the ADC must be put in the LOW SPEED mode. This mode can be entered by one of the following:

- Setting the <LOW SPEED> register bit ([Table 12](#)) through the serial interface
- Tying the SCLK pin to high (see [Table 4](#)) using the parallel configuration

**Device Functional Modes (continued)**

**7.4.2 Clock Input**

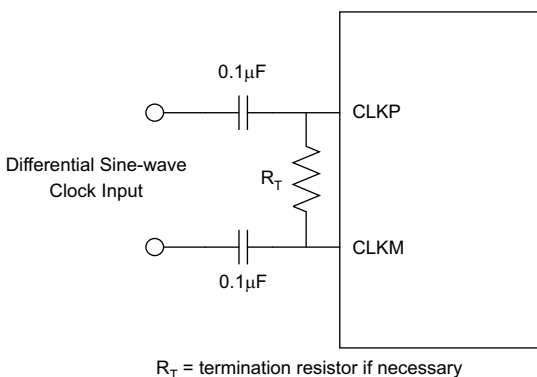
The ADS556x clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors that connect the CLKP and CLKM pins to the VCM pin, as shown in Figure 49. This connection allows using transformer-coupled drive circuits for sine wave clock or AC-coupling for LVPECL, LVDS, and LVCMOS clock sources (Figure 50, Figure 51, Figure 52, and Figure 53).



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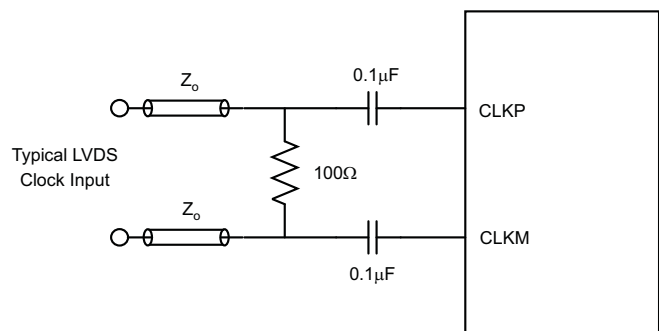
**Figure 49. Clock Inputs**

For best performance, the clock inputs must be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends to use a clock source with very low jitter. Bandpass filtering of the clock source can help reduce the effect of jitter. No change in performance occurs with a non-50% duty cycle clock input. Single-ended CMOS clock can be AC-coupled to the CLKP input, with CLKM connected to ground with 0.1-μF capacitor, as shown in Figure 53.



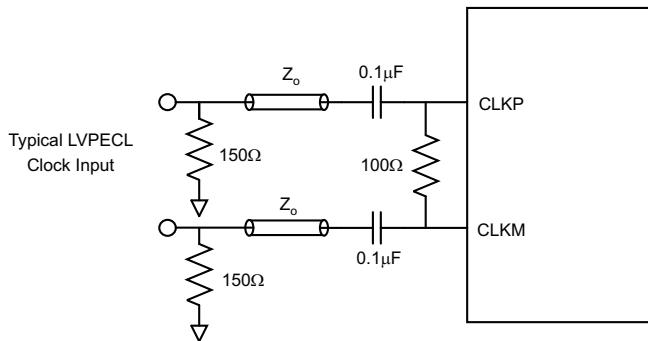
$R_T$  = termination resistor if necessary

**Figure 50. Differential Sine-Wave Clock Driving Circuit**

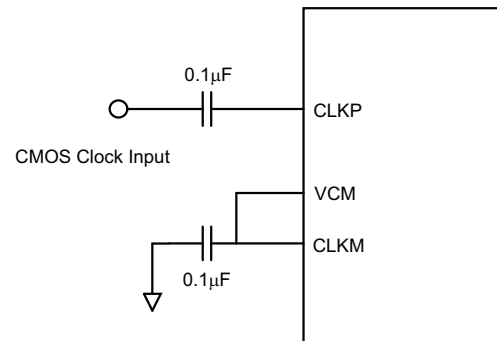


**Figure 51. Typical LVDS Clock Driving Circuit**

## Device Functional Modes (continued)



**Figure 52. Typical LVPECL Clock Driving Circuit**



**Figure 53. Typical LVCMOS Clock Driving Circuit**

For high input frequency sampling, TI recommends using a clock source with very low jitter. Bandpass filtering of the clock source can help reduce the effect of jitter. A small change in performance occurs with a non-50% duty cycle clock input.

### 7.4.2.1 Power-Down

The ADS556x device has three power-down modes: global STANDBY, output buffer disabled, and input clock stopped.

#### 7.4.2.1.1 Global STANDBY

This mode can be initiated by controlling SDATA or by setting the <STBY> register bit through the serial interface. In this mode, the ADC, reference block and the output buffers are powered down resulting in reduced total power dissipation of about 155 mW. The wake-up time from global power-down to valid data is typically 60 μs.

#### 7.4.2.1.2 Output Buffer Disable

The output buffers can be disabled using the OE pin in both the LVDS and CMOS modes. With the buffers disabled, the digital outputs are in the tri-state. The wake-up time from this mode to data becoming valid in normal mode is typically 700 ns in LVDS mode and 200 ns in CMOS mode.

#### 7.4.2.1.3 Input Clock Stop

The converter enters this mode when the input clock frequency falls below 1 MSPS. The power dissipation is about 125 mW and the wake-up time from this mode to data becoming valid in normal mode is typically 80 μs.

### 7.4.2.2 Power Supply Sequence

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated inside the device. Externally, the supplies can be driven from separate supplies or from a single supply.

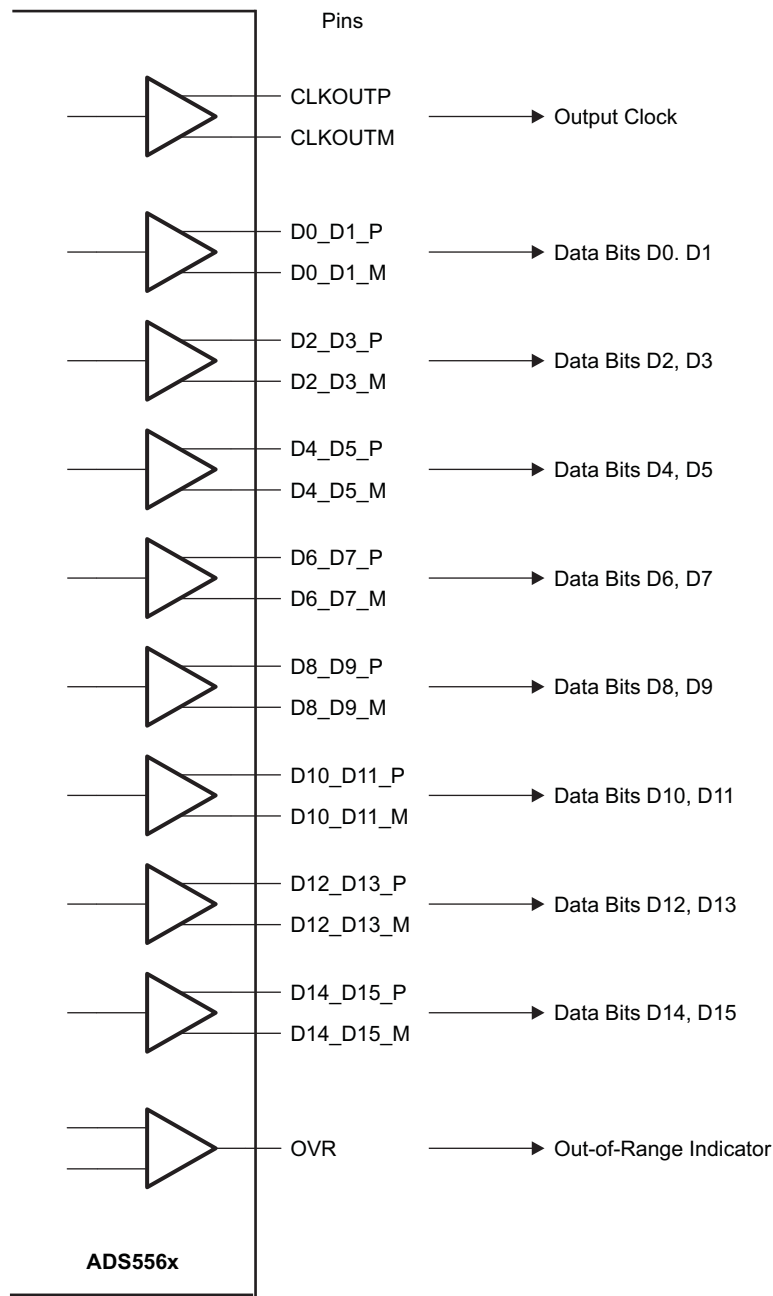
### 7.4.3 Output Interface

The ADS556x device provides 16-bit data, an output clock synchronized with the data, and an out-of-range indicator that goes high when the output reaches the full-scale limits. In addition, output enable control (OE) is provided to power-down the output buffers and put the outputs in high-impedance state.

Two output interface options are available: Double Data Rate (DDR) LVDS and parallel CMOS. These options are selected using the DFS or the serial-interface <ODI> register bit (see [Table 7](#)).

**Device Functional Modes (continued)**
**7.4.3.1 DDR LVDS Outputs**

In this mode, the 16 data bits and the output clock are put out using LVDS (low voltage differential signal) levels. Two successive data bits are multiplexed and output on each LVDS differential pair as shown in [Figure 54](#). Therefore, 8 LVDS output pairs are available for the data bits and 1 LVDS output pair for the output clock.



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**Figure 54. DDR LVDS Outputs**



### Device Functional Modes (continued)

Even data bits (D0, D2 through D14) are output at the falling edge of CLKOUTP and the odd data bits (D1, D3 through D15) are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP must be used to capture all the data bits (see Figure 55).

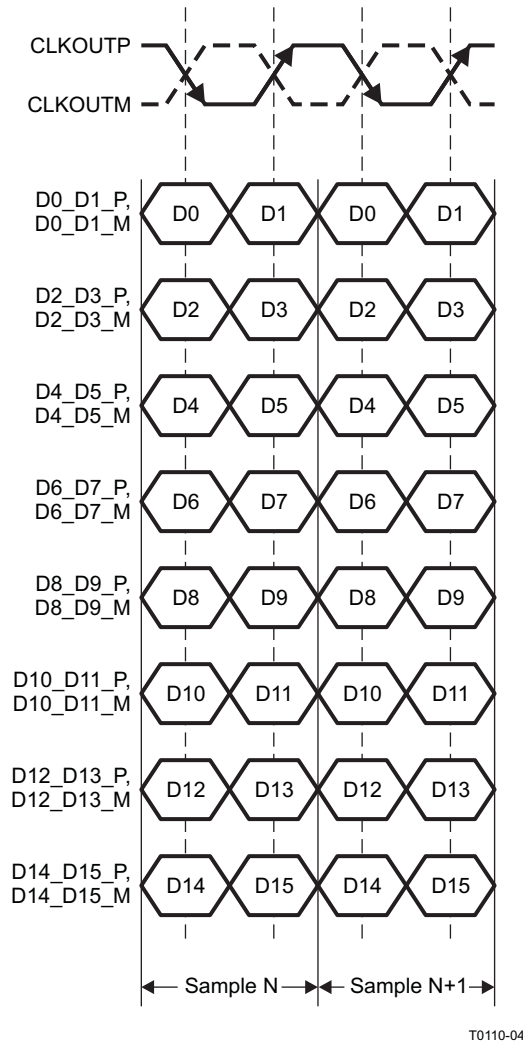


Figure 55. DDR LVDS Interface

#### 7.4.3.2 LVDS Buffer Current Programmability

The default LVDS buffer output current is 3.5 mA. Terminating the buffer current by 100  $\Omega$  results in logic HIGH of 350 mV and logic LOW of -350 mV. The LVDS buffer currents can also be programmed to 2.5 mA, 4.5 mA, and 1.95 mA using the serial interface. In addition, a current double mode exists in which this current is doubled for the data and output clock buffers.

Both the buffer current programming and the current double mode can be done separately for the data buffers and the output clock buffer (<LVDS CURR> register bits).

## Device Functional Modes (continued)

### 7.4.3.3 LVDS Buffer Internal Termination

An internal termination option is available (using the serial interface), by which the LVDS buffers are differentially terminated inside the device. These termination resistances are available: 325, 200, and 175  $\Omega$  (nominal with  $\pm 20\%$  variation). Any combination of these three terminations can be programmed; the effective termination will be the parallel combination of the selected resistances. This results in eight effective terminations from open (no termination) to 75  $\Omega$ .

The internal termination helps to absorb any reflections coming from the receiver end, improving the signal integrity. With 100- $\Omega$  internal and 100- $\Omega$  external termination, the voltage swing at the receiver end is halved (compared to no internal termination). The terminations can be controlled using the <DATA TERM> and <CLKOUT TERM> register bits.

The voltage swing can be restored by using the LVDS current double mode (<CURR DOUBLE> register bit).

### 7.4.3.4 Parallel CMOS

In this mode, the digital data and output clock are put out as 3.3-V CMOS voltage levels. Each data bit and the output clock is available on a separate pin in parallel. By default, the data outputs are valid during the rising edge of the output clock. The output clock is CLKOUT.

### 7.4.3.5 Output Clock Position Programmability

In both the LVDS and CMOS modes, the output clock can be moved around the default position which occurs using the SEN pin (as described in [Table 6](#)) or using the serial-interface <CLKOUT POSN> register bits ([Table 11](#)).

## 7.4.4 Output Data Format

Two output data formats are supported: 2s-complement and offset binary. These formats can be selected using the DFS pin or the serial-interface <DFS> register bit (see [Table 9](#)). In the event of an input voltage overdrive, the digital outputs go to the appropriate full scale level. For a positive overdrive, the output code is 0xFFFF in offset binary output format, and 0x7FFF in 2s-complement output format. For a negative input overdrive, the output code is 0x0000 in offset binary output format and 0x8000 in 2s complement output format.

## 7.4.5 Reference

The ADS556x device has a built-in internal reference that does not require external components. Design schemes are used to linearize the converter load seen by the reference; this and the integration of the requisite reference capacitors on-chip eliminates the need for external decoupling capacitors. The full-scale input range of the converter can be controlled in the external reference mode as explained in the [External Reference](#) section. The internal or external reference modes can be selected by controlling the MODE pin 23 (see [Table 8](#) for details) or by programming the serial-interface <REF> register bit.

### 7.4.5.1 Internal Reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. The common-mode voltage (1.5 V nominal) is output on VCM pin, which can be used to externally bias the analog input pins.

### 7.4.5.2 External Reference

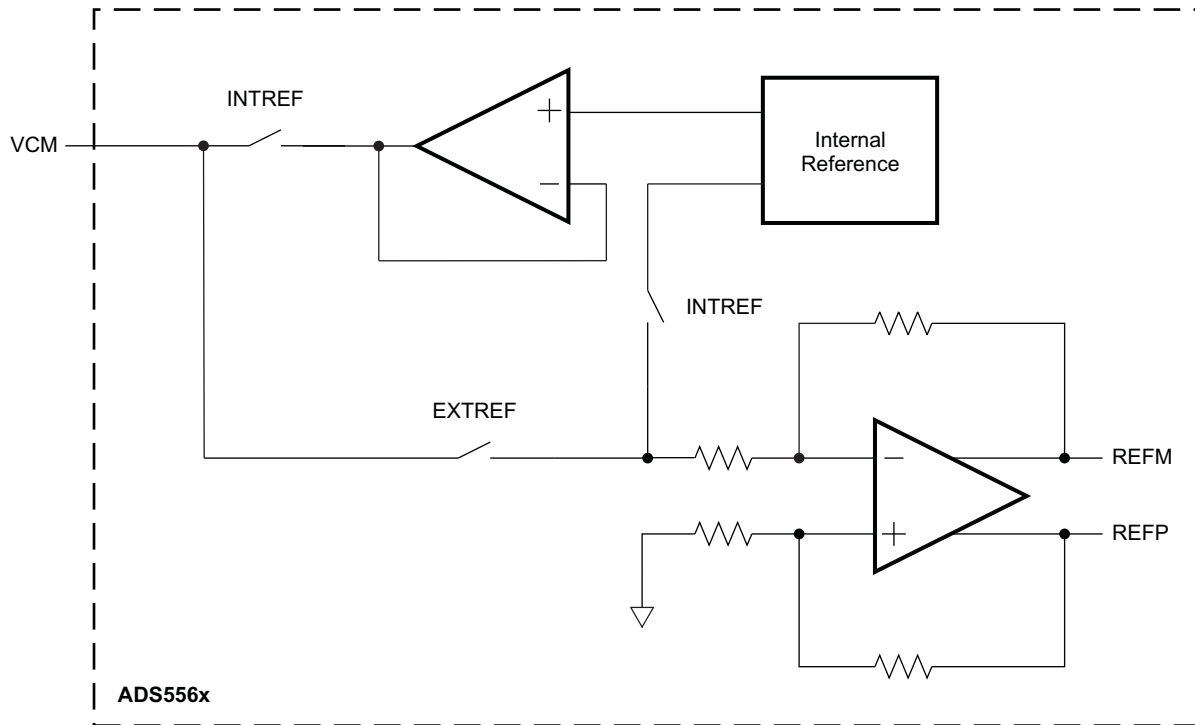
When the device is in external reference mode, the VCM acts as a reference input pin. The voltage forced on the VCM pin is buffered and gained internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given by [Equation 1](#). In this mode, the 1.5-V common-mode voltage to bias the input pins must be generated externally.

Full-scale differential input voltage,  $pp = (\text{Voltage forced on VCM pin}) \times 2.67 \times G$

where

- $G = 10^{-(\text{Fine gain in db}/20)}$  (1)

## Device Functional Modes (continued)



S0165-08

Figure 56. Reference Section

## 7.5 Programming

### 7.5.1 Device Programming Modes

The ADS556x device offers flexibility with several programmable features that are easily configured.

The device can be configured independently using either parallel interface control or serial interface programming.

In addition, the device supports a third configuration mode, where both the parallel interface and the serial control registers are used. In this mode, the priority between the parallel and serial interfaces is determined by a priority table (Table 3). If this additional level of flexibility is not required, the user can select either the serial interface programming or the parallel interface control.

### 7.5.2 Using Parallel Interface Control Only

To control the device using parallel interface, keep RESET tied to **high** (DRVDD). The DFS, MODE, SEN, SCLK, and SDATA pins are used to directly control certain modes of the ADC. The device is configured by connecting the parallel pins to the correct voltage levels (as described in Table 4 to Table 8). Applying a reset is not required.

In this mode, the SEN, SCLK, and SDATA pins function as parallel interface control pins. Frequently used functions are controlled in this mode: standby, selection between LVDS/CMOS output format, internal and external reference, 2s-complement and offset-binary output format, and position of the output clock edge.

Table 2 lists a description of the modes controlled by the parallel pins.

**Programming (continued)**
**Table 2. Parallel Pin Definition**

| PIN   | CONTROL MODES  |
|-------|--|
| DFS   | DATA FORMAT and the LVDS/CMOS output interface                                       |
| MODE  | Internal or external reference   |
| SEN   | CLKOUT edge programmability  |
| SCLK  | LOW SPEED mode control for low sampling frequencies ( $\leq 30$ MSPS)                |
| SDATA | STANDBY mode – Global (ADC, internal references and output buffers are powered down) |

**7.5.2.1 Using Serial Interface Programming Only**

To program using the serial interface, the internal registers must first be reset to the default values, and the RESET pin must be kept **low**. In this mode, the SEN, SDATA, and SCLK pins function as serial interface pins and are used to access the internal registers of ADC. The registers are reset either by applying a pulse on the RESET pin (of width greater than 10 ns), or by a **high** setting on the <RST> bit (D1 in register 0x6C). The [Serial Interface](#) section describes the register programming and register reset in more detail.

Because the parallel pins, DFS and MODE, are not used in this mode, they must be tied to ground.

**7.5.2.2 Using Both Serial Interface And Parallel Controls**

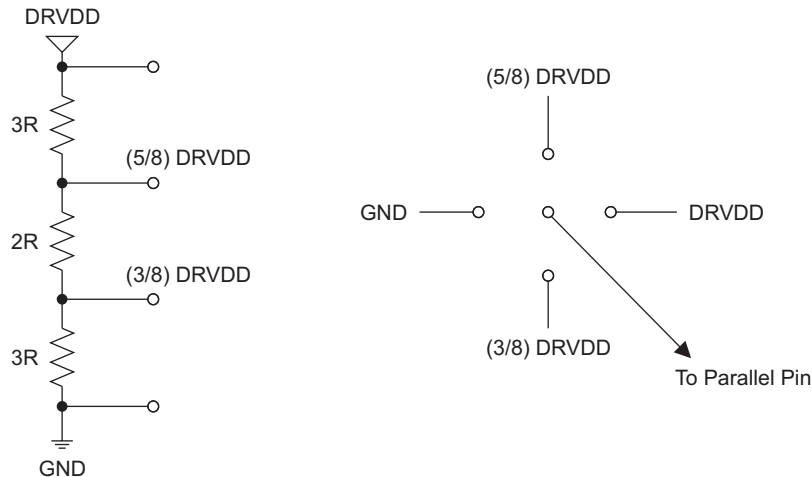
For increased flexibility, a combination of serial interface registers and parallel pin controls (DFS, MODE) can also be used to configure the device.

The serial registers must first be reset to the default values and the RESET pin must be kept **low**. In this mode, the SEN, SDATA, and SCLK pins function as serial interface pins and are used to access the internal registers of ADC. The registers are reset either by applying a pulse on RESET pin or by a **high** setting on the <RST> bit (D1 in register 0x6C). The [Serial Interface](#) section describes the register programming and register reset in more detail.

The parallel interface control pins, DFS and MODE, are used and their function is determined by the appropriate voltage levels as described in [Table 7](#) and [Table 8](#). The voltage levels are derived by using a resistor string as shown in [Figure 57](#). Because some functions are controlled using both the parallel pins and serial registers, the priority between the two is determined by a priority table ([Table 3](#)).

**Table 3. Priority Between Parallel Pins and Serial Registers**

| PIN  | FUNCTIONS SUPPORTED             | PRIORITY  |
|------|---------------------------------|---|
| MODE | Internal and external reference | When using the serial interface, <REF> bit (register 0x6D, bit D4) controls this mode, ONLY if the MODE pin is tied low.  |
| DFS  | DATA FORMAT                     | When using the serial interface, <DF> bit (register 0x63, bit D3) controls this mode, ONLY if the DFS pin is tied low.  |
|      | LVDS and CMOS                   | When using the serial interface, <ODI> bit (register 0x6C, bits D3-D4) controls the LVDS or CMOS selection independent of the state of DFS pin, only if the <ODI> bit is not programmed as 00. The DFS pin controls LVDS/CMOS selection if the <ODI> bit is programmed as 00. |



S0321-02

Figure 57. Simple Scheme to Configure Parallel Pins

7.5.2.3 Description of Parallel Pins

Table 4. SCLK Control Pin

| SCLK  | DESCRIPTION  |
|-------|--|
| 0     | DEFAULT SPEED mode - Use for sampling frequencies > 25 MSPS, 3dB Gain.     |
| DRVDD | LOW SPEED mode Enabled - Use for sampling frequencies ≤ 25 MSPS, 1dB Gain. |

Table 5. SDATA Control Pin

| SDATA | DESCRIPTION   |
|-------|---|
| 0     | Normal operation (Default)  |
| DRVDD | STANDBY. This is a global power-down, where ADC, internal references and the output buffers are powered down. |

Table 6. SEN Control Pin

| SEN                        | DESCRIPTION   |
|----------------------------|---|
| <b>WITH CMOS INTERFACE</b> |   |
| 0                          | CLKOUT Rising edge later by (3/36)Ts<br>CLKOUT Falling edge later by (3/36)Ts     |
| (3/8)DRVDD                 | CLKOUT Rising edge later by (5/36)Ts<br>CLKOUT Falling edge later by (5/36)Ts     |
| (5/8)DRVDD                 | CLKOUT Rising edge earlier by (3/36)Ts<br>CLKOUT Falling edge earlier by (3/36)Ts |
| DRVDD                      | Default CLKOUT position   |
| <b>WITH LVDS INTERFACE</b> |   |
| 0                          | CLKOUT Rising edge later by (7/36)Ts<br>CLKOUT Falling edge later by (6/36)Ts     |
| (3/8)DRVDD                 | CLKOUT Rising edge later by (7/36)Ts<br>CLKOUT Falling edge later by (6/36)Ts     |
| (5/8)DRVDD                 | CLKOUT Rising edge later by (3/36)Ts<br>CLKOUT Falling edge later by (3/36)Ts     |
| DRVDD                      | Default CLKOUT position   |

**Table 7. DFS Control Pin**

| DFS        | DESCRIPTION                                      |
|------------|--|
| 0          | 2s-complement data and DDR LVDS output (Default) |
| (3/8)DRVDD | 2s-complement data and parallel CMOS output      |
| (5/8)DRVDD | Offset binary data and parallel CMOS output      |
| DRVDD      | Offset binary data and DDR LVDS output           |

**Table 8. MODE Control Pin**

| MODE      | DESCRIPTION        |
|-----------|--------------------|
| 0         | Internal reference |
| (3/8)AVDD | External reference |
| (5/8)AVDD | External reference |
| AVDD      | Internal reference |

### 7.5.3 Serial Interface

The ADC has a set of internal registers, which can be accessed through the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and RESET pins. After device power-up, the internal registers must be reset to the default values by applying a high-going pulse on RESET (of width greater than 10 ns), or by a high setting on the <RST> bit (D1 in register 0x6C).

A serial shift of bits into the device is enabled when the SEN pin is low. The serial data pin, SDATA, is latched at every falling edge of the SCLK pin when the SEN pin is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when the SEN pin is low. If the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data is loaded in multiples of 16-bit words within a single active SEN pulse.

The first 8 bits form the register address and the remaining 8 bits form the register data. The interface can work with a SCLK frequency from 20 MHz down to very low speeds (few Hertz) and also with non-50% SCLK duty cycle.

### 7.5.4 Register Initialization

After power-up, the internal registers *must* be reset to the default values which occurs in one of the following ways:

1. A hardware reset by applying a high-going pulse on the RESET pin (of width greater than 10 ns) as shown in [Figure 58](#).
2. A software reset by using the serial interface and setting the <RST> bit (D1 in register 0x6C) to **high**. This configuration initializes the internal registers to the default values and then self-resets the <RST> bit to **low**. In this case the RESET pin is kept **low**.

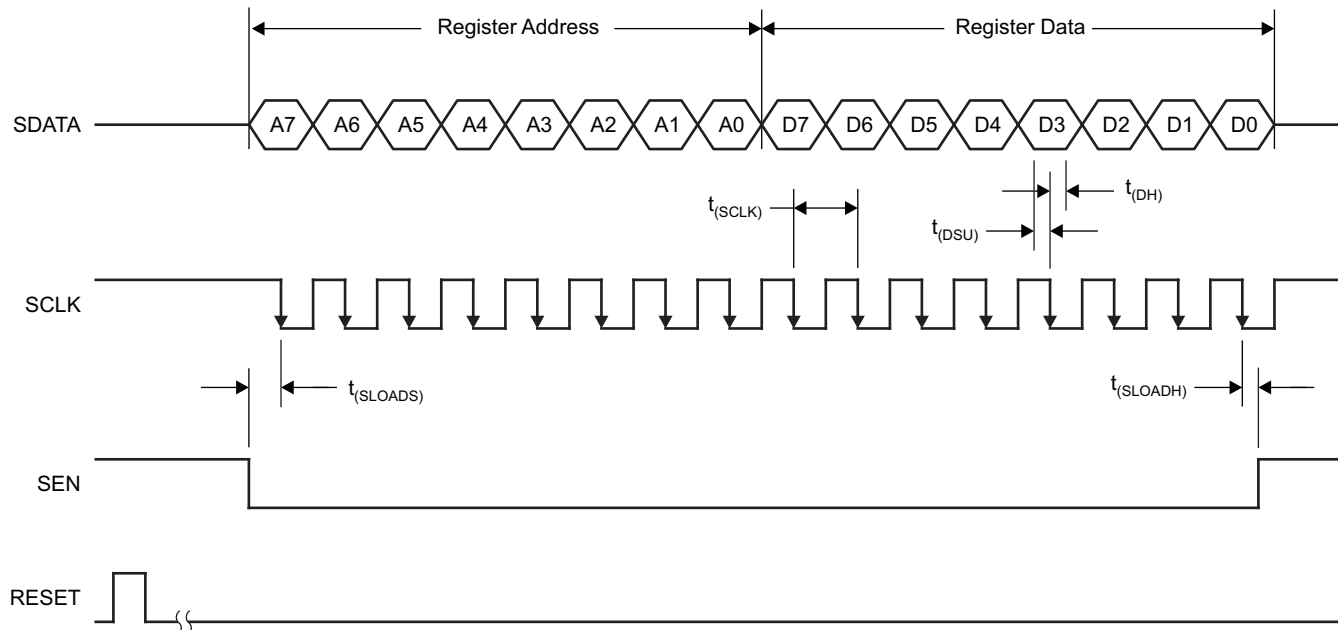


Figure 58. Serial Interface Timing Diagram

## 7.6 Register Maps

Table 9 gives a summary of all the modes that can be programmed through the serial interface.

Table 9. Summary of Functions Supported by Serial Interface<sup>(1) (2)</sup>

| REGISTER ADDRESS IN HEX | REGISTER FUNCTIONS   |    |    |  |  |    |  |   |
|-------------------------|--|----|----|--|--|----|--|---|
|                         | D7   | D6 | D5 | D4   | D3   | D2 | D1   | D0  |
| 5D                      |  |    |    |  |  |    |  | <LF NOISE SUPPRESSION>                                    |
| 62                      |  |    |    |  | <CLKOUT POSN><br>Output clock position programmability     |    |  |   |
| 63                      | <STBY><br>Global power down                                      |    |    |  | <DF><br>DATA FORMAT -<br>2s complement or<br>offset binary |    |  | <LOW SPEED><br>Enable low sampling<br>frequency operation |
| 65                      | <TEST PATTERN> – All 0s, all 1s, toggle,<br>ramp, custom pattern |    |    |  |  |    |  |   |
| 68                      |  |    |    |  | <GAIN><br>Fine gain 0 dB to 6 dB, in 1-dB steps            |    |  |   |
| 69                      | <CUSTOM A> Custom pattern (D7 TO D0)                             |    |    |  |  |    |  |   |
| 6A                      | <CUSTOM B> Custom pattern (D15 TO D8)                            |    |    |  |  |    |  |   |
| 6C                      |  |    |    |  | <ODI> Output data interface<br>DDR LVDS or parallel CMOS   |    |  |   |
| 6D                      |  |    |    | <REF> Internal or<br>external reference              |  |    |  |   |
| 6E                      |  |    |    |  |  |    |  | <RST><br>Software reset                                   |
| 7E                      | <DATA TERM><br>Internal termination – data outputs               |    |    | <CLKOUT TERM><br>Internal termination – output clock |  |    | <LVDS CURR><br>LVDS current<br>programmability |   |
| 7F                      | <CURR DOUBLE><br>LVDS current double                             |    |    |  |  |    |  |   |

(1) The unused bits in each register (shown by blank cells in above table) must be programmed as 0.

(2) Multiple functions in a register can be programmed in a single write operation. See the [Serial Interface](#) section for details.

### 7.6.1 Register Description

This section explains each register function in detail.

**Table 10. Register 5D**

| A7 - A0 (hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0                     |
|---------------|----|----|----|----|----|----|----|------------------------|
| 5D            |    |    |    |    |    |    |    | <LF NOISE SUPPRESSION> |

- D0 <LF NOISE SUPPRESSION> [Low-Frequency Noise Suppression](#)
- 0 Disable low-frequency noise suppression
  - 1 Enable low-frequency noise suppression

**Table 11. Register 62**

| A7 - A0 (hex) | D7 | D6 | D5 | D4   | D3 | D2 | D1 | D0 |
|---------------|----|----|----|--|----|----|----|----|
| 62            |    |    |    | <CLKOUT POSN><br>Output clock position programmability |    |    |    |    |

- D4 - D0 <CLKOUT POSN> [Output Clock Position Programmability](#)
- 00000 Register value after reset (corresponds to default CLKOUT position)  
Setup/hold timings with this clock position are specified in the [Timing Characteristics for LVDS and CMOS Modes](#) table.
  - 00001 Default CLKOUT position.  
Setup and hold timings with this clock position are specified in the [Timing Characteristics for LVDS and CMOS Modes](#) table.
  - XX011 CMOS - Rising edge earlier by (3/36) Ts  
LVDS - Falling edge later by (3/36) Ts
  - XX101 CMOS - Rising edge later by (3/36) Ts  
LVDS - Falling edge later by (6/36) Ts
  - XX111 CMOS - Rising edge later by (5/36) Ts  
LVDS - Falling edge later by (6/36) Ts
  - 01XX1 CMOS - Falling edge earlier by (3/36) Ts  
LVDS - Rising edge later by (3/36) Ts
  - 10XX1 CMOS - Falling edge later by (3/36) Ts  
LVDS - Rising edge later by (7/36) Ts
  - 11XX1 CMOS - Falling edge later by (5/36) Ts  
LVDS - Rising edge later by (7/36) Ts



**Table 12. Register 63**

| A7 - A0 (hex) | D7                             | D6 | D5 | D4 | D3  | D2 | D1 | D0  |
|---------------|--------------------------------|----|----|----|---|----|----|---|
| 63            | <STBY><br>Global power<br>down |    |    |    | <DF><br>DATA<br>FORMAT -<br>2s<br>complement<br>or<br>offset binary |    |    | <LOW SPEED><br>Enable low<br>sampling<br>frequency<br>operation |

D3 <DF> [Output Data Format](#)

0 2s-complement

1 Offset binary

D0 <LOW SPEED> [Low Sampling Frequency Operation](#)

0 DEFAULT SPEED mode (for  $F_s > 25$  MSPS)

1 LOW SPEED mode eabled (for  $F_s \leq 25$  MSPS)

D7 <STBY> [Global STANDBY](#)

0 Normal operation

1 Global power-down (includes ADC, internal references and output buffers)

**Table 13. Register 65**

| A7 - A0 (hex) | D7  | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------|---|----|----|----|----|----|----|----|
| 65            | <TEST PATTERNS> — All 0s, all 1s,<br>toggle, ramp, custom pattern |    |    |    |    |    |    |    |

D7 - D5 <TEST PATTERN> Outputs selected test pattern on data lines

000 Normal operation

001 All 0s

010 All 1s

011 Toggle pattern - alternate 1s and 0s on each data output and across data outputs

100 Ramp pattern - Output data ramps from 0x0000 to 0xFFFF by one code every clock cycle

101 Custom pattern - Outputs the custom pattern in CUSTOM PATTERN registers A and B

111 Unused

**Table 14. Register 68**

| A7 - A0 (hex) | D7 | D6 | D5 | D4 | D3   | D2 | D1 | D0 |
|---------------|----|----|----|----|--|----|----|----|
| 68            |    |    |    |    | <GAIN> Fine gain 0 dB to 6 dB, in 1-dB steps |    |    |    |

|         |   |
|---------|---|
| D3 - D0 | <GAIN> <a href="#">Programmable Fine Gain</a> |
|         | 0XXX 1 dB                                     |
|         | 1000 0 dB                                     |
|         | 1001 1 dB, default register value after reset |
|         | 1010 2 dB                                     |
|         | 1011 3 dB                                     |
|         | 1100 4 dB                                     |
|         | 1101 5 dB                                     |
|         | 1110 6 dB                                     |

**Table 15. Register 69 and Register 6A**

| A7 - A0 (hex) | D7                                 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------|------------------------------------|----|----|----|----|----|----|----|
| 69            | <CUSTOM A> Custom pattern (D7–D0)  |    |    |    |    |    |    |    |
| 6A            | <CUSTOM B> Custom pattern (D15–D8) |    |    |    |    |    |    |    |

|                         |  |
|-------------------------|--|
| Register 69<br>D7 - D0  | <CUSTOM A> Custom pattern (D7–D0)<br>Program bits D7 to D0 of custom pattern   |
| Register 6A<br>D15 - D8 | <CUSTOM B> Custom pattern (D15–D8)<br>Program bits D15 to D8 of custom pattern |

**Table 16. Register 6C**

| A7 - A0 (hex) | D7 | D6 | D5 | D4   | D3 | D2 | D1 | D0 |
|---------------|----|----|----|--|----|----|----|----|
| 6C            |    |    |    | <ODI> Output data interface -<br>DDR LVDS or parallel CMOS |    |    |    |    |

|         |   |
|---------|---|
| D4 - D3 | <ODI> <a href="#">Output Interface</a>  |
|         | 00 default after reset, state of DFS pin determines interface type. See <a href="#">Table 7</a> . |
|         | 01 DDR LVDS outputs, independent of state of DFS pin.   |
|         | 11 Parallel CMOS outputs, independent of state of DFS pin.  |

**Table 17. Register 6D**

| A7 - A0 | D7 | D6 | D5 | D4   | D3 | D2 | D1 | D0 |
|---------|----|----|----|--|----|----|----|----|
| 6D      |    |    |    | <REF><br>Internal or external<br>reference |    |    |    |    |

|    |   |
|----|---|
| D4 | <REF> <a href="#">Reference</a>                                   |
|    | 0 Internal reference  |
|    | 1 External reference mode, force voltage on VCM to set reference. |

**Table 18. Register 6E**

| A7 - A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0                   |
|---------|----|----|----|----|----|----|----|----------------------|
| 6E      |    |    |    |    |    |    |    | <RST> Software reset |

D0 <RST> Software resets the ADC  
 1 Resets all registers to default values

**Table 19. Register 7E**

| A7 - A0 | D7  | D6 | D5 | D4  | D3 | D2 | D1                                       | D0 |
|---------|---|----|----|---|----|----|--|----|
| 7E      | <DATA TERM> Internal termination – data outputs |    |    | <CLKOUT TERM> Internal termination – output clock |    |    | <LVDS CURR> LVDS current programmability |    |

D1 - D0 <LVDS CURR> [LVDS Buffer Current Programmability](#)

00 3.5 mA, default  
 01 2.5 mA  
 10 4.5 mA  
 11 1.75 mA

D4 - D2 <CLKOUT TERM> [LVDS Buffer Internal Termination](#)

000 No internal termination  
 001 325  
 010 200  
 011 125  
 100 170  
 101 120  
 110 100  
 111 75

D7 - D5 <DATA TERM> [LVDS Buffer Internal Termination](#)

000 No internal termination  
 001 325  
 010 200  
 011 125  
 100 170  
 101 120  
 110 100  
 111 75

**Table 20. Register 7F**

| A7 - A0 | D7                                   | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|--------------------------------------|----|----|----|----|----|----|----|
| 7F      | <CURR DOUBLE> LVDS<br>current double |    |    |    |    |    |    |    |

D7 - D6 <CURR DOUBLE> *LVDS Buffer Internal Termination*

00 Value specified by <LVDS CURR>

01 2x data, 2x clockout currents

10 1x data, 2x clockout currents

11 2x data, 4x clockout currents

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

In the design of any application involving a high-speed data converter, particular attention should be paid to the design of the analog input, the clocking solution, and careful layout of the clock and analog signals. The ADS5562 evaluation module (EVM) is one practical example of the design of the analog input circuit and clocking solution, as well as a practical example of good circuit board layout practices around the ADC.

### 8.2 Typical Application

The analog inputs of the ADS5562 device must be fully differential and biased to an appropriate common mode voltage, VCM. End equipment typically does not have a signal that already meets the requisite amplitude and common mode and is fully differential. Therefore, a signal conditioning circuit is required for the analog input. If the amplitude of the input circuit is such that no gain is needed to make full use of the full-scale range of the ADC, then a transformer coupled circuit as used on the EVM can be used with good results. The transformer coupling is inherently low-noise, and inherently AC-coupled so that the signal may be biased to VCM after the transformer coupling. Figure 59 shows an example of transformer coupling as used on the ADS556x EVM.

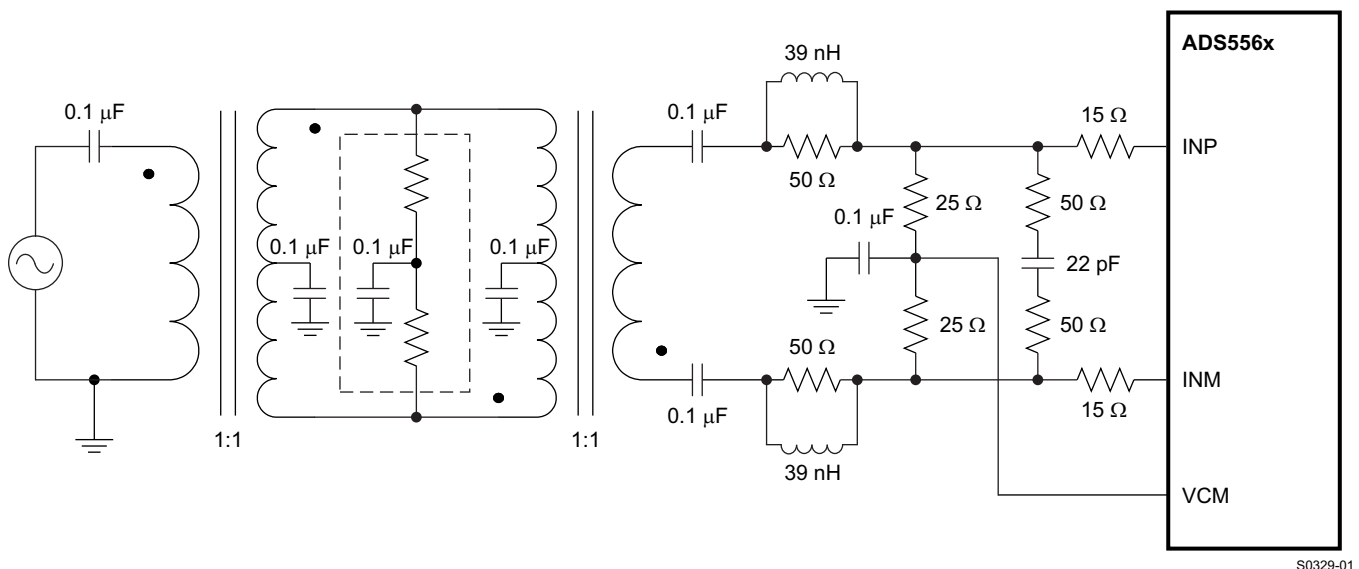
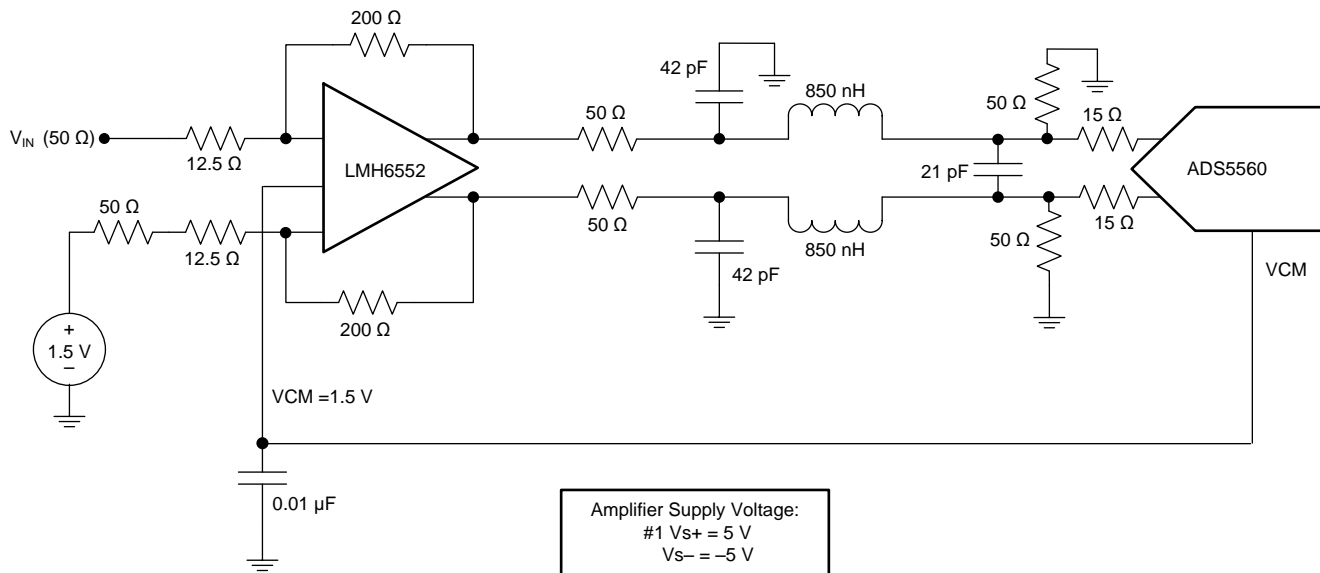


Figure 59. Drive Circuit Using RF Transformers

If signal gain is required, or the input bandwidth is to include the spectrum all the way down to DC such that AC coupling is not possible, then an amplifier-based signal conditioning circuit would be required. Figure 60 shows the LMH6552 device interfaced with the ADS5562 device. The LMH6552 device is configured to have a single-ended input with a differential outputs follow by the first Nyquist-based low-pass filter with 40-MHz bandwidth. Figure 60 also shows the power supply recommendations for the amplifier.

**Typical Application (continued)**

**Figure 60. Drive Circuit Using LMH6552 Fully Differential Amplifier**

Clocking a high-speed ADC such as the ADS5562 device requires a fully differential-clock signal from a clean, low-jitter clock source and driven by an appropriate clock buffer, often with LVPECL or LVDS signaling levels. The sample clock must also be biased up to the appropriate common mode voltage, but unlike the analog input, the data converter itself will often internally bias the clock to the appropriate VCM if the clock signal is AC coupled as in the typical clock driver circuit shown in [Figure 50](#) through [Figure 53](#).

**8.2.1 Design Requirements**

The ADS5562 device requires a fully differential analog input with a full-scale range not to exceed 3.56-V peak-to-peak differential, biased to a common-mode voltage of 1.5 V. In addition the input circuit must provide proper transmission line termination (or proper load resistors in an amplifier-based solution) so the input of the impedance of the ADC analog inputs should be considered as well.

The ADS5562 device is capable of a typical SNR of 82.8 dBFS for input frequencies of about 30 MHz, which is well under the Nyquist limit for this ADC operating at 80 Msps. The amplifier and clocking solution have a direct impact on performance in terms of SNR. Therefore the amplifier and clocking solution should be selected such that the SNR performance of at least 82 dBFS is preserved.

**8.2.2 Detailed Design Procedure**

The ADS5562 device has a maximum sample rate of 80 MHz and an input bandwidth of approximately 300 MHz. For this application, the first Nyquist zone is involved, so the frequency bandwidth must be limited under 40 MHz.

**8.2.2.1 Clocking Source for ADC5562**

The signal-to-noise ratio of the ADC is limited by three different factors: the quantization noise, the thermal noise, and the total jitter of the sample clock. Quantization noise is driven by the resolution of the ADC, which is 16 bits for the ADS5562 device. Thermal noise is typically not noticeable in high-speed pipelined converters such as the ADS5562 device, but may be estimated by looking at the signal to noise ratio of the ADC with very-low input frequencies and using [Equation 3](#) to solve for thermal noise. For this estimation, use the specified SNR for the lowest frequency listed (see the [Specifications](#) section. The lowest input frequency listed for the ADS5562 device is at 3 MHz, and the SNR at that frequency is 84 dB. Therefore, use 84 dB as the SNR limit for this application because of thermal noise. This value is just an approximation, and the lower the input frequency that has an SNR specification the better this approximation is. The thermal noise limits the SNR at low input frequencies while the clock jitter sets the SNR for higher input frequencies.

## Typical Application (continued)

Quantization noise is also a limiting factor for SNR, as the theoretical maximum achievable SNR as a function of the number of bits of resolution is set by [Equation 2](#).

$$\text{SNR}_{\text{max}} = 1.76 + (6.02 \times N)$$

where

- N = number of bits resolution. (2)

For a 16-bit ADC, the maximum SNR = 1.76 + (6.02 × 16) = 98.08 dB. This value is the number that is entered into [Equation 3](#) for quantization noise as we solve for total SNR for different amounts of clock jitter using [Equation 3](#).

$$\text{SNR}_{\text{ADC}} [\text{dBc}] = -20 \times \text{Log} \sqrt{\left(10^{\frac{\text{SNR}_{\text{Quantization\_Noise}}}{20}}\right)^2 + \left(10^{\frac{\text{SNR}_{\text{Thermal\_Noise}}}{20}}\right)^2 + \left(10^{\frac{\text{SNR}_{\text{Jitter}}}{20}}\right)^2} \quad (3)$$

Use [Equation 4](#) to calculate the SNR limitation because of sample clock jitter.

$$\text{SNR}_{\text{Jitter}} [\text{dBc}] = -20 \times \log(2\pi \times f_{\text{IN}} \times t_{\text{Jitter}}) \quad (4)$$

Note that the clock jitter in [Equation 4](#) is the total amount of clock jitter, whether the jitter source is internal to the ADC or external because of the clocking source. The total clock jitter ( $T_{\text{Jitter}}$ ) has two components – the internal aperture jitter (90 fs for ADS5562) which is set by the noise of the clock input buffer, and the external clock jitter from the clocking source and all associated buffering of the clock signal. Use [Equation 5](#) to calculate the total clock jitter from the aperture jitter and the external clock jitter.

$$T_{\text{Jitter}} = \sqrt{\left(T_{\text{Jitter,Ext.Clock\_Input}}\right)^2 + \left(T_{\text{Aperture\_ADC}}\right)^2} \quad (5)$$

The external clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as a bandpass filter at the clock input while a faster clock slew rate may at times also improve the ADC aperture jitter slightly.

The ADS5562 device has an internal aperture jitter of 90 fs, which is largely fixed. The SNR depending on amount of external jitter for different input frequencies is shown in [Figure 61](#). Often the design requirements list a target SNR for a system, and [Equation 3](#) through [Equation 5](#) are then used to calculate the external clock jitter needed from the clocking solution to meet the system objectives.

[Figure 61](#) shows that with an external clock jitter of 200 fs rms, the expected SNR of the ADS5562 device is greater than 82 dBFS at an input tone of 40 MHz, which is the Nyquist limit. Having less external clock jitter such as 150 fs rms, or even 100 fs rms, results in an SNR that exceeds the design target, but possibly at the expense of a more costly clocking solution. An external clock jitter of greater than 200 fs does not meet the design target. Because the design target for SNR is established at 82 dB, and a margin of error is necessary for the SNR contribution from the amplifier and filter on the analog signal, the design goal of 150 fs external clock jitter is established to achieve an SNR for the ADC of approximately 83 dB.

### 8.2.2.2 Amplifier Selection

The amplifier and any input filtering has its own SNR performance, and the SNR performance of the amplifier front end combines with the SNR of the ADC to yield a system SNR that is less than that of the ADC. System SNR can be calculated from the SNR of the amplifier conditioning circuit and the overall ADC SNR as in [Equation 6](#). In [Equation 6](#), the SNR of the ADC is the value derived from the data sheet specifications and the clocking derivation presented in the [Clocking Source for ADC5562](#) section.

$$\text{SNR}_{\text{System}} = -20 \cdot \log \sqrt{\left(10^{\frac{-\text{SNR}_{\text{ADC}}}{20}}\right)^2 + \left(10^{\frac{-\text{SNR}_{\text{Amp+Filter}}}{20}}\right)^2} \quad (6)$$

## Typical Application (continued)

The SNR of the amplifier and filter can be calculated from the noise specifications in the data sheet for the amplifier, the amplitude of the signal and the bandwidth of the filter. The noise from the amplifier is band-limited by the filter, and the rolloff of the filter depends on the order of the filter. Therefore, replacing the filter rolloff with an equivalent brick-wall filter bandwidth is convenient. For example, a 1st order filter can be approximated by a brick-wall filter with bandwidth of 1.57 times the bandwidth of the 1st order filter. For this design, assume a 1st order filter is used. Use [Equation 7](#) to calculate the amplifier and filter noise.

$$\text{SNR}_{\text{Amp+Filter}} = 10 \times \log \left( \frac{V_O^2}{E_{\text{FILTEROUT}}^2} \right) = 20 \times \log \left( \frac{V_O}{E_{\text{FILTEROUT}}} \right)$$

Where

- $V_O$  = the amplifier output signal (which will be full scale input of the ADC expressed in rms)
- $E_{\text{FILTEROUT}} = E_{\text{NAMPOUT}} \times \sqrt{\text{ENB}}$ 
  - $E_{\text{NAMPOUT}}$  = the output noise density of the LMH6552 (1.1 nV/ $\sqrt{\text{Hz}}$  times amplifier gain)
  - ENB = the brick-wall equivalent noise bandwidth of the filter

(7)

In [Equation 7](#), the parameters of the equation may be seen to be in terms of signal amplitude in the numerator and amplifier noise in the denominator, or SNR. For the numerator, use the full-scale voltage specification of the ADS5562 device, or 3.56-V peak-to-peak differential. Because [Equation 7](#) requires the signal voltage to be in rms, convert 3.56  $V_{\text{PP}}$  to 1.26 V rms.

The noise specification for the LMH6552 device is listed as 1.1 nV/ $\sqrt{\text{Hz}}$  times the amplifier gain. Therefore, use this value to integrate the noise component from DC out to the filter cutoff, using the equivalent brick wall filter of 40 MHz  $\times$  1.57, or 62.8 MHz. The result of 1.1 nV/ $\sqrt{\text{Hz}}$  over  $\sqrt{62.8}$  MHz times gain yields 8717 nV, or 8.717  $\mu\text{V}$ , assuming a gain factor of 2 for the amplifier.

Using 1.26-V rms for  $V_O$  and 8.717  $\mu\text{V}$  for  $E_{\text{FILTEROUT}}$ , the SNR of the amplifier and filter as given by [Equation 7](#) is approximately 103.2 dB.

Taking the SNR of the ADC as 83 dB from [Figure 61](#), and SNR of the amplifier and filter as 103.2 dB, [Equation 6](#) predicts the system SNR to be 82.96 dB. In other words, the SNR of the ADC and the SNR of the front end combine as the square root of the sum of squares, and because the SNR of the amplifier front end is much greater than the SNR of the ADC in this example, the SNR of the ADC dominates [Equation 6](#) and the system SNR is almost the SNR of the ADC. The assumed design requirement is 82 dB, and after a clocking solution was selected and an amplifier or filter solution was selected, the predicted SNR of is 82.96 dB. At this point, consider making tradeoffs of either the clocking specification or amplifier gain to see how such tradeoffs begin to affect the expected system performance.



## Typical Application (continued)

### 8.2.3 Application Curve

Figure 61 shows the SNR of the ADC as a function of clock jitter and input frequency for the ADS5562 device. This plot of curves take into account the aperture jitter of the ADC, the number of bits of resolution, and the thermal noise estimation so that the plot can be used to predict SNR for a given input frequency and external clock jitter. Figure 61 then may be used to set the jitter requirement for the clocking solution for a given input bandwidth and given design goal for SNR.

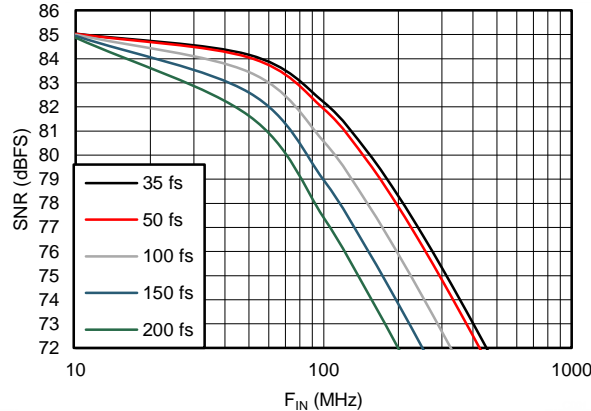


Figure 61. SNR vs Input Frequency and External Clock Jitter

## 9 Power Supply Recommendations

The device requires a 3.3-V nominal supply for AVDD. The device also requires a 3.3-V supply for DRVDD. There are no specific sequence power-supply requirements during device power-up. AVDD, and DRVDD can power up in any order. It is recommended that the analog supply be low noise, such as would be the case if each analog supply was generated by its own linear regulator. The digital supply would be much more tolerant of supply noise and a DC-DC switching supply could be suitable for DRVDD.

At each power-supply pin, a 0.1- $\mu$ F decoupling capacitor should be kept close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10- $\mu$ F, 1- $\mu$ F, and 0.1- $\mu$ F capacitors can be kept close to the supply source.

## 10 Layout

### 10.1 Layout Guidelines

Figure 62 is a section of the layout of the ADS5562 that illustrates good layout practices for the clocking, analog input, and digital outputs. In this example, the analog input enters from the left while the clocking enters from the top, keeping the clock signal away from the analog signals so as to not allow coupling between the analog signal and the clock signal. On the layout of the differential traces, note the symmetry of the trace routing between the two sides of the differential signals.

The digital outputs are routed off to the right, so as to keep the digital signals away from the analog inputs and away from the clock. Note the circuitous routing added to some of the LVDS differential traces but not to others; this is to equalize the lengths of the routing across all of the LVDS traces so as to preserve the setup/hold timing at the end of the digital signal routings. If the timing closure in the receiving device (such as an FPGA or ASIC) has enough timing margin, then the circuitous routing to equalize trace lengths may not be necessary.

In addition, the solid gray areas are ground planes, providing more isolation between the clocking and the analog inputs as well as between the clocking and the digital outputs.

## Layout Guidelines (continued)

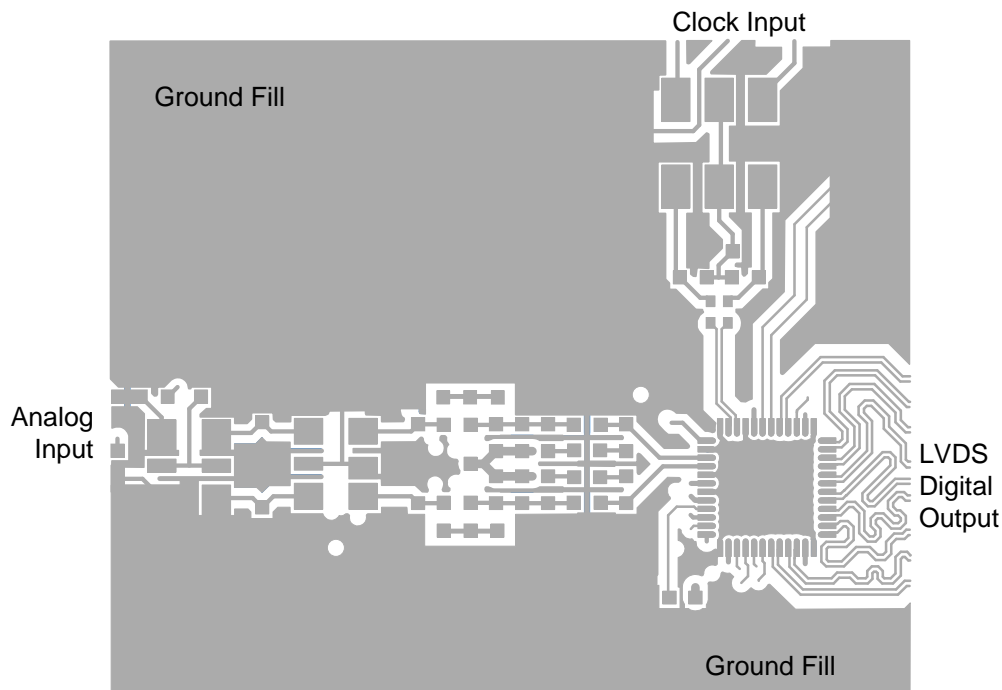
### 10.1.1 Supply Decoupling

As ADS556x already includes internal decoupling, minimal external decoupling can be used without loss in performance. Decoupling capacitors can help to filter external power supply noise, so the optimum number of capacitors would depend on the actual application. The decoupling capacitors should be placed very close to the converter supply pins. TI recommends using separate supplies for the analog and digital supply pins to isolate digital switching noise from sensitive analog circuitry. In case only a single 3.3-V supply is available, it should be routed first to AVDD. The supply can then be tapped and isolated with a ferrite bead (or inductor) with decoupling capacitor, before being routed to DRVDD.

### 10.1.2 Exposed Thermal Pad

The exposed pad must be soldered at the bottom of the package to a ground plane for best thermal performance. For detailed information, see the TI application notes, *QFN Layout Guidelines* (SLOA122) and *QFN/SON PCB Attachment* (SLUA271).

## 10.2 Layout Example



**Figure 62. Typical Layout of ADS5562**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Device Nomenclature

**Analog Bandwidth** The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

**Aperture Delay** The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

**Aperture Jitter** The sample-to-sample variation in aperture delay.

**Clock Pulse Width/Duty Cycle** The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

**Differential Nonlinearity (DNL)** An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs

**Effective Number of Bits (ENOB)** The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \quad (8)$$

**Gain Error** The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

**Integral Nonlinearity (INL)** The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

**Maximum Sample Rate** The maximum conversion rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

**Minimum Sample Rate** The minimum conversion rate at which the ADC functions.

**Offset Error** The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

**Signal-to-Noise and Distortion (SINAD)** SINAD is the ratio of the power of the fundamental ( $P_S$ ) to the power of all the other spectral components including noise ( $P_N$ ) and distortion ( $P_D$ ), but excluding DC.

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the full-scale range of the converter.

$$\text{SINAD} = 10 \log_{10} \frac{P_S}{P_N + P_D} \quad (9)$$

**Signal-to-Noise Ratio** SNR is the ratio of the power of the fundamental ( $P_S$ ) to the noise floor power ( $P_N$ ), excluding the power at DC and the first nine harmonics.

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the full-scale range of the converter.

$$\text{SNR} = 10 \log_{10} \frac{P_S}{P_N} \quad (10)$$

**Spurious-Free Dynamic Range (SFDR)** The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

**Temperature Drift** The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from  $T_{\text{MIN}}$  to  $T_{\text{MAX}}$ . It is calculated by dividing the

## Device Support (continued)

maximum deviation of the parameter across the  $T_{MIN}$  to  $T_{MAX}$  range by the difference  $T_{MAX} - T_{MIN}$ .

**Total Harmonic Distortion (THD)** THD is the ratio of the power of the fundamental ( $P_S$ ) to the power of the first nine harmonics ( $P_D$ ).

$$THD = 10 \log_{10} \frac{P_S}{P_N} \quad (11)$$

THD is typically given in units of dBc (dB to carrier).

**Two-Tone Intermodulation Distortion** IMD3 is the ratio of the power of the fundamental (at frequencies  $f_1$  and  $f_2$ ) to the power of the worst spectral component at either frequency  $2f_1 - f_2$  or  $2f_2 - f_1$ . IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

**Voltage Overload Recovery** The number of clock cycles taken to recover to less than 1% error for a 6-dB overload on the analog inputs.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

- *ADS5560/62EVM User's Guide*, [SLAU260](#)
- *ADS6149EVM User's Guide*, [SLWU061](#)
- *ADS5547 14-BIT, 210 MSPS ADC With DDR LVDS/CMOS Outputs*, [SLWS192](#)
- *CDCE72010 as a Clocking Solution for High-Speed Analog-to-Digital Converters*, [SCAA902](#)
- *CDCE72010 Phase Noise Performance and Jitter Cleaning Ability*, [SCAA091](#)
- *Design Considerations for Avoiding Timing Errors During High-Speed ADC, LVDS Data Interface with FPGA*, [SLAA592](#)
- *Driving High-Speed, Analog-to-Digital Converters - Part I, Circuit Topologies and System-Level Parameters*, [SLAA416](#)
- *QFN Layout Guidelines*, [SLOA122](#)
- *QFN/SON PCB Attachment*, [SLUA271](#)
- *Smart Selection of ADC/DAC Enables Better Design of Software-Defined Radio*, [SLAA407](#)
- *Why Oversample When Undersampling Can Do The Job?*, [SLAA594](#)

### 11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 21. Related Links**

| PARTS   | PRODUCT FOLDER             | SAMPLE AND BUY             | TECHNICAL DOCUMENTS        | TOOLS AND SOFTWARE         | SUPPORT AND COMMUNITY      |
|---------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| ADS5560 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| ADS5562 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

## 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.5 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

## 11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">ADS5560IRGZR</a> | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | AZ5560              |
| ADS5560IRGZR.A               | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | AZ5560              |
| <a href="#">ADS5560IRGZT</a> | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | AZ5560              |
| ADS5560IRGZT.A               | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | AZ5560              |
| ADS5560IRGZTG4               | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | AZ5560              |
| ADS5560IRGZTG4.A             | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | AZ5560              |
| <a href="#">ADS5562IRGZR</a> | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | AZ5562              |
| ADS5562IRGZR.A               | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | AZ5562              |
| <a href="#">ADS5562IRGZT</a> | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | AZ5562              |
| ADS5562IRGZT.A               | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | AZ5562              |
| ADS5562IRGZTG4               | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | AZ5562              |
| ADS5562IRGZTG4.A             | Active        | Production           | VQFN (RGZ)   48 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 85    | AZ5562              |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS5560IRGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.5     | 12.0    | 16.0   | Q2            |
| ADS5562IRGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.5     | 12.0    | 16.0   | Q2            |



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS5560IRGZR | VQFN         | RGZ             | 48   | 2500 | 350.0       | 350.0      | 43.0        |
| ADS5562IRGZR | VQFN         | RGZ             | 48   | 2500 | 350.0       | 350.0      | 43.0        |

## GENERIC PACKAGE VIEW

**RGZ 48**

**VQFN - 1 mm max height**

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224671/A



4219044/D 02/2022

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGZ0048A

VQFN - 1 mm max height

PLASTIC QUADFLAT PACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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