

AN-1826 Extending the Reach of a FPD-Link II Interface With Cable Drivers and Equalizers

ABSTRACT

TI's family of embedded clock LVDS SER/DES (FPD-link II) provides a 2-wire serial interface for display applications up to distances of 10 meters.

Contents

1	Cable Extender Chipset Enables Long Reach Applications for SER/DES	2
2	Cable Extender Chipset Overview	3
3	Detailed Connection Diagram	5
4	Design Considerations	6
5	How Far, How Fast?	8
6	Conclusion	9
7	References	9

List of Figures

1	FPD-Link II SER/DES Application Example (10 meters or less)	2
2	Long Reach FPD-Link II SER/DES Application (100 meters or more).....	3
3	DS15EA101 Output Residual Jitter as a Function of Launch Amplitude	4
4	Line Driver Output, Equalizer Input, and Equalizer Output Eye Patterns	5
5	Extended Reach FPD-Link II SER/DES Connection Diagram	6
6	Twisted Pair Cable Attenuation	7
7	Twisted Pair Cable NEXT.....	7
8	How Far, How Fast – CAT5e and CAT7 Twisted Pair Cables.....	8

In the application example illustrated in [Figure 1](#), the DS90UR241 is the SER device. It serializes the 18-bit RGB color information along with the three video control signals (VS, HS, and DE) and up to three additional general purpose (GP0, GP1, and GP2) signals into a single high-speed FPD-Link II serial stream. The display in the example is a dual VGA (1280 x 480) resolution. At 60 fps and 10% blanking, the required PCLK is 40.5 MHz. Therefore, the serial rate is 28 times the PCLK or 1.134 Gbps. For applications up to 10 meters, the companion DES device, the DS90UR124, can be used. It performs the clock and data recovery (CDR) function and recreates the wide parallel bus.

In some applications, longer cables may be required that are beyond the capability of the integrated FPD-Link II line drivers and receivers. Instead of using repeaters that would require circuitry and power in the middle of the link, a long haul cable driver/equalizer pair can be used to extend the reach of the cable to 100s of meters. In addition, a repeater would normally be able to restore only the signal amplitude, but would not be able to reduce jitter induced by cable losses and inter-symbol interference; therefore, a repeater approach would provide a rather limited extension to a SER/DES link.

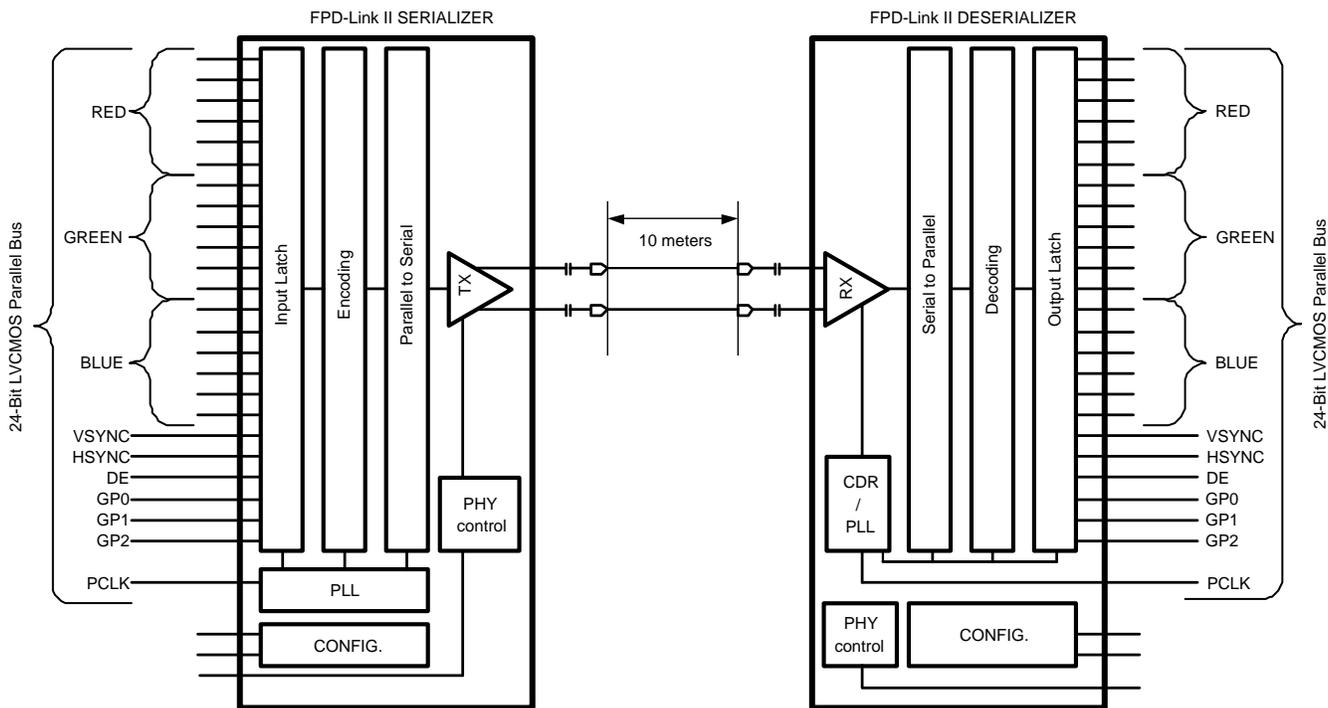


Figure 1. FPD-Link II SER/DES Application Example (10 meters or less)

1 Cable Extender Chipset Enables Long Reach Applications for SER/DES

The DS15BA101 and DS15EA101 can be used as a cable extender chipset to enable long reach applications for FPD-Link II SER/DES display links as shown in [Figure 2](#). The length of the cable can now be greatly extended to more than 100 meters depending upon the serial transmission rate and also the cable characteristics.

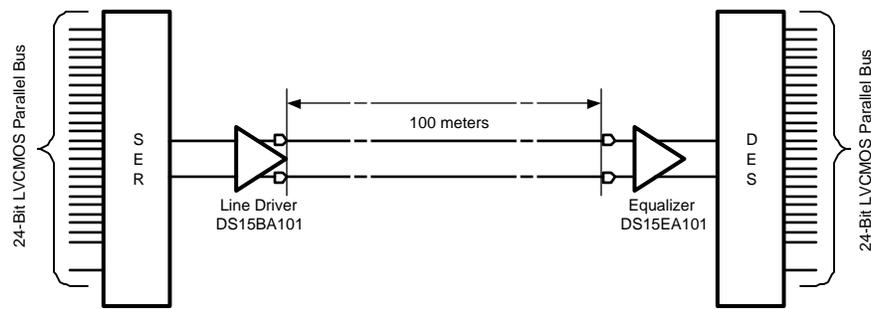


Figure 2. Long Reach FPD-Link II SER/DES Application (100 meters or more)

2 Cable Extender Chipset Overview

The cable extender chipset consists of the DS15BA101 and DS15EA101 devices. These are flexible devices that can be used with LVDS, LVPECL or CML signaling.

The DS15BA101 is a high-speed differential buffer with adjustable output amplitude. It can be used for cable driving, level translation, signal buffering and signal repeating. It operates from DC to 1.5+ Gbps. In the application example, the serial line rate is roughly 1 Gbps and the DS15BA101 is well suited for the application. To set the optimal signal amplitude for the equalization, the buffering is required.

The companion device is the DS15EA101. It is an adaptive equalizer optimized for equalizing data transmitted over coaxial, twinax and twisted pair cables. The operating range for the equalizer is from 150 Mbps to 1.5+ Gbps. Due to the encoding of the FPD-Link II serial stream, the switching rate will remain above 150 Mbps even when sending flat field color data. The equalizer automatically equalizes any cable length from zero meters to lengths that attenuate the signal by approximately 35 dB at 750 MHz.

It is important to realize that the performance of the DS15EA101's automatic equalization circuitry is dependant on the signal amplitude at the transmitter or cable driver end of the cable, the launch amplitude. For 100 Ω differential cables (twinax or twisted pair cables), the optimal launch amplitude is ± 400 mV (800 mVp-p), and for 50 Ω coaxial cables, it is also 800 mV ($V_{OH}-V_{OL}$). The energy detector circuitry in the DS15EA101 quantifies the energy of the incoming signal and feeds this analog information to the automatic equalization control circuitry, which compares it with the assumed energy of the original signal and instructs the equalizer filter to apply certain amount of gain to the high frequency components of the signal based on the comparison. Any deviation from the optimal launch amplitude and as a result deviation in the signal energy from the assumed energy of the original signal in either direction causes the equalizer filter to assert either excessive or insufficient amount of gain as illustrated in [Figure 3](#). The DS15BA101 can provide signals with optimal launch amplitude for equalization of both, differential and single ended cables with minimal deviation over process, voltage and temperature. This is the reason the FPD-Link II SER Line Driver is buffered by the DS15BA101 in the application example.

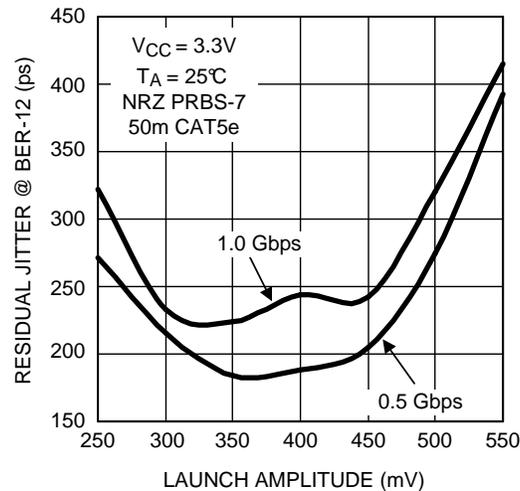


Figure 3. DS15EA101 Output Residual Jitter as a Function of Launch Amplitude

Figure 3 shows how the launch amplitude affects the DS15EA101 output residual jitter when equalizing a 50 m CAT5e cable. It is clear that having a launch amplitude that is smaller or larger than the optimal amplitude (± 400 mV $\pm 10\%$ for 100 Ω differential cables) results in a higher output residual jitter. The data provided in Figure 3 was measured using a single twisted pair of the 50m CAT5e cable. The other twisted pairs in the cable were doubly terminated with 100 Ω resistors to minimize reflections and crosstalk.

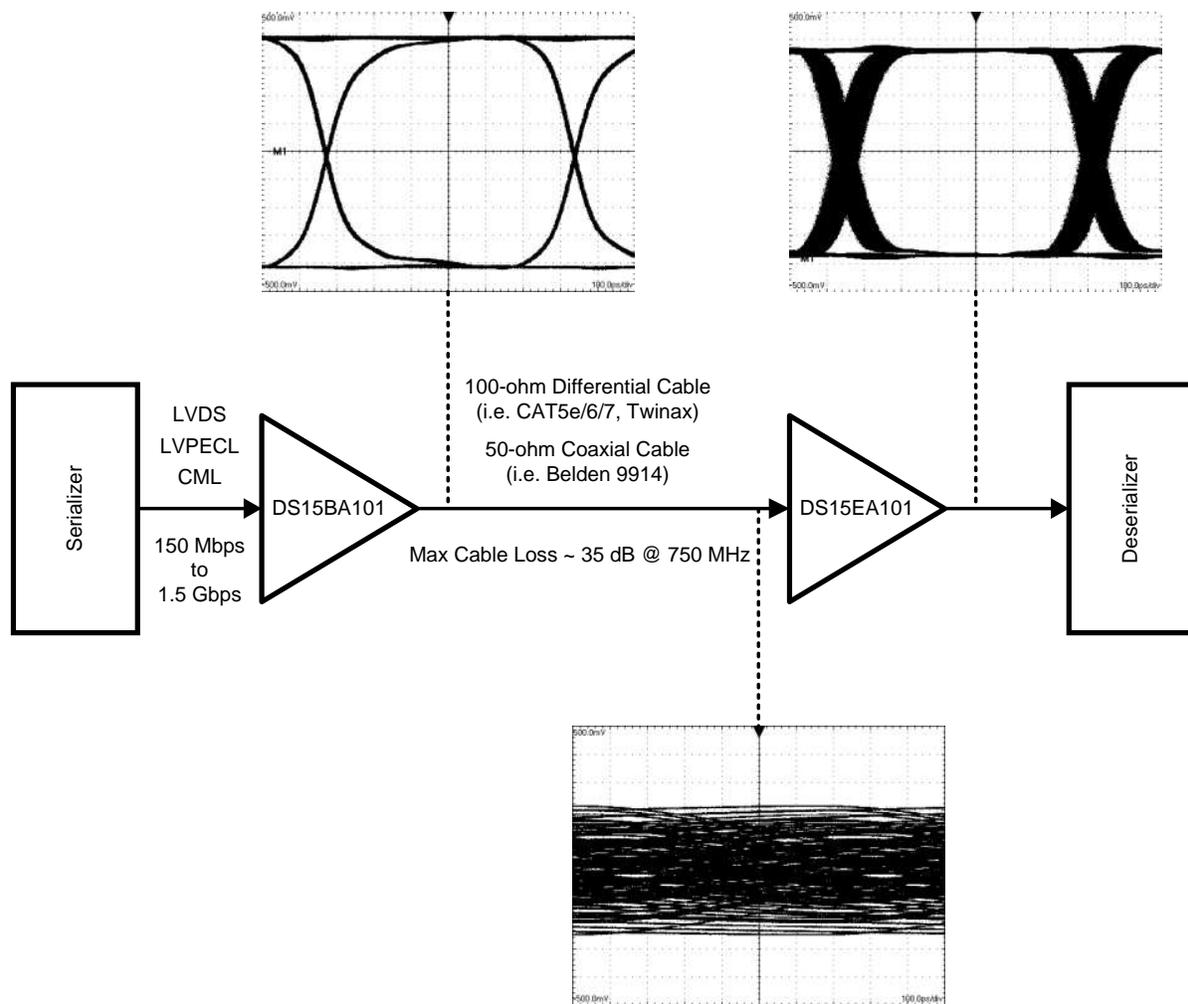


Figure 4. Line Driver Output, Equalizer Input, and Equalizer Output Eye Patterns

Figure 4 illustrates three important eye pattern locations in the example application. The serial signal is repeated and level shifted by the cable driver. The eye pattern at this location has optimal launch amplitude and very low jitter. After the losses due to the long twisted pair cable, the eye pattern is essentially closed. The signal amplitude is attenuated and jitter is excessive. The equalizer provides gain that compensates for the cable losses and also repeats and level shifts the recovered eye pattern. Jitter is greatly reduced, and the signal swing is also recovered. The FPD-Link II DES receives this signal, performs the CDR operation, and provides the parallel output bus to the display.

3 Detailed Connection Diagram

The FPD-Link II SER is typically loaded with a DC100 Ω load at the output and is AC coupled to the receiving device. The line is also terminated with a 100 Ω termination as close to the DS15BA101 inputs as possible. This is done to minimize the resulting stub length. The AC coupling is used to isolate the offset voltage of the FPD-Link II driver (1.2 V) from the DS15BA101 input, which is optimized for a higher input offset for the lowest jitter performance. Coupling capacitors should be 0.1 μ F or greater (1 μ F), use standard values.

The DS15BA101 device requires an external resistor to V_{DD} to set the optimal launch amplitude. A value of 953 Ω is recommended for differential 100 Ω applications. The DS15BA101 outputs also require two 50 Ω resistors pulled to V_{DD} . All three resistors need to have 1% or better tolerance to ensure minimal variation of the launch amplitude.

The long reach cable is AC coupled at both ends to provide maximum isolation of the source and sink ends due to cable faults. The link is also compatible with AC coupling due to the encoding provided to the data by the FPD-Link II SER.

The DS15EA101 device requires an external filter cap as shown and recommended in the data sheet. Its differential outputs include internal 50 Ω pull up resistors. Therefore, the common-mode offset is outside the range of the DS90UR124 inputs and this link needs to be AC coupled for compatibility reasons. Termination should be placed as close to the DES inputs to minimize any resulting stub lengths.

The detailed connection diagram is shown in [Figure 5](#).

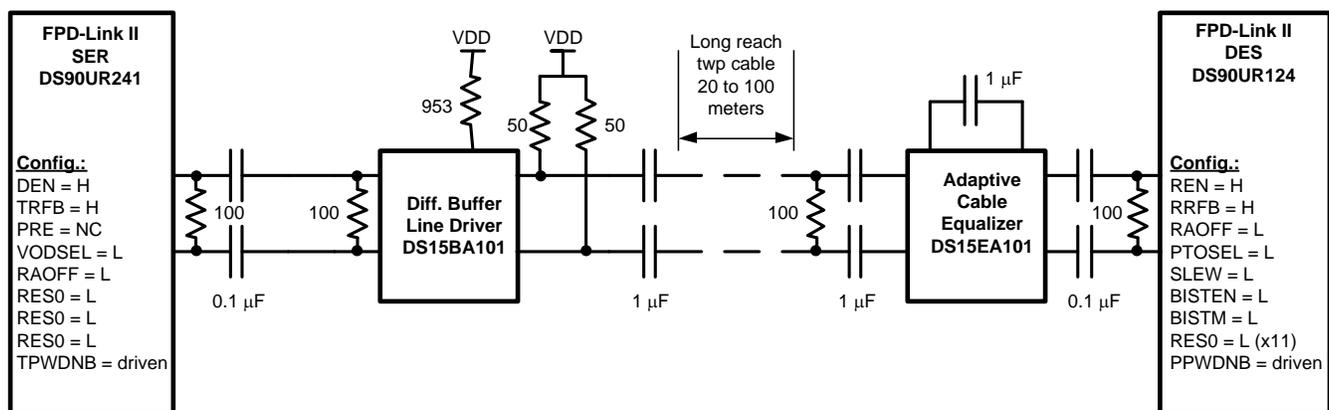


Figure 5. Extended Reach FPD-Link II SER/DES Connection Diagram

The link may be tested by either employing parallel BERT test equipment around this application or by using the on-chip BIST mode of the DS90UR241/124 chipset. The device is configured to output a PRBS stream that the DES detects and sets a status flag to indicate a PASS for error free transmission. For more details, see the *DS90UR241Q DS90UR124Q 5-43 MHz DC-Balanced 24-Bit FPD-Link II Serializer and Deserializer Chipset Data Sheet* ([SNLS231](#)).

4 Design Considerations

While factors such as pattern characteristics, SER/DES I/O characteristics, clock characteristics, connector and cable characteristics, power supply noise and system noise characteristics are important aspects of any design involving SER/DES devices, long reach applications require special attention to cable characteristics. There are three key twisted pair cable parameters that need to be considered when using TWP cable in long reach applications: cable attenuation, near-end crosstalk and pair-to-pair skew also need to be taken into account for multi-pair applications.

Cable attenuation is a measure of the decrease in signal strength along the length of a transmission line. Its two dominant parts are the skin effect and dielectric loss. While the skin effect is directly proportional to the square root of frequency, the dielectric loss is directly proportional to the frequency. Cable attenuation is the major jitter contributor when transmitting signals over long cables, thus, the need for equalization.

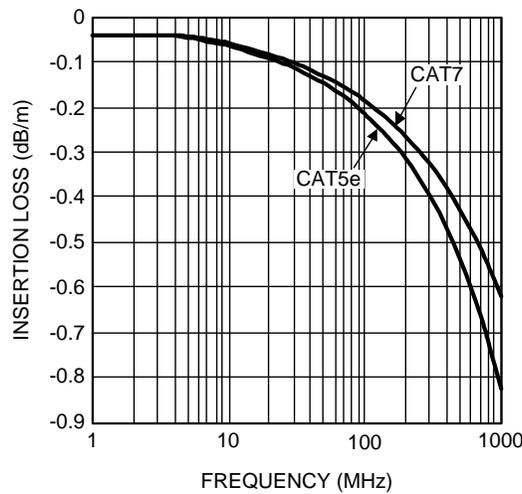


Figure 6. Twisted Pair Cable Attenuation

Figure 6 illustrates cable attenuation per unit length for various twisted pair cables. This data can be used to get an idea of what kind of attenuation signals will experience in a system. Let's say, a 50m CAT5e cable is employed in an FPD-Link II application, in a DVGA application operating at 40.5 MHz. The raw serial bit rate is 1.134 Gbps and corresponding Nyquist frequency is 567 MHz. Based on the data in Figure 6, CAT5e loss at 567 MHz is about -0.595 dB/m. A 50m CAT5e link would attenuate a sinusoidal 567 MHz signal by about -30 dB. If that sinusoidal signal had the amplitude of 400 mV, after 50m of CAT5e, its amplitude would be attenuated to 13 mV! Interestingly enough, amplitude of a 567 MHz square wave would roughly be the same if transmitted over a 50m CAT5e. This could be proven by performing a discrete Fourier transform (DFT) on the ideal square wave and attenuating each harmonic based on Figure 6 data.

For this application report, it is important to realize that signal amplitudes are very small when transmitted over long cables. Small signal amplitudes imply that even small amounts of noise can corrupt data. An equalizer, such as the DS15EA101 is a wide band, high gain, analog amplifier-filter that will boost high frequency components of an attenuated signal regardless of whether it has been corrupted or not, thus, the importance of designing for low noise. For details about PCB Layout techniques that ensure well isolated, low noise environment for adaptive equalizers, see *AN-1347 PCB Layout Techniques for Adaptive Cable Equalizers* (SNLA069). This discussion also brings about another important cable parameter, near end crosstalk (NEXT), a type of system noise that occurs when two or more signals are being transmitted over the same cable in a bi-directional manner.

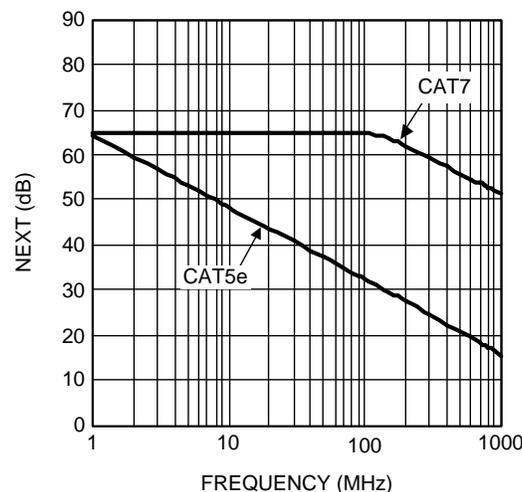


Figure 7. Twisted Pair Cable NEXT

Figure 7 illustrates NEXT for various category cables. For unshielded twisted pair (UTP) cables, the NEXT increases quickly with frequency and leaves little room for cable attenuation, therefore, the maximum cable length for bi-directional transmission is much shorter versus unidirectional transmission such as in the example application. The cables with individually shielded or foiled twisted pairs (FTP) have much better NEXT performance and allow bidirectional transmission at frequencies beyond 1 GHz.

As a rule of thumb, signal-to-noise ratio or attenuation-to-crosstalk ratio (a cabling industry term), needs to be 15-20 dB if bi-directional transmission is desired. For example, if you go back to the DVGA application where there is an FPD-Link II application over a 50m CAT5e cable that attenuates a signal by 30 dB at 567 MHz and want to add a back channel using the same cable. The back channel would have to be a signal that does not couple to the primary channel by more than 45-50 dB assuming the same amplitude for both channels. A signal that would satisfy this requirement would have to have no significant frequency components above approximately 10 MHz.

The pair-to-pair skew is a parameter that should not be overlooked when the timing relationship between signals being transmitted on the same twisted cable is critical. Novice CAT5e users find themselves surprised when they discover that pair-to-pair skew can be as large as 45 ns (typically 25 ns) per 100 meters (TIA/EIA-568-B.2). This is a high number of nanoseconds when dealing with signals running at hundreds of megabits per second. The FPD-Link II SER/DES in our example is not impacted by pair-to-pair skew as the entire bus is serialized to a single pair and thus can be dismissed.

5 How Far, How Fast?

Next, bench data was collected to illustrate the operating boundaries of the part under the tested conditions. The recommended operating conditions for the DS90UR241/124 chipset is between TxCLKs (PCLK) of 5 to 43 MHz. The direct connection of SER to DES is typically limited to 10 meters or less. This is shown by the small operating box in Figure 8.

The lines on the chart were obtained from a bench test using external parallel BERT test equipment. It shows the operating margin obtained for two different types of twisted pair cable interconnects with the DS15BA101 and DS15EA101 devices employed for extending the length of the FPD-Link II serial link.

For the example, the DVGA application operating at 40.5 MHz, 50 meter lengths are possible with the higher loss CAT5e cabling. By using a lower loss cable with individually shielded twisted pairs (CAT7), the length is extended to almost 100 meters.

For a WVGA application, PCLK in the 30 MHz range, lengths of 75 to 100 meters are possible depending upon the cable selected.

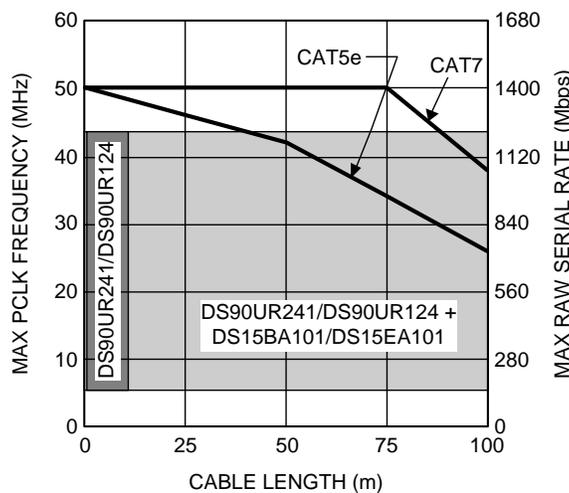


Figure 8. How Far, How Fast – CAT5e and CAT7 Twisted Pair Cables

6 Conclusion

Using the DS15BA101 & DS15EA101 cable driver and equalizer allows for long reach cables to be used between the FPD-Link II SER/DES devices. The equalizer provides up to 35 dB of gain to compensate for the cable losses. Armed with the adaptive equalizer's high gain capability and good design practices addressed in this application report, long reach FPD-Link II applications can be designed with ease. The long reach capability is useful for many industrial display applications where the display is located at a great distance from the source.

7 References

- *DS90UR241Q DS90UR124Q 5-43 MHz DC-Balanced 24-Bit FPD-Link II Serializer and Deserializer Chipset Data Sheet* ([SNLS231](#))
- *AN-1347 PCB Layout Techniques for Adaptive Cable Equalizers* ([SNLA069](#))

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