Major Component Product Pages

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TI 66AK2L06 DSP+ARM® Processor JESD204B Attach to ADC32RF80 & DAC38J84

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Revision History

Revision	Notes
Rev 1.0	Initial revision release

Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 8/27/2016
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Number: TIDEP0081	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: k2l_adjacent_market_solution	Sheet 1 of 38
Drawn By:		File: CoverSheet_01.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

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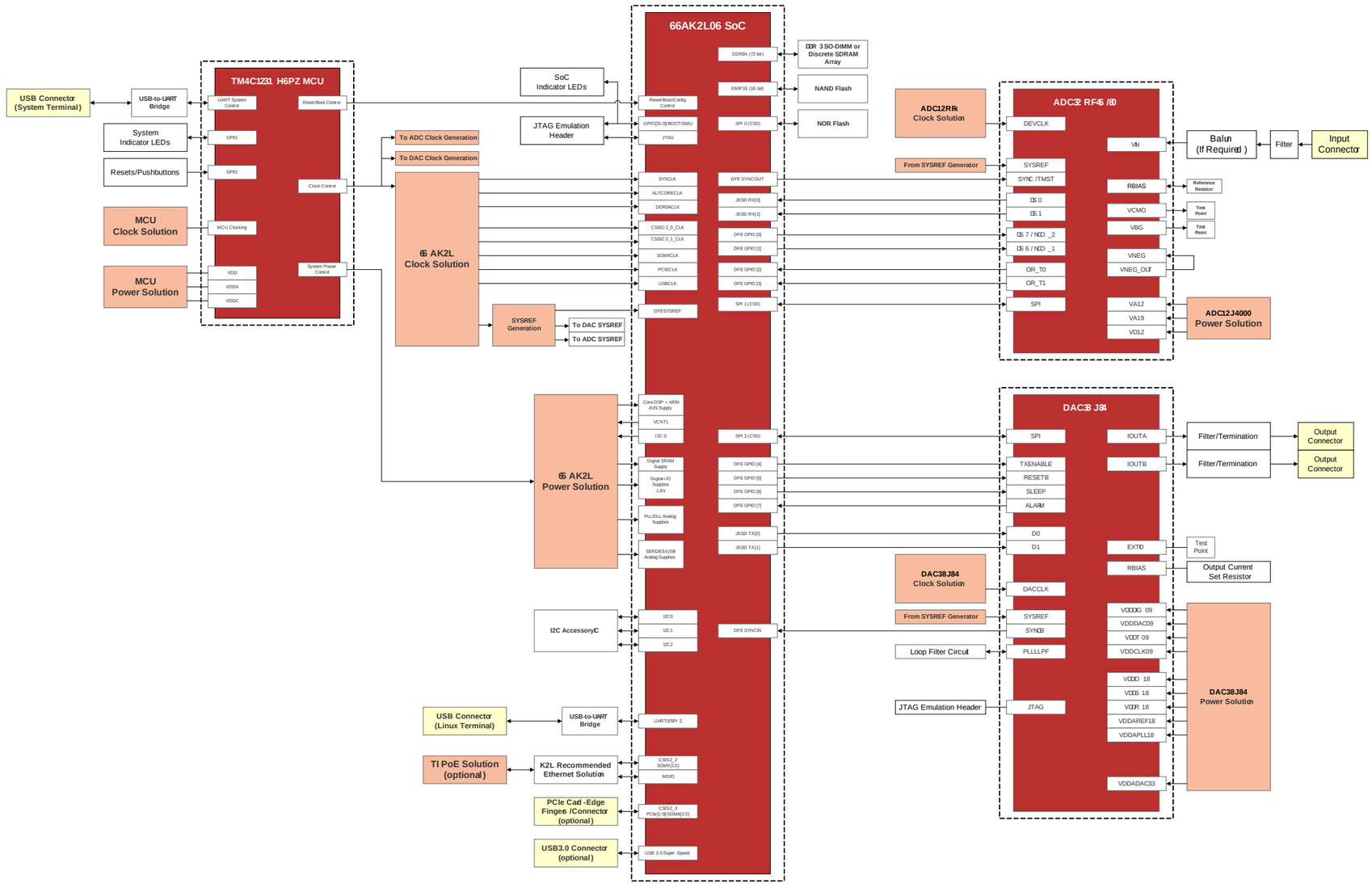

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TID #: TIDEP00XX	Project Title: TI 66AK2L06 DSP+ARM® Processor JESD204B Att	
Number: TIDEP0081 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: k2l_adjacent_market_solution	Sheet 2 of 38
Drawn By: a0271760	File: system_diagram.SchDoc	Size: B
Engineer: a0271760	Contact: http://www.ti.com/support	

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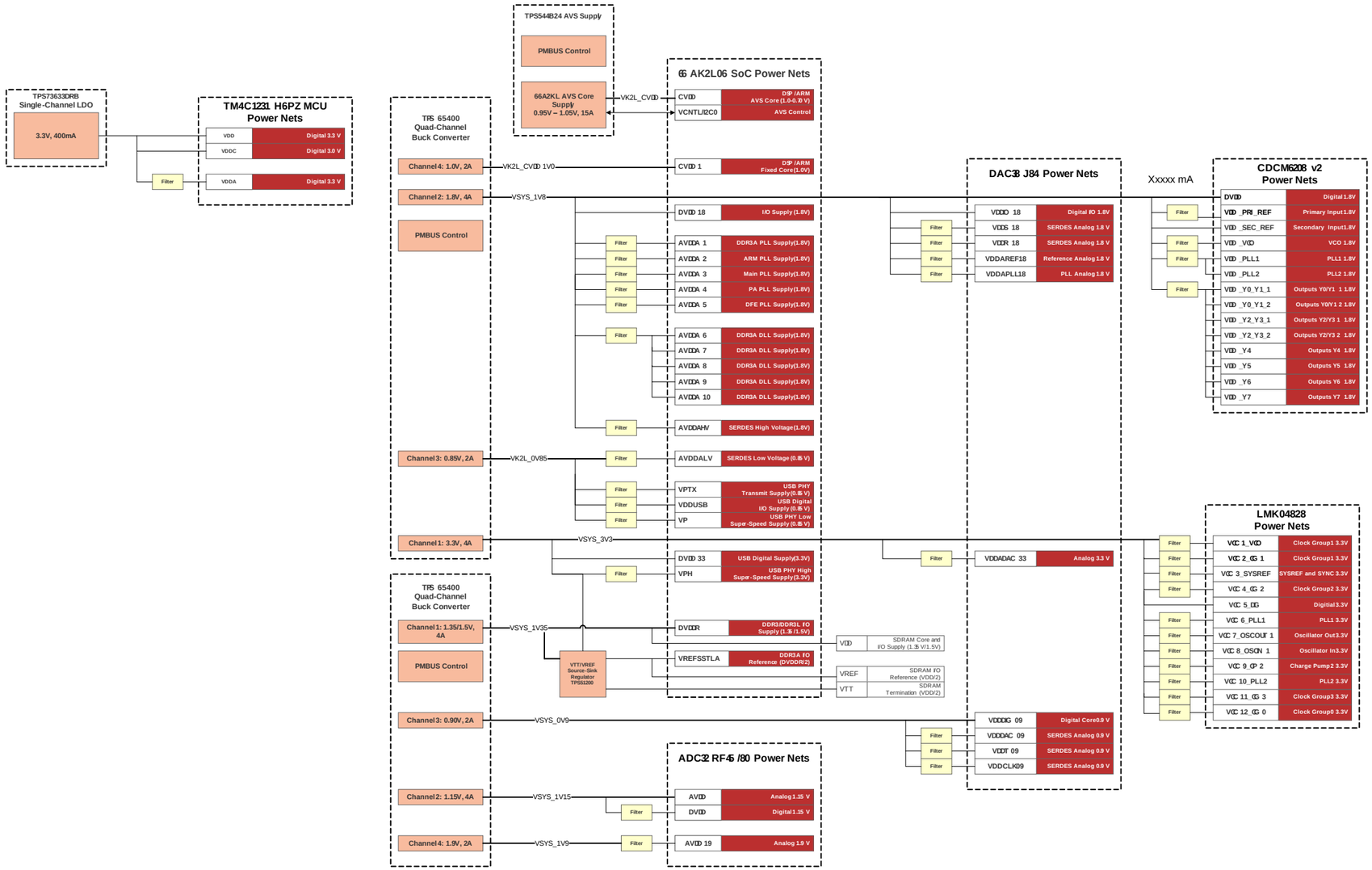

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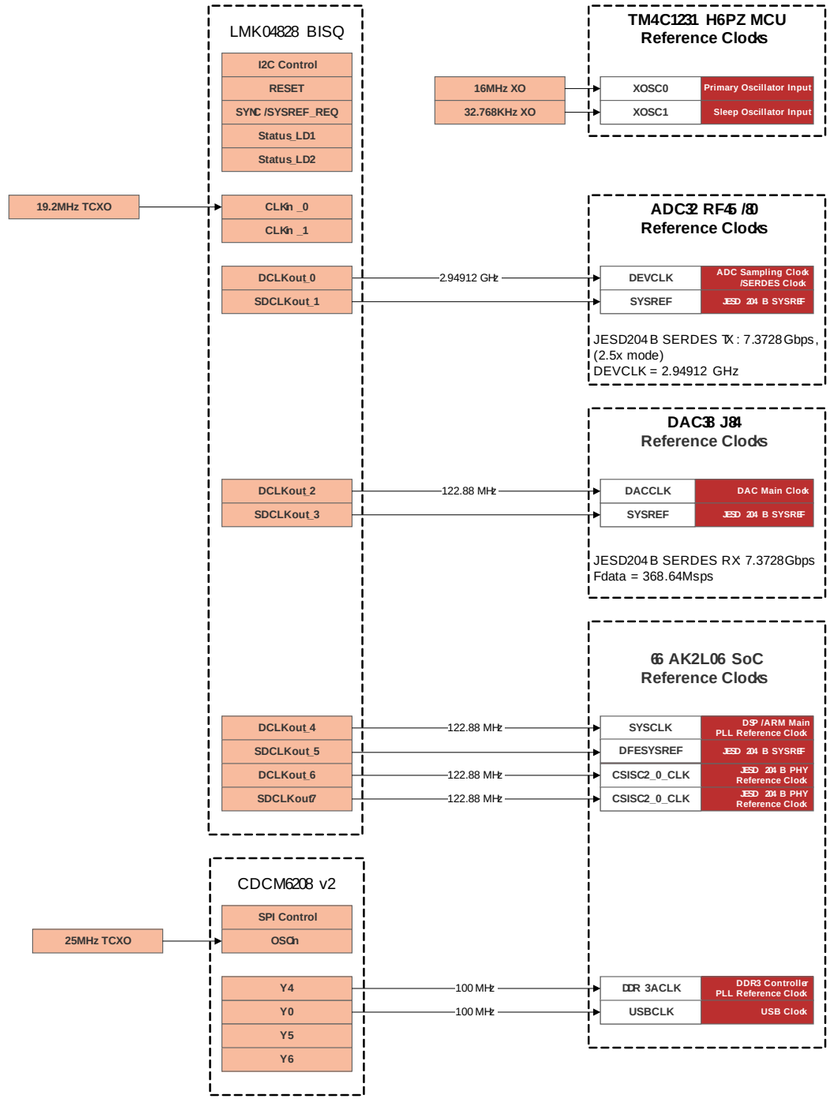

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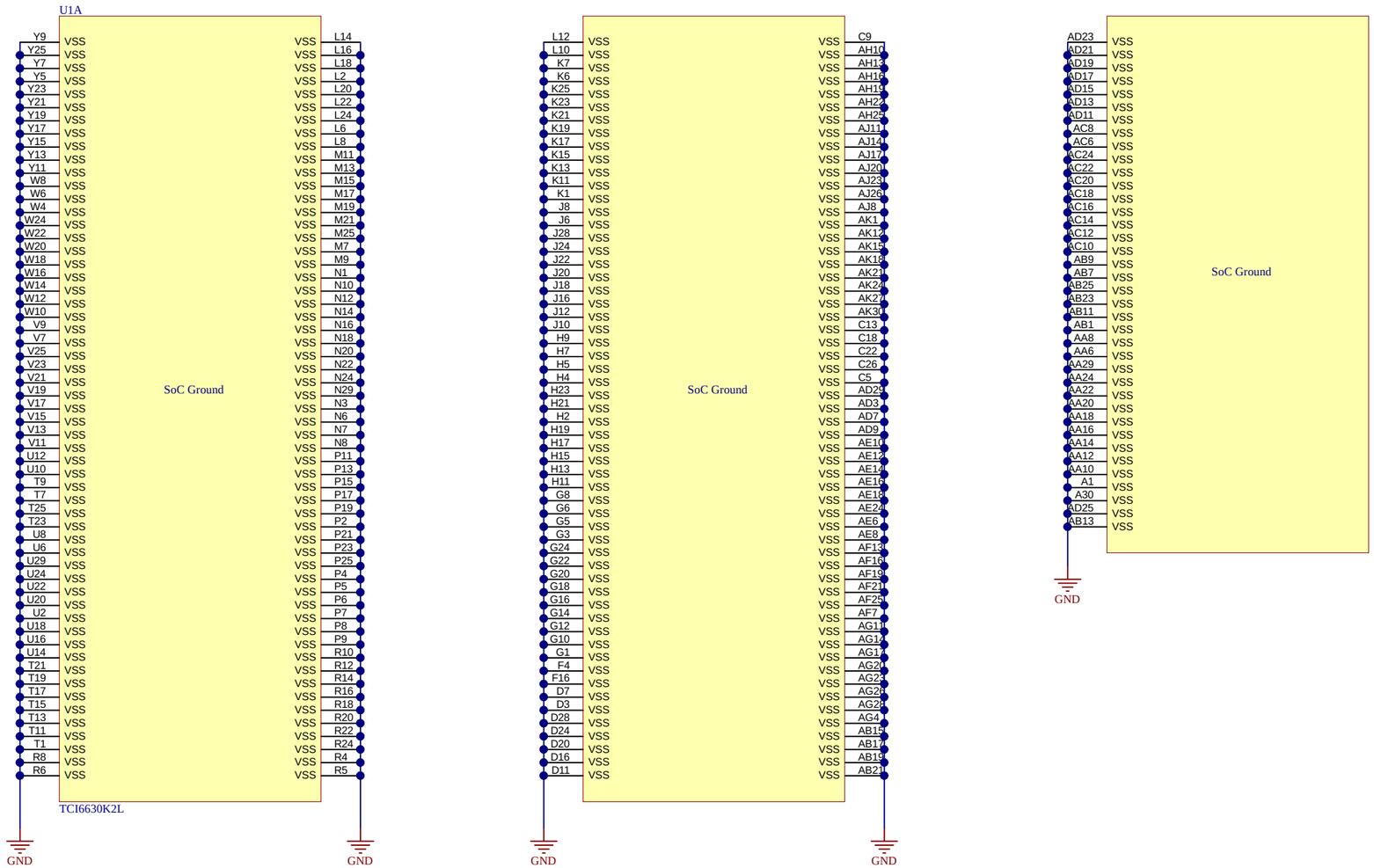
Engineer: a0271760		Contact: http://www.ti.com/support	

K2L GND Reference Pins



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Engineer: a0271760	Contact: http://www.ti.com/support	

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K2L CVDD CorePower Supply Pins and Decoupling

71 CVDD pins

VK2L_CVDD

U1B

Core Supply
Smart-Reflex (0.95V to 1.05V)

Y10 Y18 Y12 W13 W17 W19 W21 W9 W11 V22 V20 V18 V16 V14 V12 U21 U19 U17 U15 U13 U11 T22 T20 T18 T16 T14 T12 R21 R19 R17 R15 R13 R11 P22 P18 P14 P12 P10 N9 N17 N13 M22 M20 M18 M14 L9 L21 L19 — CVDD

K16 K18 K20 K22 L11 L13 L15 L17 AA9 AB10 AB12 AB20 AB22 K12 K14 Y22 AA11 AA19 Y20 AA13 AA15 AA17 AA21 — CVDD

VDDC/VSSCMON CVDD feedback signals routed to TPS544x regulator feedback pins

Core Supply Monitor

VDDCMON — K10 — K2L_VDDCMON → K2L_VDDCMON
VSSCMON — K9 — K2L_VSSCMON → K2L_VSSCMON

VDDTMON — N23 — K2L_VDDTMON
VSSTMON — M23 — K2L_VSSTMON

TCI6630K2L

VSYS_1V8

R25 4.75k R26 4.75k R27 4.75k R28 4.75k R29 4.75k R30 4.75k

U1K

Smart-Reflex VCNTL

K2L_VCNTL0 — AJ27 — VCNTL0
K2L_VCNTL1 — AK28 — VCNTL1
K2L_VCNTL2 — AJ28 — VCNTL2
K2L_VCNTL3 — AG27 — VCNTL3
K2L_VCNTL4_VCL — AH27 — VCNTL4_VCL
K2L_VCNTL5_VD — AH26 — VCNTL5_VD

VCNTL signals routed to TPS544x regulator for Smart-Reflex control of CVDD voltage

Reserved

Y4 — RSV009
W5 — RSV010

J25 — RSV011
H25 — RSV012

TCI6630K2L

0201 caps place directly under BGA

VK2L_CVDD — 20 caps

C13 0.01µF C14 0.01µF C15 0.01µF C16 0.01µF C17 0.01µF C18 0.01µF C19 0.01µF C20 0.01µF C21 0.01µF C22 0.01µF C23 0.01µF C24 0.01µF C25 0.01µF C26 0.01µF C27 0.01µF C28 0.01µF C29 0.01µF C30 0.01µF C31 0.01µF C32 0.01µF

GND

Recommend PDN layout simulation to select exact capacitor value in given location and package type.

VK2L_CVDD — 20 caps

C33 0.022µF C34 0.022µF C35 0.022µF C36 0.022µF C37 0.022µF C38 0.022µF C39 0.022µF C40 0.022µF C41 0.022µF C42 0.022µF C43 0.022µF C44 0.022µF C45 0.022µF C46 0.022µF C47 0.022µF C48 0.022µF C49 0.022µF C50 0.022µF C51 0.022µF C52 0.022µF

GND

VK2L_CVDD — 11 caps

C53 0.047µF C54 0.047µF C55 0.047µF C56 0.047µF C57 0.047µF C58 0.047µF C59 0.047µF C60 0.047µF C61 0.047µF C62 0.047µF C63 0.047µF

GND

VK2L_CVDD — 10 caps

C64 0.1µF C65 0.1µF C66 0.1µF C67 0.1µF C68 0.1µF C69 0.1µF C70 0.1µF C71 0.1µF C72 0.1µF C73 0.1µF

GND

Place larger package caps as close to BGA as possible

VK2L_CVDD

C74 0.22µF C75 0.22µF C76 0.22µF C77 0.22µF C78 0.22µF C79 0.22µF C80 0.22µF C81 0.22µF C82 0.22µF C83 0.22µF C84 0.47µF C85 0.47µF C86 0.47µF C87 0.47µF C88 0.47µF C89 0.47µF C90 0.47µF C91 0.47µF C92 0.47µF C93 0.47µF

GND

VK2L_CVDD

C94 1µF C95 1µF C96 1µF C97 1µF C98 1µF C99 1µF C100 1µF C101 1µF C102 1µF C103 1µF C104 10µF C105 10µF C106 10µF C107 10µF C108 10µF C109 10µF C110 10µF C111 10µF

GND

VK2L_CVDD

C120 22µF C121 22µF C122 22µF C123 22µF C124 22µF C125 47µF C126 47µF C127 47µF C128 47µF C129 47µF C112 100µF C113 100µF C114 100µF C115 100µF C116 470µF C117 470µF C118 470µF C119 470µF

GND

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Engineer: a0271760		Contact: http://www.ti.com/support	

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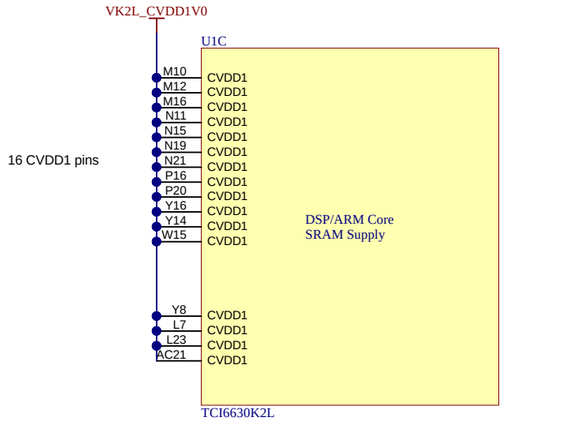
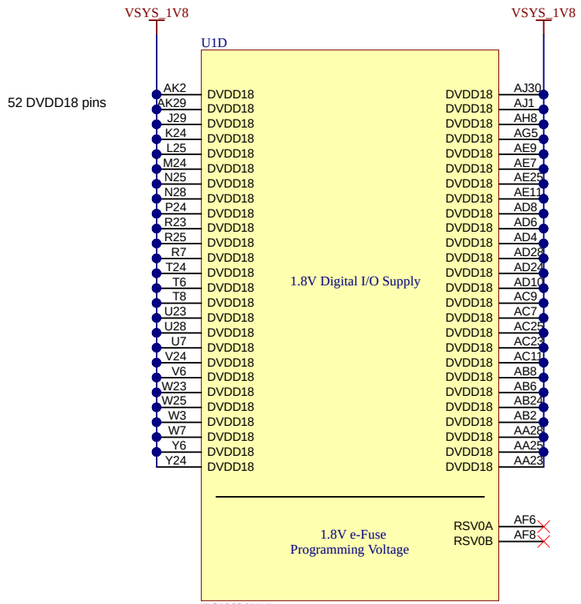
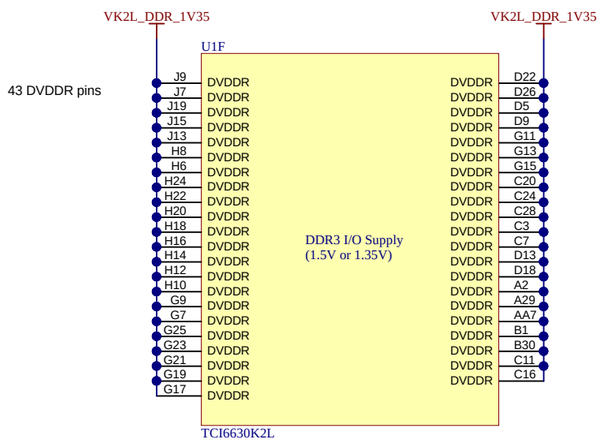
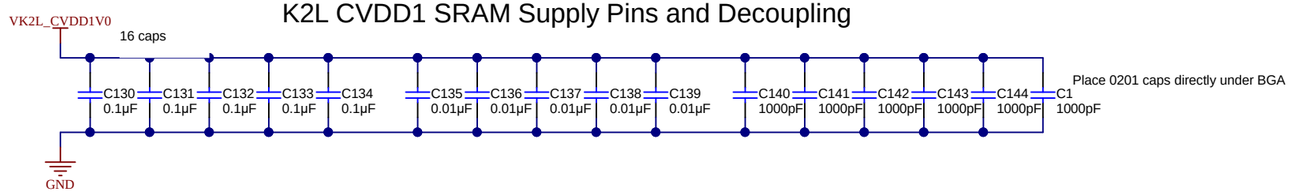
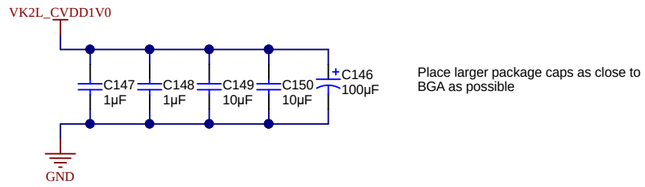






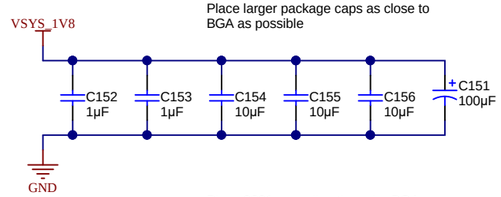
K2L CVDD1 SRAM Supply Pins and Decoupling

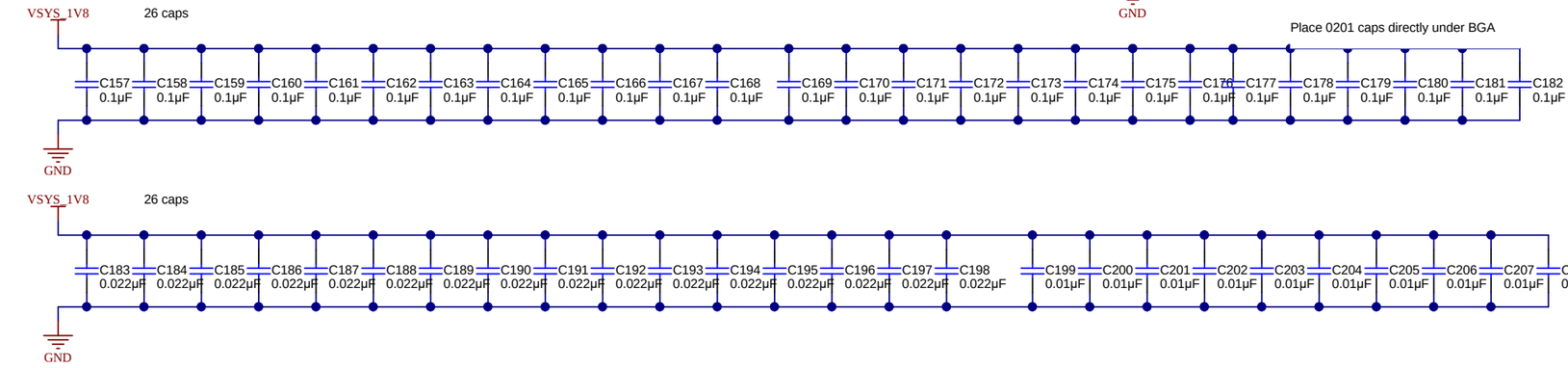




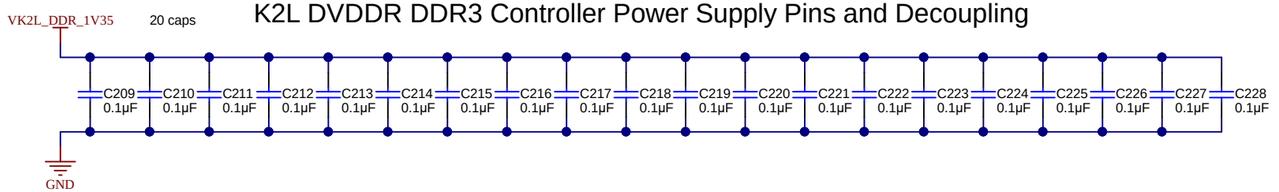
Recommend PDN layout simulation to select exact capacitor value in given location and package type.

K2L DVDD18 Digital I/O Supply Pins and Decoupling

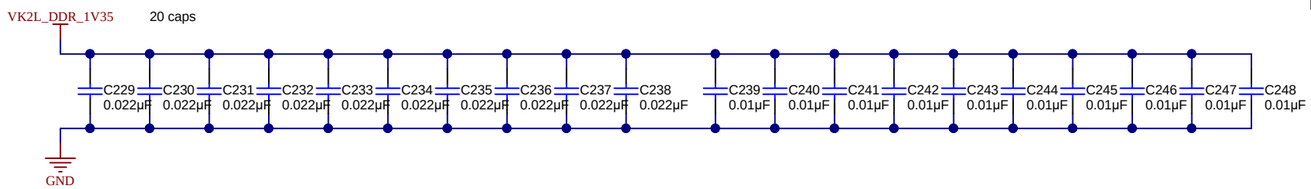


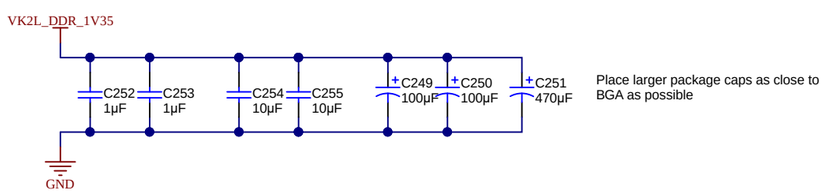


K2L DVDDR DDR3 Controller Power Supply Pins and Decoupling



Recommend PDN layout simulation to select exact capacitor value in given location and package type.





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Engineer: a0271760		Contact: http://www.ti.com/support	

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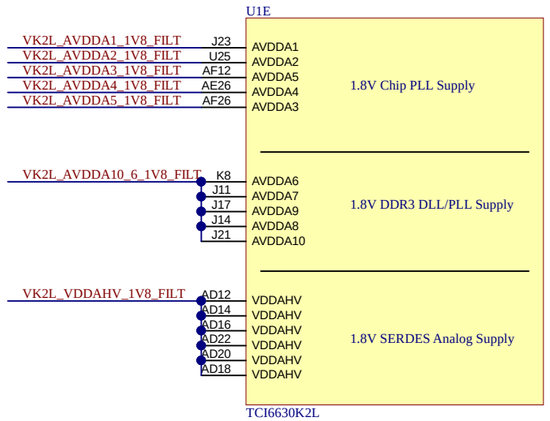
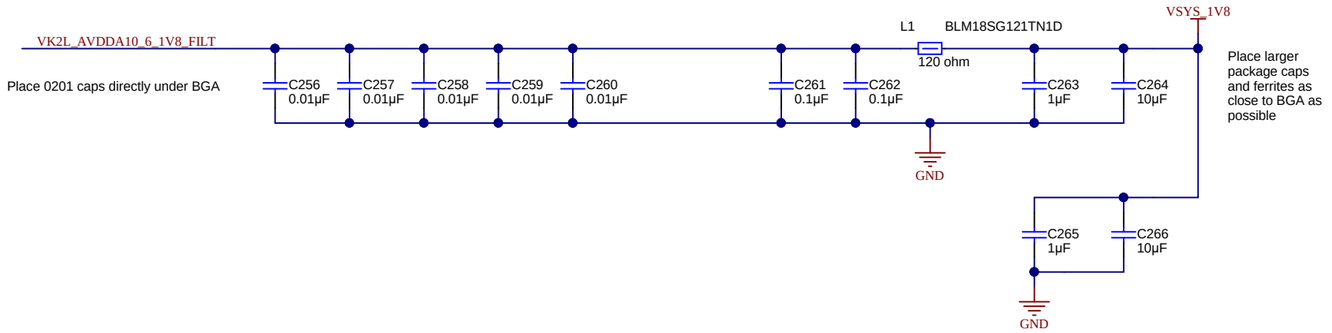
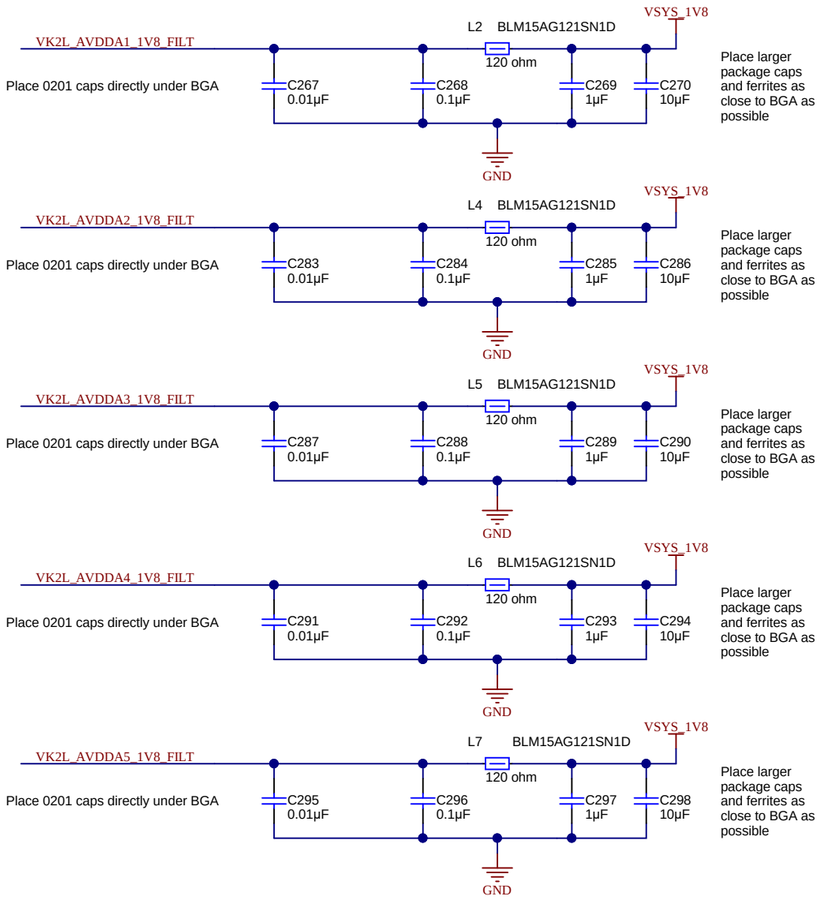


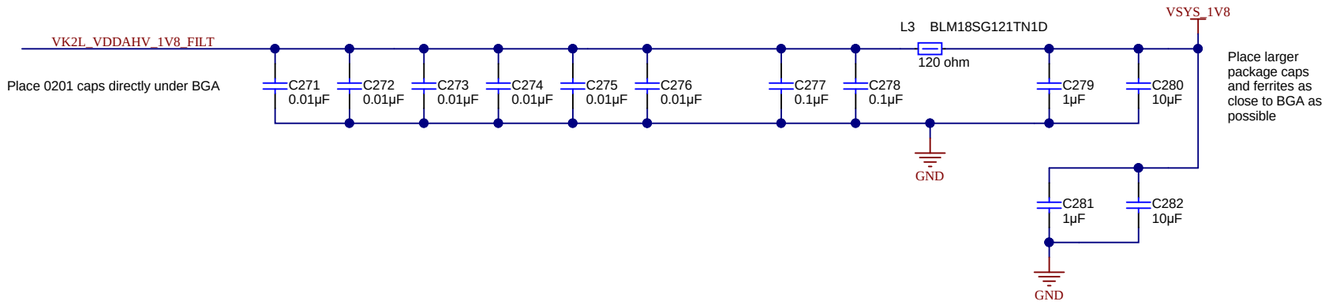
K2L AVDDA[10:6] DDR3 DLL Supply Pins and Decoupling



K2L Core PLL 1.8V Supply Pins and Decoupling



K2L SERDES 1.8V Supply Pins and Decoupling



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Engineer: a0271760	Contact: http://www.ti.com/support	

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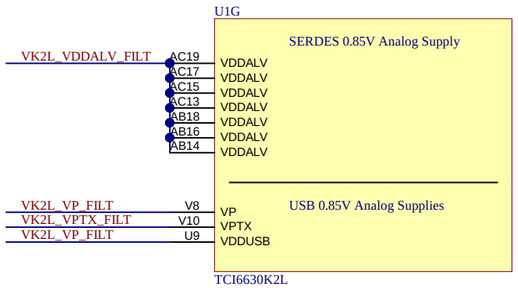
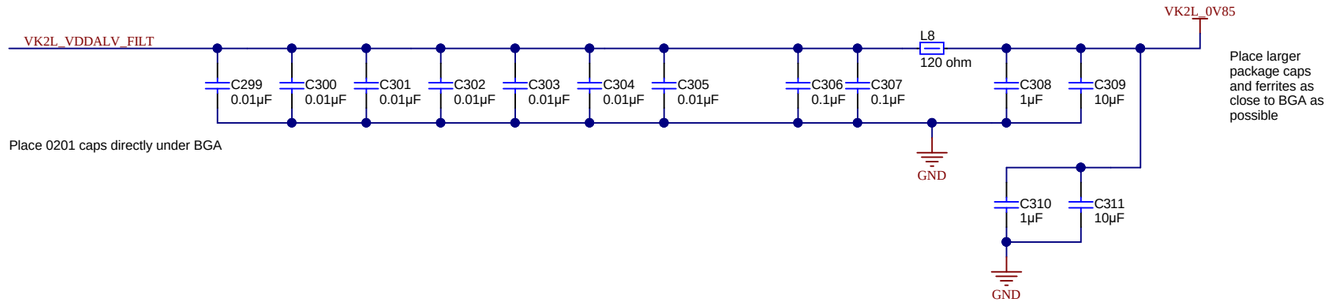
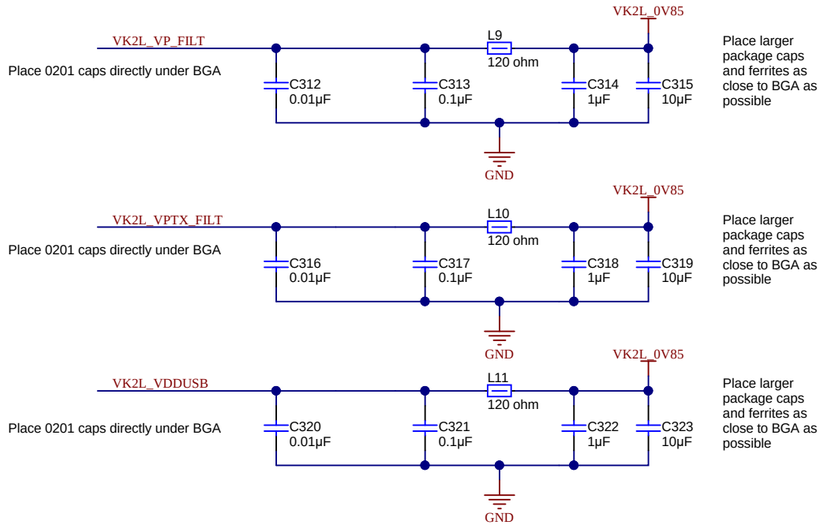
K2L SERDES 0.85V Supply Pins and Decoupling

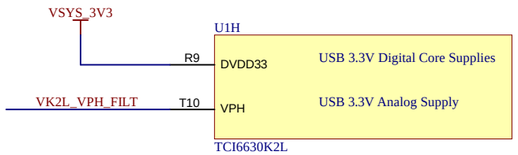


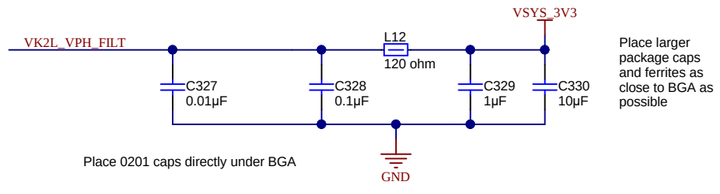


K2L USB 0.85V Supply Pins and Decoupling

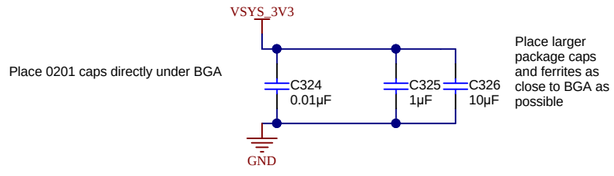


K2L USB 3.3V Supply Pins and Decoupling





K2L USB 3.3V Supply Pins and Decoupling



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Engineer: a0271760	Contact: http://www.ti.com/support	

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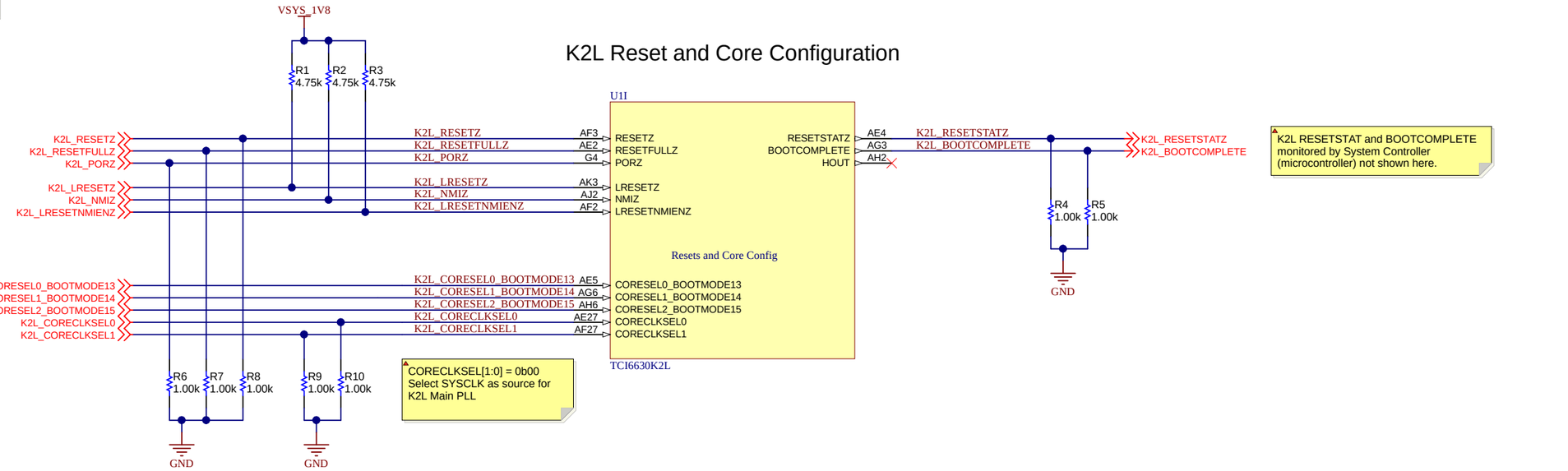
For schematic and layout recommendations and requirements see the K2L product page linked below.

TI 66AK2L06 Product Page

K2L Reset and Core Configuration

K2L BOOTMODE and RESET pins mastered by Board Mangement Controller (microcontroller) not shown here.

K2L CORESEL[2:0] and LRESET/NMIZ/LRESETNMIENZ signals all mastered by Board Management Controller (microcontroller) not shown here.



CORECLKSEL[1:0] = 0b00
Select SYSCLK as source for K2L Main PLL

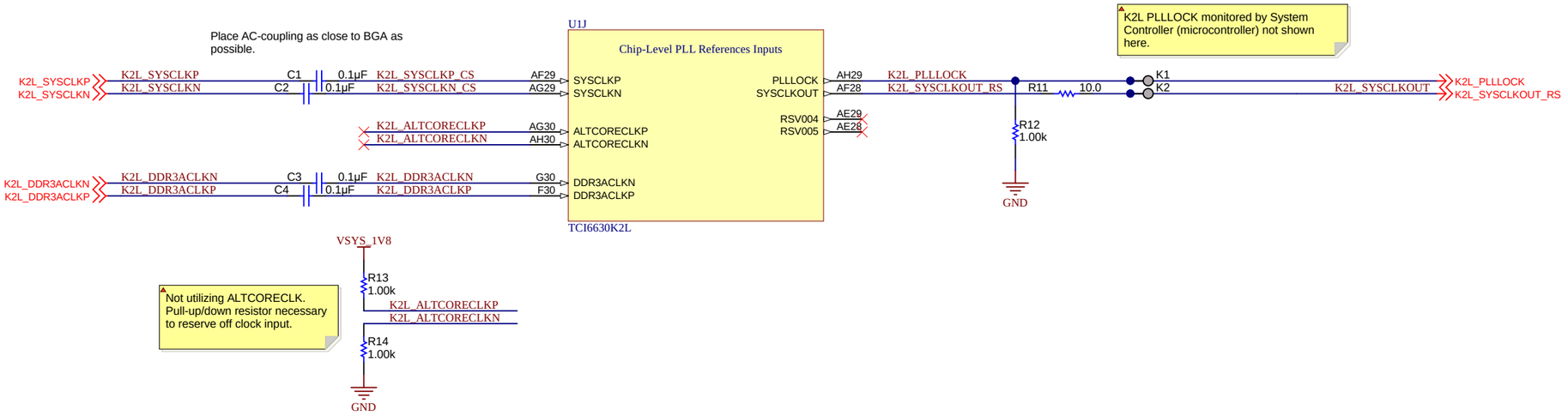
K2L RESETSTAT and BOOTCOMPLETE monitored by System Controller (microcontroller) not shown here.

K2L Core and Peripheral PLL Reference Clock Inputs

K2L SYSCLK sourced my LMK04828. When utilizing LVDS outputs of LMK04828 only AC-coupling is necessary.

Place AC-coupling as close to BGA as possible.

DDR3 controller reference clock solution not shown. Please see K2L EVM schematics.



K2L PLLLOCK monitored by System Controller (microcontroller) not shown here.

Not utilizing ALTCORECLK. Pull-up/down resistor necessary to reserve off clock input.

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Engineer: a0271760		Contact: http://www.ti.com/support	

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K2L Boot-Config, GPIO, SPI, Timer and extended emulation port

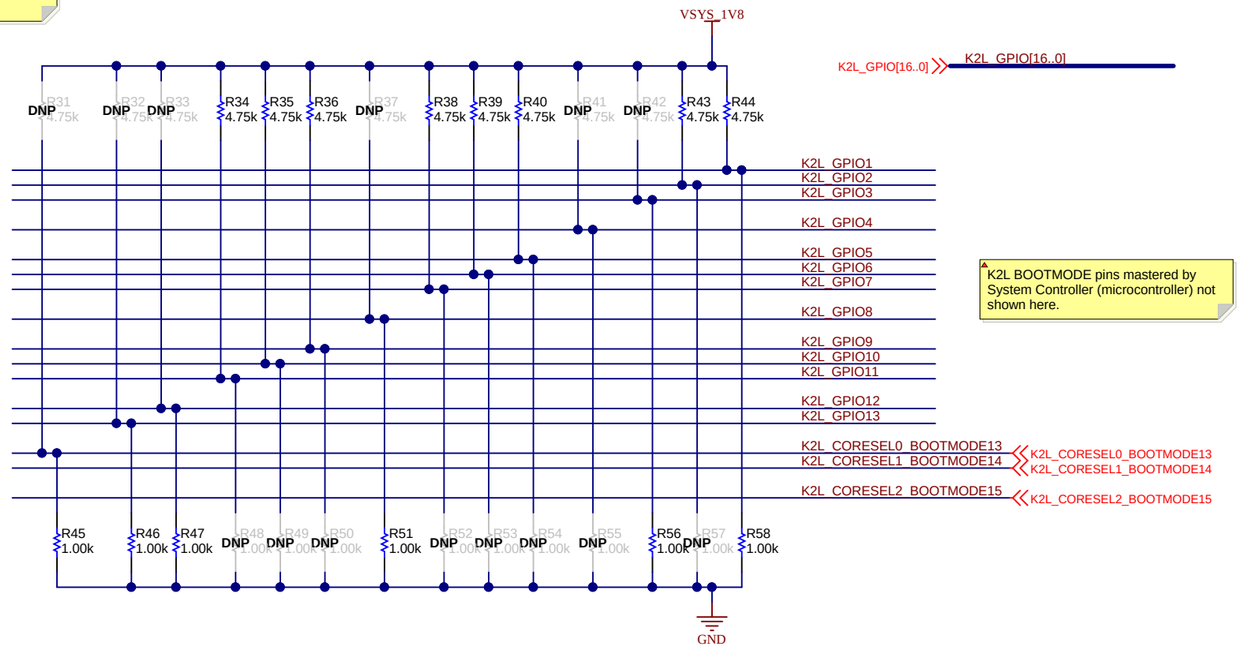
Selecting ARM-mastered, full NAND flash EMIF boot in this example.

BOOTMODE[15:00]/ CORESEL[2:0] + GPIO[13:1] = 0x00

BOOTMODE[2:0] = MODE = 0x5, NAND boot
BOOTMODE[3] = MIN = 0x0, Full NAND boot
BOOTMODE[6:4] = MAIN PLL Setting = 0x7, 122.88 MHz input clock
BOOTMODE[7] = BOOT Master = 0x0, ARM Boot Master
BOOTMODE[10:8] = ARM PLL Setting = 0x7, 122.88 Mhz input clock
BOOTMODE[12:11] = EMIF16 Chip-Select = 0x0, CE0 selected
BOOTMODE[14:13] = First block read = 0x0, initial byte offset
BOOTMODE[15] = ClearNAND select = 0x0, device is not a ClearNAND

Recommend designer to utilize pull-up/pull-downs to select default device boot configuration options as required by application.

K2L Default Boot Configuration Options



K2L_GPIO[16..0] → K2L_GPIO[16..0]

K2L BOOTMODE pins mastered by System Controller (microcontroller) not shown here.

K2L Default Static Configuration Options

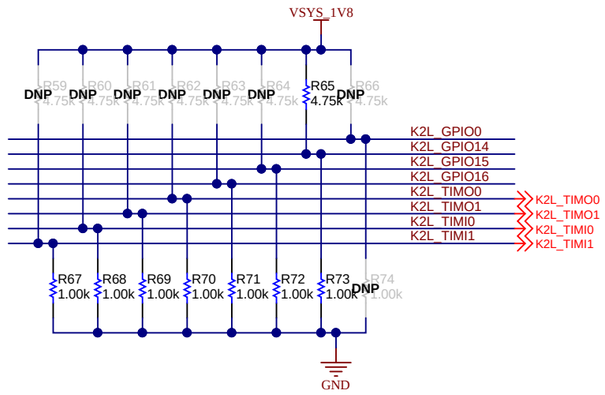
Selecting the following static configuration options:

LENDIAN = 0b1
MAIN_PLL_OD_SEL = 0b0
ARM_BENDIAN = 0b0
CSISC2_0_MUX = 0 - Selects JESD Lane0/1
CSISC2_3_MUX = 0 - Selects PCIe 0 / PCIe1
AVSIFSEL[1:0] = 0b0

Recommend designer should utilize pull-up/pull-downs to select default device static configuration options as required by application.

Board management controller (microcontroller) can also master the boot-mode pins and reset pins during RESETFULLz cycle.

Please see the K2L Data Manual Boot Configuration sections for details.



K2L static configuration pins mastered by System Controller (microcontroller) not shown here.

Not utilizing GPIO[31:17]

U1L — TCI6630K2L

GPIO[7:0]/BOOTMODE[6:0]/Bootstrap/SPI/Timer

K2L_GPIO0	G26	GPIO00_SPI2SCS1_LENDIAN
K2L_GPIO1	F27	GPIO01_SPI2SCS2_BOOTMODE00
K2L_GPIO2	F26	GPIO02_SPI2SCS3_BOOTMODE01
K2L_GPIO3	G29	GPIO03_SPI2SCS4_BOOTMODE02
K2L_GPIO4	F28	GPIO04_TIMI2_BOOTMODE03
K2L_GPIO5	G27	GPIO05_TIMI3_BOOTMODE04
K2L_GPIO6	H30	GPIO06_TIMI4_BOOTMODE05
K2L_GPIO7	J26	GPIO07_TIMI5_BOOTMODE06

GPIO[15:8]/Bootstrap/BOOTMODE[12:7]

K2L_GPIO8	H26	GPIO08_TIMI6_BOOTMODE07
K2L_GPIO9	H29	GPIO09_TIMI7_BOOTMODE08
K2L_GPIO10	J27	GPIO10_TIMO2_BOOTMODE09
K2L_GPIO11	H28	GPIO11_TIMO3_BOOTMODE10
K2L_GPIO12	G28	GPIO12_TIMO4_BOOTMODE11
K2L_GPIO13	H27	GPIO13_TIMO5_BOOTMODE12
K2L_GPIO14	J30	GPIO14_TIMO6_MAINPLL_OD_SEL
K2L_GPIO15	K27	GPIO15_TIMO7_ARM_BENDIAN

GPIO[23:16]/Bootstrap/BOOTMODE/EMU[32:17]

K2L_GPIO16	K26	GPIO16_CSISC_2_3_MUX
K2L_GPIO17	W2	GPIO17_EMU19
K2L_GPIO18	Y1	GPIO18_EMU20
K2L_GPIO19	V3	GPIO19_EMU21
K2L_GPIO20	W1	GPIO20_EMU22
K2L_GPIO21	V1	GPIO21_EMU23
K2L_GPIO22	V2	GPIO22_EMU24
K2L_GPIO23	U4	GPIO23_EMU25

GPIO[31:24]/EMU[33:26]

K2L_GPIO24	V5	GPIO24_EMU26
K2L_GPIO26	V4	GPIO25_EMU27
K2L_GPIO27	U1	GPIO26_EMU28
K2L_GPIO28	T3	GPIO27_EMU29
K2L_GPIO29	U3	GPIO28_EMU30
K2L_GPIO30	T5	GPIO29_EMU31
K2L_GPIO31	U5	GPIO30_EMU32
K2L_GPIO32	T4	GPIO31_EMU33

Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 8/27/2016
TID #: TIDEP00XX		Project Title: TI 66AK2L06 DSP+ARM® Processor JESD204B Att	
Number: TIDEP0081	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: k2l_adjacent_market_solution_sheet_1.1.0	Sheet 1 of 38
Drawn By:		File: k2l_soc_06.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

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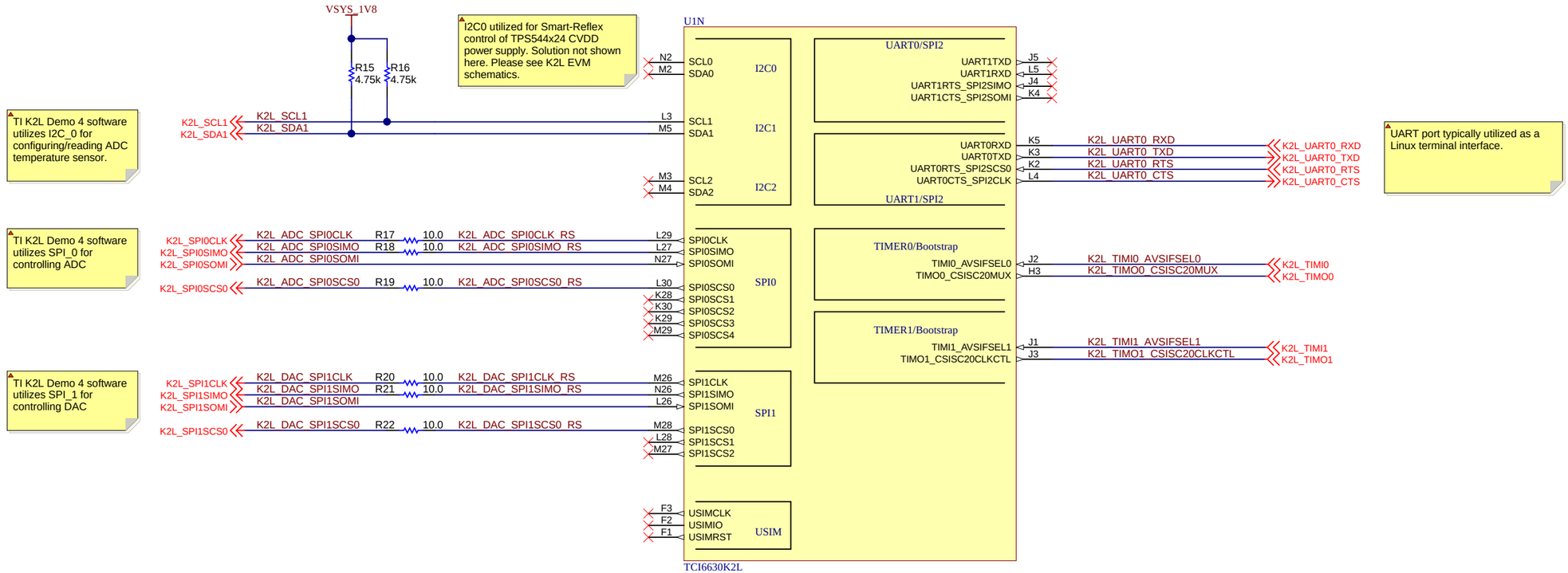
K2L Boot-Config, I2C, SPI, UART, Timer, and USIM



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Number: TIDEP0081 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: k2l_adjacent_market_solution Sheet 12 of 38	
Drawn By:	File: k2l_soc_06_1.SchDoc	Size: B
Engineer: a0271760	Contact: http://www.ti.com/support	

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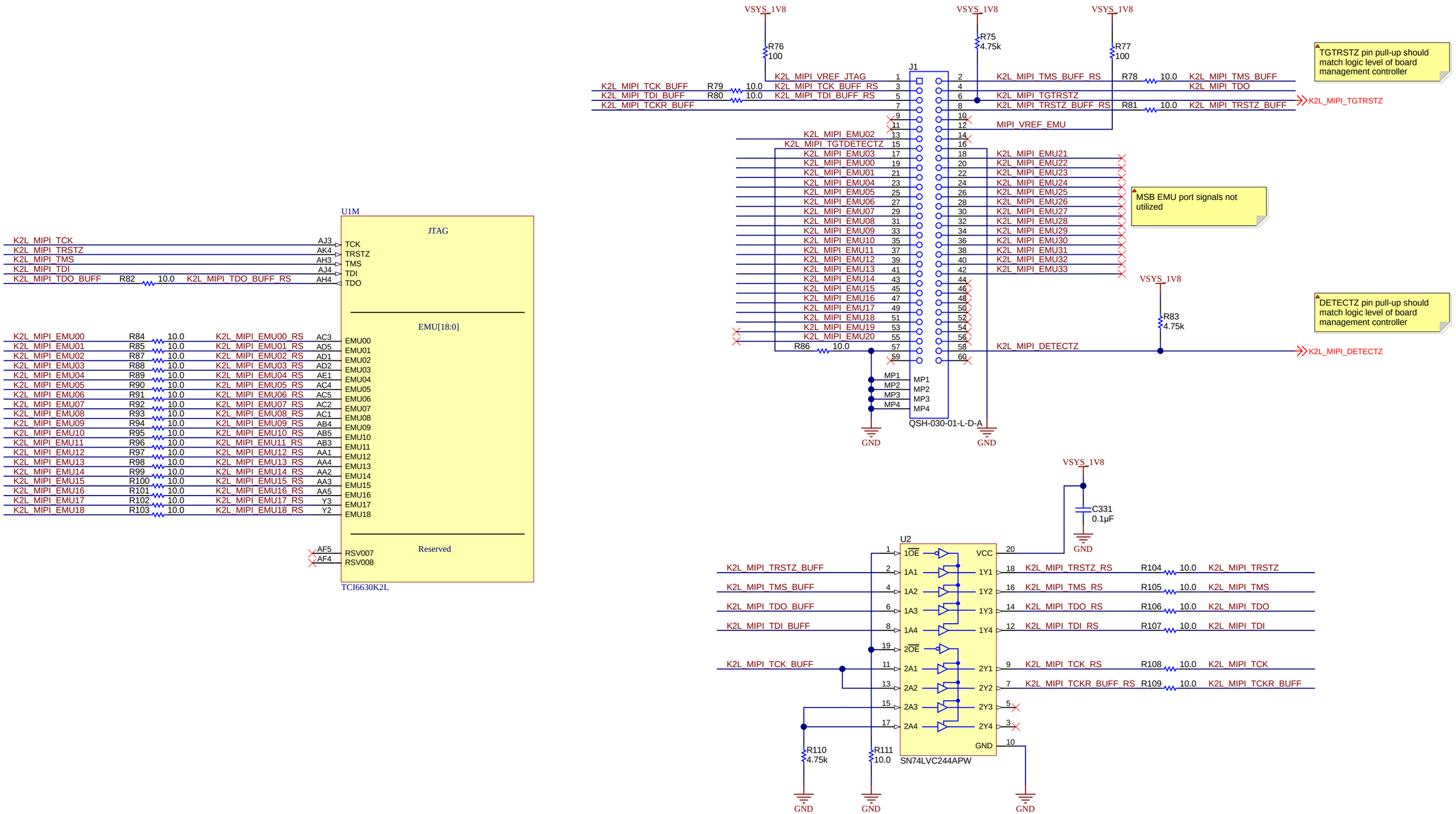
K2L JTAG and Emulation Trace Port



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TID #: TIDEP00XX		Project Title: TI 66AK2L06 DSP+ARM® Processor JESD204B Att	
Number: TIDEP0081	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: k2l_adjacent_market_solution	Sheet 13 of 38
Drawn By:		File: k2l_soc_07.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

For schematic and layout recommendations and requirements see the K2L product page linked below.

[TI 66AK2L06 Product Page]

JESD204B SERDES shall be routed according to routing rules specified in the Keystone 2 SERDES User Guide (SPRUH03)

Keystone2 SERDES User Guide (SPRUHO3)

DFE JESD204B SERDES

JESDRX[3:0] input from ADC

JESDTX[3:0] Output to DAC

K2L JESD SERDES0/1 reference clock sourced by LMK04828. When utilizing LVDS outputs of LMK04828 no AC-coupling or external bias or termination network is necessary.

JESD204B SYSREF and SYNC shall be utilized according to DFE User Guide (SPRUHX8) and routed according to Keystone 2 Hardware Design Guide (SPRAVB0) DFE peripheral section.

Keystone2 Hardware Design Guide (SPRAVB0)

DFE JESD204B SYSREF, SYNCIN/OUT and DFE I/O

K2L SYSREF driven by LMK04828 LVDS Output - Directly compatible with K2L DFESYSREF LVDS RX input.

K2L DFESYNCIN0 driven by DAC SYNC output - Directly compatible with K2L DFESYSREF LVDS RX input.

K2L DFESYNCIN1 is unused, but routed out to test point for potential debug.

K2L DFESYNCOUT0 drives ADC SYNC input

K2L DFESYNCOUT1 is unused, but routed out to test point for potential debug.

K2L DFE GPIO used to control and sense various DAC and ADC pins.

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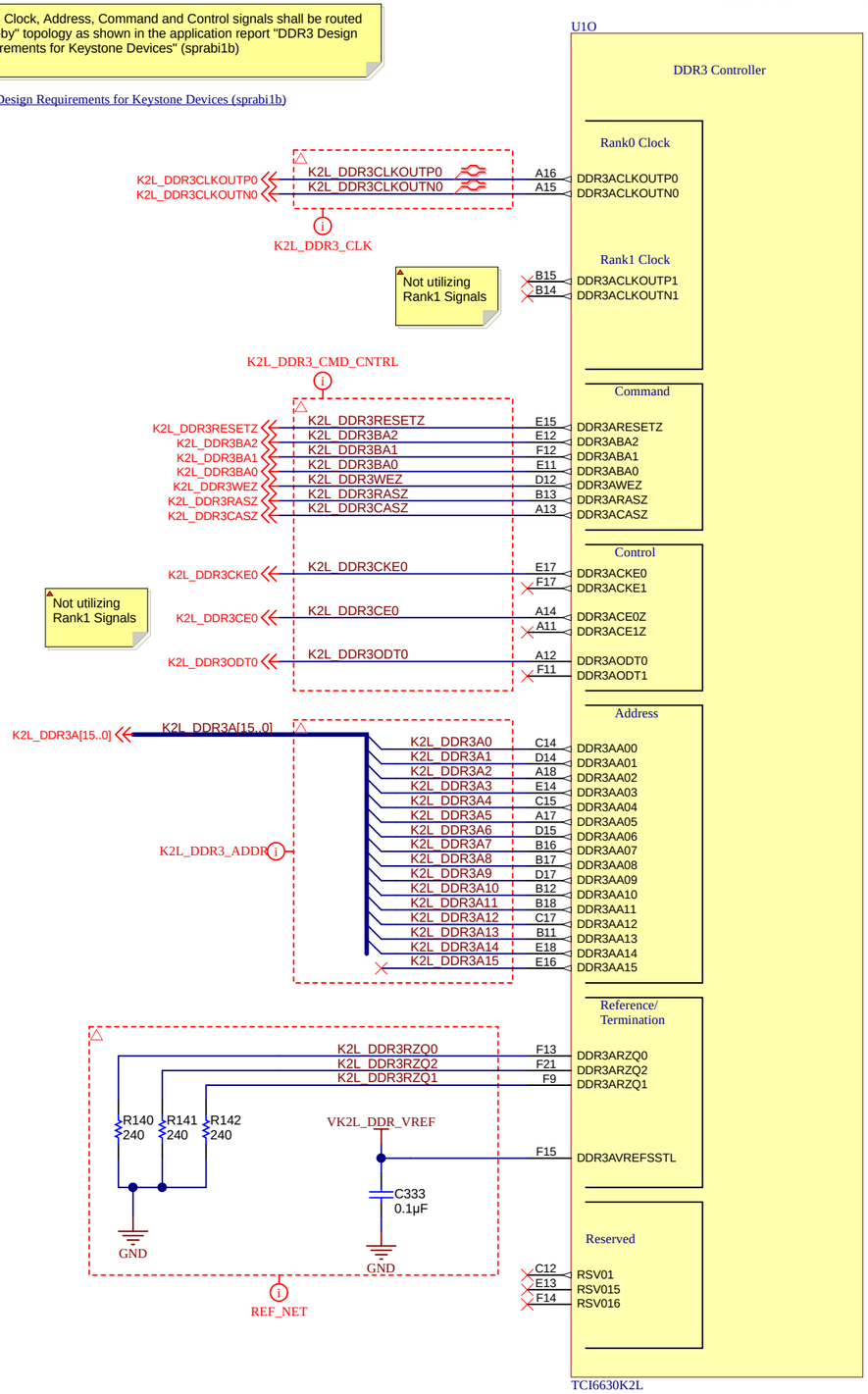
Drawn By:		File: k2l_soc_08.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

K2L DDR3 Controller - Clock, Address, Command and Control

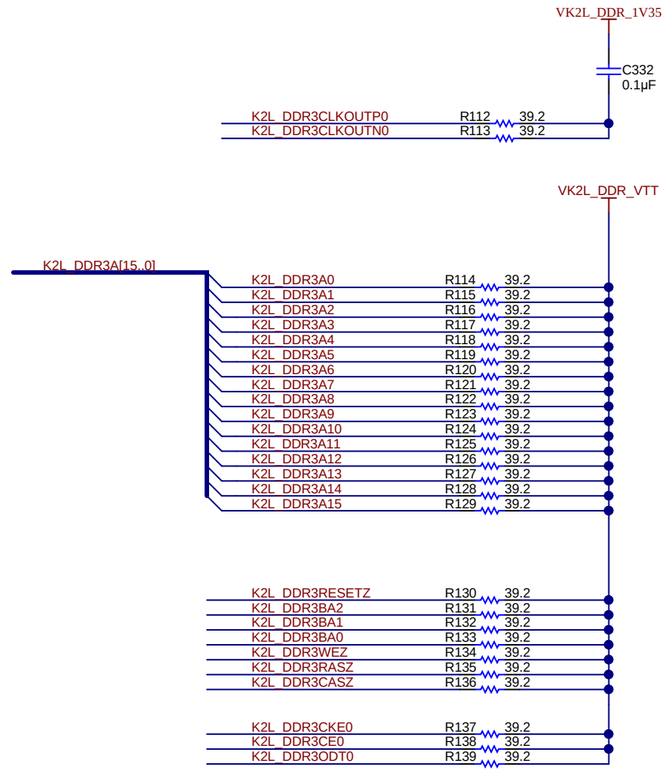
DDR3 Clock, Address, Command and Control signals shall be routed in "fly-by" topology as shown in the application report "DDR3 Design Requirements for Keystone Devices" (sprabi1b)

DDR3 Design Requirements for Keystone Devices (sprabi1b)

All termination for clock, address, command and control nets shall be placed at the end of the "fly-by" routing.



DDR3 Clock, Address, Command and Control "Fly-by" Termination



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TID #: TIDEP00XX		Project Title: TI 66AK2L06 DSP+ARM® Processor JESD204B Att	
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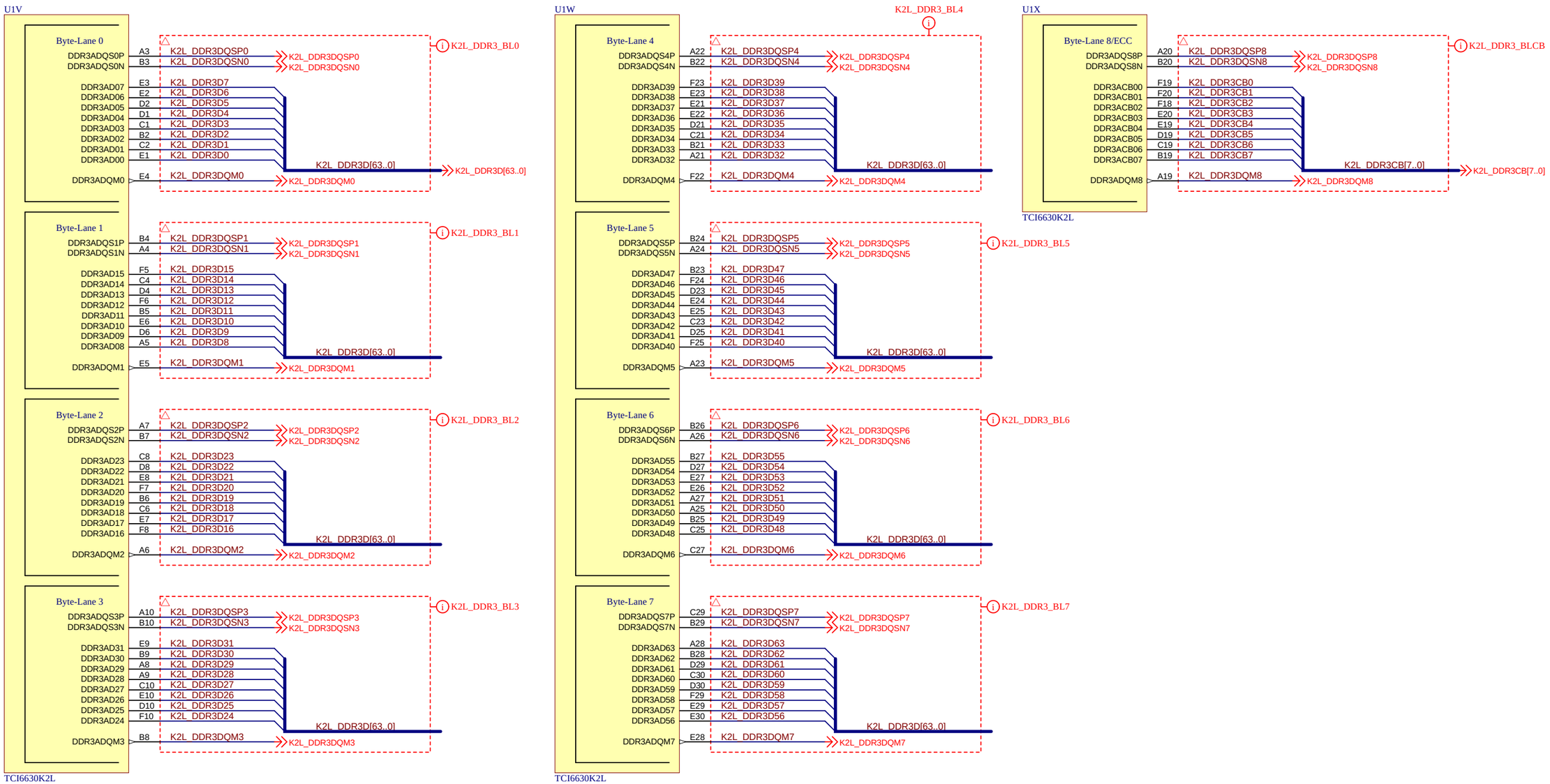
Engineer: a0271760		Contact: http://www.ti.com/support	

K2L DDR3 Controller - Data Byte-Lanes

DDR3 byte-lane signals shall be routed in point to point topology as shown in the application report "DDR3 Design Requirements for Keystone Devices" (sprabi1b)

DDR3 Design Requirements for Keystone Devices (sprabi1b)



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Drawn By:		File: k2l_soc_09_1.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

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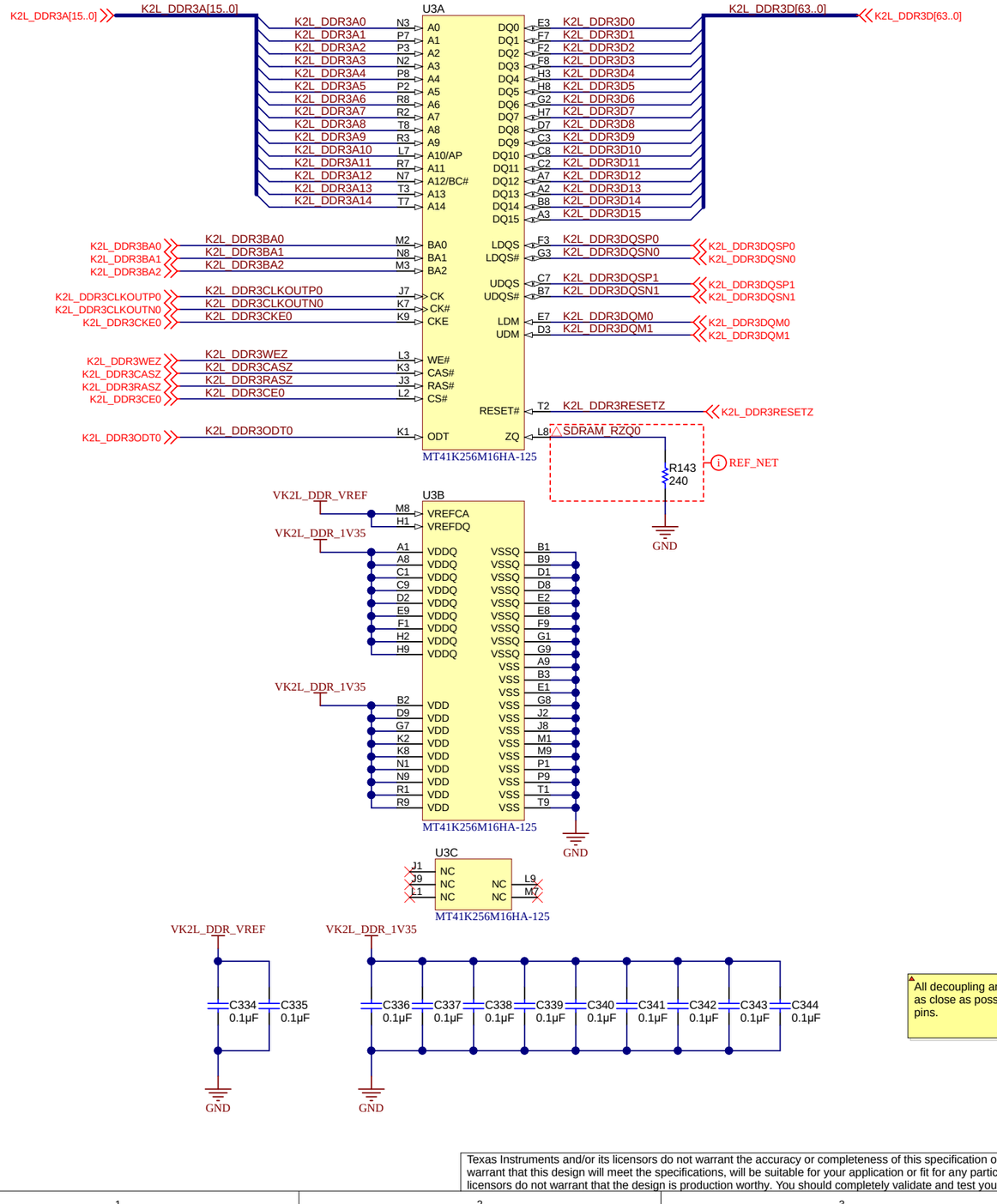
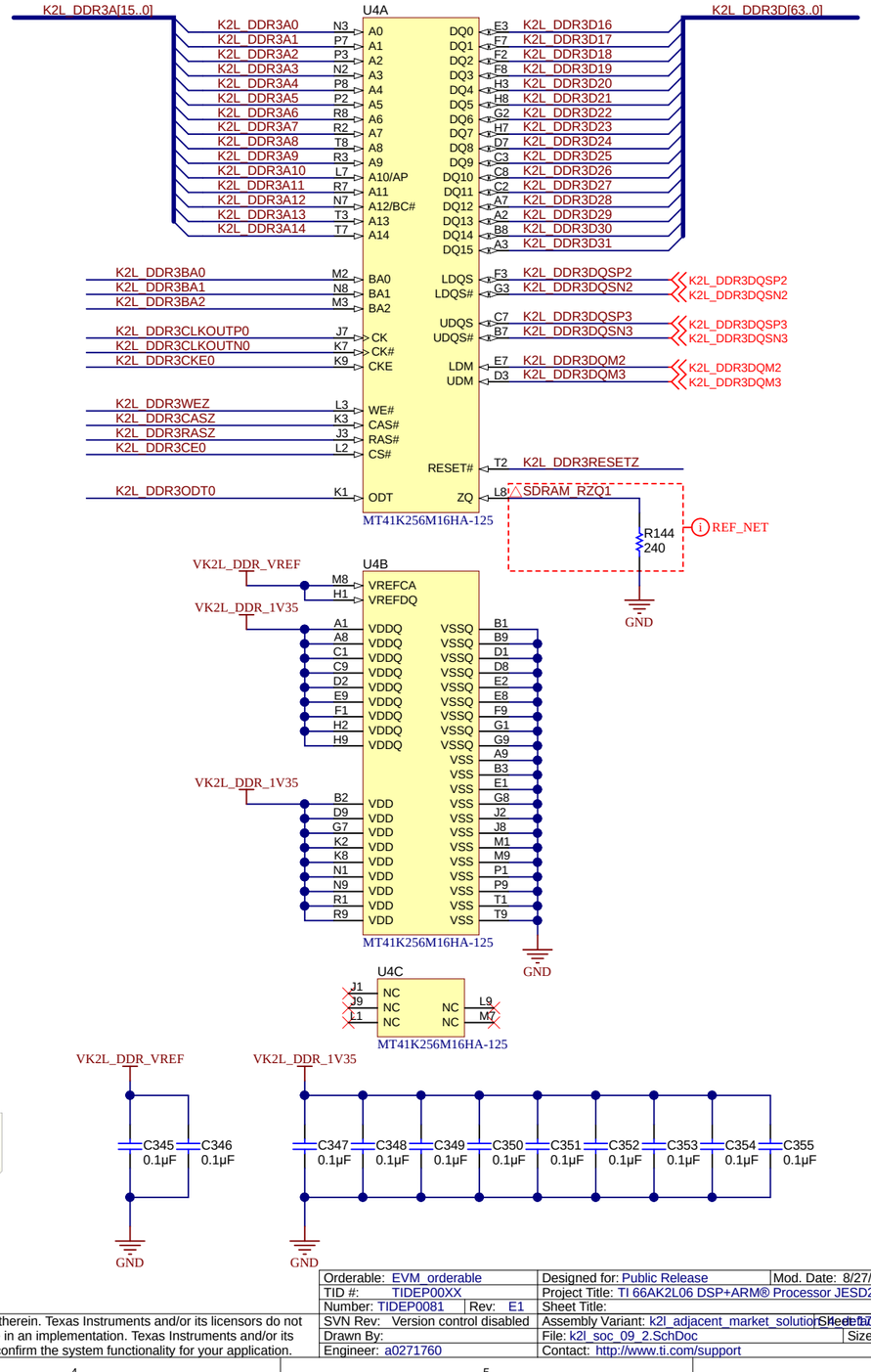
K2L DDR3 SDRAM Byte-Lane 0/1



All decoupling and ferrites shall be placed as close as possible to the SDRAM power pins.

K2L DDR3 SDRAM Byte-Lane 2/3



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TID #: TIDEP00XX		Project Title: TI 66AK2L06 DSP+ARM® Processor JESD204B Att	
Number: TIDEP0081	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: k2l_adjacent_market_solution	Sheet 7 of 38
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Engineer: a0271760		Contact: http://www.ti.com/support	

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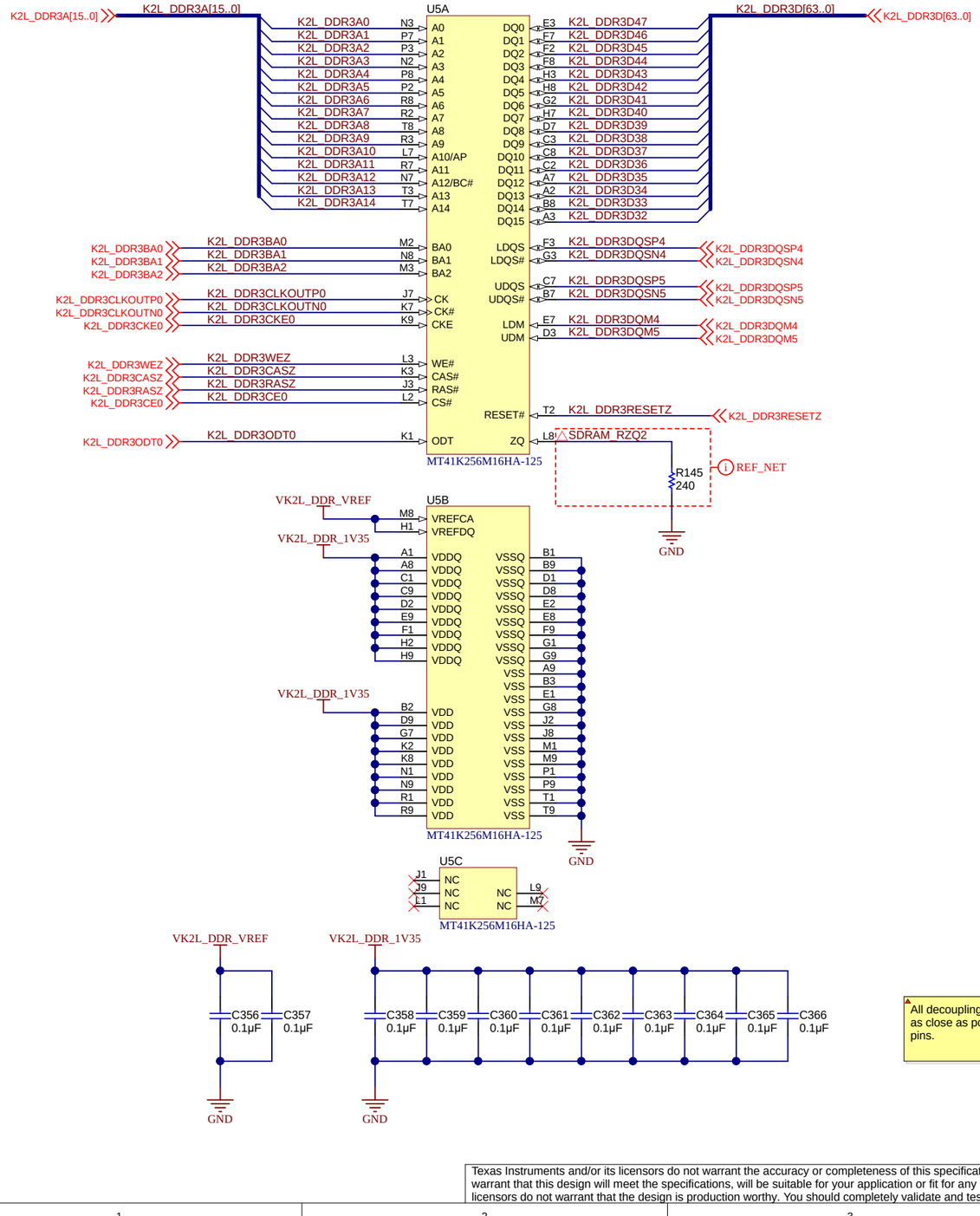
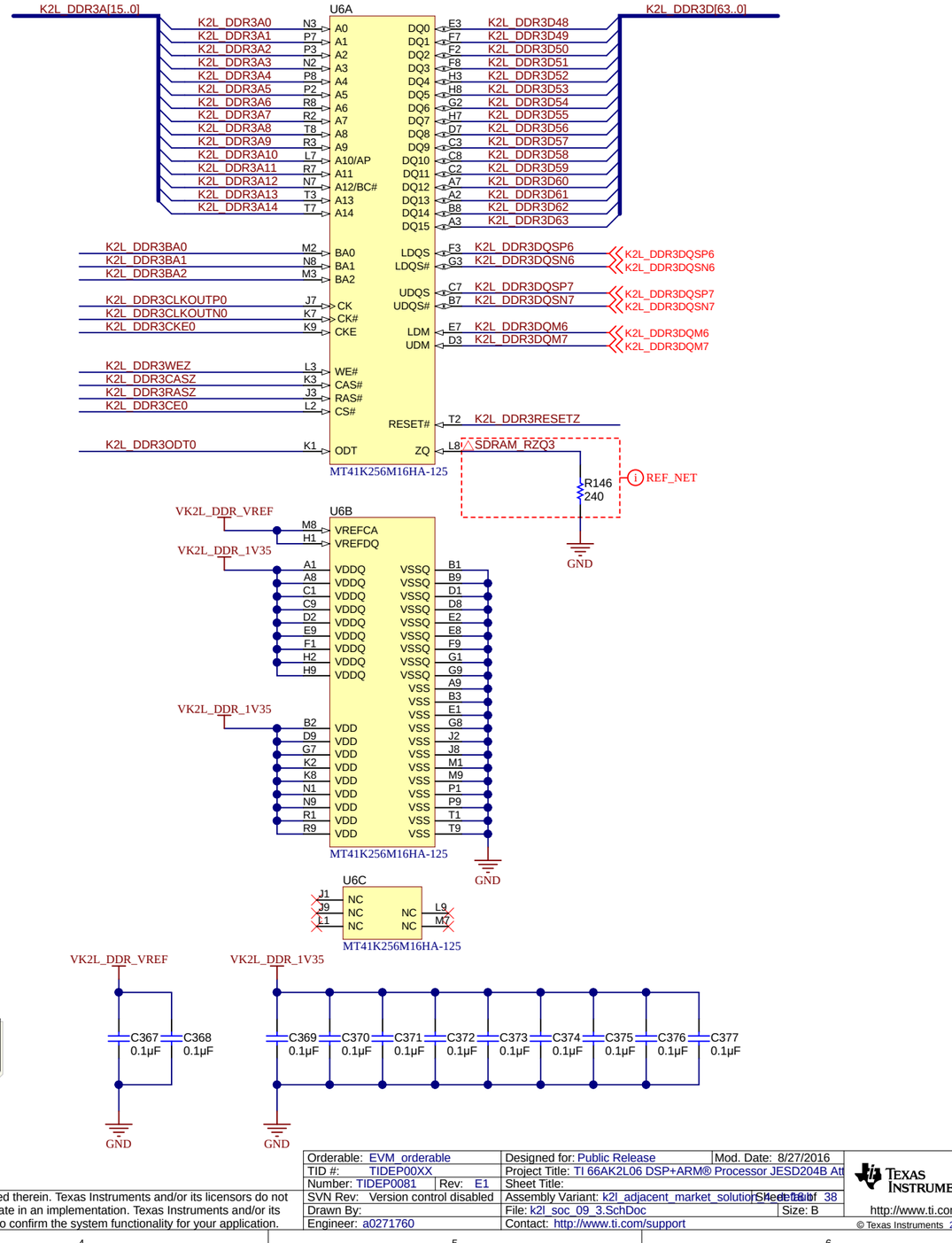
K2L DDR3 SDRAM Byte-Lane 4/5



All decoupling and ferrites shall be placed as close as possible to the SDRAM power pins.

K2L DDR3 SDRAM Byte-Lane 6/7



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TID #: TIDEP00XX		Project Title: TI 66AK2L06 DSP+ARM® Processor JESD204B Att	
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SVN Rev: Version control disabled		Assembly Variant: k2l_adjacent_market_solution	Sheet 18 of 38
Drawn By:		File: k2l_soc_09_3.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

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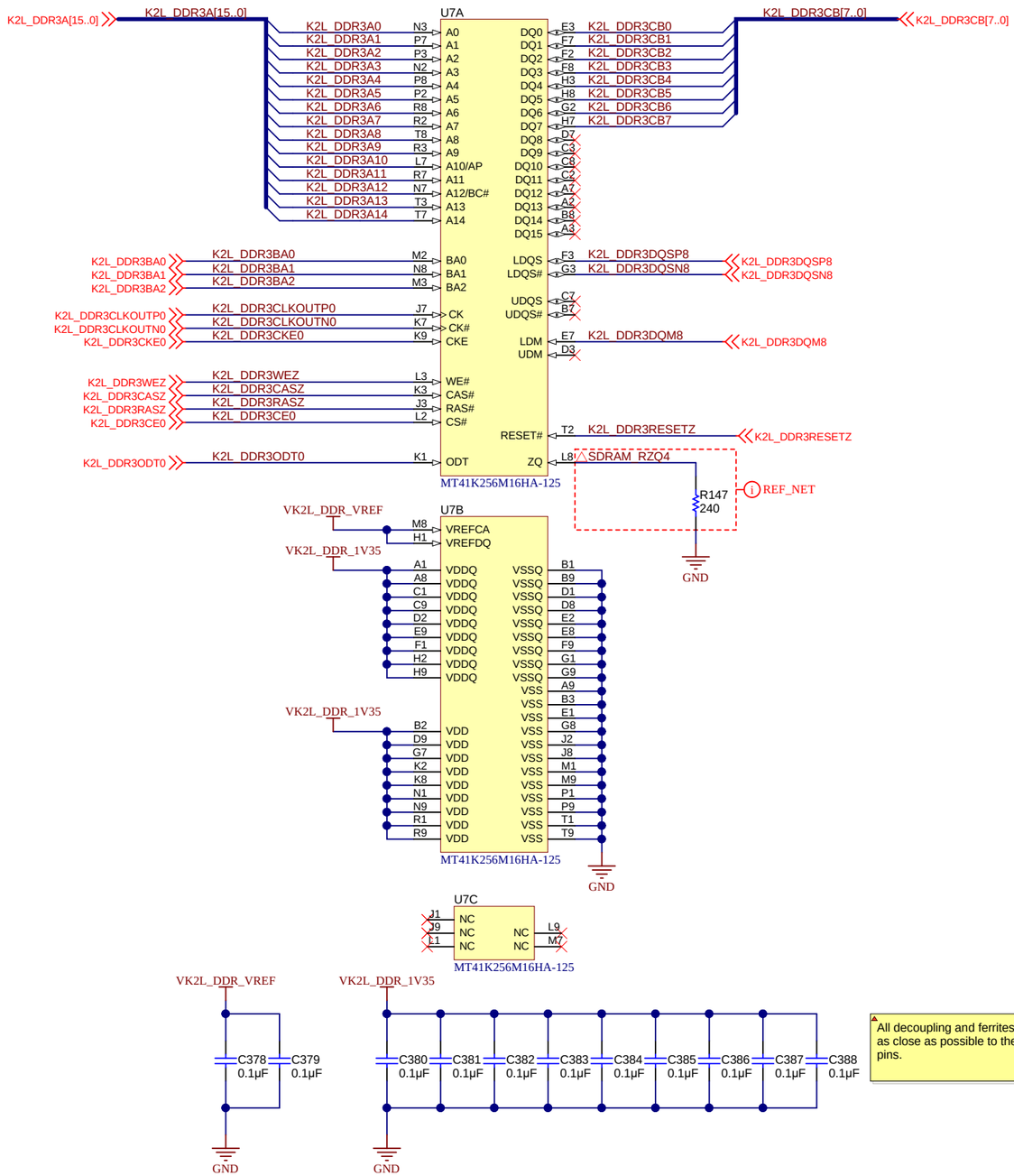
K2L DDR3 SDRAM Byte-Lane ECC



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SVN Rev: Version control disabled		Assembly Variant: k2l_adjacent_market_solution	Sheet 19 of 38
Drawn By:		File: k2l_soc_09_4.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

K2L USB Super-Speed and High-Speed Peripheral

0.1uF capacitors DC-block the bias voltage setup by the clock driver output buffer.

1k-ohm resistor divider sets up a Vp/2 common-mode bias which maximizes single-ended input margin.

Minimize stubs on P/N signals by placing capacitors inline with signal trace.

K2L_USBCLK_P/N are outputs from an clock driver (LVDS or LVPECL...etc) that meet the differential voltage swing requirements, slew-rate requirements, frequency and jitter reuqirements of the USBCLKP/N inputs.

100-ohm resistor across P/N pair provides for 100-ohm differential input termination (USBCLK buffer does not provide termination).

Place as close as possible to USBCLK BGA pins.

VK2L_0V85

R148 1.00k R149 1.00k

K2L_USBCLKP K2L_USBCLKN

K2L_USBCLKP C389 0.1µF K2L_USBCLKP_CS

K2L_USBCLKN C390 0.1µF K2L_USBCLKP_CS

R150 100

R151 1.00k R152 1.00k

GND

U1U

USB3.0

P3 USBCLKP

R3 USBCLKM

N5 USBID0

M6 USBDRVVBUS

N4 USBVBUS

M8 USBRESREF

USBDP P1 K2L_USBDP

USBDM R1 K2L_USBDM

USBTX0M M1 K2L_USBTXM C391 0.1µF K2L_USBTXM_CS

USBTX0P L1 K2L_USBTXP C392 0.1µF K2L_USBTXP_CS

USBRX0M T2 K2L_USBRXM

USBRX0P R2 K2L_USBRXP

TCI6630K2L

Place 200-ohm reference as close as possible to K2L BGA

K2L_USBDRVVBUS

K2L_USBVBUS R153 0 K2L_USBVBUS_RS

Place 0201 cap directly under K2L BGA

C393 0.01µF

GND

R154 1.00k R155 200

GND GND

REF_NET

VBUS_USB_5V0

J2

1 VBUS

K2L_USBDP 3 D+

K2L_USBDM 2 D-

K2L_USBRXP 6 SSRX+

K2L_USBRXM 5 SSRX-

K2L_USBTXP_CS 9 SSTX+

K2L_USBTXM_CS 8 SSTX-

7 GND_DRAIN

4 GND

L13 30 ohm

S1 SHIELD

S2 SHIELD

GND GND_CHASSIS

Place TVS diode as close as possible to USB3 connector. TVS diode pads shall be placed inline with USB3 signal traces.

K2L_USBDP 1 14 ED1

K2L_USBDM 2 13 ED2

K2L_USBTXM_CS 3 12 ED3

K2L_USBTXP_CS 4 11 ED4

K2L_USBRXM 6 9 ED5

K2L_USBRXP 7 8 ED6

NC1 NC2 NC3 NC4 NC5 NC6

NCG 5 GND 10

U8

GND_CHASSIS

Buffer needed for 1.8V to 5.5V logic translation so K2L can drive TPS2065 power switch EN input.

VSYS_1V8

U11

SN74LVC1G07DBVR

K2L_USBDRVVBUS R158 0 K2L_USBDRVVBUS_RS

K2L_USBDRVVBUS_INVOUT

R160 0

GND

VSYS_5V0

R156 4.75k R157 4.75k

5V, 1A, USB power switch used to allow USB controller USBDRVBUS controls VBUS to attached USB devices as well as current regulates the VBUS power net.

U9

IN OUT

FLT

EN/EN GND

TPS2065CDBVR

K15

Place switch and caps near USB3 Connector

VBUS_USB_5V0

C396 22µF C397 47µF C395 100µF

GND

VSYS_5V0

C399 1µF C400 1µF

Place caps near IC pins

GND

TPS2291 provides 5V power isolation for the K2L USB controller during startup power on sequence.

K2L_USBVBUS_EN driven by power sequencing logic.

VBUS_USB_5V0 U10

A2 VIN VOUT A1 K2L_USBVBUS

K2L_USBVBUS_EN K2L_USBVBUS_EN B2 ON GND B1

TPS22913BYZVR

R159 1.00k

C394 1µF

GND GND

USB_VBUS

C398 1µF Place caps near IC pins

GND

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Number: TIDEP0081	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: k2l_adjacent_market_solution	Sheet 20 of 38
Drawn By:		File: k2l_soc_10.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

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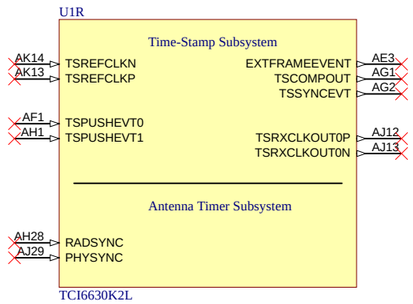
K2L Time-Stamp (IEEE1588) Peripheral

Time-Stamp peropheral not utilized.



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SVN Rev: Version control disabled		Assembly Variant: k2l_adjacent_market_solution	Sheet 21 of 38
Drawn By:		File: k2l_soc_12.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

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K2L EMIF16 Interface

U1T

EMIF16

K2L_EMIFCE0Z	R161	10.0	K2L_EMIFCE0Z_RS	N30	EMIFCE0Z	EMIFD00	U26	K2L_EMIFD00_RS	R162	10.0	K2L_EMIFD00	H4	IO0
				U30	EMIFCE1Z	EMIFD01	AB28	K2L_EMIFD01_RS	R163	10.0	K2L_EMIFD01	J4	IO1
				W29	EMIFCE2Z_UART3RTS	EMIFD02	W27	K2L_EMIFD02_RS	R164	10.0	K2L_EMIFD02	K4	IO2
				P30	EMIFCE3Z_UART3CTS	EMIFD03	AC28	K2L_EMIFD03_RS	R165	10.0	K2L_EMIFD03	K5	IO3
						EMIFD04	Y27	K2L_EMIFD04_RS	R166	10.0	K2L_EMIFD04	K6	IO4
K2L_EMIFOEZ	R167	10.0	K2L_EMIFOEZ_RS	T30	EMIFOEZ	EMIFD05	AB27	K2L_EMIFD05_RS	R168	10.0	K2L_EMIFD05	J7	IO5
K2L_EMIFWEZ	R169	10.0	K2L_EMIFWEZ_RS	V30	EMIFWEZ	EMIFD06	AA27	K2L_EMIFD06_RS	R170	10.0	K2L_EMIFD06	K7	IO6
K2L_EMIFRNW	R171	10.0	K2L_EMIFRNW_RS	M30	EMIFRNW	EMIFD07	V26	K2L_EMIFD07_RS	R172	10.0	K2L_EMIFD07	J8	IO7
						EMIFD08	AD27					H3	NC/IO8
K2L_EMIFBE0Z	R174	10.0	K2L_EMIFBE0Z_RS	AB30	EMIFBE0Z	EMIFD09	AC27					J3	NC/IO9
				P29	EMIFBE1Z	EMIFD10	W26					H5	NC/IO10
						EMIFD11	AD26					J5	NC/IO11
K2L_EMIFWAIT0				Y30	EMIFWAIT0	EMIFD12	AC26					H6	NC/IO12
K2L_EMIFWAIT1				AC30	EMIFWAIT1	EMIFD13	AA26					G6	NC/IO13
						EMIFD14	Y26					H7	NC/IO14
						EMIFD15	AB26					G7	NC/IO15
				W30	EMIFA00_GPIO32								
				R29	EMIFA01_GPIO33								
				R30	EMIFA02_GPIO34								
				P28	EMIFA03_GPIO35								
				P26	EMIFA04_GPIO36								
				R26	EMIFA05_GPIO37								
				V29	EMIFA06_GPIO38								
				AA30	EMIFA07_GPIO39								
				T29	EMIFA08_GPIO40								
				R28	EMIFA09_GPIO41								
				P27	EMIFA10_GPIO42								
K2L_EMIFA11	R177	10.0	K2L_EMIFA11_RS	AD30	EMIFA11								
K2L_EMIFA12	R178	10.0	K2L_EMIFA12_RS	V28	EMIFA12								
				Y29	EMIFA13_GPIO43								
				T28	EMIFA14_GPIO44								
				Y28	EMIFA15_GPIO45								
				T26	EMIFA16_GPIO46								
				T27	EMIFA17_GPIO47								
				R27	EMIFA18_UART2RTS								
				AC29	EMIFA19_UART2CTS								
				AB29	EMIFA20_UART2RXD								
				U27	EMIFA21_UART2TXD								
				W28	EMIFA22_UART3RXD								
				V27	EMIFA23_UART3TXD								

TCI6630K2L

VSYS_1V8

R173 4.75k

2Gbyte, x8 NAND Flash

U12

K2L_EMIFCE0Z	C6	CE#	VCC	J6		
K2L_EMIFWAIT0	C8	R/B#	VCCQ	H8		
K2L_EMIFA12	D5	CLE	NC_VCC1	D3		
K2L_EMIFA11	C4	ALE	NC_VCC2	G4		
K2L_EMIFWEZ	C7	WE#				
K2L_EMIFOEZ	D4	RE#				
			NC1	A1		
			NC2	A2		
			NC3	A9		
			NC4	A10		
			NC5	B1		
			NC6	B9		
			NC7	B10		
			NC8	L1		
			NC9	L2		
			NC10	L9		
			NC11	L10		
			NC12	M1		
			NC13	M2		
			NC14	M9		
			NC15	M10		
			NC16	D6		
			NC17	D7		
			NC18	D8		
			NC19	E3		
			NC20	E4		
			NC21	E5		
			NC22	E6		
			NC23	E7		
			NC24	E8		
			NC25	F3		
			NC32	G8		
NAND_LOCKPRE	G5	LOCKPRE/DNU	WP#	C3		
	G3	DNU				
	F4	NC26	VSS3	K8		
	F5	NC27	VSS2	K3		
	F6	NC28	VSS1	C5		
	F8	NC29	NC_VSS1	F7		

MT29F16G08ADBCAH4:C

VSYS_1V8

C401 1µF C402 1µF C403 1µF C404 10µF

GND

VSYS_1V8

R175 4.75k

R179 4.75k

GND

VSYS_1V8

R176 4.75k

R180 4.75k

GND

MCU_NAND_WP_EN#

WP# pin driven by Board Management Controller (microcontroller)

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Number: TIDEP0081	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: k2l_adjacent_market_solution	Sheet 22 of 38
Drawn By:		File: k2l_soc_13.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

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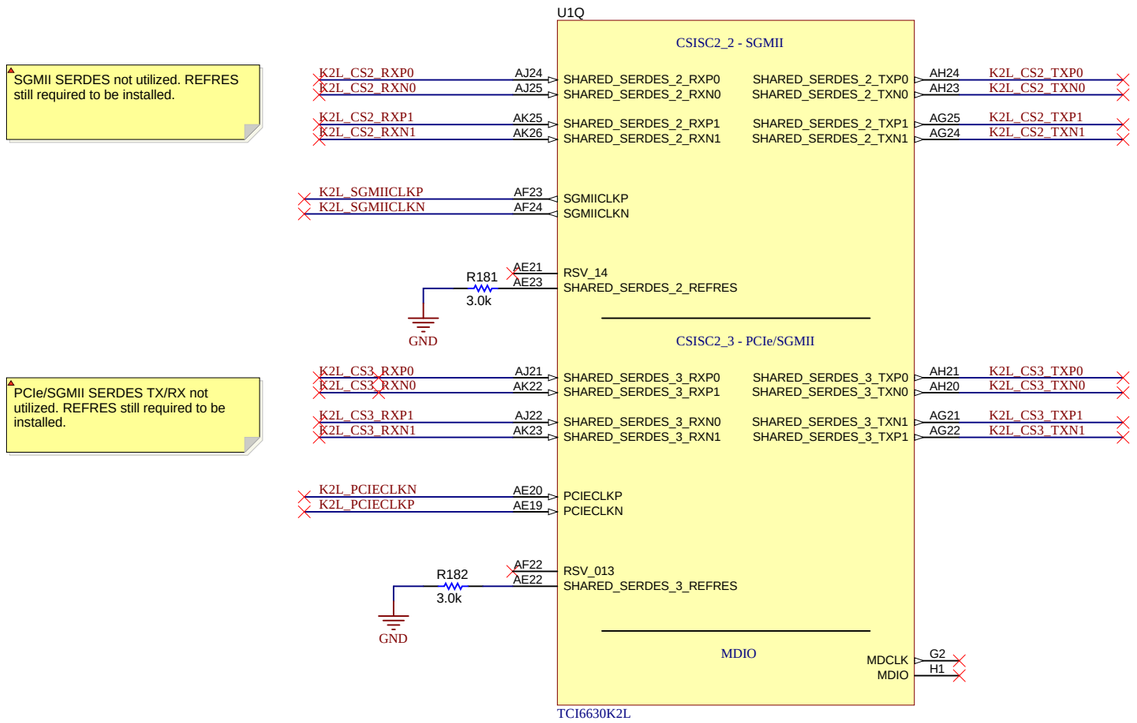
K2L PCIe and SGMII Interfaces



Orderable: EVM_orderable	Designed for: Public Release	Mod. Date: 8/27/2016
TID #: TIDEP00XX	Project Title: TI 66AK2L06 DSP+ARM® Processor JESD204B Att	
Number: TIDEP0081 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: k2l_adjacent_market_solution	Sheet 23 of 38
Drawn By:	File: k2l_soc_14.SchDoc	Size: B
Engineer: a0271760	Contact: http://www.ti.com/support	

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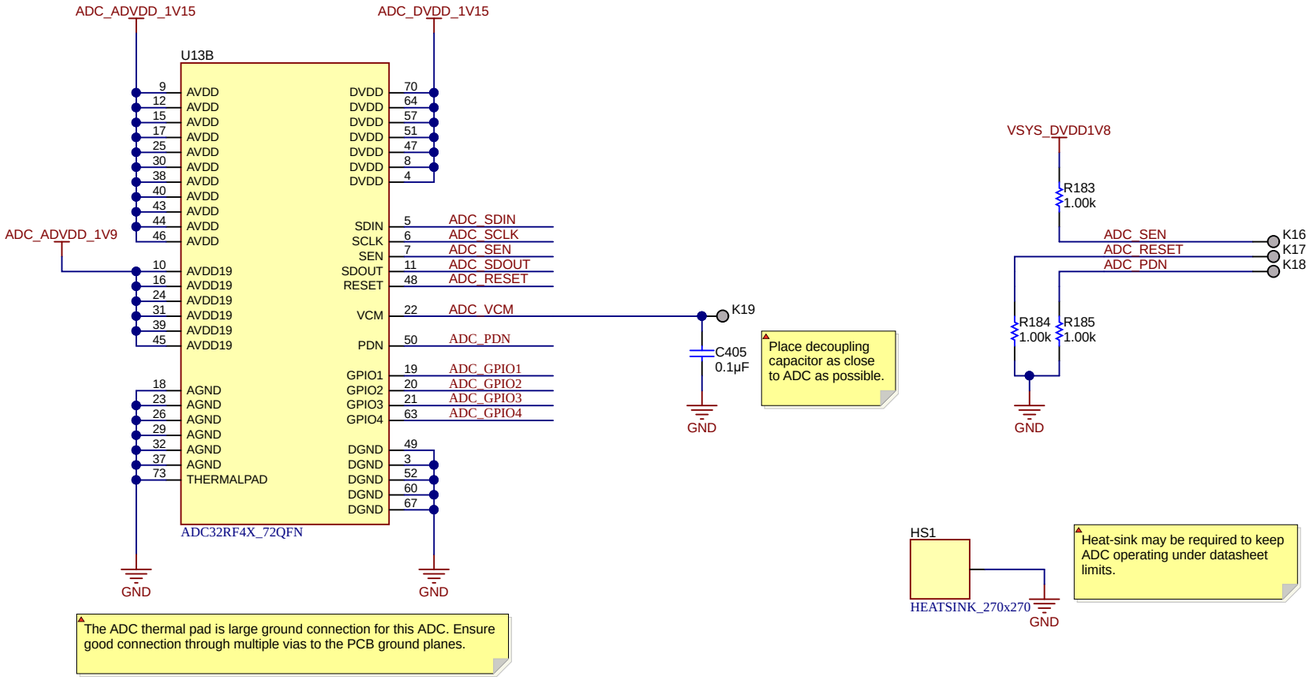
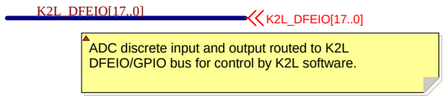
ADC Power Pins, Decoupling Capacitors GPIO, SDIO



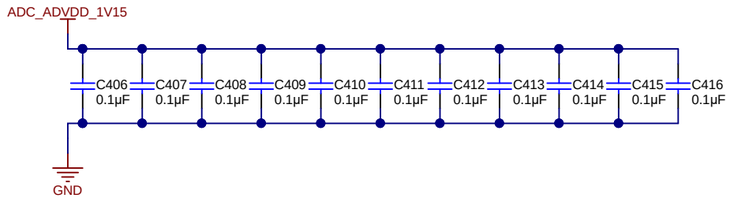


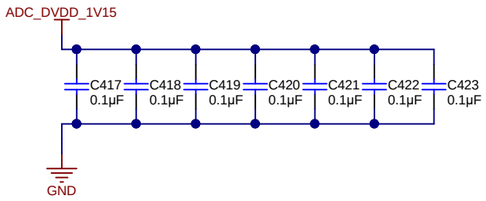
ADC digital inputs VIH = 0.8V, VIL = 0.4V
ADC digital outputs VOH = AVDD19 (1.9V), VOL = 0.1V
Directly compatible with K2L LVCMOS18 GPIO buffers

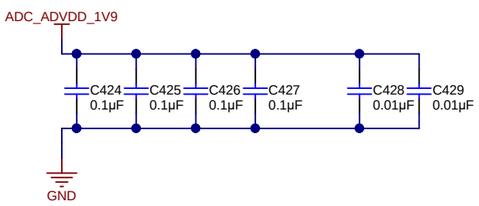
ADC_PDN	R186	10.0	K2L_DFEIO2
ADC_RESET	R187	10.0	K2L_DFEIO3
ADC_GPIO1	R188	10.0	K2L_DFEIO4
ADC_GPIO2	R189	10.0	K2L_DFEIO5
ADC_GPIO3	R190	10.0	K2L_DFEIO6
ADC_GPIO4	R191	10.0	K2L_DFEIO7
ADC_SCLK	R192	10.0	K2L_SPI0CLK
ADC_SEN	R193	10.0	K2L_SPI0SCS0
ADC_SDIN	R194	10.0	K2L_SPI0SIMO
ADC_SDOUT	R195	10.0	K2L_SPI0SOMI

K2L_SPI0CLK
K2L_SPI0SCS0
K2L_SPI0SIMO
K2L_SPI0SOMI

Decoupling caps shall be placed as close to ADC power pins as possible.







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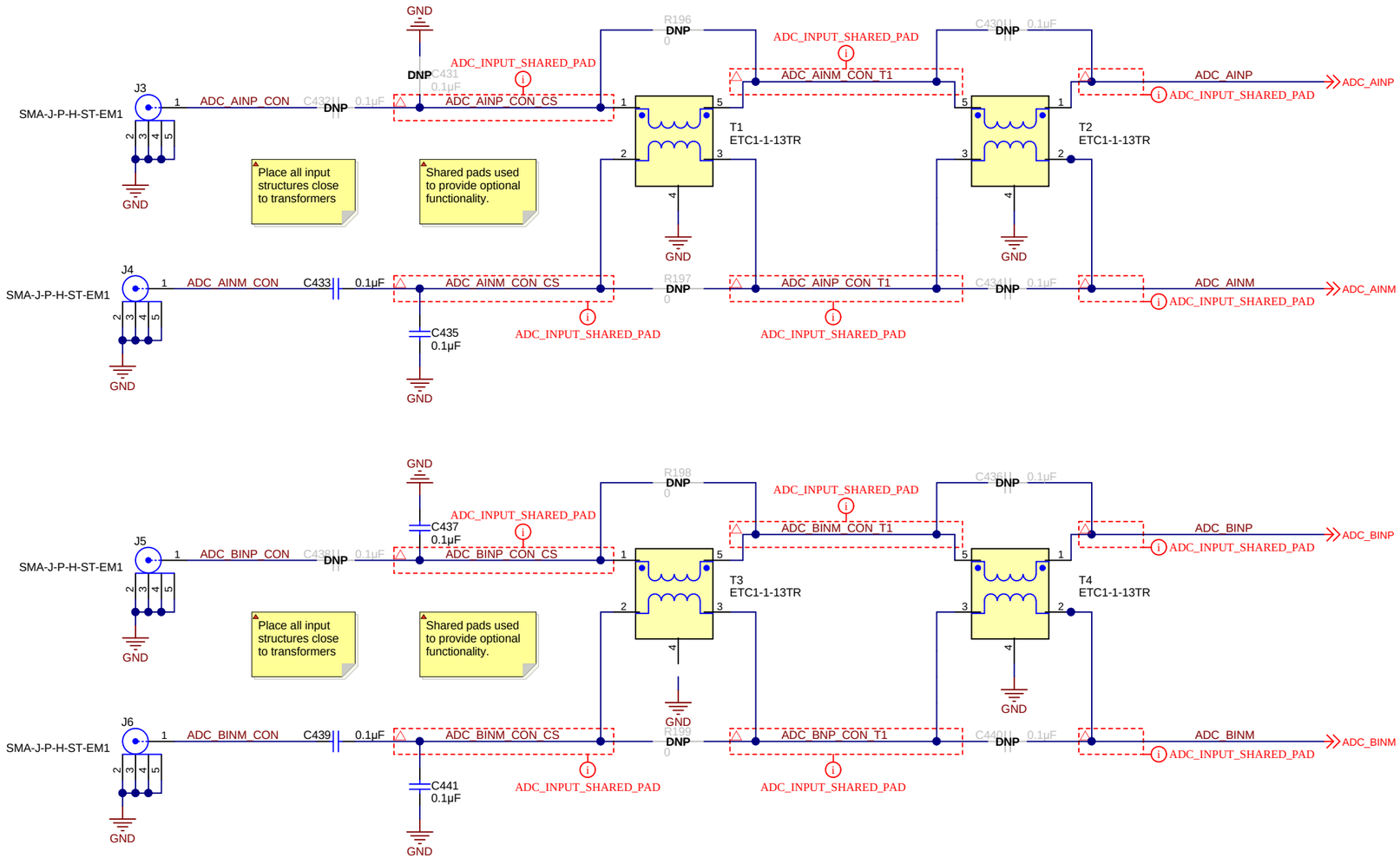
Number: TIDEP0081 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: k2l_adjacent_market_solution Sheet 2 of 38	
Drawn By:	File: adc32rf4x_01.SchDoc	Size: B
Engineer: a0271760	Contact: http://www.ti.com/support	

ADC Analog Input Filtering and Balancing

Default resistor/capacitor configuration matching ADC32RF4x EVM

Exact transformer characteristics should be chosen based on bandwidth of interest for signals being detected. Please see the ADC32RF80/45 collateral for additional design considerations.

All ADC input channel signal paths shall be routed as 50-ohm characteristic impedance paths.



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Number: TIDEP0081 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: k2l_adjacent_market_solution	Sheet 25 of 38
Drawn By:	File: adc32rf4x_02.SchDoc	Size: B
Engineer: a0271760	Contact: http://www.ti.com/support	

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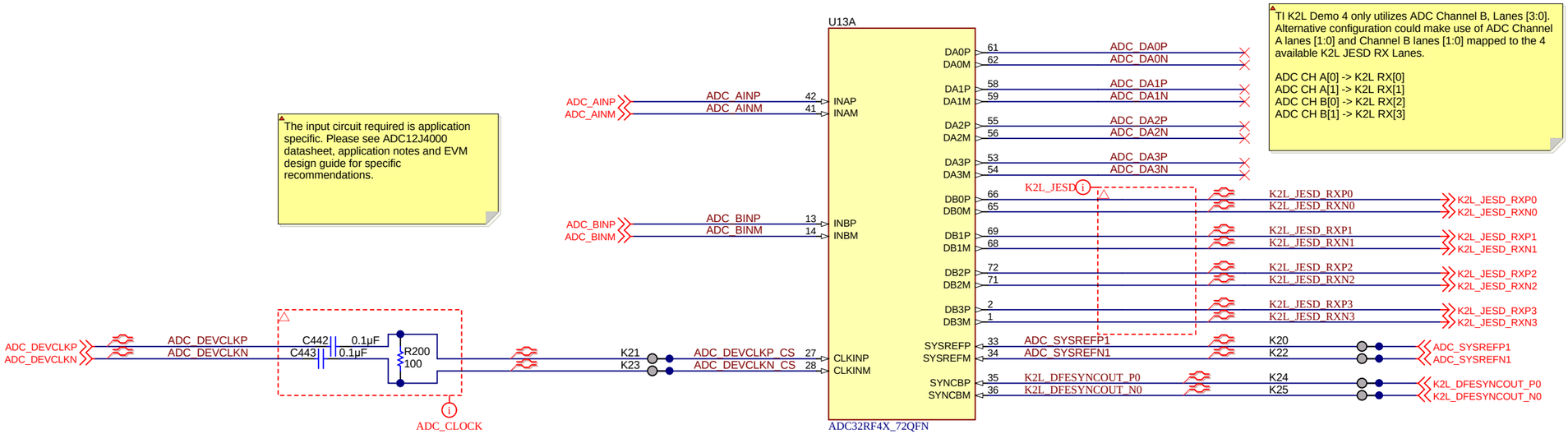
ADC Analog Input, Reference Clock Input and JESD204 Interface to K2L SoC

The input circuit required is application specific. Please see ADC12J4000 datasheet, application notes and EVM design guide for specific recommendations.

TI K2L Demo 4 only utilizes ADC Channel B, Lanes [3:0]. Alternative configuration could make use of ADC Channel A lanes [1:0] and Channel B lanes [1:0] mapped to the 4 available K2L JESD RX Lanes.

ADC CH A[0] -> K2L RX[0]
ADC CH A[1] -> K2L RX[1]
ADC CH B[0] -> K2L RX[2]
ADC CH B[1] -> K2L RX[3]



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Number: TIDEP0081 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: k2l_adjacent_market_solution Sheet 26 of 38	
Drawn By:	File: adc32rf4x_03.SchDoc	Size: B
Engineer: a0271760	Contact: http://www.ti.com/support	

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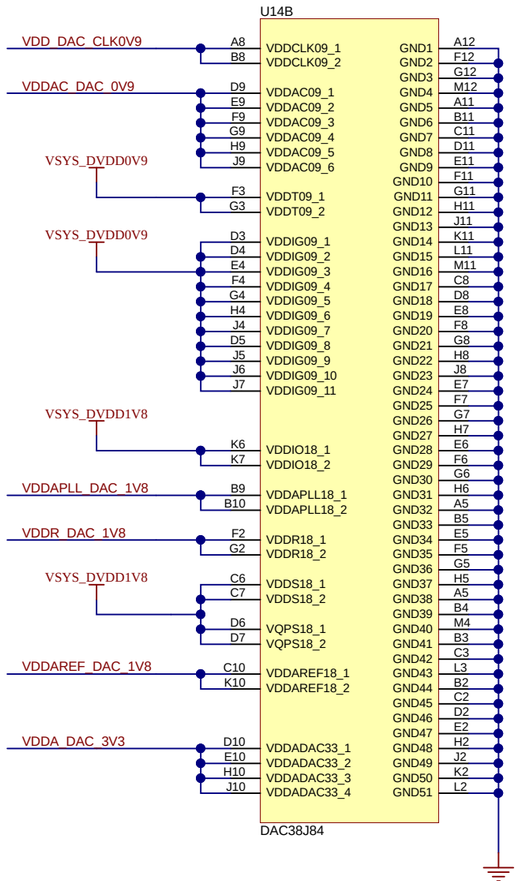
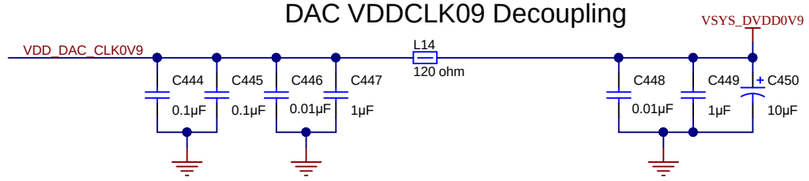
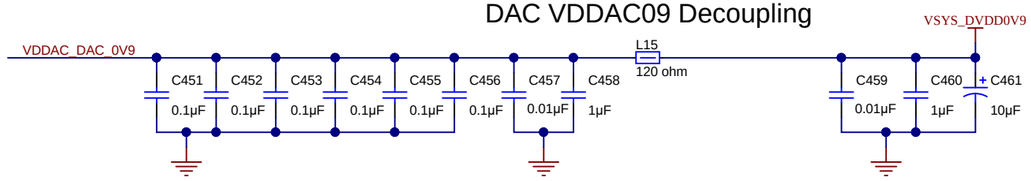
DAC Power Pins, Decoupling Capacitors



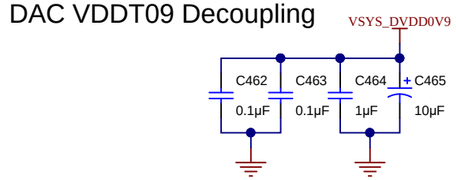
DAC VDDCLK09 Decoupling



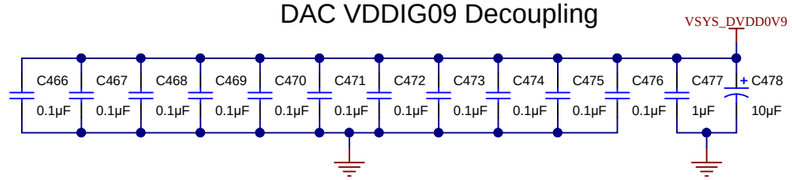
DAC VDDAC09 Decoupling



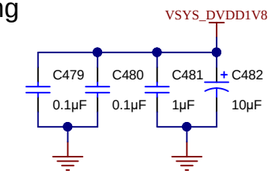
DAC VDDT09 Decoupling



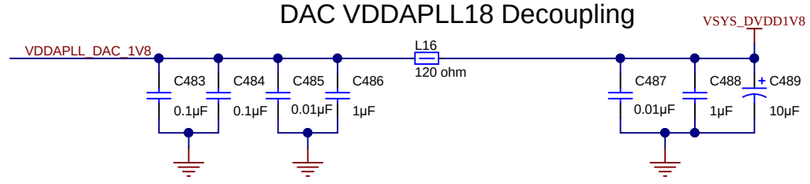
DAC VDDIG09 Decoupling



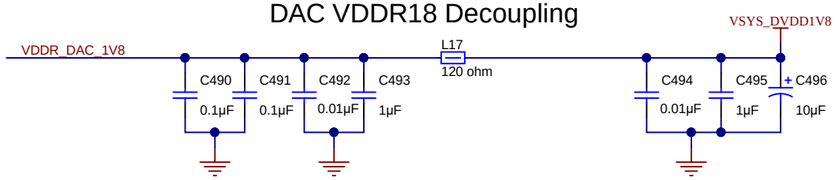
DAC VDDIO18 Decoupling



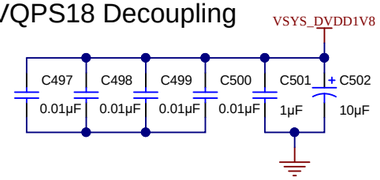
DAC VDDAPLL18 Decoupling



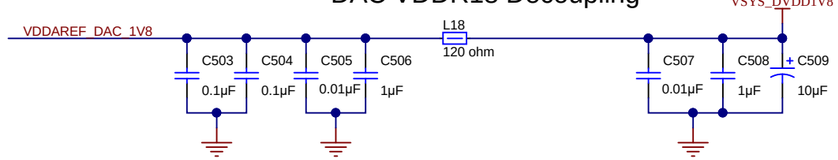
DAC VDDR18 Decoupling



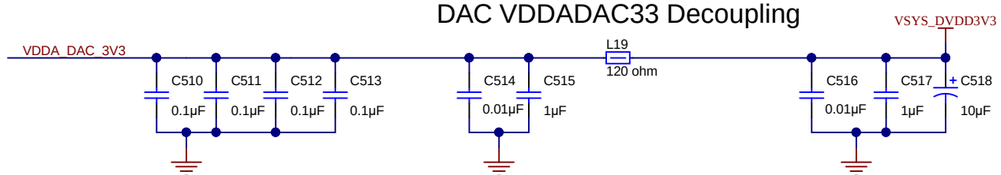
DAC VDDS18/VQPS18 Decoupling



DAC VDDR18 Decoupling



DAC VDDADAC33 Decoupling



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SVN Rev: Version control disabled		Assembly Variant: k2l_adjacent_market_solution	Sheet 27 of 38
Drawn By:		File: dac38j84_01.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

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DAC Output, JESD204B Interface, SPI and Discrete I/O Control

For schematic and layout recommendations and requirements see the DAC38J84 product page linked below.

TI DAC38J84 Product Page

Optional external low-pass filter element. Shall be placed as close as possible to DAC BGA.

Please see DAC38J84 datasheet, application notes and EVM design guide for specific recommendations.

K2L_DFEIO[17..00] — K2L_DFEIO[17..00]

DAC discrete input and output routed to K2L DFEIO/GPIO bus for control by K2L software.

DAC DACCLK driven by LMK04828 LVPECL source.

DAC SYSREF driven by LMK04828 LVPECL source.

U14A

DAC_DACCLKP / DAC_DACCLKN → C520 0.1µF, C522 0.1µF → DAC_DACCLKP_CS / DAC_DACCLKN_CS → A10 / A9 → DACCLKP / DACCLKN

DAC_SYSREFP / DAC_SYSREFN → C523 0.1µF, C524 0.1µF → DAC_SYSREFP_CS / DAC_SYSREFN_CS → A7 / A6 → SYSREFP / SYSREFN

LPF — C9 — R202 0 — R201 1.00k — C519 1000pF — C521 0.1µF — GND — REF_NET

RX7P / RX7N ← A3 / A2
RX6P / RX6N ← B1 / A1
RX5P / RX5N ← C1 / D1
RX4P / RX4N ← F1 / E1

K2L_JESD_TXP3 / K2L_JESD_TXN3 → C525 0.1µF, C526 0.1µF → K2L_JESD_TXP3_CS / K2L_JESD_TXN3_CS → M3 / M2 → RX3P / RX3N

K2L_JESD_TXP2 / K2L_JESD_TXN2 → C527 0.1µF, C528 0.1µF → K2L_JESD_TXP2_CS / K2L_JESD_TXN2_CS → L1 / M1 → RX2P / RX2N

K2L_JESD_TXP1 / K2L_JESD_TXN1 → C529 0.1µF, C530 0.1µF → K2L_JESD_TXP1_CS / K2L_JESD_TXN1_CS → K1 / J1 → RX1P / RX1N

K2L_JESD_TXP0 / K2L_JESD_TXN0 → C531 0.1µF, C532 0.1µF → K2L_JESD_TXP0_CS / K2L_JESD_TXN0_CS → G1 / H1 → RX0P / RX0N

IOUTAP / IOUTAN → B12 / C12 → DAC_OUT0P / DAC_OUT0N → DAC_OUT0P / DAC_OUT0N

IOUTBP / IOUTBN → E12 / D12 → DAC_OUT1P / DAC_OUT1N → DAC_OUT1P / DAC_OUT1N

IOUTCP / IOUTCN → H12 / J12 → DAC_OUT2P / DAC_OUT2N → DAC_OUT2P / DAC_OUT2N

IOUTDP / IOUTDN → L12 / K12 → DAC_OUT3P / DAC_OUT3N → DAC_OUT3P / DAC_OUT3N

The output circuit required for the DAC is application specific. Please see DAC38J84 datasheet, application notes and EVM design guide for specific recommendations.

TXENABLE ← K5 ← K2L_DFEIO9 ← K26

EXTIO ← F10 ← DAC_EXTIO ← K27 — C533 0.1µF — GND

RBIAS ← G10 ← DAC_RBIAS — R204 1.91k — GND

R203 10.0k — GND

DAC_SYNCBP / DAC_SYNCBN → DAC_SYNCBP / DAC_SYNCBN → B7 / B6 → SYNCBP / SYNCBN

K28 / K29 → DAC_AMUX0 / DAC_AMUX1 → H3 / E3 → AMUX0 / AMUX1

DAC38J84

Rbias controls the full-scale current output according to datasheet equation:

IOUTFS = (coarse_dac + 1) /16 x IBIAS x 64 = (coarse_dac + 1) /16 x VEXTIO / RBIAS x 64

U14C

DAC SPI port mastered by K2L SPI_1

K2L_SPI1SIMO → K2L_DAC_SPI1SIMO → K30 → L10 → SDIO
K2L_SPI1SCS0 → K2L_DAC_SPI1SCS0 → K32 → M9 → SDENB
K2L_SPI1CLK → K2L_DAC_SPI1CLK → K34 → L9 → SCLK
K2L_SPI1SOMI → K2L_DAC_SPI1SOMI_RS — R205 10.0 — K36 → M10 → SDO

IFORCE ← C5 ← DAC_IFORCE ← K31
VSENSE ← C4 ← DAC_VSENSE ← K33
ATEST ← K9 ← DAC_ATEST ← K35
ALARM ← L8 ← DAC_ALARM ← K37
TESTMODE ← K3 ← DAC_TESTMODE ← K38

JTAG interface not utilized. JTAG subsystem held in reset per datasheet insuctions by TRSTB tied to GND.

TCLK ← K4
TDI ← L5
TDO ← M5
TMS ← L4
TRSTB ← J3

SYNC_N_AB ← L6
SYNC_N_CD ← L7

TI K2L Demo 4 software shall utilize the differential, LVDS SYNCBP/N interface. Utilizing the SYNC_AB and SYNC_CD pins is an optional usage of the K2L DFEIO pins to recieve the SYNC signal from the DAC.

See DAC38J84 datasheet for implemenation details.

K39 → K2L_DFEIO10 → K8 → RESETB — R206 10.0k — GND
K40 → K2L_DFEIO11 → M8 → SLEEP — R207 10.0k — GND

NC3 ← M6
NC4 ← M7

R208 0 — GND

DAC38J84

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SVN Rev: Version control disabled		Assembly Variant: k2l_adjacent_market_solution	Sheet 28 of 38
Drawn By:		File: dac38j84_02.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

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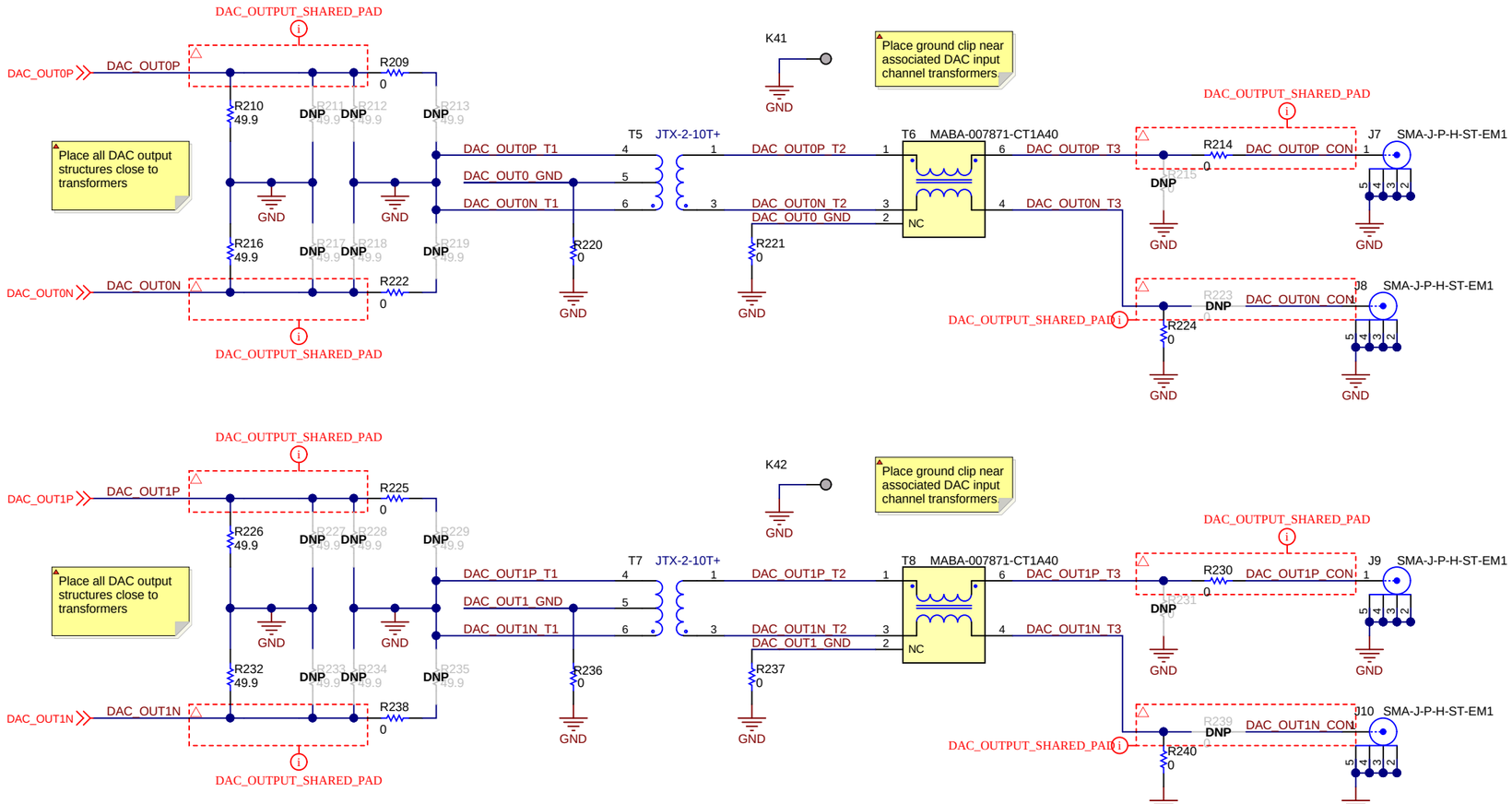
DAC Analog Output Filtering and Balancing - Channels 0 and 1

Exact transformer characteristics should be chosen based on bandwidth of interest for signals being detected. Please see the ADC32RF80/45 collateral for additional design considerations.

All ADC input channel signal paths shall be routed as 50-ohm characteristic impedance paths.



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Drawn By:		File: dac38j84_03.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

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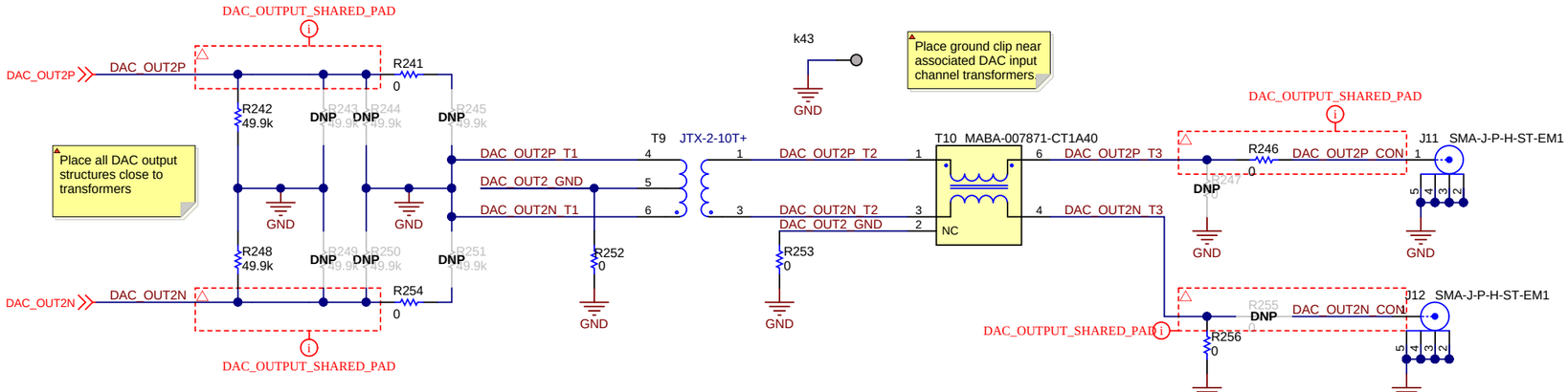
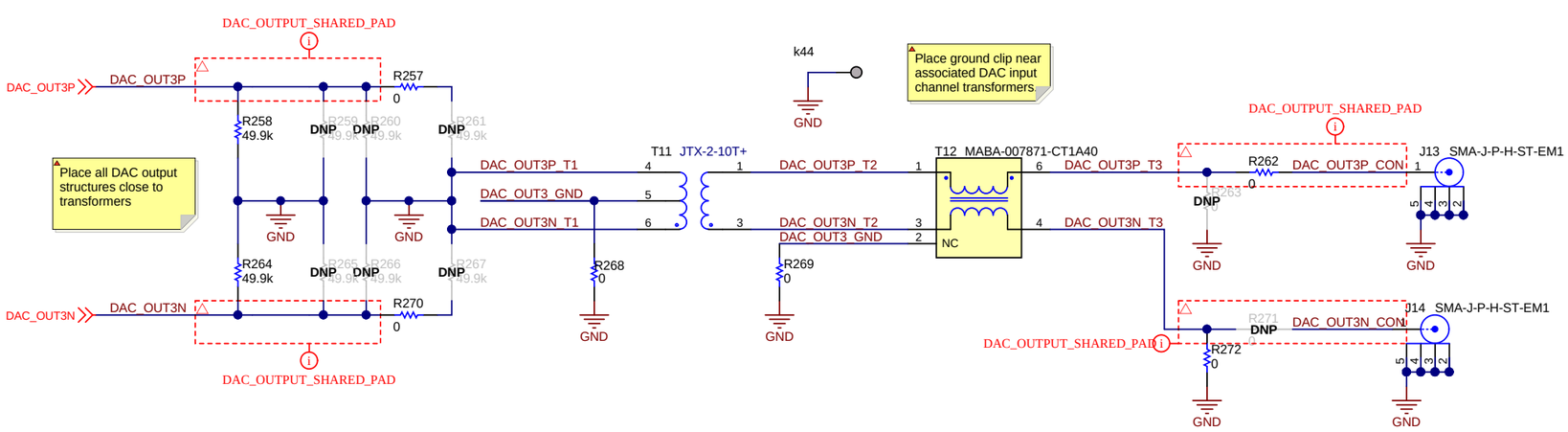
DAC Analog Output Filtering and Balancing - Channels 2 and 3

Exact transformer characteristics should be chosen based on bandwidth of interest for signals being detected. Please see the ADC32RF80/45 collateral for additional design considerations.

All ADC input channel signal paths shall be routed as 50-ohm characteristic impedance paths.





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Engineer: a0271760		Contact: http://www.ti.com/support	

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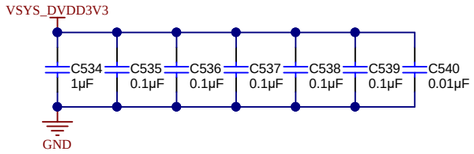
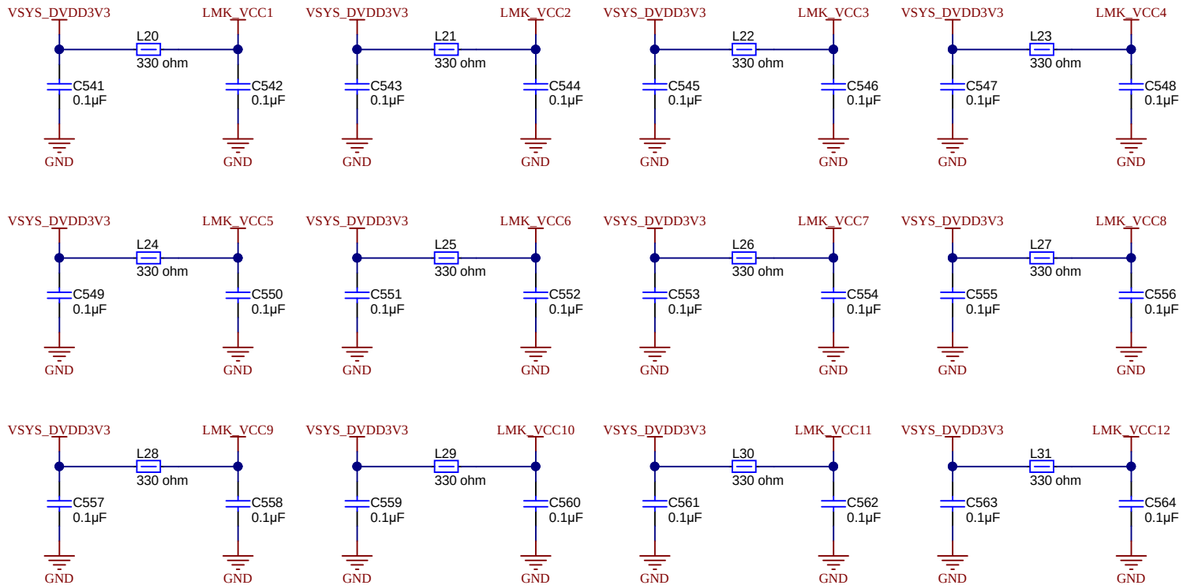
LMK04828 Decoupling Capacitors

LMK04828 decoupling shall be placed as close to the IC package as possible. See LMK04828 datasheet and EVM for example decoupling layout.





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SVN Rev: Version control disabled	Assembly Variant: k2l_adjacent_market_solution Sheet 31 of 38	
Drawn By:	File: lmk04828_01.SchDoc	Size: B
Engineer: a0271760	Contact: http://www.ti.com/support	

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LMK04828 Reference Clock Input, SPI Control, SYSCLK, SYSREF and Reference Clock Output

For schematic and layout recommendations and requirements see the LMK04828 product page linked below.

TI LMK04828 Product Page

LMK04828 RESET and SYNC mastered by System Controller (microcontroller) not shown here.

All unused pins shall be routed with short stubs to aid in solderability and mechanical robustness. Indicated by the LMK-xx unused pin nets names.

U15
LMK04828BISQ/NOPB

LMK_VCC12 LMK_VCC11

PAD 65
Vcc2_CG0 64
DCLKout12* 63 LMK-63
DCLKout12 62 LMK-62
SDCLKout13 61 LMK-61
SDCLKout13 60 LMK-60
CLKin_SEL1 59 LMK-59
CLKin_SEL0 58 LMK-58
SDCLKout11* 57 LMK-57
SDCLKout11 56 LMK-56
DCLKout10* 55 LMK-55
DCLKout10 54 LMK-54
Vcc11_CG3 53
DCLKout8* 52 LMK-52
DCLKout8 51 LMK-51
SDCLKout9* 50 LMK-50
SDCLKout9 49 LMK-49

DCLKout0 1 ADC_DEVCLKP
DCLKout0* 2 ADC_DEVCLKN
SDCLKout1 3 ADC_SYSREFP
SDCLKout1* 4 ADC_SYSREFN
RESET 5 LMK_RESET
SYNC 6 LMK_SYNC
NC 7 LMK-7
NC 8 LMK-8
NC 9 LMK-9
Vcc1_VCO 10 LMK_VCC1
LDObyp1 11 LMK_LDOBYP1
LDObyp2 12 LMK_LDOBYP2
SDCLKout3 13 DAC_DACCLKP
SDCLKout3* 14 DAC_DACCLKN
DCLKout2 15 DAC_SYSREFP
DCLKout2* 16 DAC_SYSREFN

Vcc2_CG1 17 LMK_VCC2
CS* 18 LMK_SPI_CSB
SCK 19 LMK_SPI_CLK
SDIO 20 LMK_SPI_DATA
Vcc3_SYSREF 21 LMK_VCC3
SDCLKout5 22 K2L_DFESYSREFP
SDCLKout5* 23 K2L_DFESYSREFN
DCLKout4 24 K2L_SYSCLKP
DCLKout4* 25 K2L_SYSCLKN
Vcc4_CG2 26 LMK_VCC4
DCLKout6 27 K2L_JESD_SERDES0_REFCLKP
DCLKout6* 28 K2L_JESD_SERDES0_REFCLKN
SDCLKout7 29 K2L_JESD_SERDES1_REFCLKP
SDCLKout7* 30 K2L_JESD_SERDES1_REFCLKN
Status_LD1 31 LMK_LD1
CPout1 32 LMK_CPOUT1

Status_LD2 48 LMK_LD2
Vcc10_PLL2 47 LMK_VCC10
CPout2 46 LMK_CPOUT2
Vcc9_CP2 45 LMK_VCC9
OSCin* 44 LMK-44
OSCin 43 LMK-43
Vcc8_OSCin 42 LMK_VCC8
OSCout*/CLKin2* 41 LMK-41
OSCout/CLKin2 40 LMK-40
Vcc7_OSCout 39 LMK_VCC7
CLKin0* 38 LMK_CLKIN0N_CS
CLKin0 37 LMK_CLKIN0P_CS
Vcc6_PLL1 36 LMK_VCC6
CLKin1*/Fin*/FBCLKin* 35 LMK-35
CLKin1/Fin/FBCLKin 34 LMK-34
Vcc5_DIG 33 LMK_VCC5

LMK04828 DCLKOUT0 used as the device clock for the ADC

LMK04828 SDCLKOUT0 used as the SYSREF for the ADC

VSYS_DVDD3V3
R274 2.32k
R276 1.3k
LMK_RESET
LMK_SYNC

ADC_DEVCLKP
ADC_DEVCLKN
ADC_SYSREFP
ADC_SYSREFN

C567 0.1µF
C569 10µF

LMK04828 DCLKOUT2 used as the device clock for the DAC

LMK04828 SDCLKOUT3 used as the SYSREF for the DAC

DAC_DACCLKP
DAC_DACCLKN
DAC_SYSREFP
DAC_SYSREFN

R278 240
R279 240
R280 240
R281 240

DAC DACCLK and SYSREF are LVPECL inputs which require LVPECL source biasing and AC-coupling as described in the DAC38J84 datasheet section 7.3.25

LMK_SPI_CSB
LMK_SPI_CLK
LMK_SPI_DATA
R282 10.0 LMK_SPI_DATA_RS

LMK04828 SPI port mastered by System Controller (microcontroller) not shown here.

LMK04828 SDCLKOUT5 used as the SYSREF for the K2L

LMK04828 DCLKOUT4 used as the SYSCLK for the K2L

LMK04828 DCLKOUT6 used as the JESD0 SERDES clock for the

LMK04828 SDCLKOUT7 used as the JESD1 SERDES clock for the

K2L_JESD_SERDES0_REFCLKP
K2L_JESD_SERDES0_REFCLKN
K2L_JESD_SERDES1_REFCLKP
K2L_JESD_SERDES1_REFCLKN

LMK04828 LD1 and LD2 monitored by System Controller (microcontroller) not shown here.

LMK_LD2
Status1 Green
k45
R273 270

Optional external charge-pump filter element. Shall be placed as close as possible to LMK04828.

Please see LMK04828 datasheet, application notes and EVM design guide for specific recommendations.

C566 47pF
C565 3900pF
R275 619
REF_NET

19.2 MHz TCXO

VSYS_DVDD1V8
U16
OUT VCC
GND GND
IT2100F
C571 1µF

LMK_CLKIN0P R277 10.0 LMK_CLKIN0P_RS

C568 0.1µF
C570 0.1µF

Special care should be taken to GND isolate CLKIN0 signal.

For best ADC/DAC performance the reference oscillator should be carefully selected to meet requirements of the LMK04828

k46
C573 47pF
C572 3900pF
R283 619
REF_NET

LMK_LD1
Status2 Green
R284 270

Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 8/29/2016
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Number: TIDEP0081	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: k2l_adjacent_market_solution	Sheet 32 of 38
Drawn By:		File: lmk04828_02.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

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CDCM6208 Low Phase Noise PLL - Power, Reference Clocking, SPI ,Control and Clock Output

Ferrite beads shall be placed as close as possible to the CDCM6208 power pins.

Decoupling capacitors shall be placed as close as possible to the CDCM6208 power pins

Primary input is used in 3.3V LVCMOS mode.

Primary input selected by REF_SEL pin low.

Secondary input is unused.

CDCM reset, configuration, and status pins and SPI interface mastered by System Controller (microcontroller) not shown here.

Recommend configuring CDCM6208 output for LVDS (Low-Power CML). This output mode is directly compatible with the K2L LJCB and SERDES refernce clock input buffers.

K2L DDR3ACLK @ 100 MHz

K2L USBCLK @ 100 MHz

External filter for VCO (see CDCM datasheet for details):
Synthesizer mode (high loop bandwidth)
CDCM6208V1:
With C1=100pF, R2=500, C2=22nF and
Internal components R3=100, C3=242.5pF,
fPFD=25MHz, and ICP=2.5mA:
Loop bandwidth (337kHz)

Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 8/29/2016
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Number: TIDEP0081	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: k2l_adjacent_market_solution	Sheet 3 of 38
Drawn By:		File: cdcm6208_1.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

TPS544B24 - K2L Smart-Reflex (AVS) Regulator

Debug header exposing the full PMBUS interface. Can be useful for debugging with the TI Fusion Digital Power dsign software and associated TI GPIO to USB converter.

J15 — TSW-105-07-G-S — PMBUS_CLK, PMBUS_DATA, PMBUS_ALERT, PMBUS_CNTL

K2L I2C0 is currently utilized for PMBUS control by the K2L PDK software releases. Other I2C ports could be used but software changes would be necessary.

PCA9306 bridge EN pin should be enabled such that K2L I2C pins remain isolated through power-on-reset sequence. I2C communication to the TPS544B24 should startup after a proper PORz sequence is executed on the K2L.

Recommend that the EN pin is tied to K2L GPIO or to board supervisory logic.

U18 PCA9306DCTR

Compensation and feedback RC networks setup in same manner as K2L EVM. Please see TPS544B24 datasheet and application notes for details and optimizations.

ADDR0 - 10k - ADDR0 = 0b0
ADDR1 - 10k - ADDR1 = 0b0
Selects ADDR[1:0] = 0b00

U19 TPS544B24RVF

VDDCMON/VSSCMON are die-level CVDD sense pins. These pins pass through the substrate level CVDD power planes and allow the regulator to sense CVDD right at the K2L die.

R_VSET = 86.6k sets 1.0V startup voltage when TPS544B24 is intended to be mastered through PMBUS.

K2L AVS Core 0.85V to 1.0V @ 15A

L37 SRP7030-R22M

D1 B220A-13-F

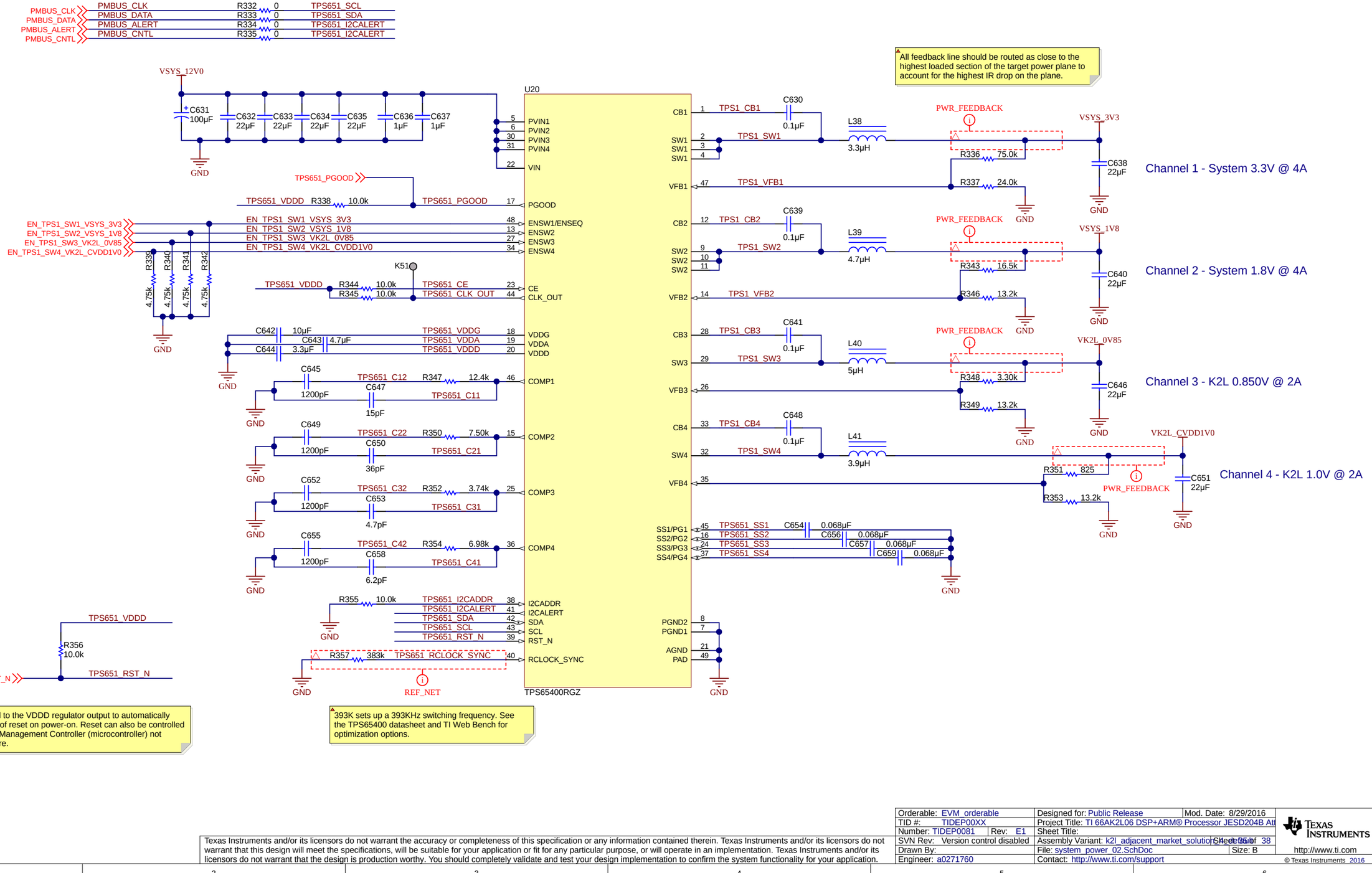
TPS544_CRITICAL

Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 8/27/2016
TID #: TIDEP00XX		Project Title: TI 66AK2L06 DSP+ARM® Processor JESD204B Att	
Number: TIDEP0081	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: k2l_adjacent_market_solution	Sheet 34 of 38
Drawn By: a0271760		File: system_power_01.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

TPS65400 Quad Channel Buck Controller #1

TI Web Bench used to construct th\is TPS65400 reference schematic shown here. Reference the link below to view as the TPS54600 datasheet for calculations and optimization options.

TI Web Bench TI K2L Design #4 - TPS54600 #1



Orderable: EVM_orderable	Designed for: Public Release	Mod. Date: 8/29/2016
TID #: TIDEP00XX	Project Title: TI 66AK2L06 DSP+ARM® Processor JESD204B Att	
Number: TIDEP0081 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: k2l_adjacent_market_solution Sheet 1 of 38	
Drawn By:	File: system_power_02.SchDoc Size: B	
Engineer: a0271760	Contact: http://www.ti.com/support	

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TPS65400 Quad Channel Buck Controller #2

TI Web Bench used to construct th\is TPS65400 reference schematic shown here. Reference the link below to view as the TPS54600 datasheet for calculations and optimization options.

TI Web Bench TI K2L Design #4 - TPS54600 #2

PMBUS_CLK — PMBUS_CLK — R358 0 — TPS651_SCL
PMBUS_DATA — PMBUS_DATA — R359 0 — TPS651_SDA
PMBUS_ALERT — PMBUS_ALERT — R360 0 — TPS651_I2CALERT
PMBUS_CNTL — PMBUS_CNTL — R361 0 — TPS651_I2CALERT

All feedback line should be routed as close to the highest loaded section of the target power plane to account for the highest IR drop on the plane.

VSYS_12V0
C661 100µF
C662 22µF
C663 22µF
C664 22µF
C665 22µF
C666 1µF
C667 1µF
GND

U21

PVIN1 5
PVIN2 6
PVIN3 30
PVIN4 31
VIN 22

TPS652_PGOOD
TPS6512_VDDD R364 10.0k
TPS652_PGOOD — PGOOD 17

EN_TPS2_SW1_VSYS_1V35 — EN_TPS2_SW1_VSYS_1V35 — ENSW1/ENSEQ 48
EN_TPS2_SW2_VSYS_1V15 — EN_TPS2_SW2_VSYS_1V15 — ENSW2 13
EN_TPS2_SW3_VSYS_0V9 — EN_TPS2_SW3_VSYS_0V9 — ENSW3 27
EN_TPS2_SW4_VSYS_1V9 — EN_TPS2_SW4_VSYS_1V9 — ENSW4 34

R366 4.75k
R367 4.75k
R368 4.75k
R369 4.75k
GND

K52
TPS652_VDDD R370 10.0k R372 10.0k
TPS652_CE — CE 23
TPS652_CLK_OUT — CLK_OUT 44

C672 10µF
C673 4.7µF
C674 3.3µF
TPS652_VDDG — VDDG 18
TPS652_VDDA — VDDA 19
TPS652_VDDD — VDDD 20
GND

C675 1200pF
C677 1pF
TPS652_C12 R374 5.62k — COMP1 46
TPS652_C11
GND

C679 1200pF
C680 1pF
TPS652_C22 R376 4.87k — COMP2 15
TPS652_C21
GND

C682 1200pF
C683 3.9pF
TPS652_C32 R378 7.32k — COMP3 25
TPS652_C31
GND

C685 1200pF
C688 180pF
TPS652_C42 R380 15.0k — COMP4 36
TPS652_C41
GND

R381 10.0k
TPS652_I2CADDR — I2CADDR 38
TPS652_I2CALERT — I2CALERT 41
TPS652_SDA — SDA 42
TPS652_SCL — SCL 43
TPS652_RST_N — RST_N 39
R383 383k TPS652_RCLOCK_SYNC — RCLOCK_SYNC 40
GND
REF_NET

TPS65400RGZ

CB1 1 — TPS2_CB1 — C660 0.1µF
SW1 2 — TPS2_SW1 — L42 3.9µH
SW1 3
SW1 4
VFB1 47 — TPS2_VFB1
PWR_FEEDBACK — R362 11.0k — R363 16k — GND
VK2L_DDR_1V35 — C668 22µF — GND

Channel 1 - K2L and DDR3 SDRAM 1.35V @ 4A

CB2 12 — TPS2_CB2 — C669 0.1µF
SW2 9 — TPS2_SW2 — L43 3.9µH
SW2 10
SW2 11
VFB2 14 — TPS2_VFB2
PWR_FEEDBACK — R365 10.5k — R371 24k — GND
VSYS_1V15 — C670 22µF — GND

Channel 2 - System 1.15V @ 4A

CB3 28 — TPS2_CB3 — C671 0.1µF
SW3 29 — TPS2_SW3 — L44 4.7µH
VFB3 26 — TPS2_VFB3
PWR_FEEDBACK — R373 1.65k — R375 13k — GND
VSYS_0V9 — C676 22µF — GND

Channel 3 - System 0.9V @ 2A

CB4 33 — TPS2_CB4 — C678 0.1µF
SW4 32 — TPS2_SW4 — L45 6.8µH
VFB4 35 — TPS2_VFB4
R377 22k — R379 16k — GND
PWR_FEEDBACK
VSYS_1V9 — C681 22µF — GND

Channel 4 - System 1.9V @ 2A

SS1/PG1 45 — TPS652_SS1 — C684 0.068µF
SS2/PG2 16 — TPS652_SS2 — C686 0.068µF
SS3/PG3 24 — TPS652_SS3 — C687 0.068µF
SS4/PG4 37 — TPS652_SS4 — C689 0.068µF
GND

PGND2 8
PGND1 7
AGND 21
PAD 49
GND

TPS652_VDDD
R382 10.0k
TPS652_RST_N — TPS652_RST_N

Reset tied to the VDDD regulator output to automatically come out of reset on power-on. Reset can also be controlled by Board Management Controller (microcontroller) not shown here.

393K sets up a 393KHz switching frequency. See the TPS65400 datasheet and TI Web Bench for optimization options.

Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 8/29/2016
TID #: TIDEP00XX		Project Title: TI 66AK2L06 DSP+ARM® Processor JESD204B Att	
Number: TIDEP0081	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: k2l_adjacent_market_solution	Sheet 36 of 38
Drawn By:		File: system_power_03.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

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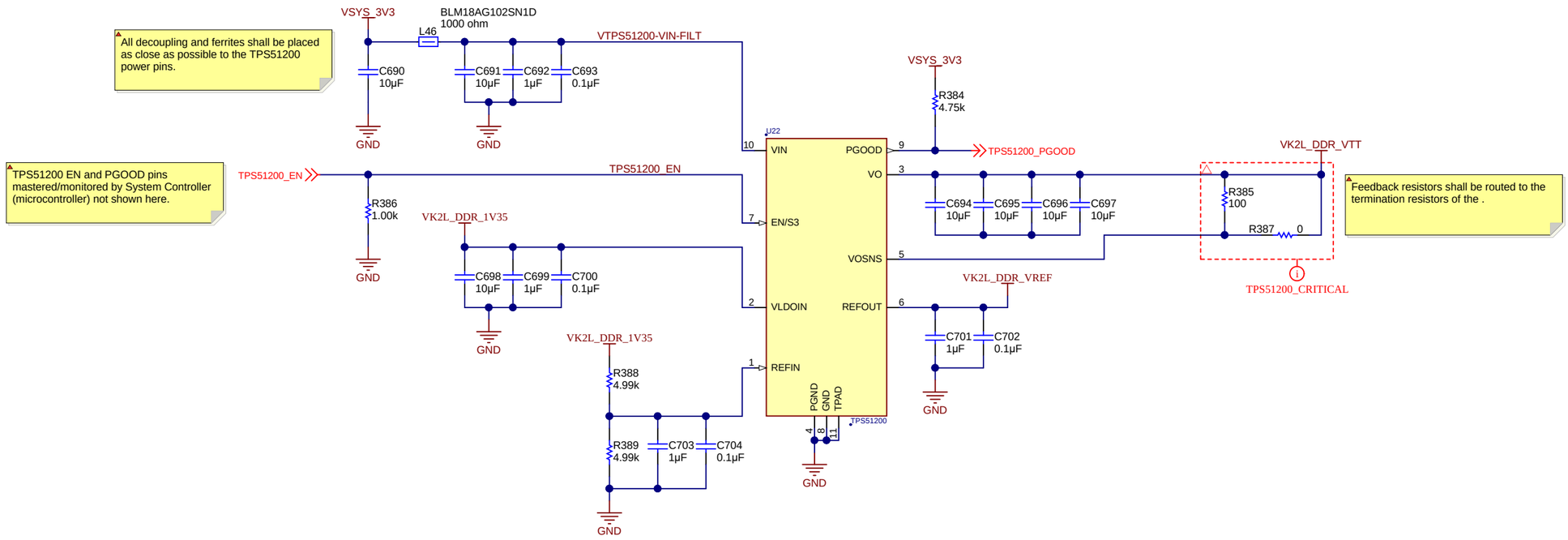
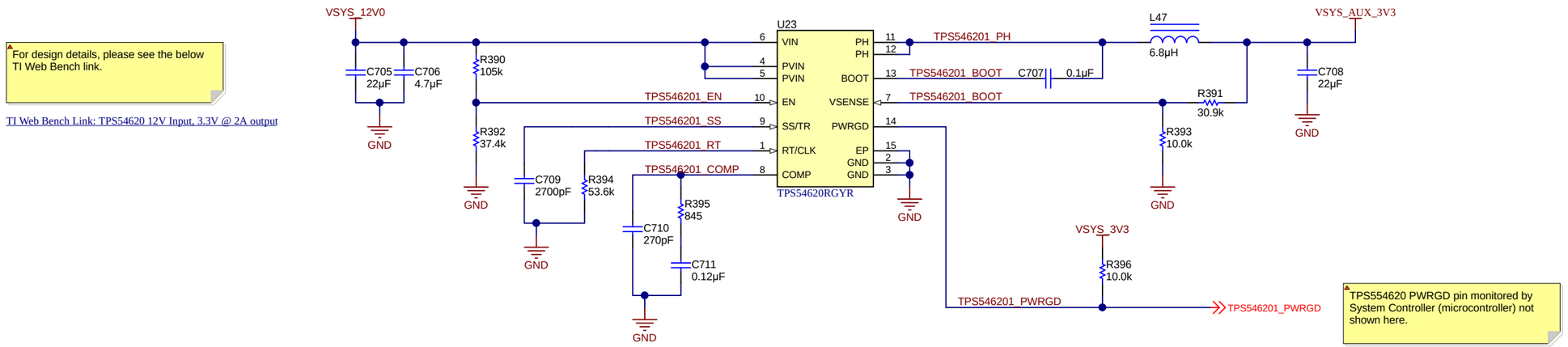
TPS51200 - DDR3 VTT/VREF Push-Pull Converter



TPS54620 #1 - 3.3V Auxillary Supply for Board Management Controller



Orderable: EVM_orderable	Designed for: Public Release	Mod. Date: 8/29/2016
TID #: TIDEP00XX	Project Title: TI 66AK2L06 DSP+ARM® Processor JESD204B Att	
Number: TIDEP0081 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: k2l_adjacent_market_solution Sheet 37 of 38	
Drawn By:	File: system_power_04.SchDoc	Size: B
Engineer: a0271760	Contact: http://www.ti.com/support	

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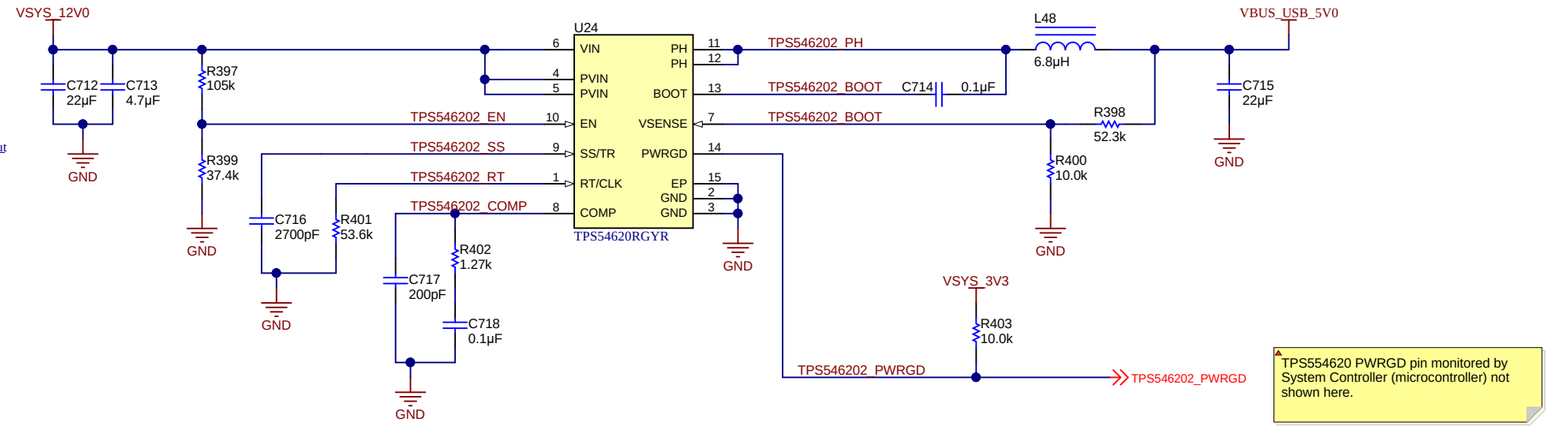
TPS54620 #2 - USB 5.0V Buck Converter

For design details, please see the below TI Web Bench link.

TI Web Bench Link: TPS54620 12V Input, 5V @ 2A output



TPS554620 PWRGD pin monitored by System Controller (microcontroller) not shown here.

Orderable: EVM_orderable	Designed for: Public Release	Mod. Date: 8/29/2016
TID #: TIDEP00XX	Project Title: TI 66AK2L06 DSP+ARM® Processor JESD204B Att	
Number: TIDEP0081 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: k2l_adjacent_market_solution Sheet 38 of 38	
Drawn By:	File: system_power_05.SchDoc	Size: B
Engineer: a0271760	Contact: http://www.ti.com/support	

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