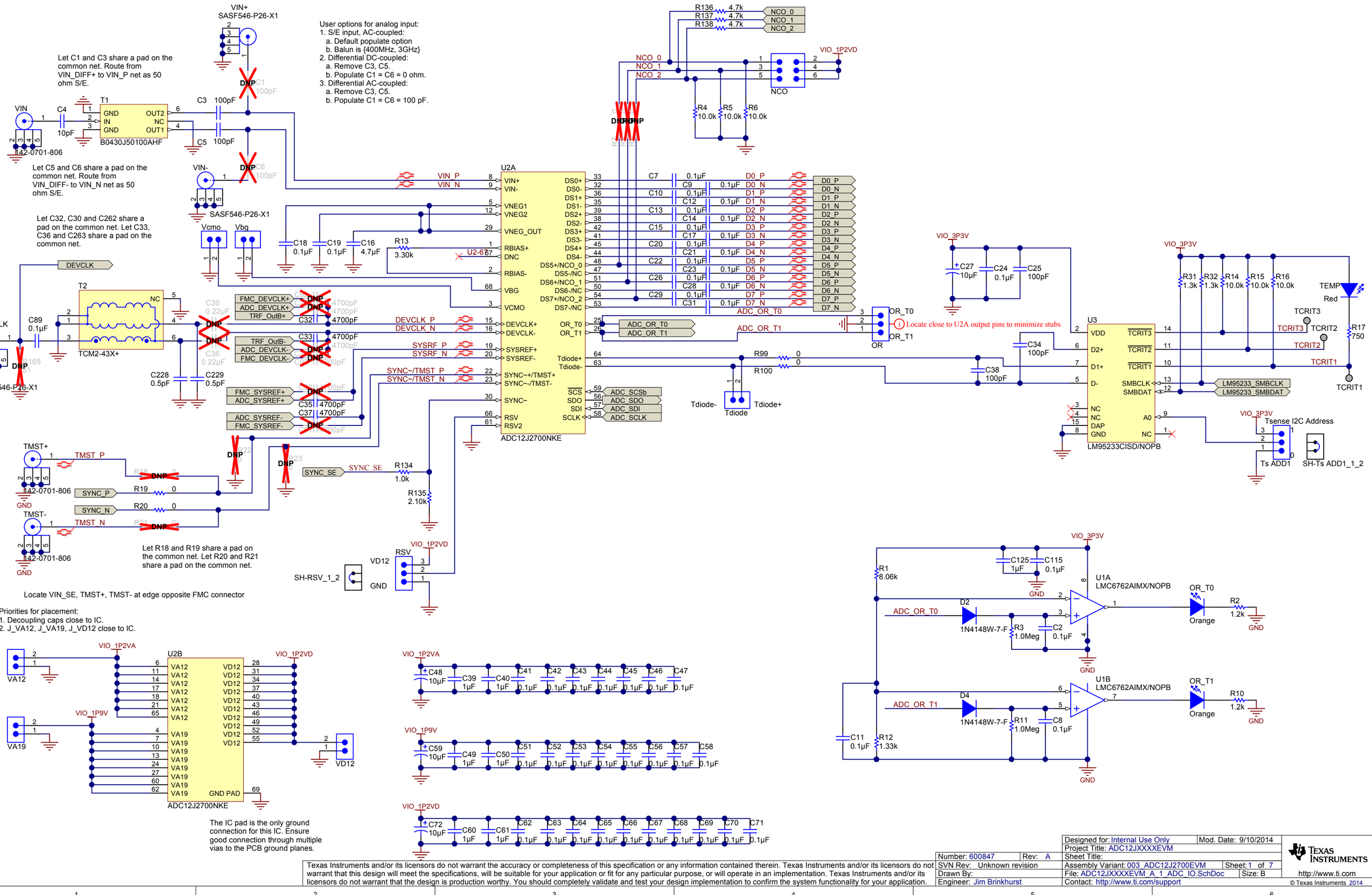

Number: 600847	Rev: A	Designed for: Internal Use Only	Mod. Date: 9/10/2014
SVN Rev: Unknown revision		Project Title: ADC12JXXXXEVM	
Drawn By:		Sheet Title:	
Engineer: Jim Brinkhurst		Assembly Variant: 003_ADC12J2700EVM	Sheet: 1 of 7
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The D<7:0> connections polarity have
been swapped from the TI standard
FMC ADC guidelines to ease routing.
This is accounted for in the FPGA code.

FMC_RX1A

DP1_M2C_P / DP1_M2C_N — D1_N / D1_P
DP2_M2C_P / DP2_M2C_N — D2_N / D2_P
DP3_M2C_P / DP3_M2C_N — D3_N / D3_P
DP4_M2C_P / DP4_M2C_N — D4_N / D4_P
DP5_M2C_P / DP5_M2C_N — D5_N / D5_P
D7_N / D7_P → DP7_M2C_P / DP7_M2C_N
D6_N / D6_P → DP6_M2C_P / DP6_M2C_N

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FMC_RX1B

DP0_M2C_P / DP0_M2C_N — D0_N / D0_P
GBTCLK0_M2C_P / GBTCLK0_M2C_N
DEVCLKARX_P / DEVCLKARX_N
ADC_OR_T1
FMC_SCL
FMC_SDA
KC705 JTAG
3P3VAUX
12P0V_RX
EE_ADDR0_RX
EE_ADDR1_RX
3P3V_RX 3P3RX
R132
0

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PG_RX1

PG_C2M_RX
PG_M2C_RX
VADJ_RX
RR6
4.99k

FMC_RX1C

NCO_0
NCO_1
NCO_2
VADJ_RX

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FMC_RX1D

LA00_P_CC / LA00_N_CC — DEVCLKBRX_P / DEVCLKBRX_N
LA03_P / LA03_N — SYSREFRX_P / SYSREFRX_N
LA08_P / LA08_N — SYNC_P / SYNC_N
ADC_OR_T0
FMC_SPI_CLK
FMC_SPI_SCSb1
FMC_SPI_SCSb2
FMC_ADC_SDI
FMC_ADC_SDO
SYNC_SE
FMC_SPI_SDIO
FMC_ADC_CLK
FMC_ADC_SCSb0

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PRSNT_M2C_L_RX

FMC_RX1E

LMK04828_SYNC
LMK04828_RESET
FMC_DEVCLK_P / FMC_DEVCLK_N → FMC_DEVCLK+ / FMC_DEVCLK-
FMC_SYSREF_P / FMC_SYSREF_N → FMC_SYSREF+ / FMC_SYSREF-
VIO_B_M2C_RX
RR7
0

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U16
DNP
24C65T/SM
3P3VAUX
C143
1µF
FMC_SDA
FMC_SCL
EE_ADDR1_RX
EE_ADDR0_RX
J1
TSW-104-07-G-S
3P3VAUX

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Engineer: Jim Brinkhurst	

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Sheet Title:
Assembly Variant: 003_ADC12J2700EVM | Sheet: 2 of 7
File: ADC12JXXXXEVM_A_2_FMC.SchDoc | Size: C
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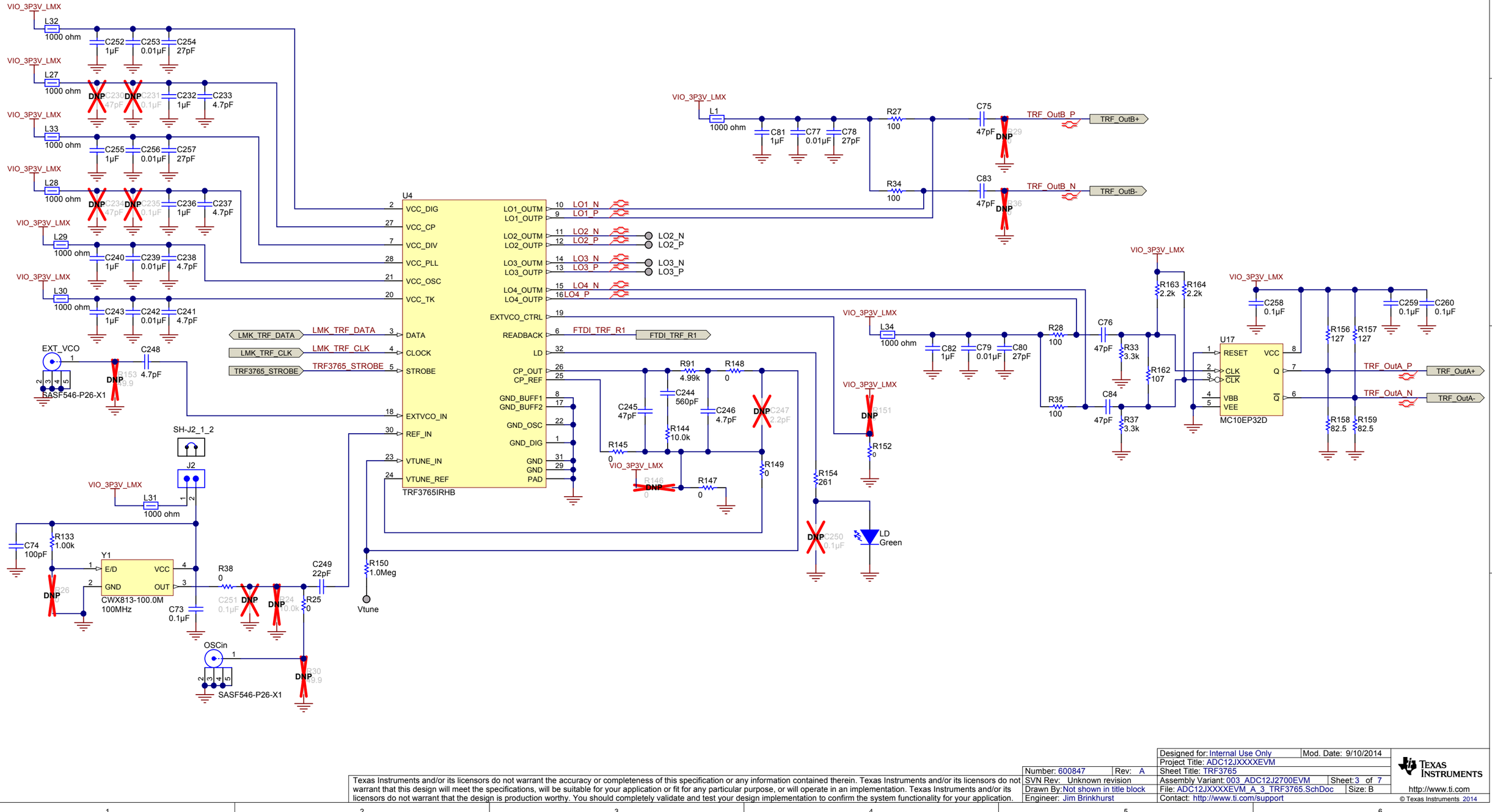

Number: 600847	Rev: A	Designed for: Internal Use Only	Mod. Date: 9/10/2014
SVN Rev: Unknown revision		Project Title: ADC12JXXXXEVM	
Drawn By: Not shown in title block		Sheet Title: TRF3765	
Engineer: Jim Brinkhurst		Assembly Variant: 003_ADC12J2700EVM	Sheet: 3 of 7
		File: ADC12JXXXXEVM_A_3_TRF3765.SchDoc	Size: B
		Contact: http://www.ti.com/support	

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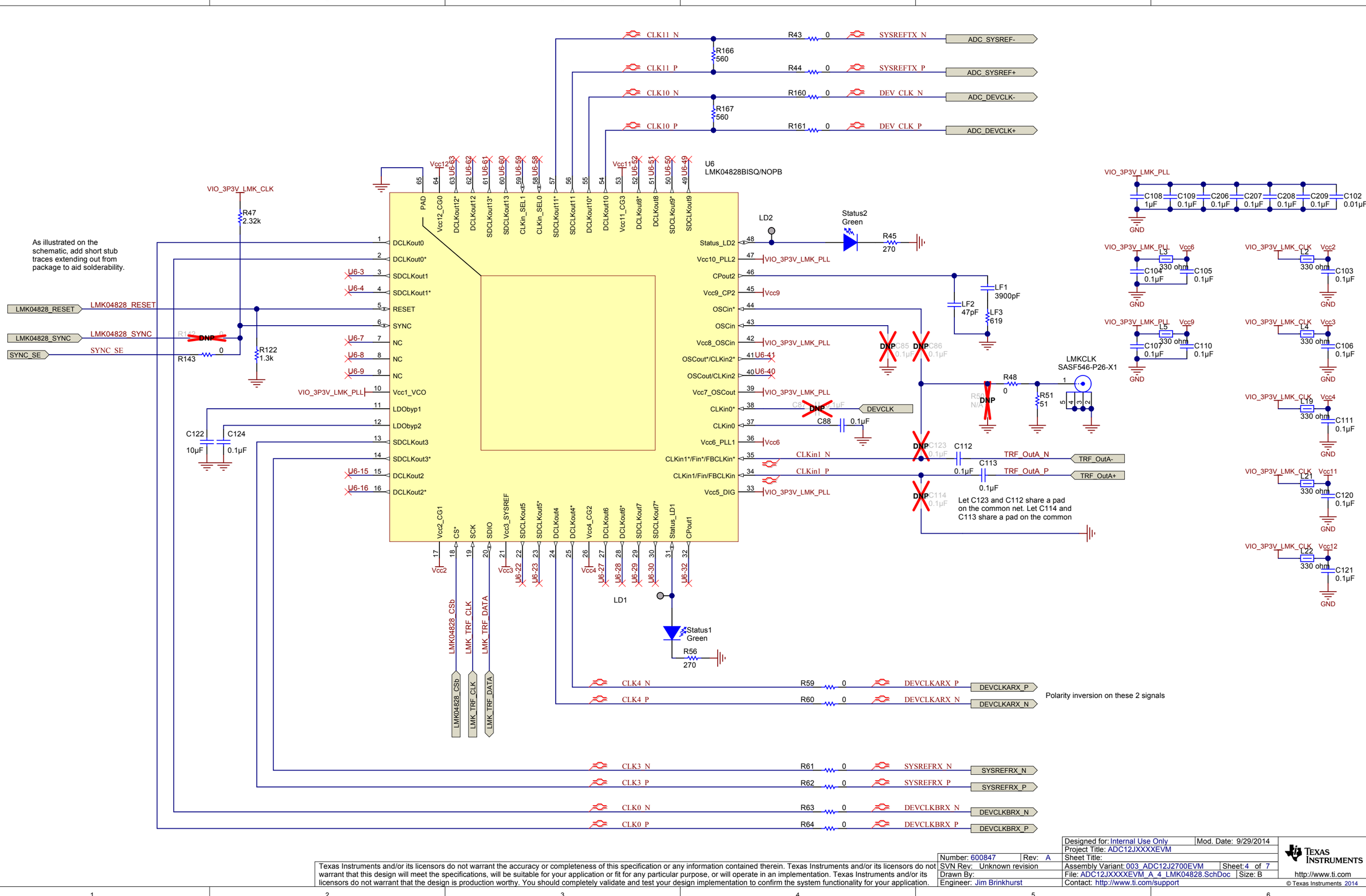

Number: 600847	Rev: A	Designed for: Internal Use Only	Mod. Date: 9/29/2014
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Drawn By:		Sheet Title:	
Engineer: Jim Brinkhurst		Assembly Variant: 003_ADC12J2700EVM	Sheet: 4 of 7
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		Contact: http://www.ti.com/support	

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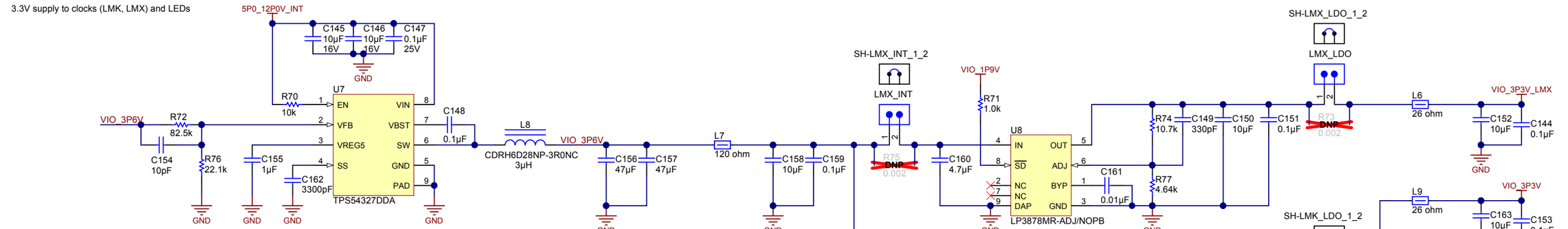
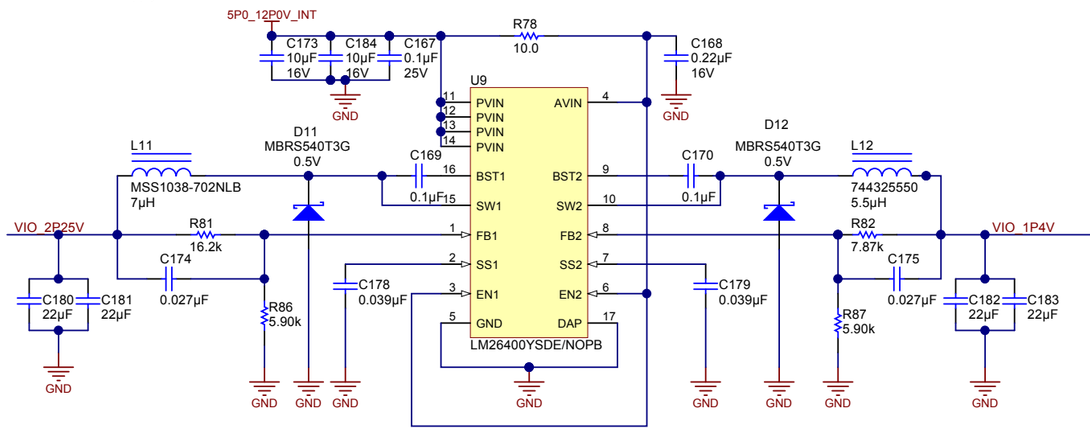
3.3V supply to clocks (LMK, LMX) and LEDs

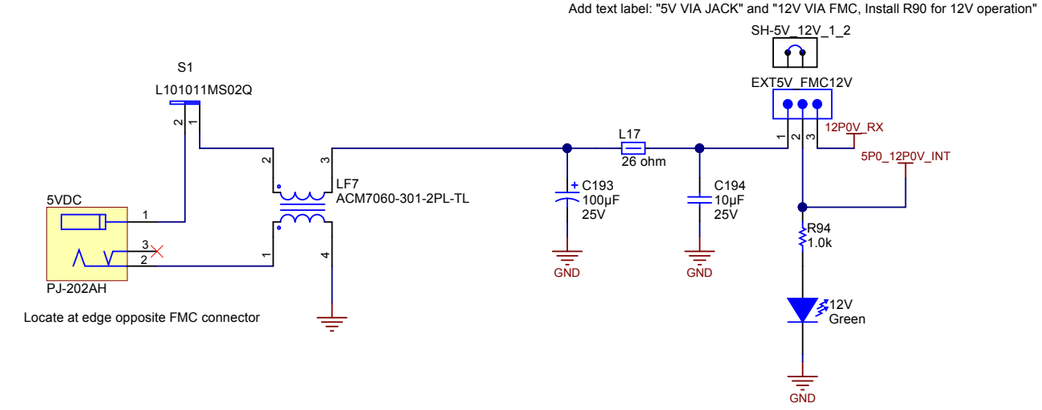


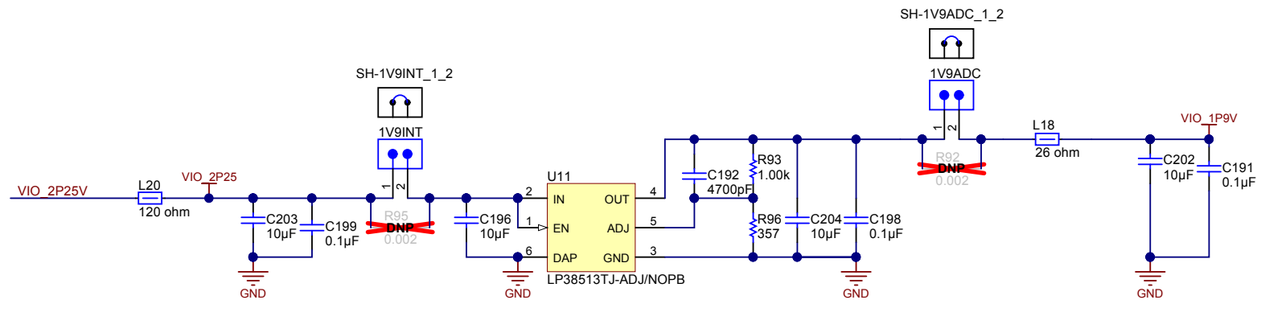
1.9V and 1.2V supply to LM15851 / ADC12JXX00



12V main supply, from jack or via FMC connector to regulators

Add text label: "5V VIA JACK" and "12V VIA FMC, Install R90 for 12V operation"





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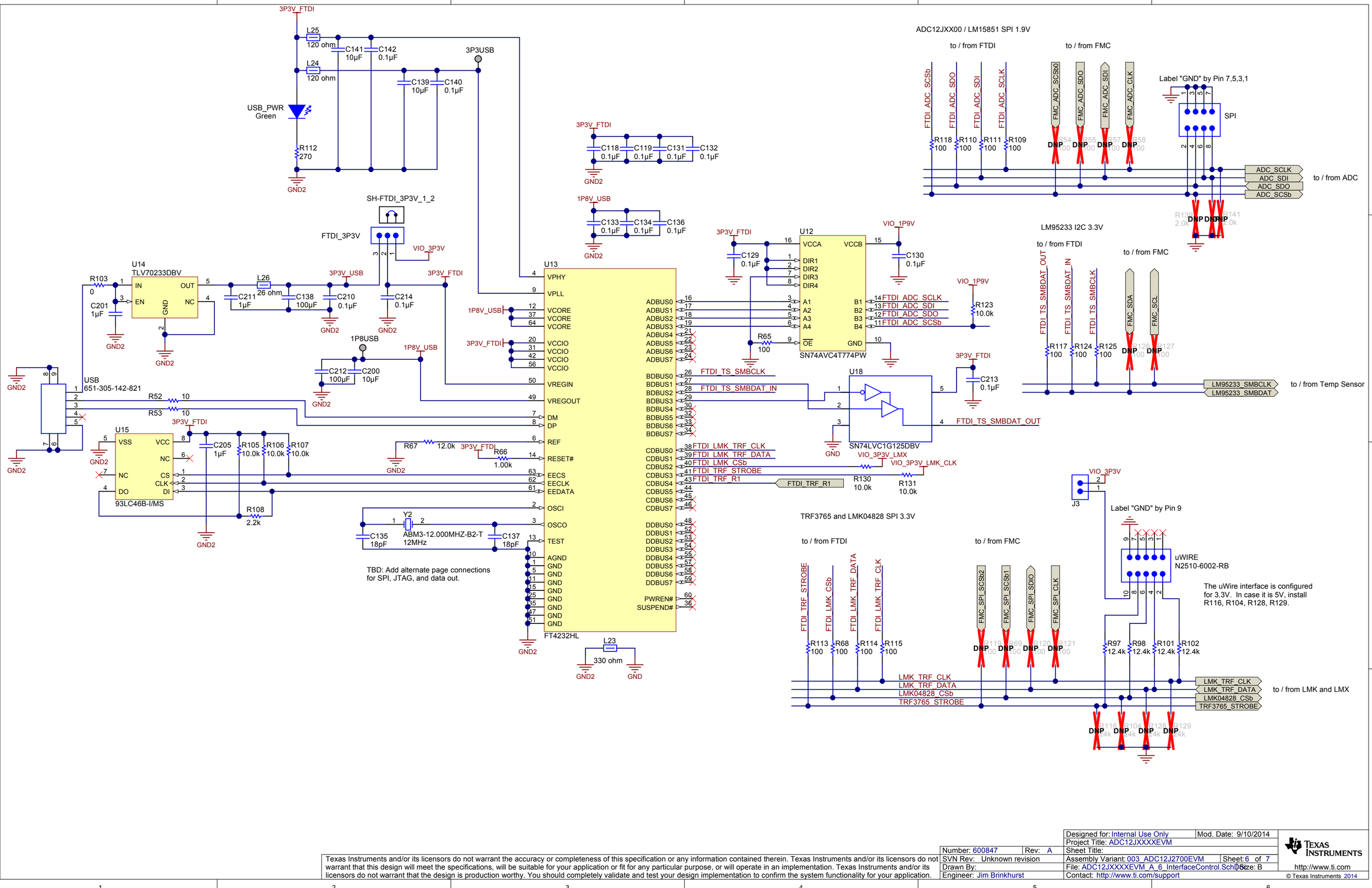

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Engineer: Jim Brinkhurst	

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DNP
FID1

PCB Number: 600847
PCB Rev: A

PCB
ESD LOGO
ESD Susceptible

PCB
LOGO
Texas Instruments

H4
H6
1648-440-AL
NY PMS 440 0025 PH
DNP
FID2

H3
H5
1648-440-AL
NY PMS 440 0025 PH
DNP
FID3

H9
MECH
FMC - FMC Screw
PMSSS 256 0075 PH

H10
MECH
FMC - FMC Nut

H11
MECH
FMC - FMC Screw
PMSSS 256 0075 PH

H12
MECH
FMC - FMC Nut

GND GND1 GND2 GND3

Place at least two of the GND test points in the power section.

LBL1
PCB Label
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2., unless otherwise specified.

VIO_3P3V C215 0.1µF GND
VIO_3P3V C216 0.1µF VIO_3P3V_LMX
VIO_3P3V C217 0.1µF VIO_3P3V_LMX
VIO_3P3V C218 0.1µF GND
VIO_1P4 C219 0.1µF VIO_3P3V
VIO_3P3V C220 0.1µF 5P0_12P0V_INT
VIO_1P4 C221 0.1µF 5P0_12P0V_INT
5P0_12P0V_INT C94 0.1µF 12P0V_RX

VIO_2P25 C222 0.1µF 5P0_12P0V_INT
VIO_2P25 C223 0.1µF 5P0_12P0V_INT
VIO_1P4 C224 0.1µF VIO_3P3V
VIO_1P4 C225 0.1µF 5P0_12P0V_INT
VIO_2P25 C226 0.1µF 5P0_12P0V_INT
VIO_2P25 C227 0.1µF 5P0_12P0V_INT
5P0_12P0V_INT C261 0.1µF GND
VIO_3P3V C95 0.1µF VIO_1P2VD
VIO_3P3V C96 0.1µF VIO_1P2VD

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Engineer: Jim Brinkhurst		Assembly Variant: 003_ADC12J2700EVM	Sheet: 7 of 7
		File: ADC12JXXXXEVM_A_7_Hardware.SchDoc	Size: B
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