NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P1P1V" represents connection to the +1.1V FPGA power plane
2. The netname "P1P1V_FIL" represents connection to the +1.1V filtered FPGA power plane
3. The netname "P1P1V_M" represents connection to the +1.1V Master ASIC power plane
4. The netname "P1P1V_S" represents connection to the +1.1V Slave ASIC power plane
5. The netname "P1P15V" represents connection to the +1.15V FPGA power plane
6. The netname "P1P15V" represents connection to the +1.15V filtered FPGA power plane
7. The netname "P1P5V" represents connection to the +1.5V FPGA power plane
8. The netname "P1P5V_FIL" represents connection to the +1.5V filtered FPGA power plane
9. The netname "P1P8V_M" represents connection to the +1.8V Master ASIC power plane
10. The netname "P1P8V_S" represents connection to the +1.8V Slave ASIC power plane
11. The netname "A1P8V_M" represents connection to the +1.8V Master ASIC power plane for the PLLs
12. The netname "A1P8V_S" represents connection to the +1.8V Slave ASIC power plane for the PLLs
13. The netname "P2P5V" represents connection to the +2.5V FPGA power plane
14. The netname "P2P5V_FIL" represents connection to the +2.5V filtered FPGA power plane
15. The netname "P2P5V_M" represents connection to the +2.5V Master ASIC power plane
16. The netname "P2P5V_S" represents connection to the +2.5V Slave ASIC power plane
17. The netname "P3P3V" represents connection to the +3.3V FPGA power plane
18. The netname "P3P3V_M" represents connection to the +3.3V Master ASIC power plane
19. The netname "P3P3V_S" represents connection to the +3.3V Slave ASIC power plane
20. The netname "P5V_M" represents connection to the +5V Master ASIC power plane
21. The netname "P5V_S" represents connection to the +5V Slave ASIC power plane
22. The netname "P12V" represents the connection to the +12.0V power plane.
23. The netname "GND" represents connection to the ground plane
24. A "Z" suffix on a signal name indicates an active low signal
25. All components with designators "U*", "Q*", "D*" are electrostactic discharge sensitive.
26. All components with designators above 500 are mounted on the bottom side of the board.
27. All resistor values are in ohms.

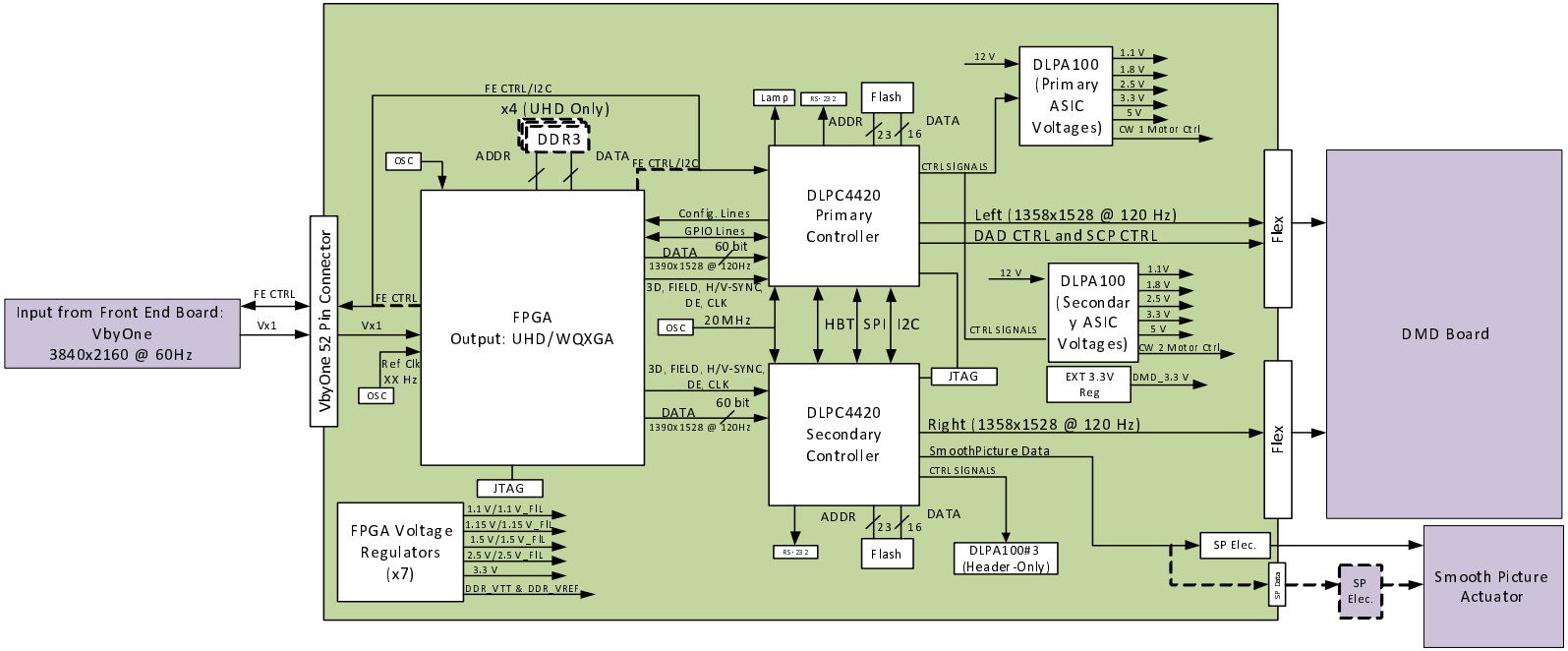
DLP®

TEXAS INSTRUMENTS

INDEX

		DWN Oscar Guevara DATE 6/29/20	TEXAS INSTRUMENTS
		ENGR Oscar Guevara	(C) COPYRIGHT 2018 TEXAS INSTRUMENTS ALL RIGHTS RESERVED
		SYST	TITLE: DLPC4420A Controller Board
		PRJ	
		QA	
NEXT ASSY	USED ON		A3 DRAWING NO DLP072 REV H
APPLICATION		SW Cadence Capture V.16.6	SCALE SHEET 1 of 36

Block Diagram



TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
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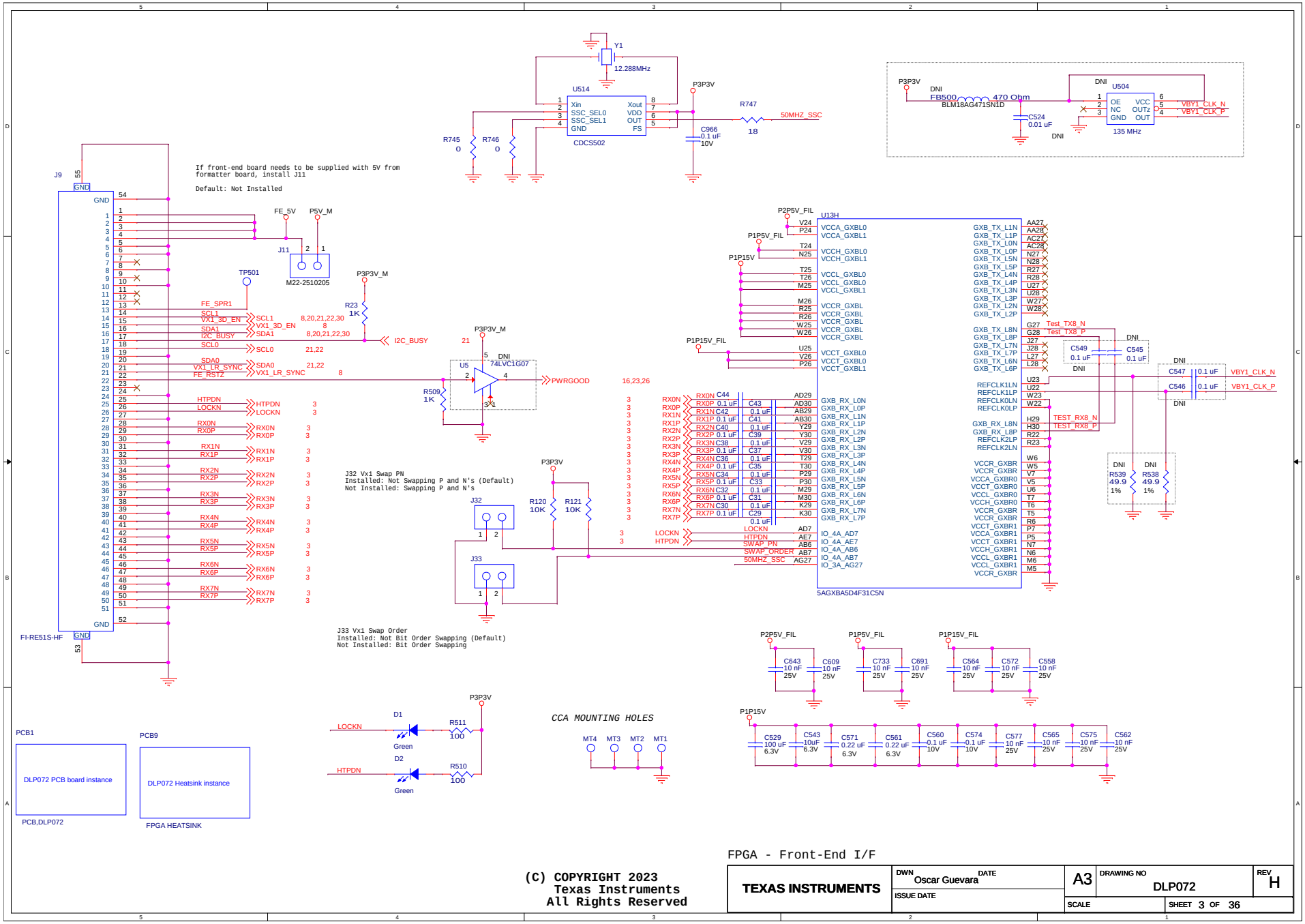
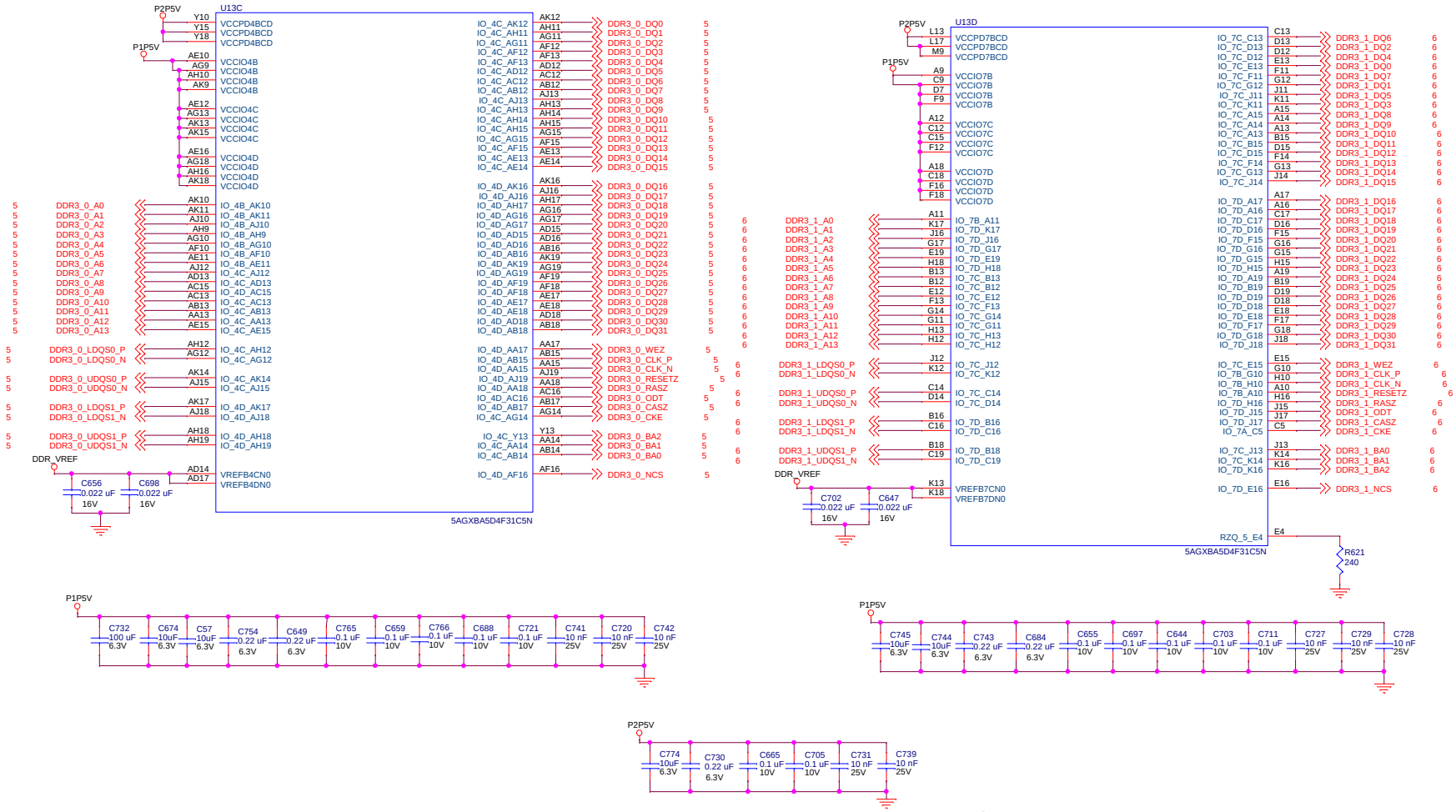


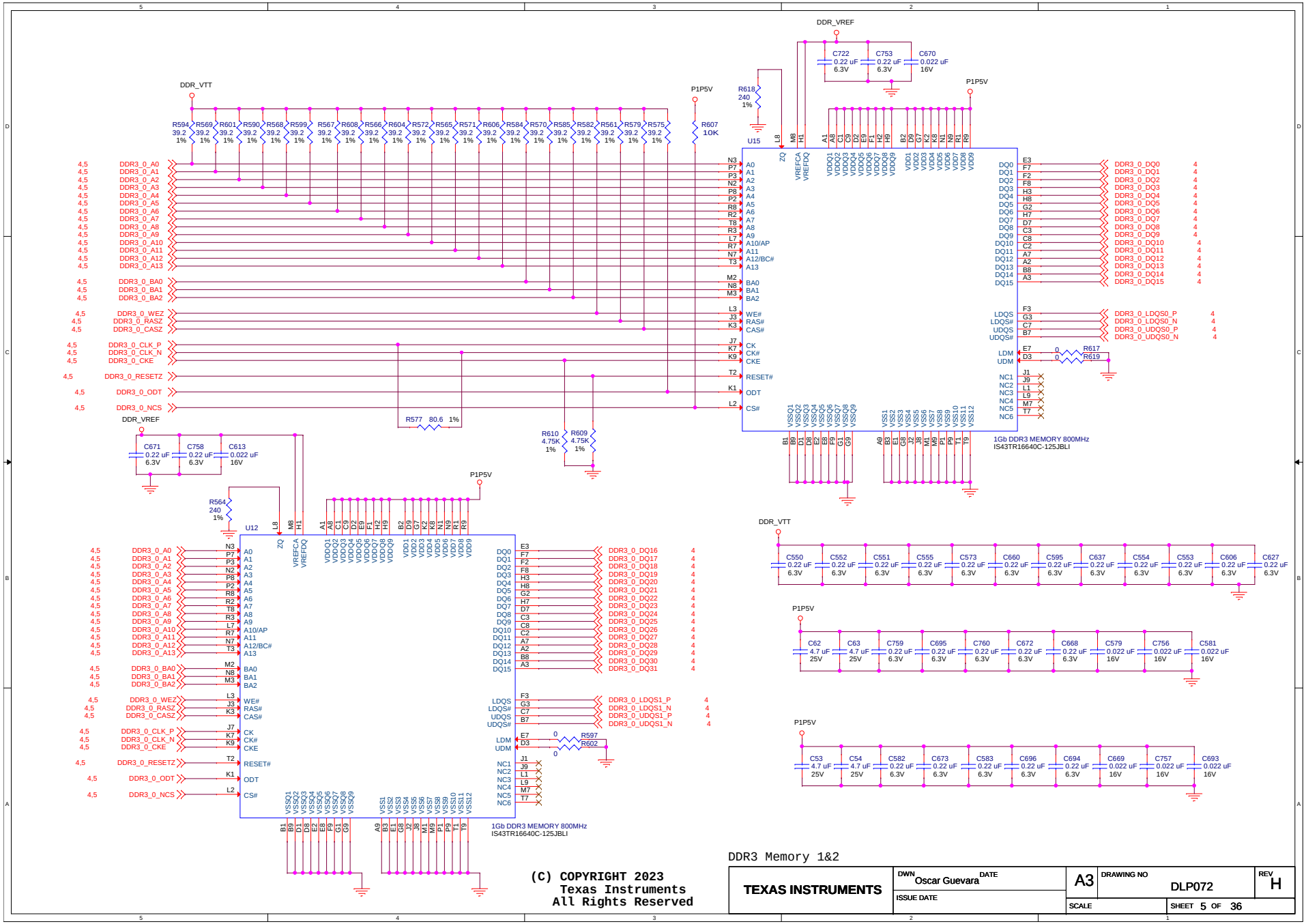
FPGA - Front-End I/F

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 3 OF 36



FPGA - DDR3 Interface

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 4 OF 36


DDR_VTT
P1P5V
DDR_VREF
R607 10K
R577 80.6 1%
R610 4.75K 1%
R609 4.75K 1%
R619 240 1%
R564 240 1%
U15
U12
1Gb DDR3 MEMORY 800MHz
IS43TR16640C-125JBLI
DDR3 Memory 1&2
TEXAS INSTRUMENTS
(C) COPYRIGHT 2023
Texas Instruments
All Rights Reserved
DWN Oscar Guevara
DATE
ISSUE DATE
A3
DRAWING NO DLP072
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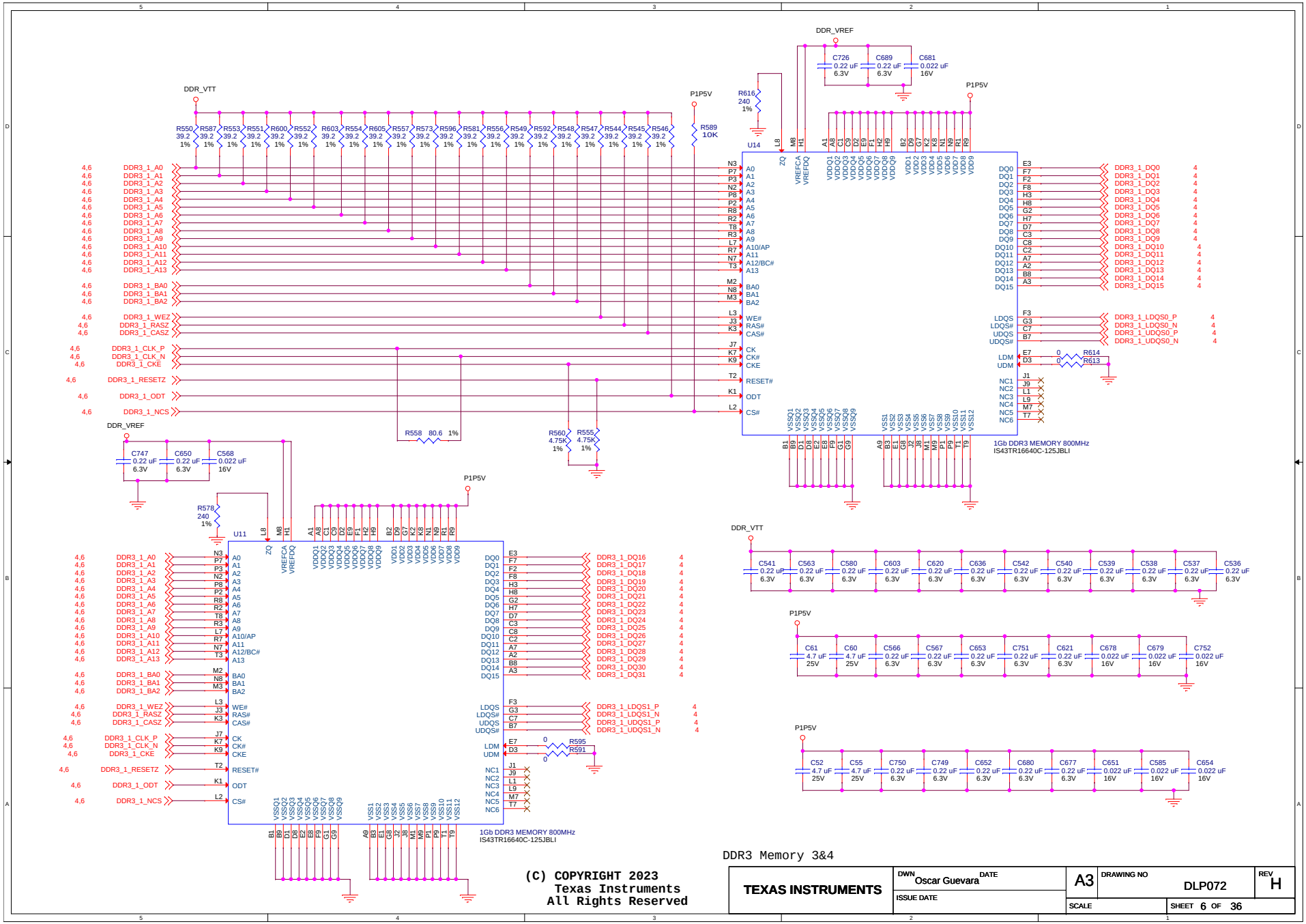
DDR_VREF
DDR_VTT
P1P5V
U14
U11
1Gb DDR3 MEMORY 800MHz
IS43TR16640C-125JBLI
DDR3 Memory 3&4
(C) COPYRIGHT 2023
Texas Instruments
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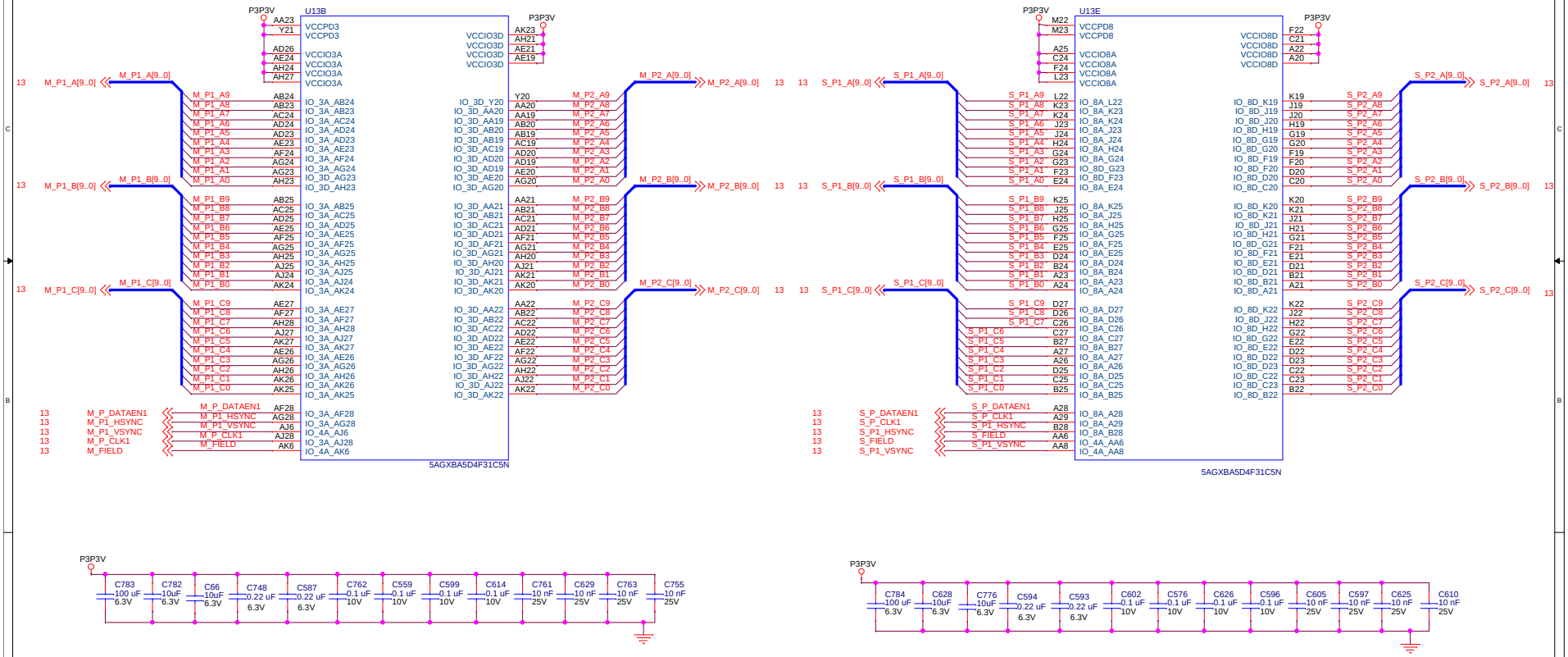
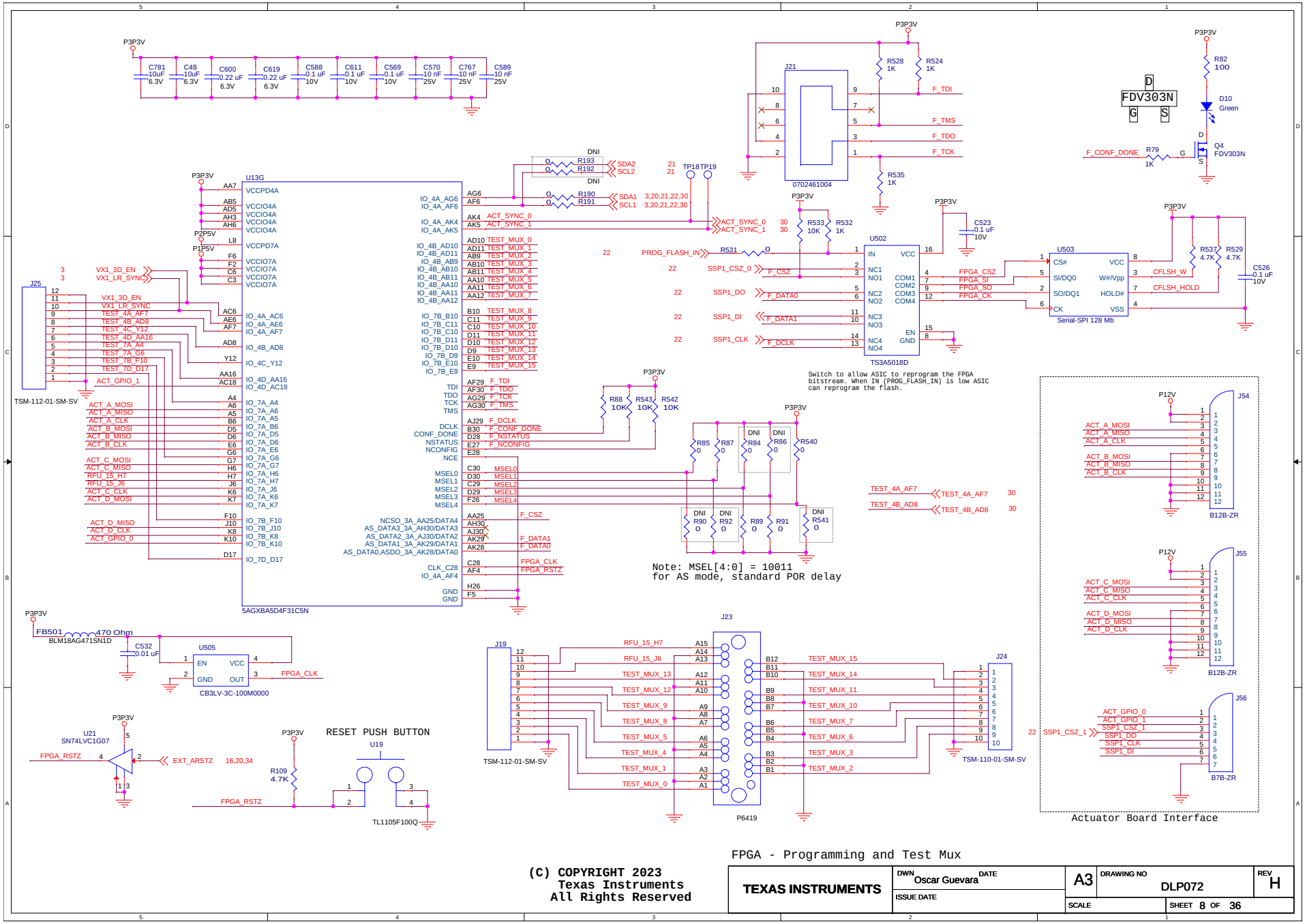


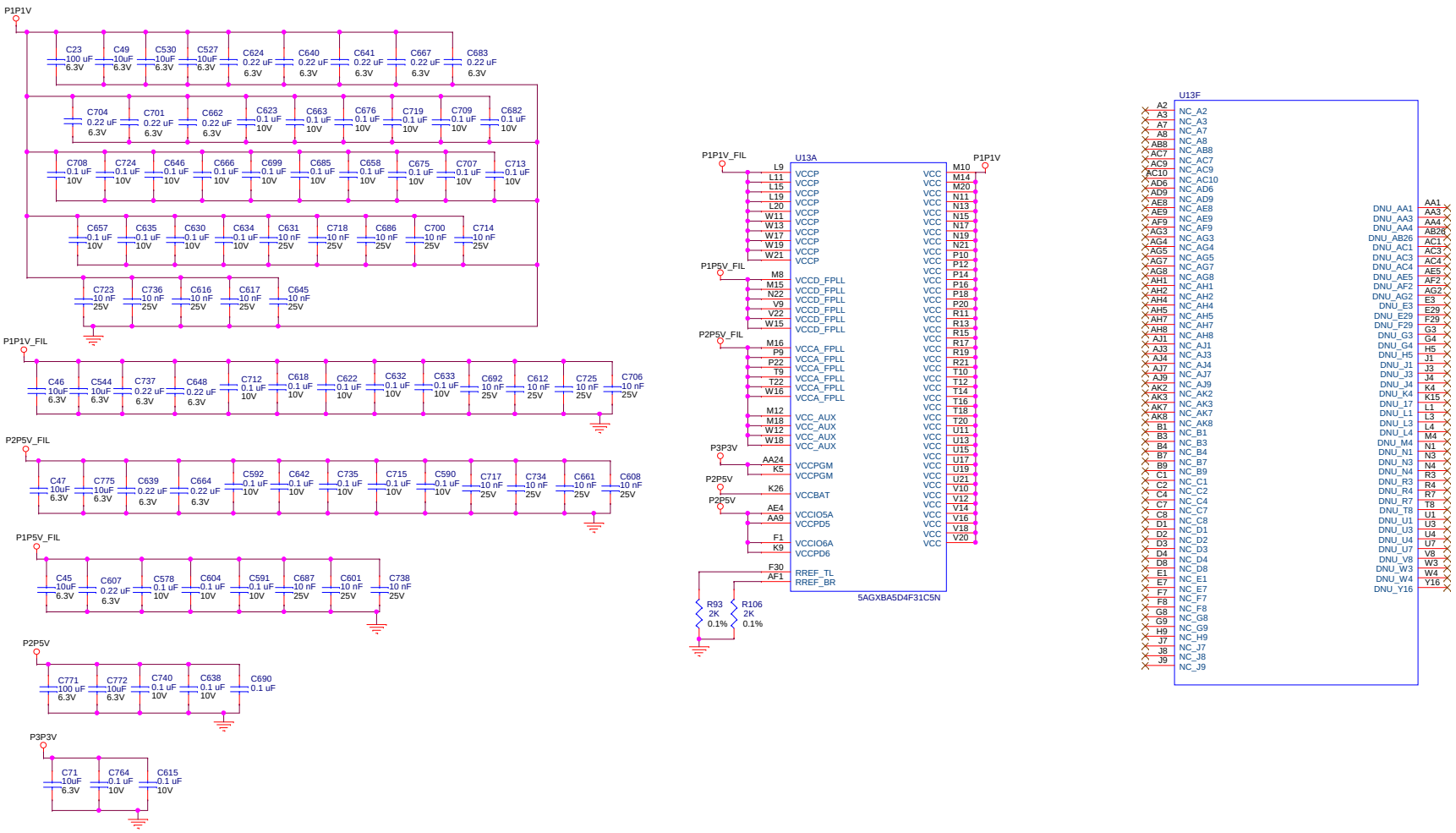
FPGA - Video I/F

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 7 OF 36



FPGA - Programming and Test Mux

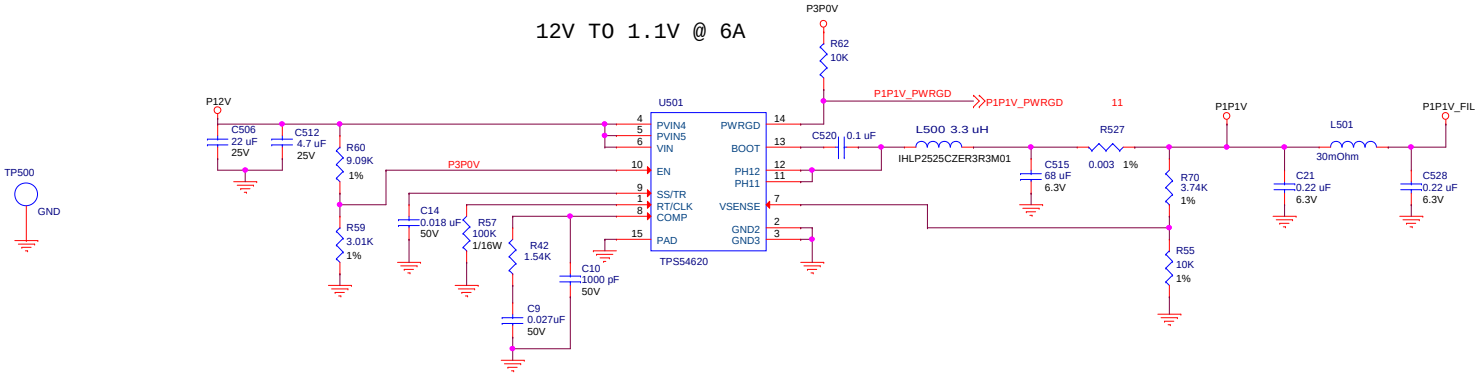
TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 8 OF 36



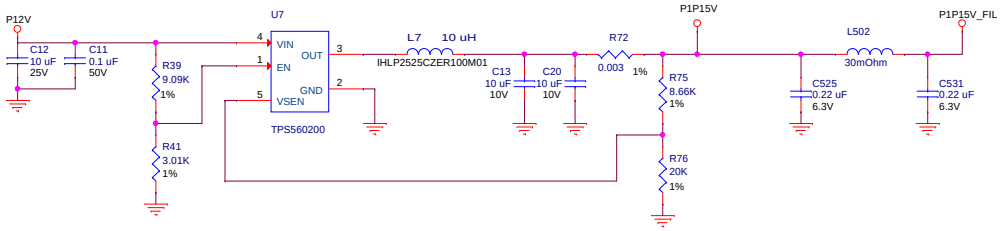
FPGA - Power

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 9 OF 36

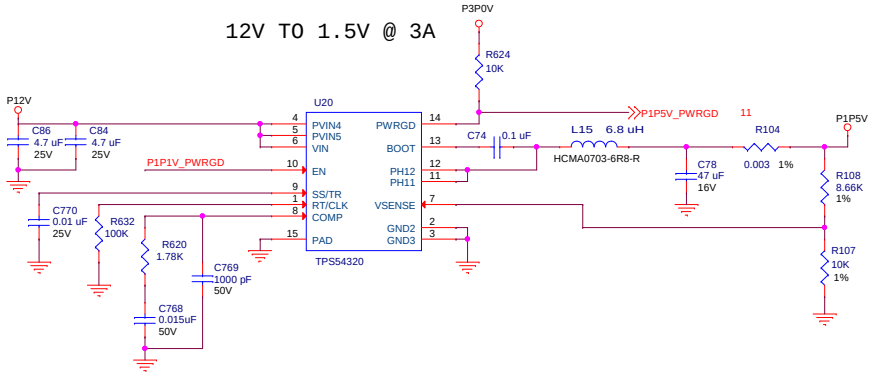
12V TO 1.1V @ 6A



12V TO 1.15V @ 500mA



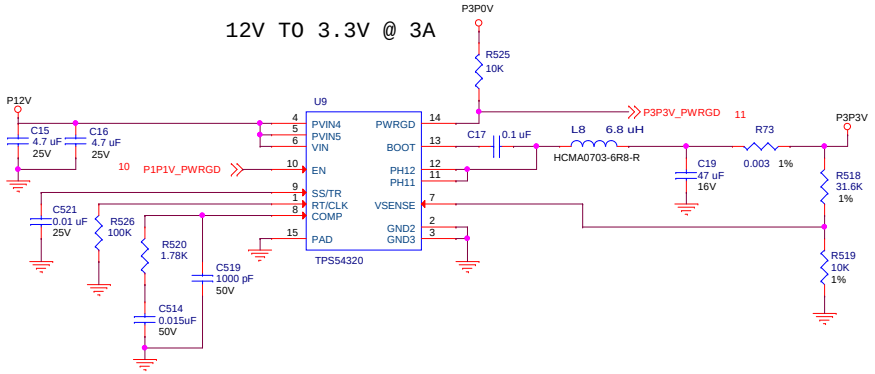
12V TO 1.5V @ 3A



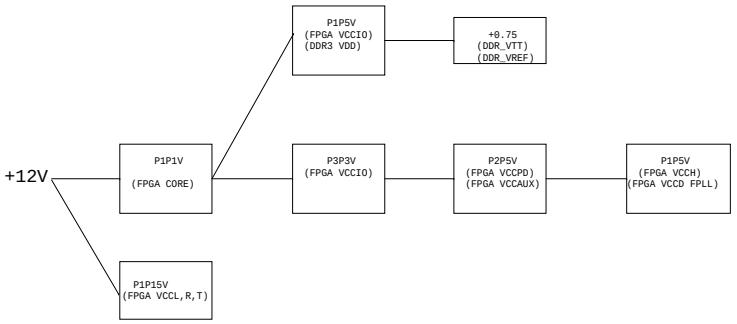
FPGA - Regulators

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 10 OF 36

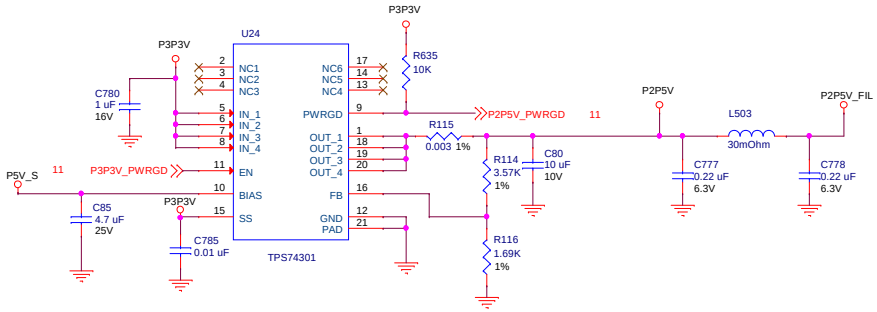
12V TO 3.3V @ 3A



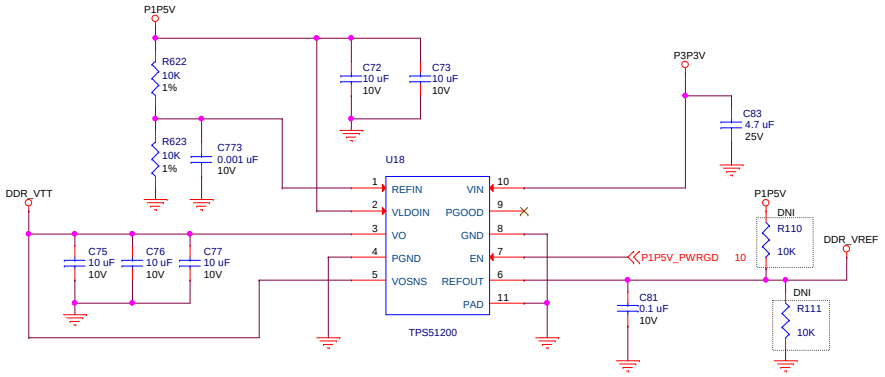
Power Sequence



3.3V TO 2.5V @ 1.5A

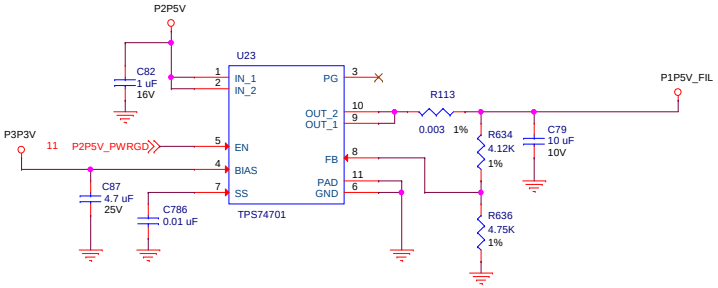


1.5V TO 0.75V DDR_VTT & DDR_VREF



DDR TERMINATION VOLTAGE

2.5V TO 1.5V @ 500mA



FPGA - Regulators

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
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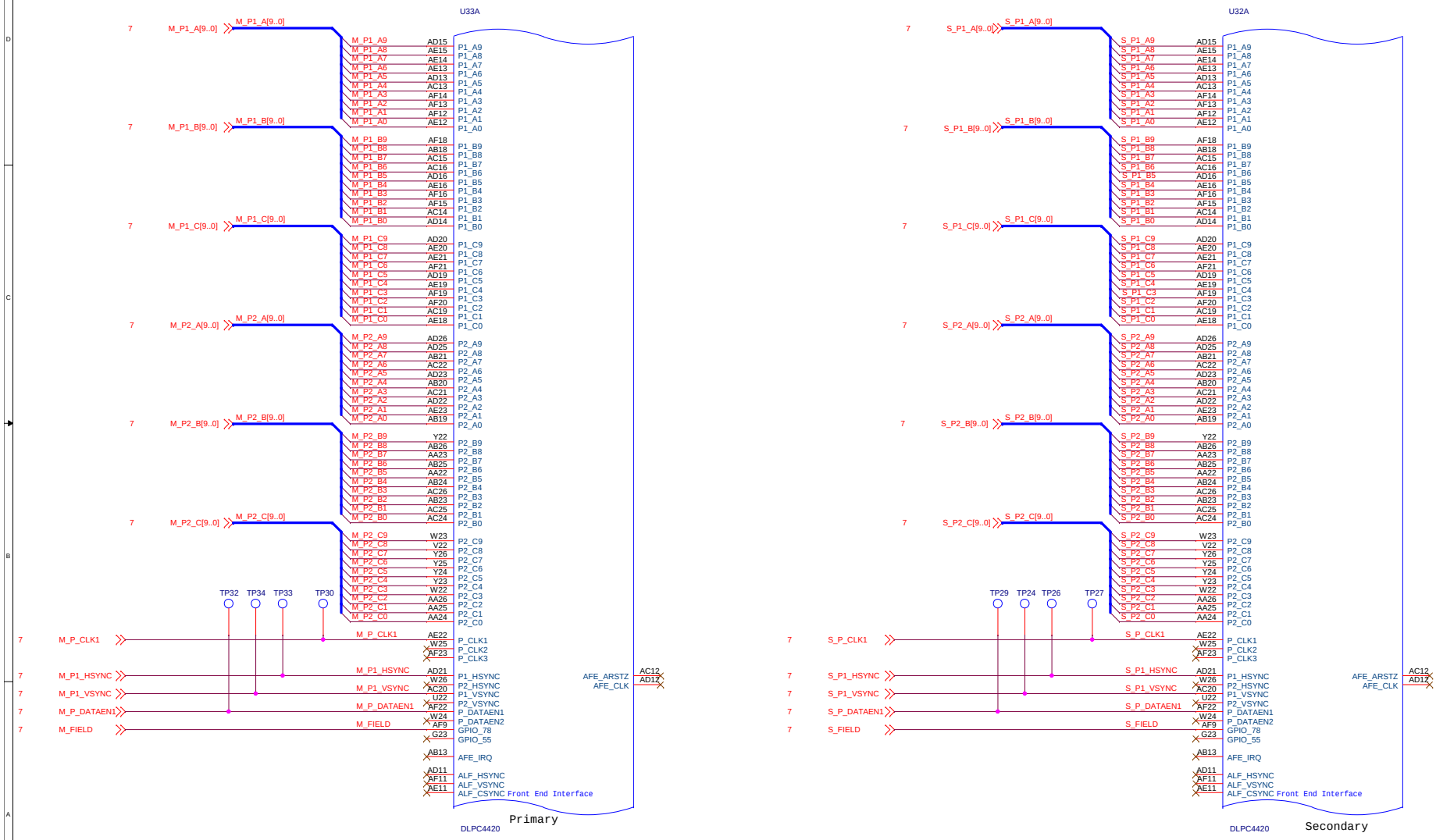
FPGA - GND

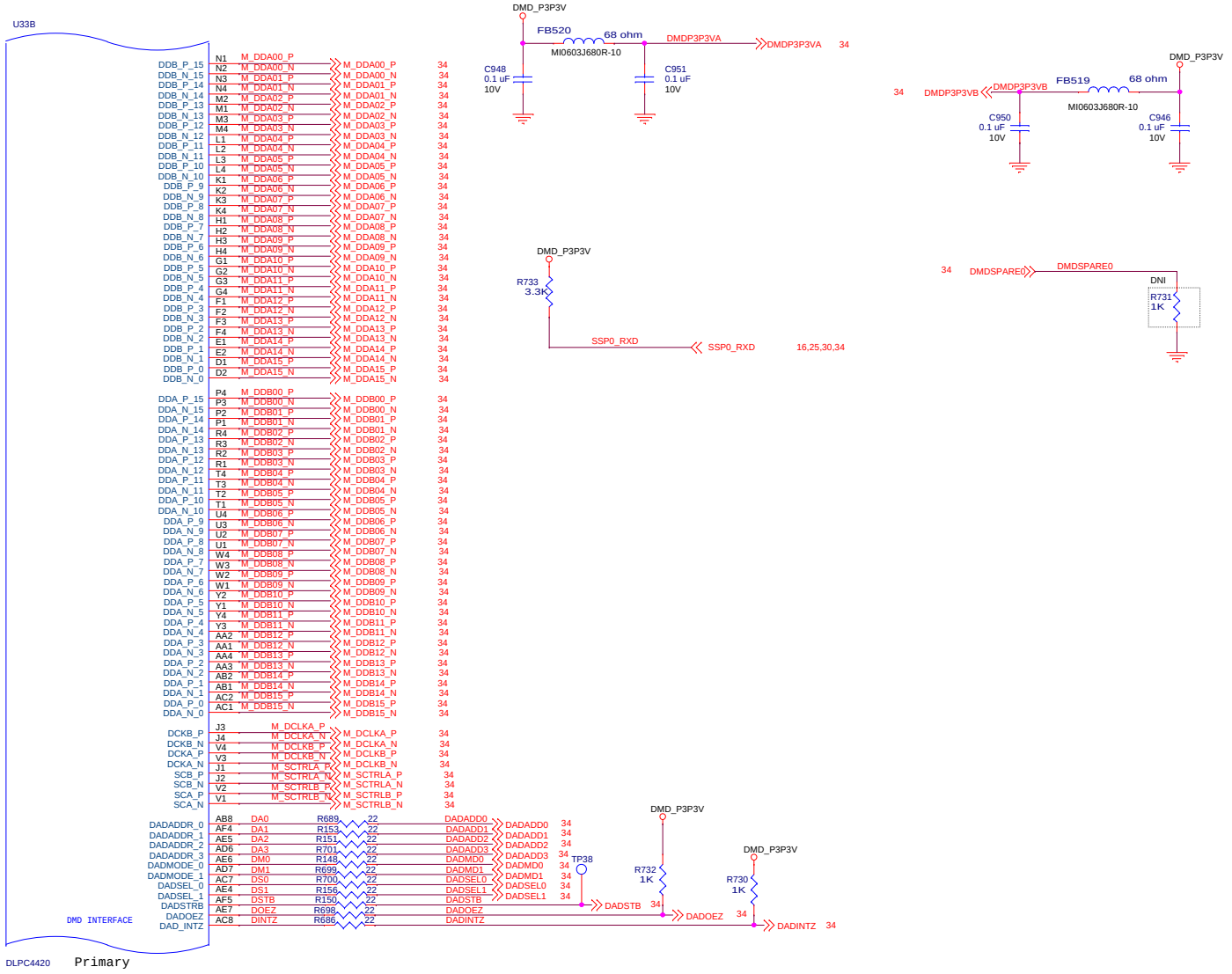
TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE	SCALE	SHEET 12 OF 34	



Primary and Secondary Front End Interface

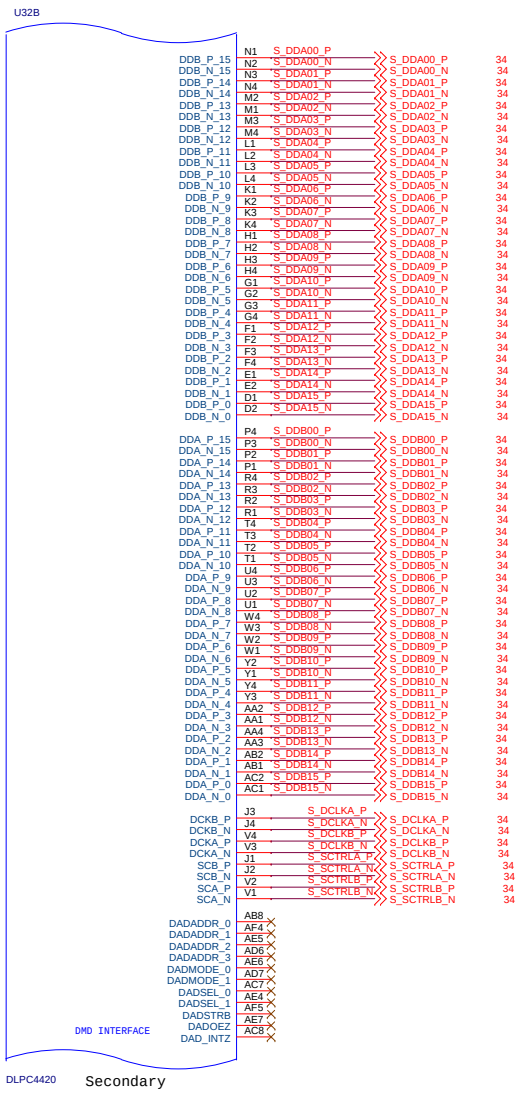
TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072 REV H
	ISSUE DATE	SCALE	SHEET 13 OF 36

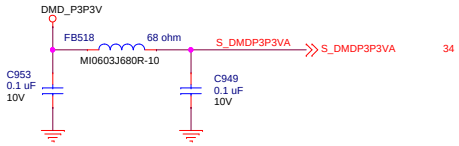
DMD Interface is BUS & BIT Swappable

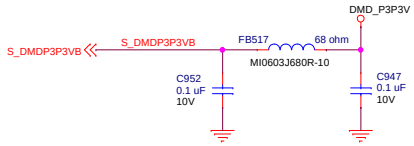


Primary Controller DMD Flex Interface

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 14 OF 36

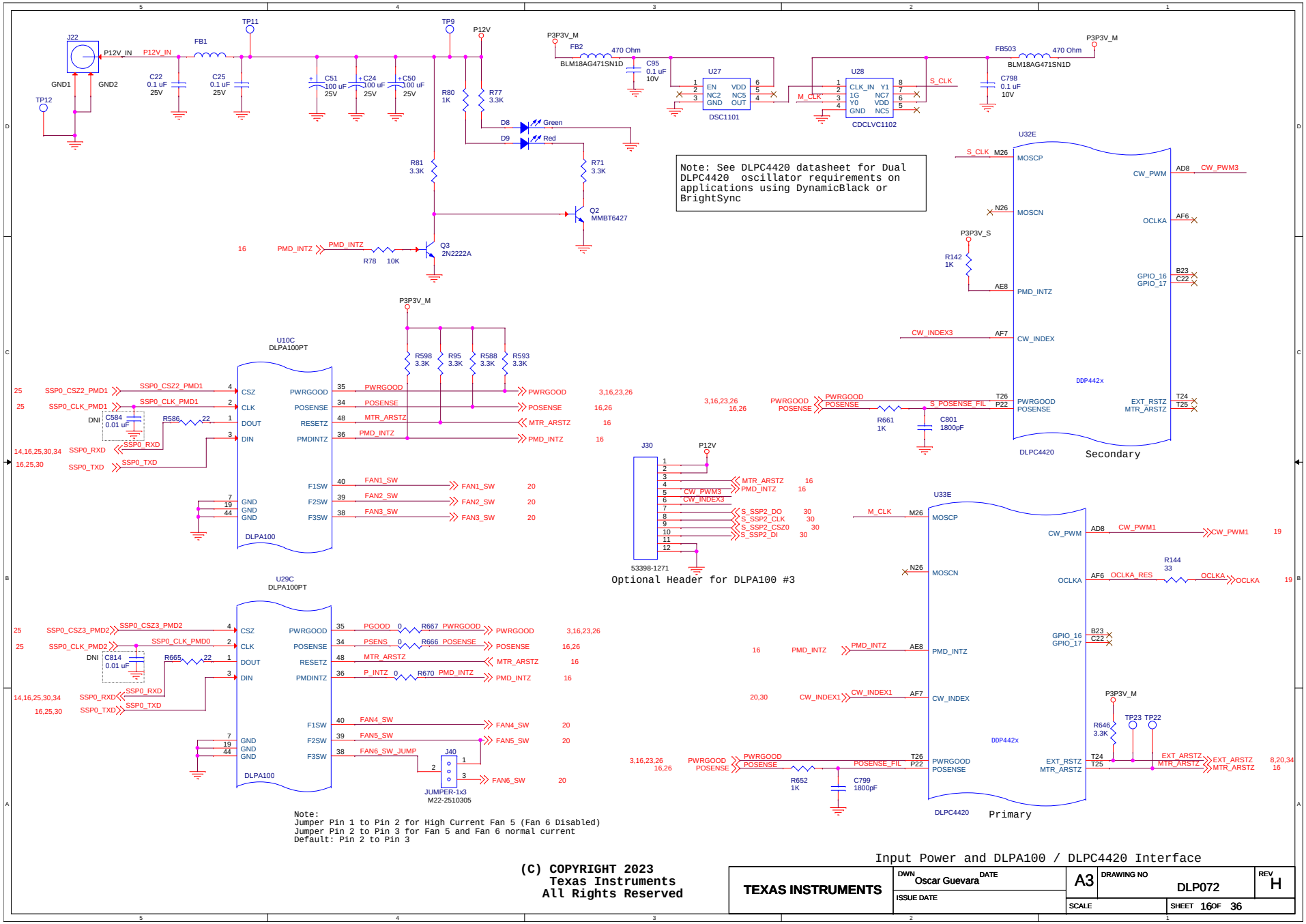






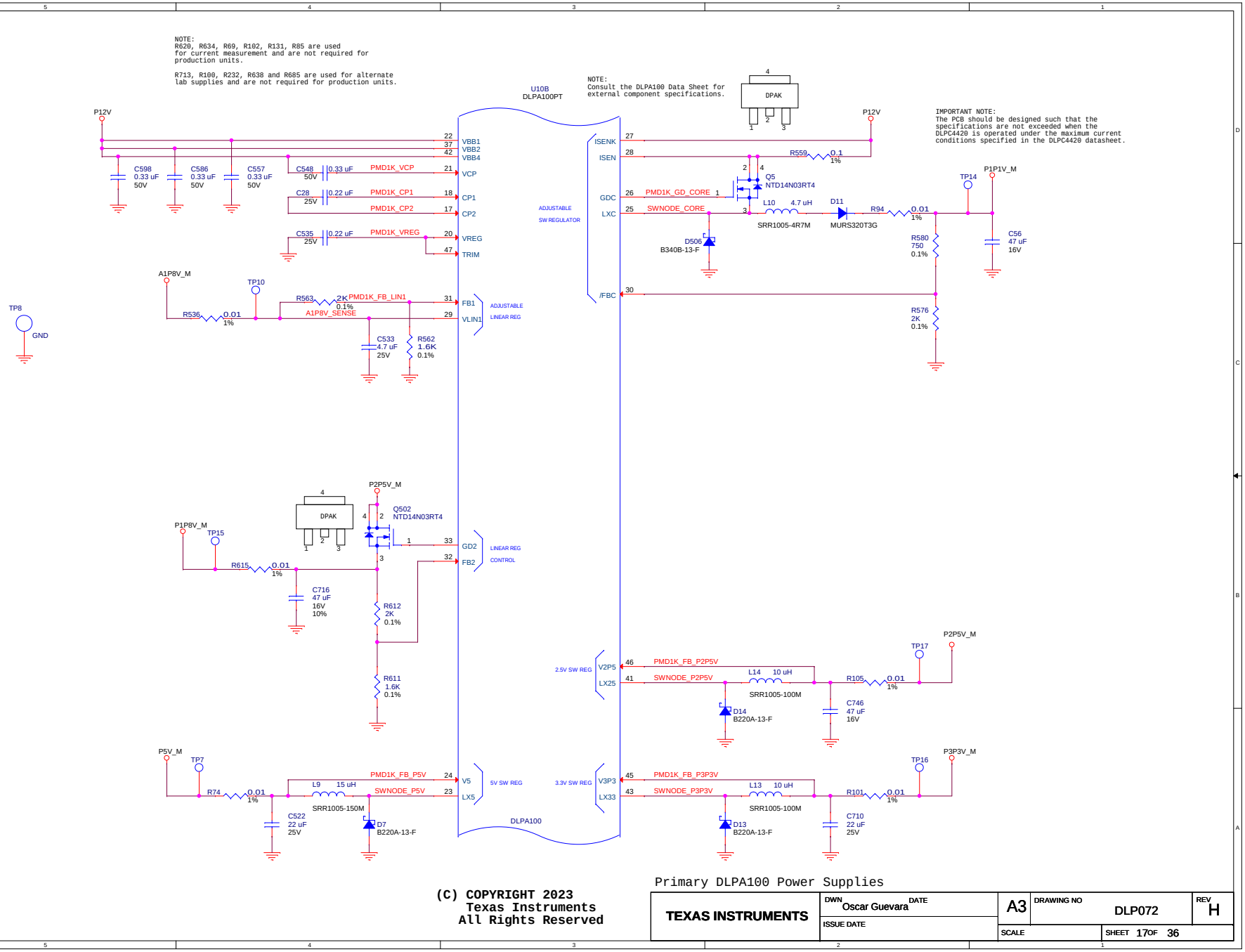
Secondary Controller DMD Flex Interface

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072 REV H
	ISSUE DATE	SCALE	SHEET 15 OF 36



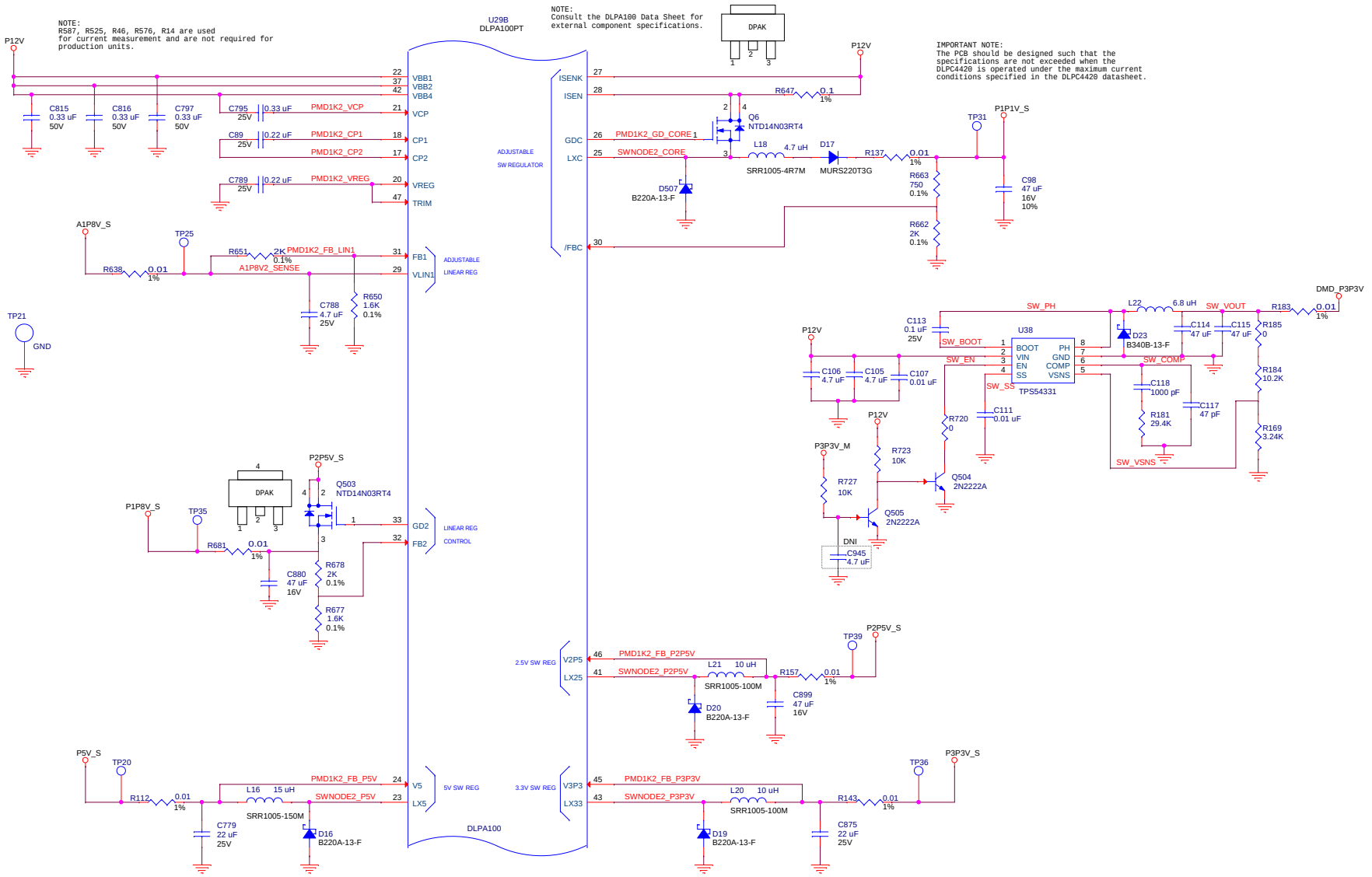
Input Power and DLPA100 / DLPC4420 Interface

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 16 OF 36



Primary DLPA100 Power Supplies

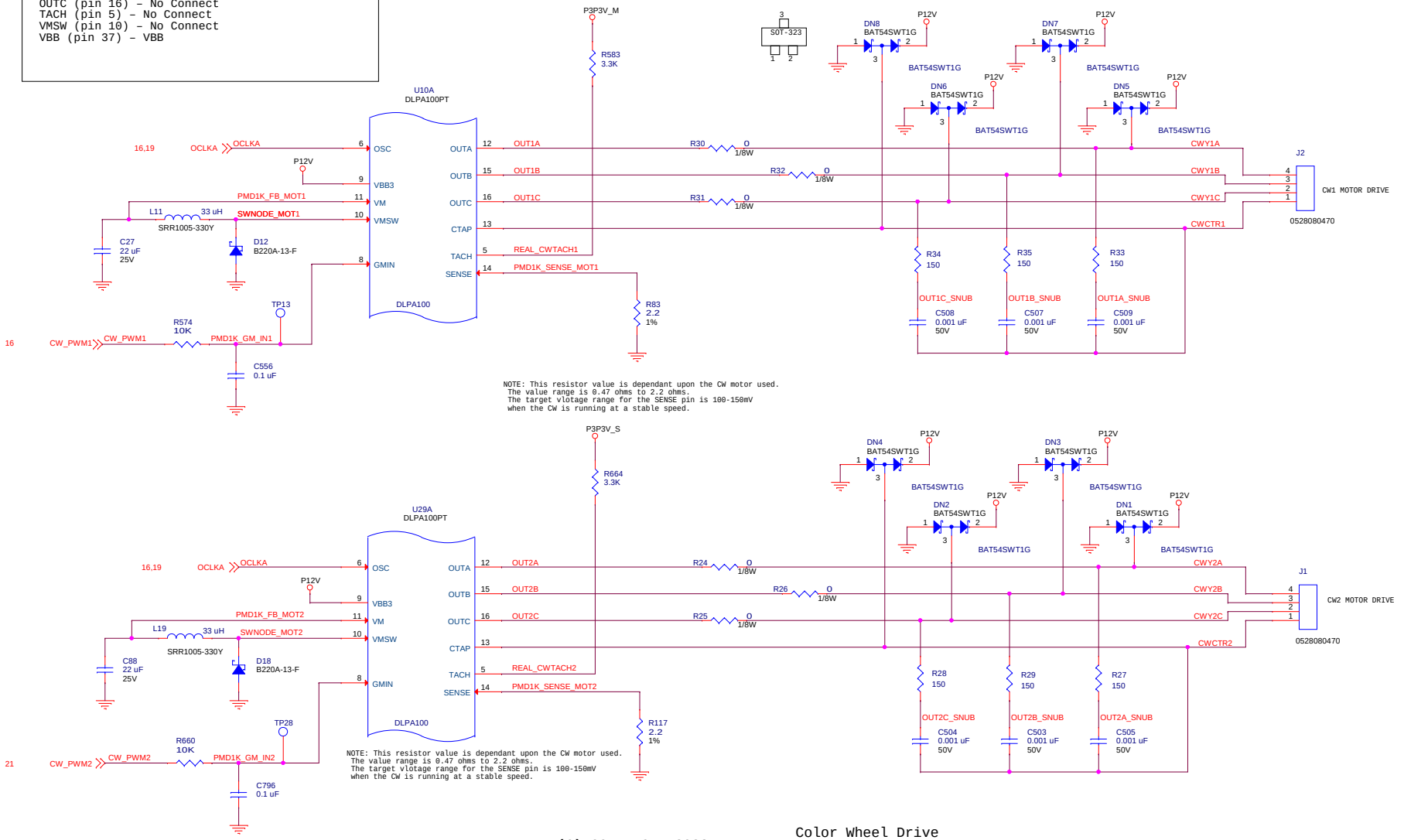
TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 17 OF 36



Secondary DLPA100 Supplies

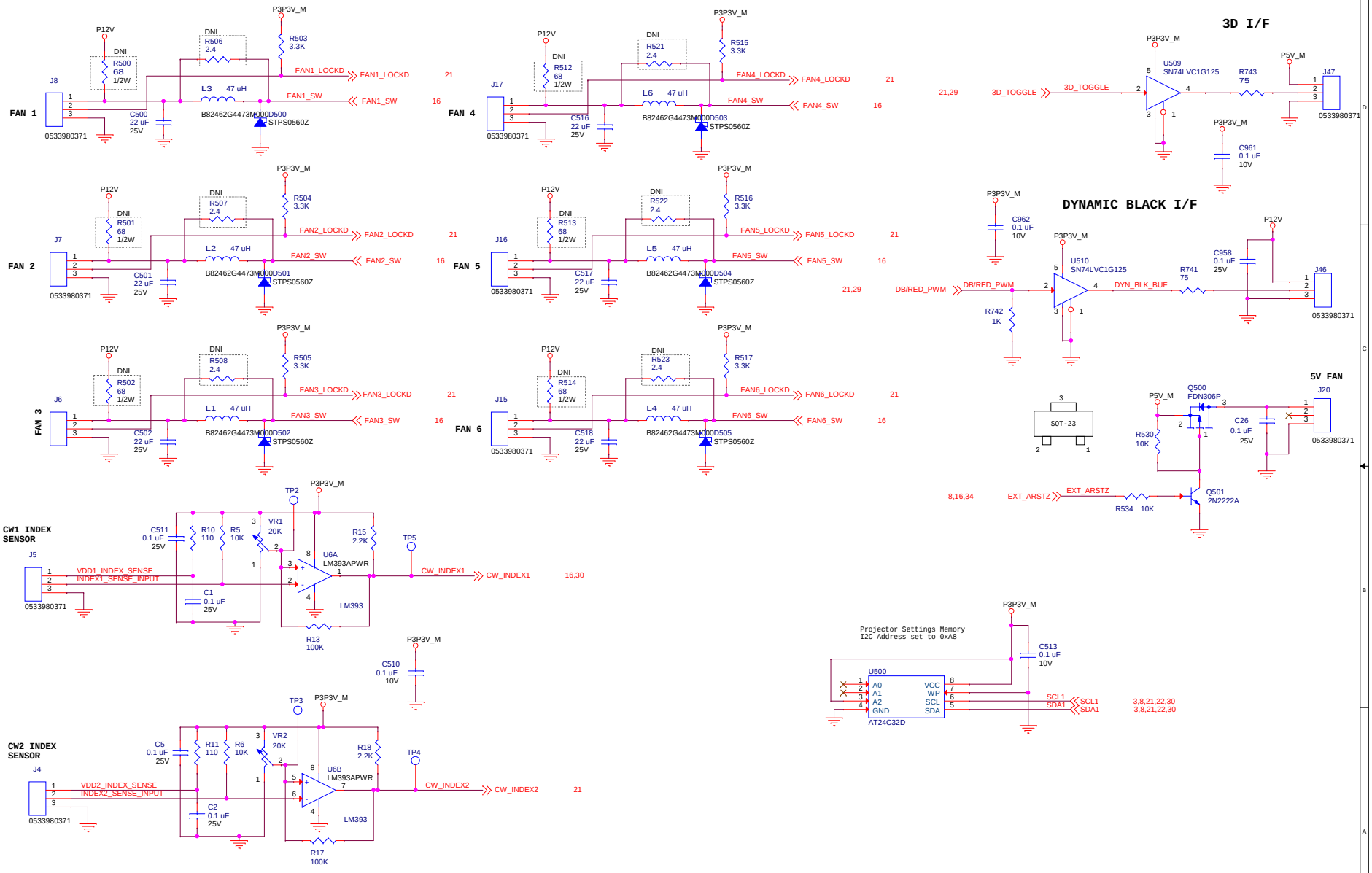
TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 18 OF 34

Note: If not using the motor driver on the
DLPA100 follow these guidelines for unused pins:
GMIN (pin 8) – Ground
OSC (pin 6) – Ground
SENSE (pin 14) – Ground
CTAP (pin 13) – VBB
VM (pin 11) – VBB
OUTA (pin 12) – No Connect
OUTB (pin 15) – No Connect
OUTC (pin 16) – No Connect
TACH (pin 5) – No Connect
VMSW (pin 10) – No Connect
VBB (pin 37) – VBB



Color Wheel Drive

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 19 OF 36



Fan, Color Wheel Interface and Peripherals

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072 REV H
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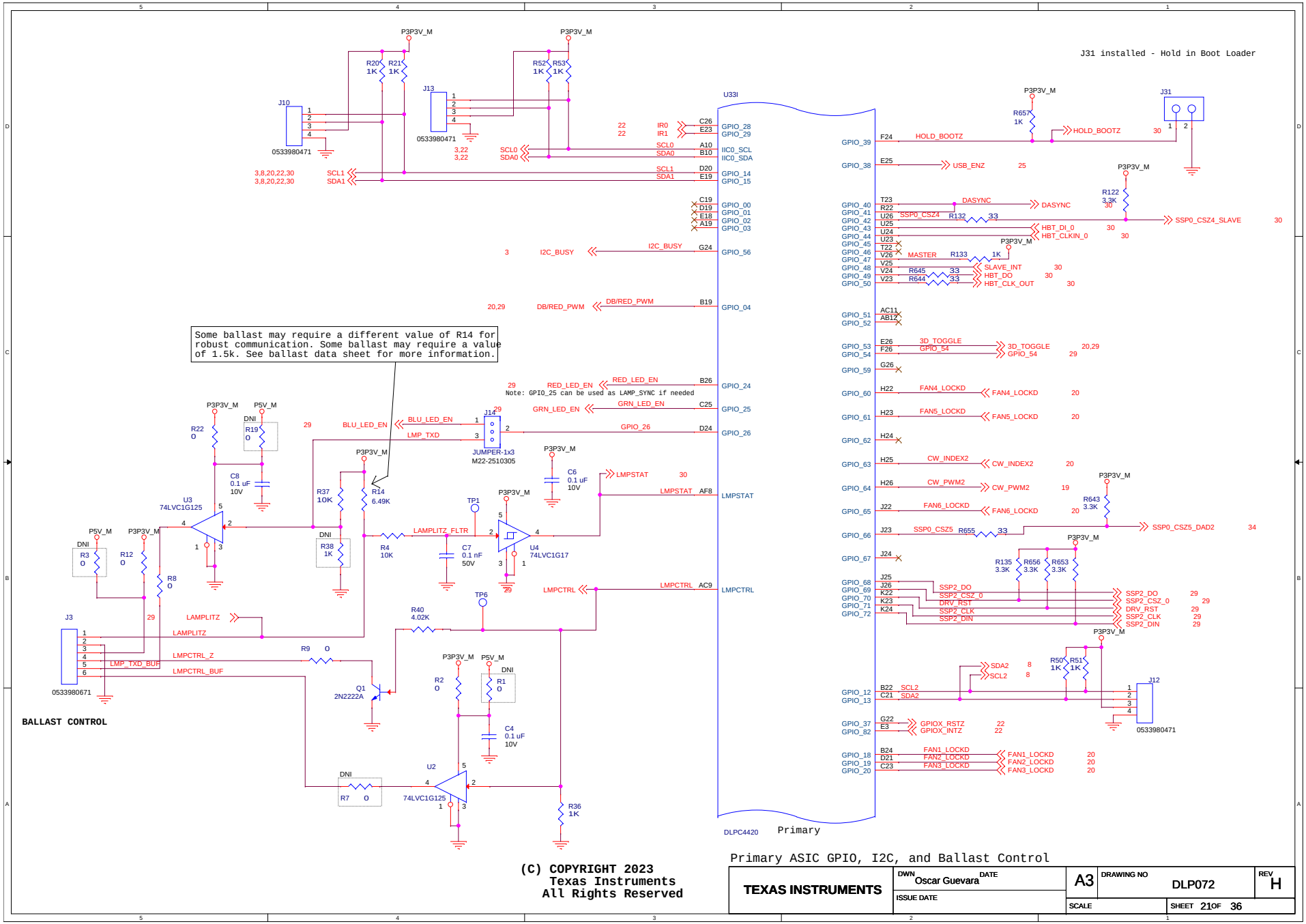
J31 installed - Hold in Boot Loader
Some ballast may require a different value of R14 for robust communication. Some ballast may require a value of 1.5k. See ballast data sheet for more information.
BALLAST CONTROL
U33I
DLPC4420
Primary
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Primary ASIC GPIO, I2C, and Ballast Control
TEXAS INSTRUMENTS
DWN Oscar Guevara
DATE
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DRAWING NO DLP072
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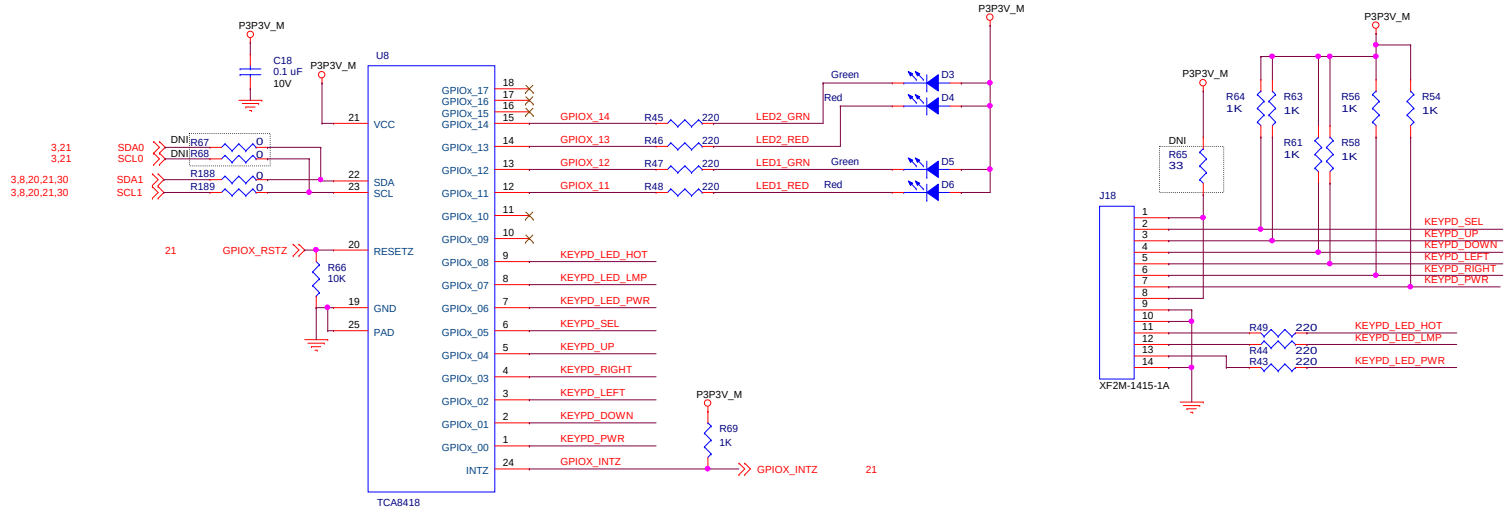
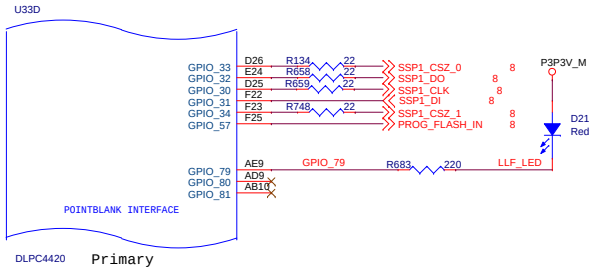
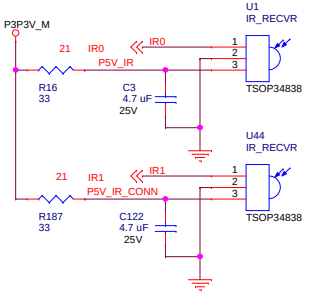
KEYBOARD INTERFACE

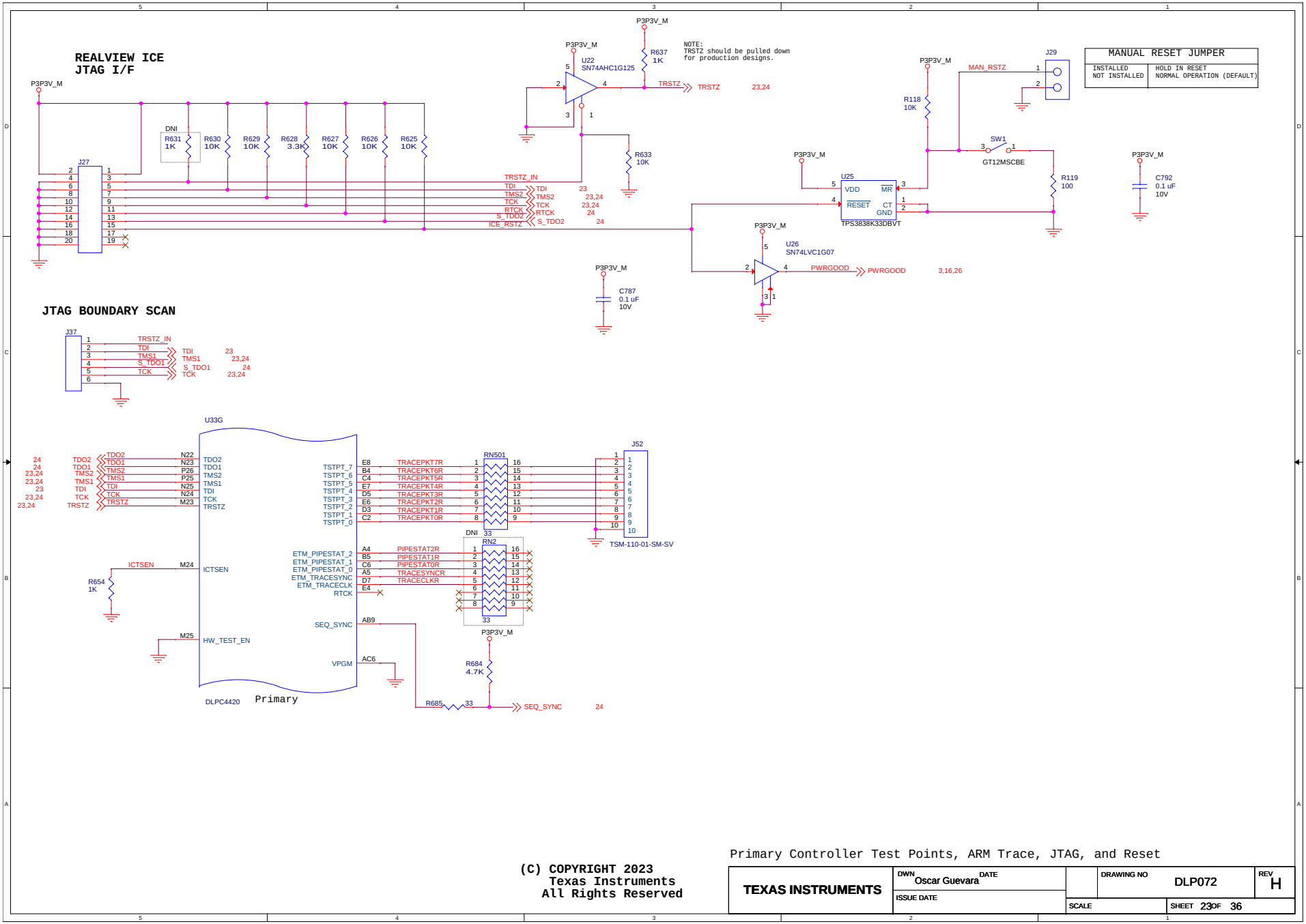






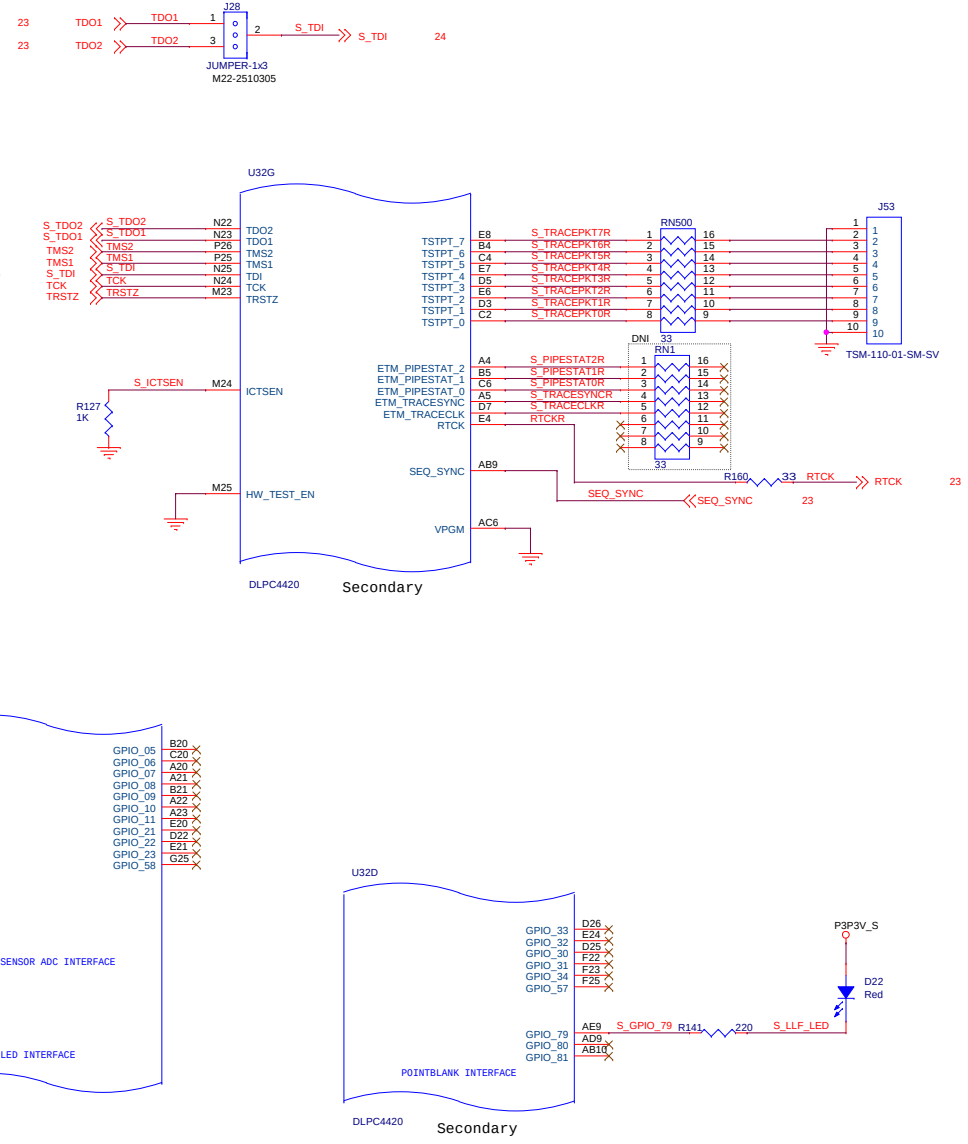
GPIO Expander, Keypad Interface and IR Interface

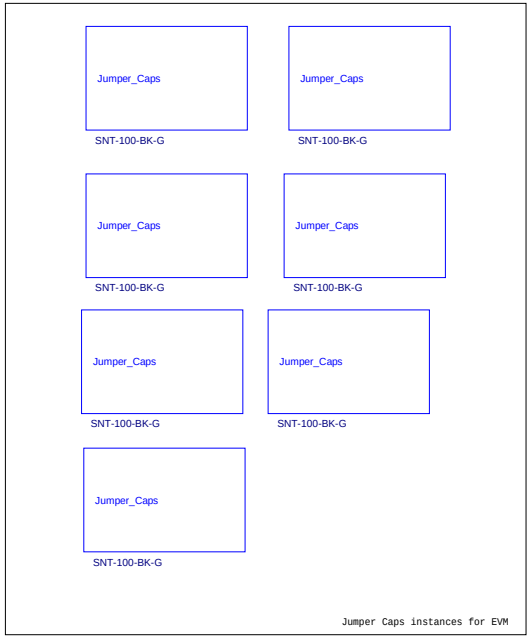
TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 22 OF 36



Primary Controller Test Points, ARM Trace, JTAG, and Reset

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	DRAWING NO DLP072	REV H
	ISSUE DATE	SCALE	SHEET 23 OF 36

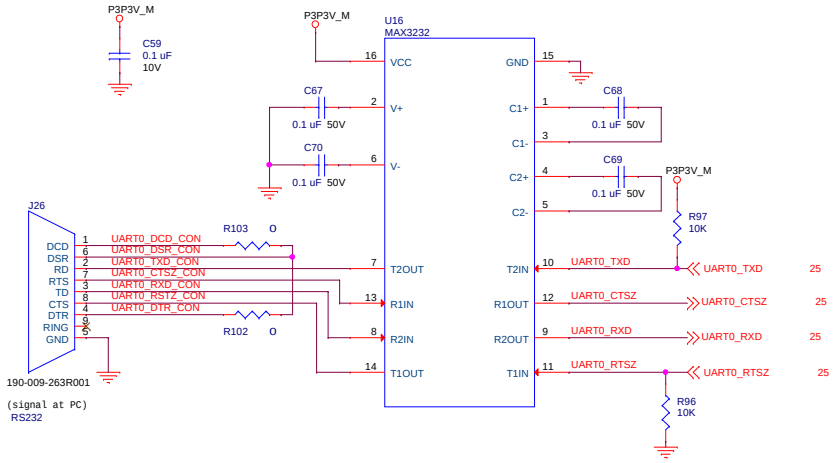


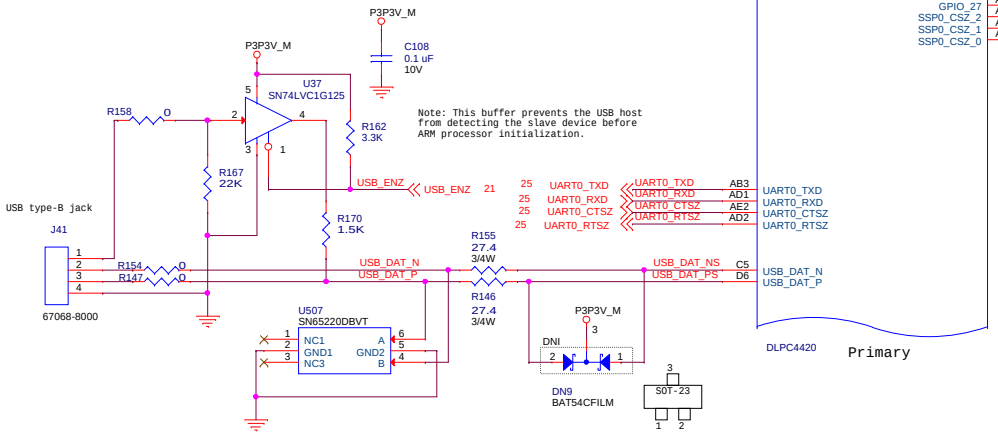


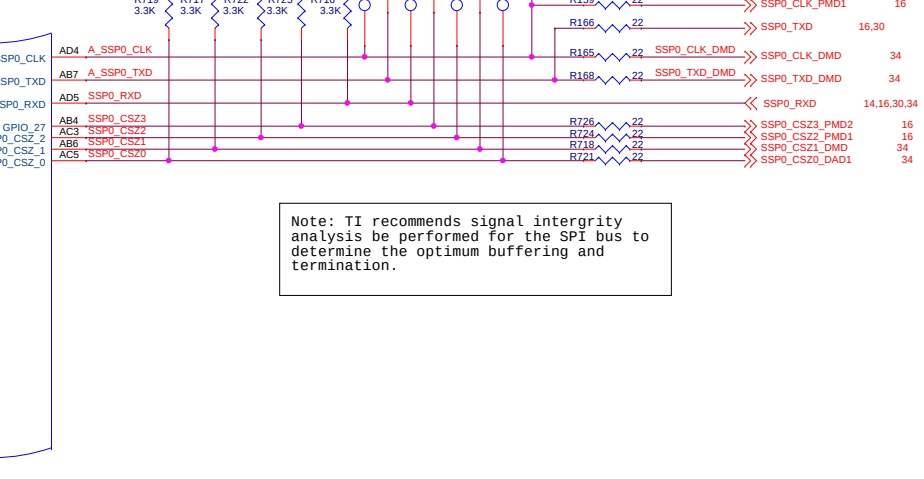
Secondary Controller Test Points, ARM Trace, and JTAG

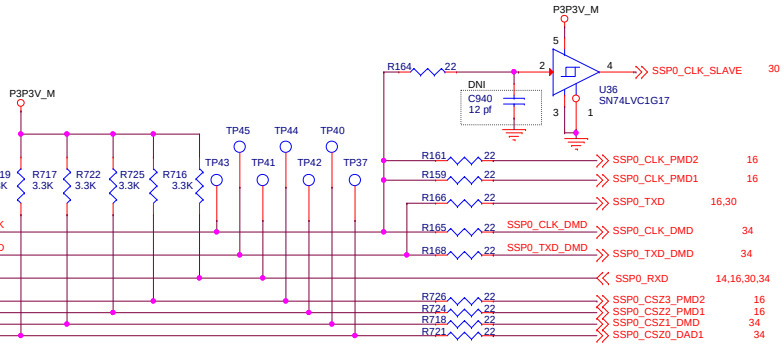
TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 24 OF 34

RS - 232 PORT 0





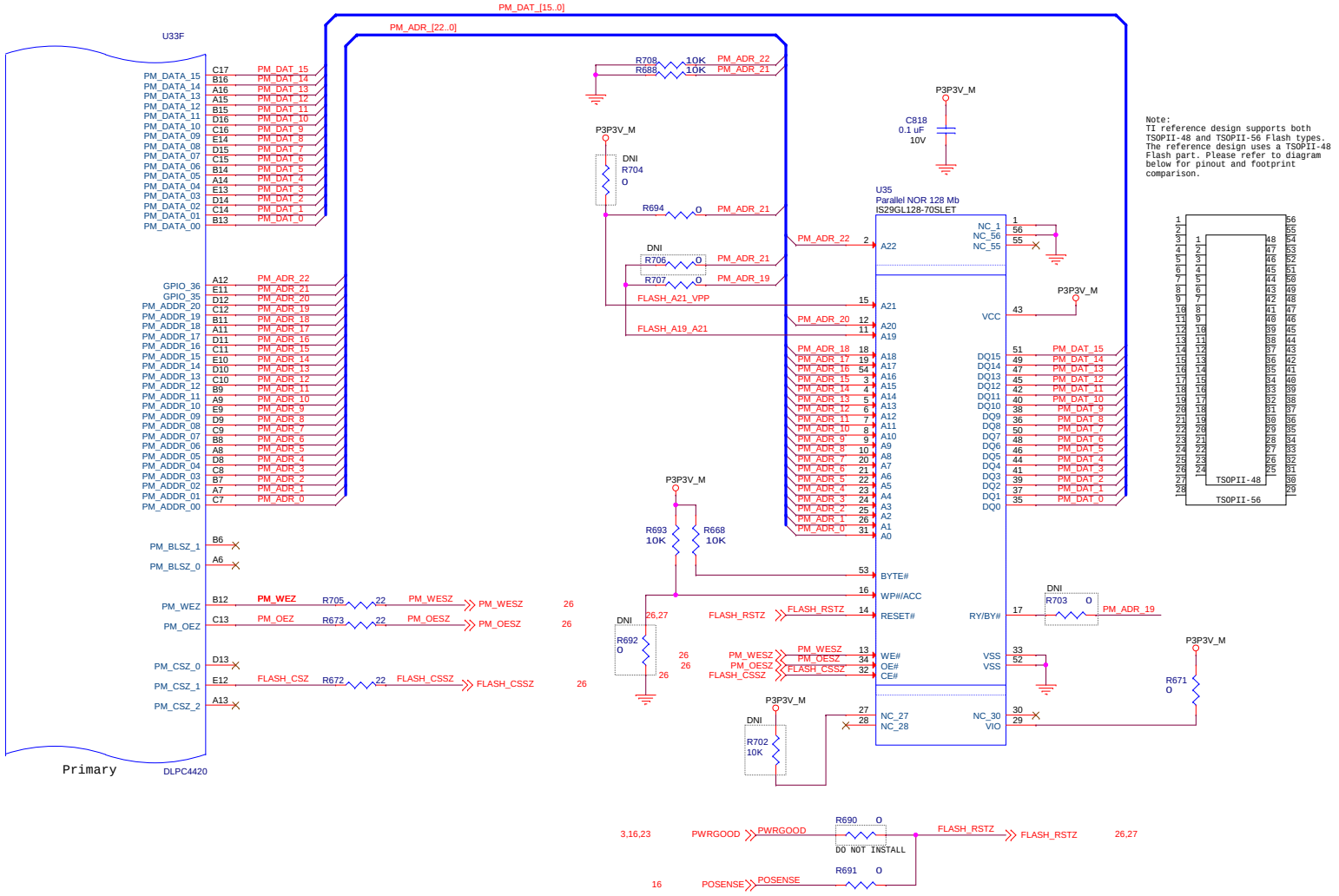




Note: TI recommends signal intergrity analysis be performed for the SPI bus to determine the optimum buffering and termination.

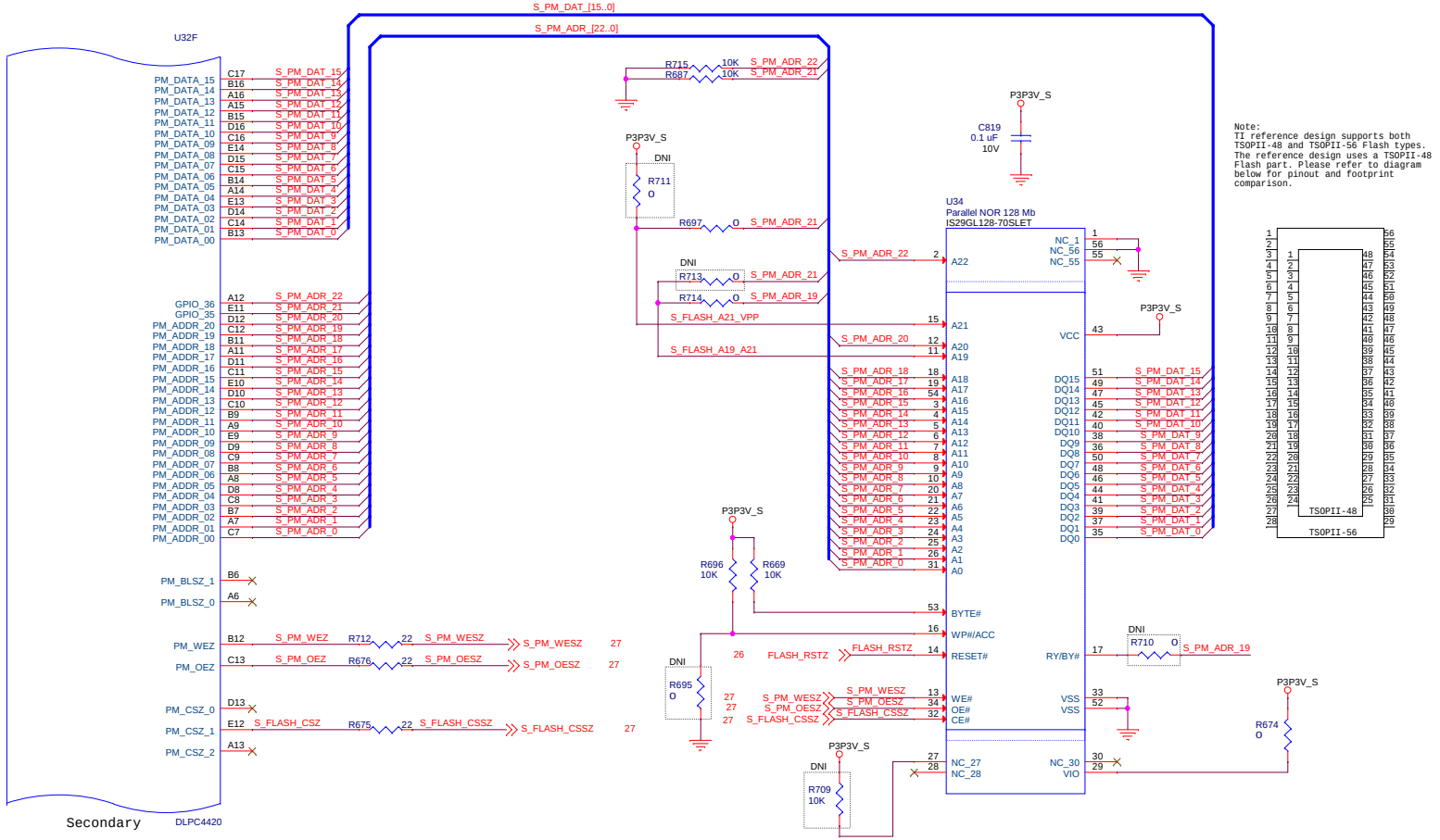
Primary Controller RS-232, Synchronous Serial Port, and USB

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072 REV H
	ISSUE DATE	SCALE	SHEET 25 OF 36



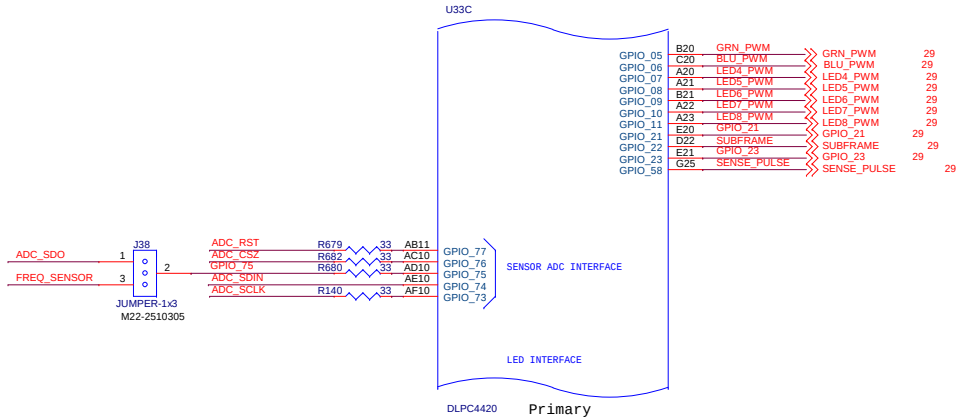
Primary Controller Flash Memory Interface

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 26 OF 36

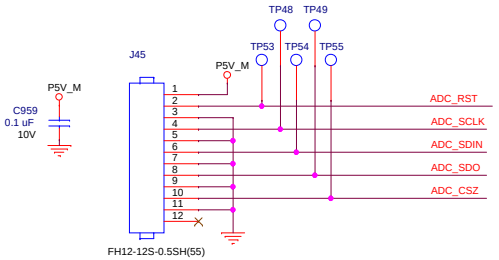


Secondary Controller Flash Memory Interface

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 27 OF 36



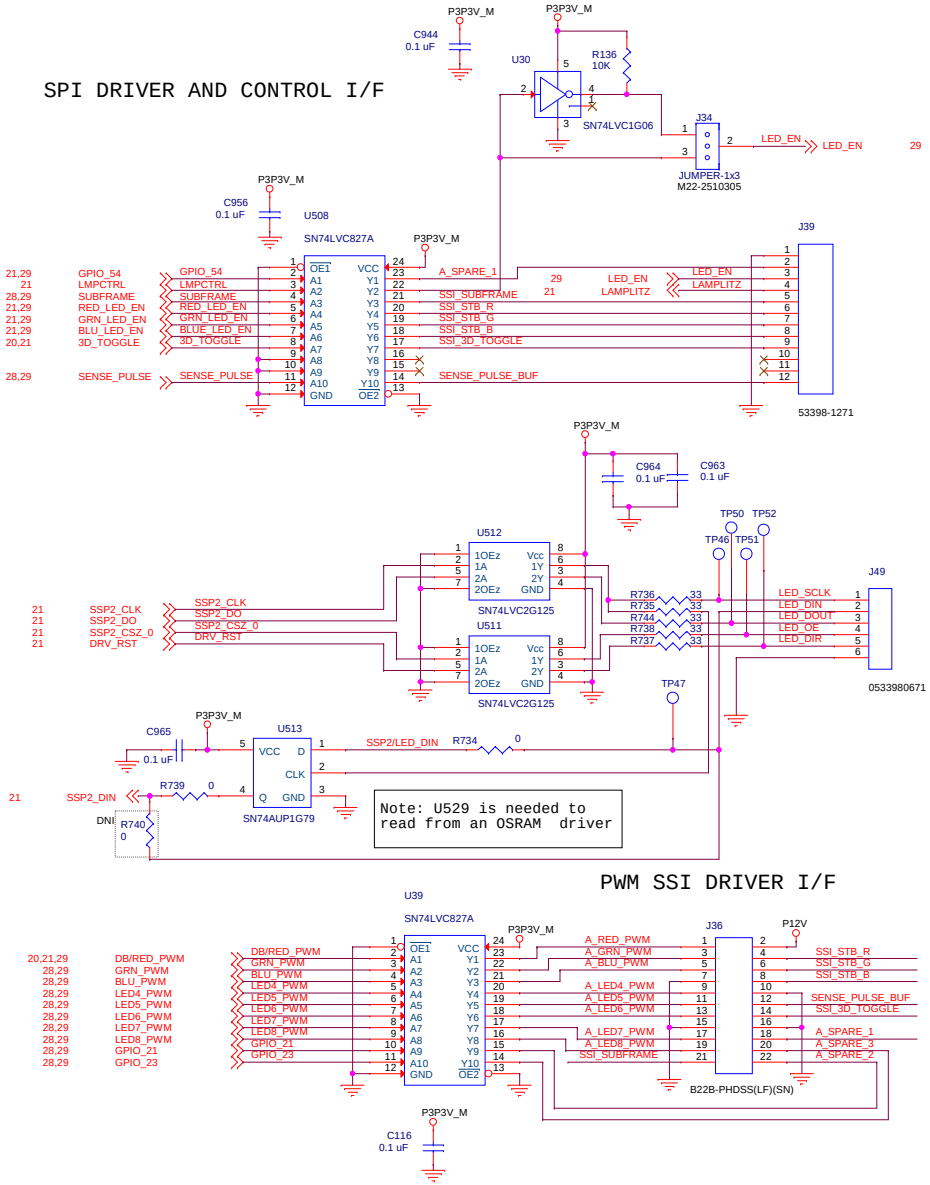
ADC INTEGRATING SENSOR BOARD I/F



LIGHT TO FREQUENCY SENSOR I/F

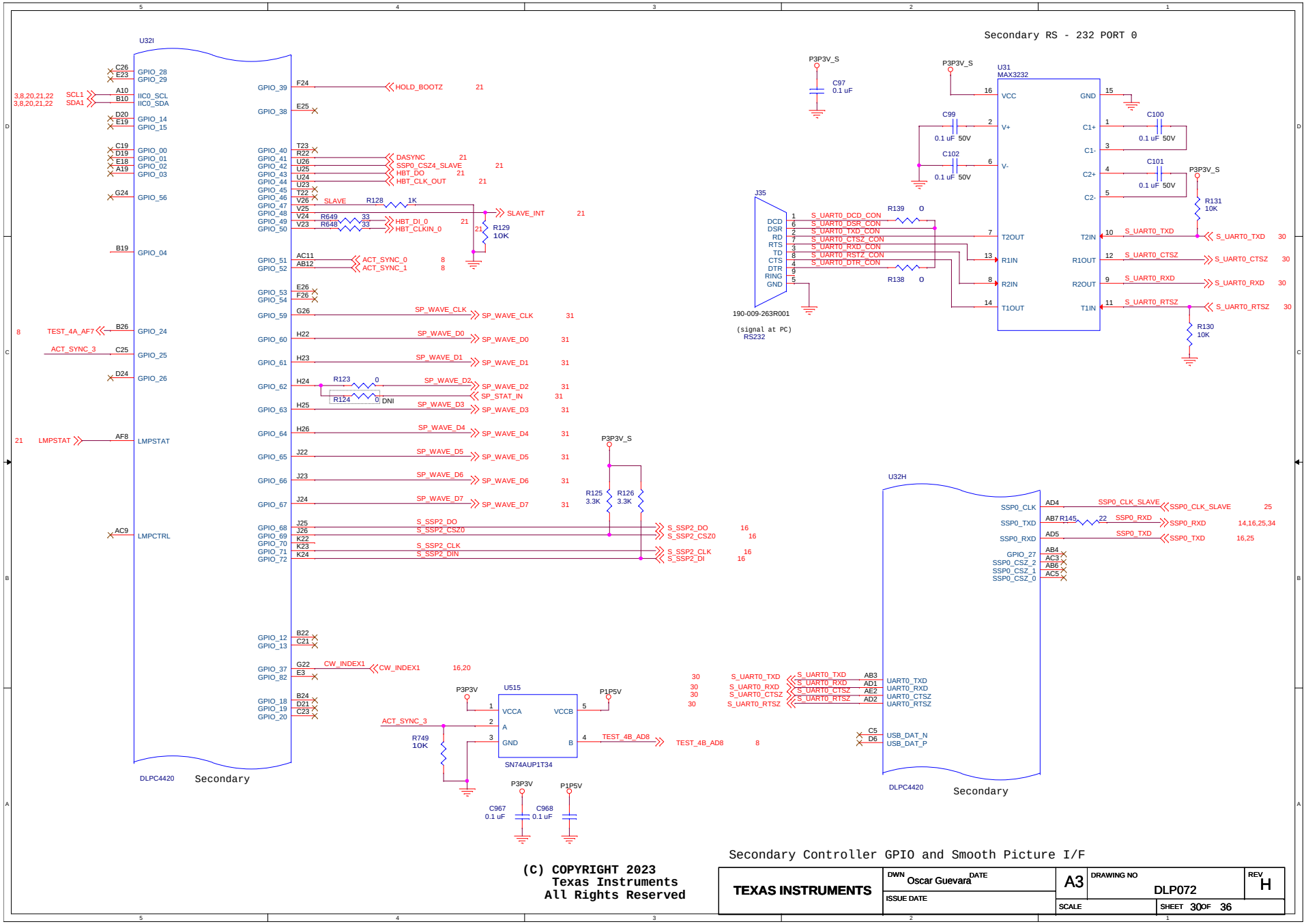
Primary Controller SSI Sensor Interface

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 28 OF 36



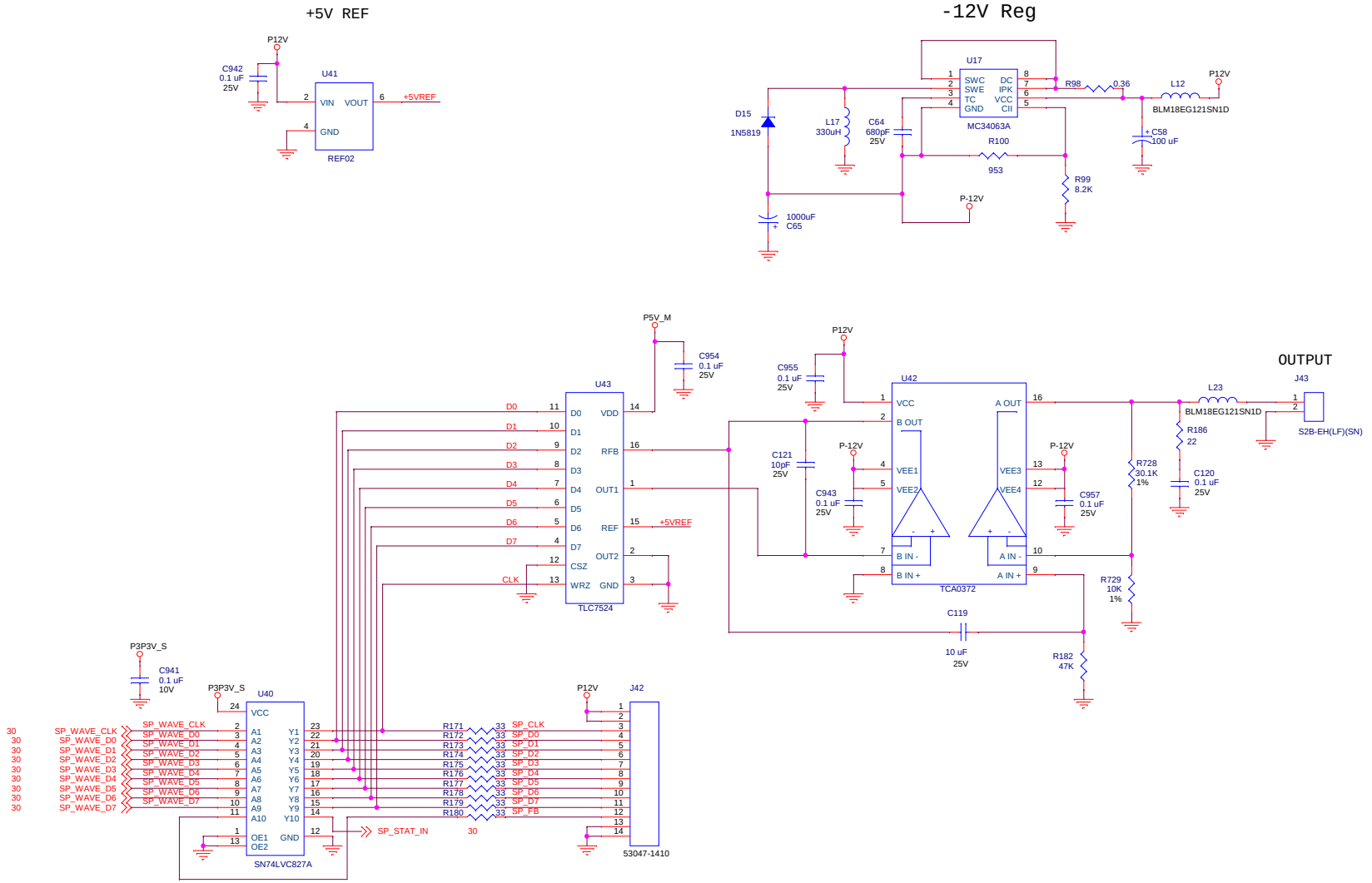
SSI Driver Interfaces

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 29 OF 36



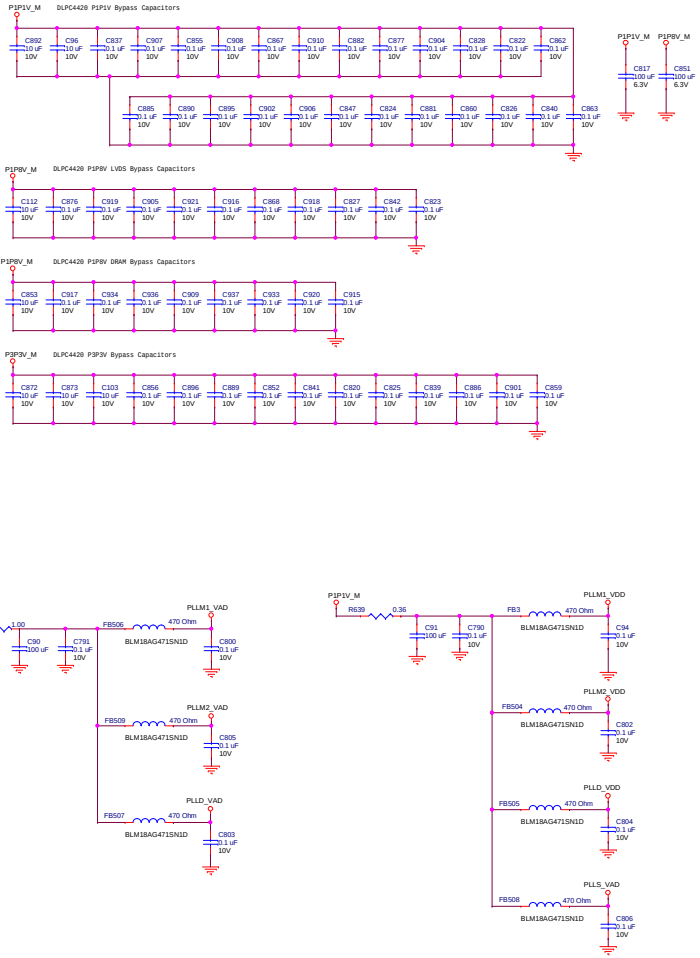
Secondary Controller GPIO and Smooth Picture I/F

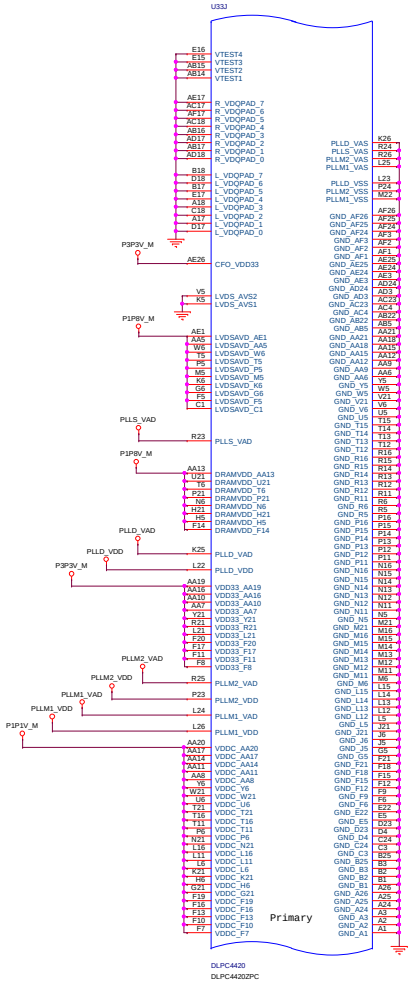
TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072	REV H
	ISSUE DATE		SCALE	SHEET 30 OF 36



Actuator I/F

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A3	DRAWING NO DLP072 REV H
	ISSUE DATE	SCALE	SHEET 31 OF 36





Primary Controller Power and Bypass Capacitors

TEXAS INSTRUMENTS	DWN Oscar Guevara DATE	A2	DRAWING NO DLP072	REV H
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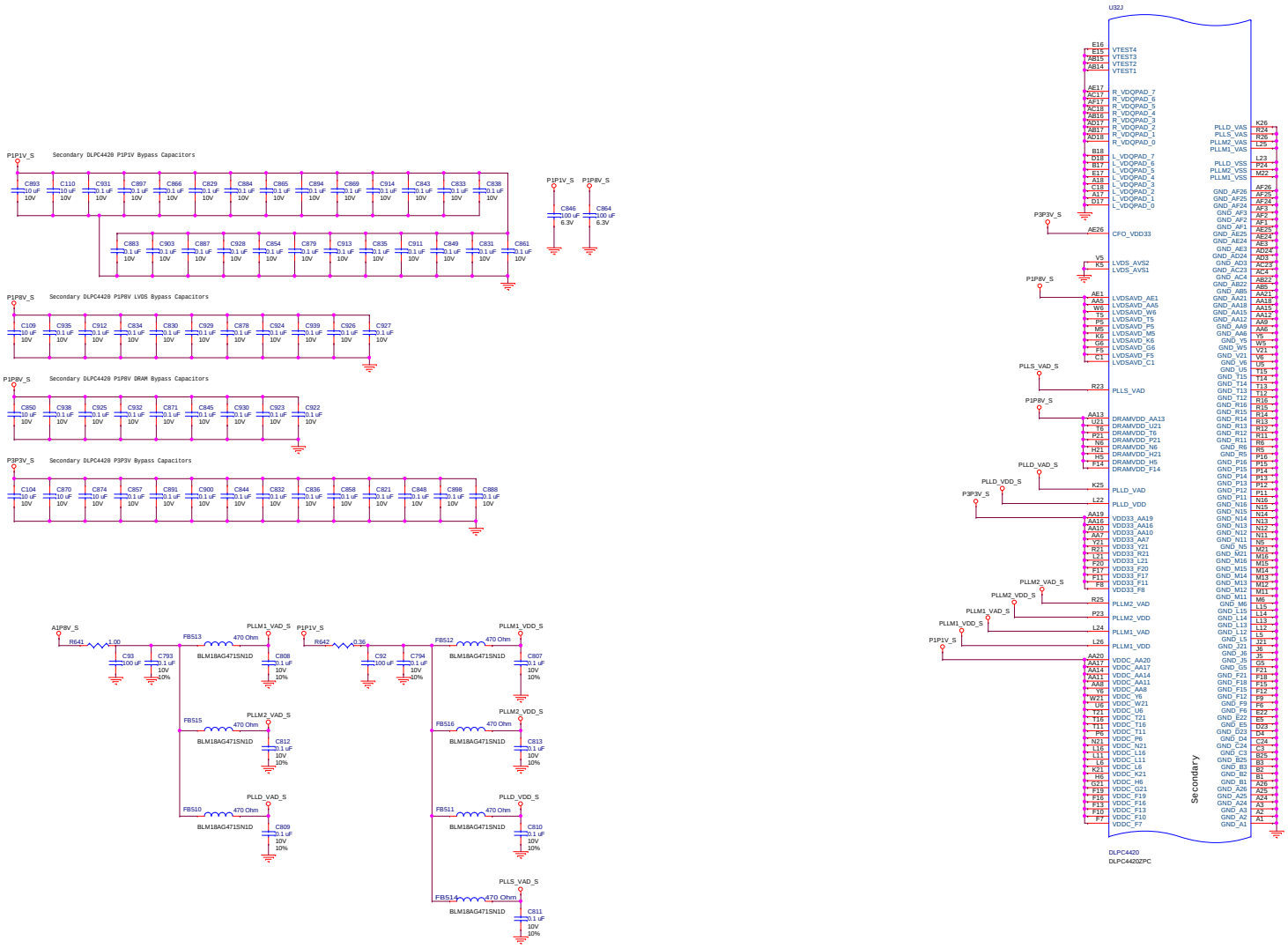
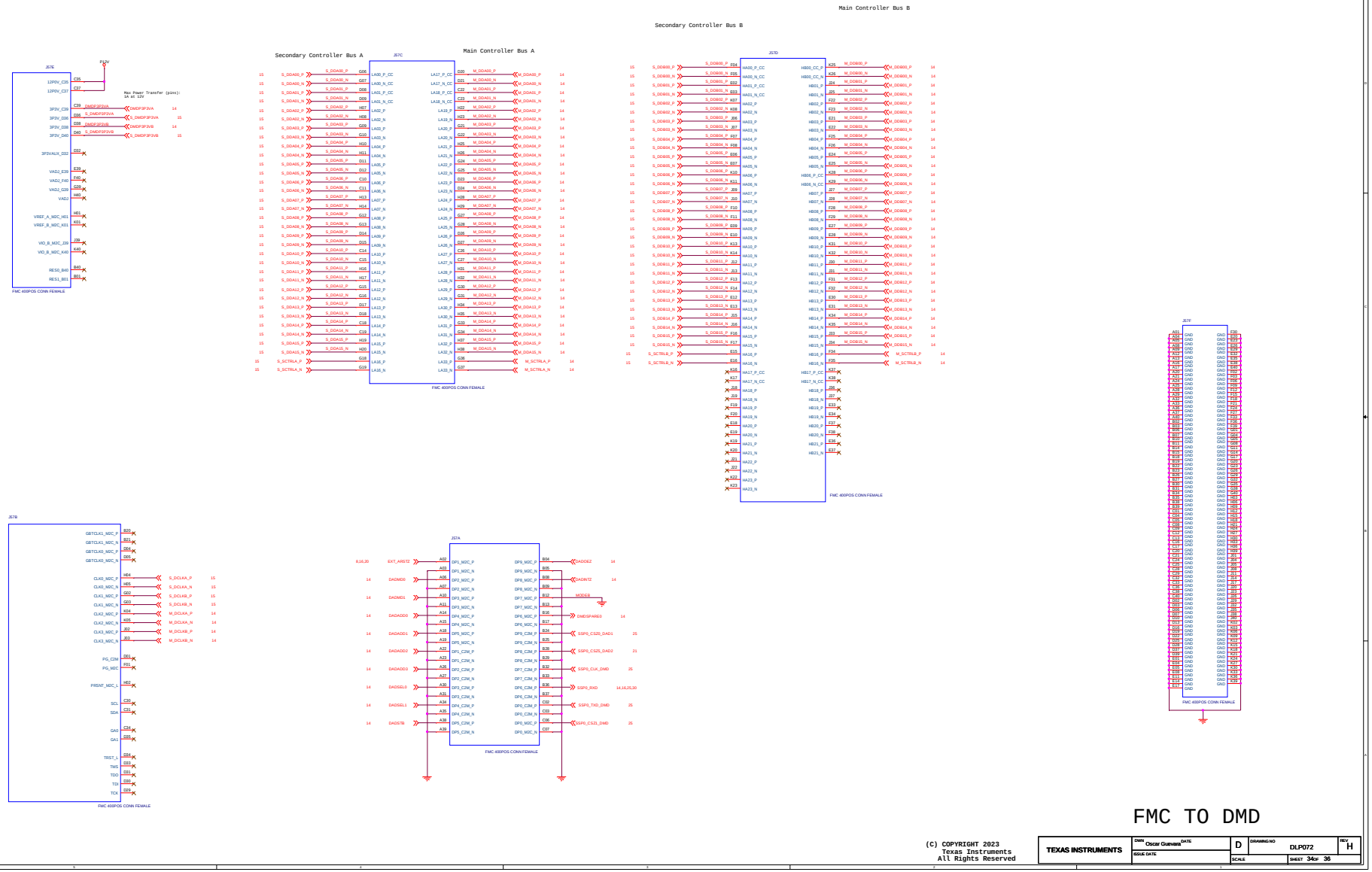


Secondary Controller Power and Bypass Capacitors

TEXAS INSTRUMENTS	DWN Oscar Guevara	DATE	A2	DRAWING NO DLP072	REV H
	ISSUE DATE			SCALE	SHEET 33 OF 36


Secondary Controller Bus A
Main Controller Bus A
Secondary Controller Bus B
Main Controller Bus B
FMC TO DMD
FMC 400POS CONN FEMALE
Max Power Transfer (pins): 1A at 12V
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Revision A:
Initial Release

Revision B:
All Pages: Resequenced reference designators to align with layout
Page 1: Updated notes with correct voltage names
Updated index
Page 4: Rearranged DDR3_1_DQ[15:0] for routability

Revision C:
Page 3: Change U5 to Do Not Install
Updated C545 and C549 as Do Not Install
Changed U506 to 75 Mhz
Page 11: Added Note Connecting pin 15 of U24 to P3P3V
Page 8: Changed R89, R90, R91, R92, and R541 to 0 ohms.

Revision D:
Page 3: Changed net name TEST_4A_AC6 to VX1_3D_EN.
Changed net name TEST_4A_AE6 to VX1_LR_SYNC.
Page 8: Added R190, R191, R192, and R193.
Changed net name TEST_4A_AC6 to VX1_3D_EN.
Changed net name TEST_4A_AE6 to VX1_LR_SYNC.
Page 11: Connected pin 15 of U24 to P3P3V.
Page 16: Changed C799 and C801 to 1800pF.
Page 21: Added note to ballast circuit.
Page 22: Added R188 and R189.
Page 23: Changed RN501 to Install, added J52 header.
Page 24: Changed RN500 to Install, added J53 header.

Revision E:
Page 11: Changed U24-10, C85 connection from P3P3V to P5V_S.

Revision F:
Page 3: Added U514, Y1, R745, R746, R747, C966
Page 3: Removed FB502, C534, U506
Page 8: Added J54, J55, and J56
Page 22: Added R748 and connection to GPIO_34

Revision G:
Page 8: Added Off-Page connections to TEST_4A_AF7 and TEST_4B_AD8.
Page 30: Added TEST_4A_AF7 connection to GPIO_24 on U32

Revision H:
Page 3: Updated FE_12V to RE_5V
Removed nets: "USB+5V", "USB_D+", USB_D-"
Added I2C nets "SCL1", "SDA1"
Rearraged nets "VX1_LR_SYNC", "FE_RST", "SDA0", "I2C_BUSY"
Page 14: Removed J51
Page 15: Removed J50
Page 34: Added J57 FMC Connector

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