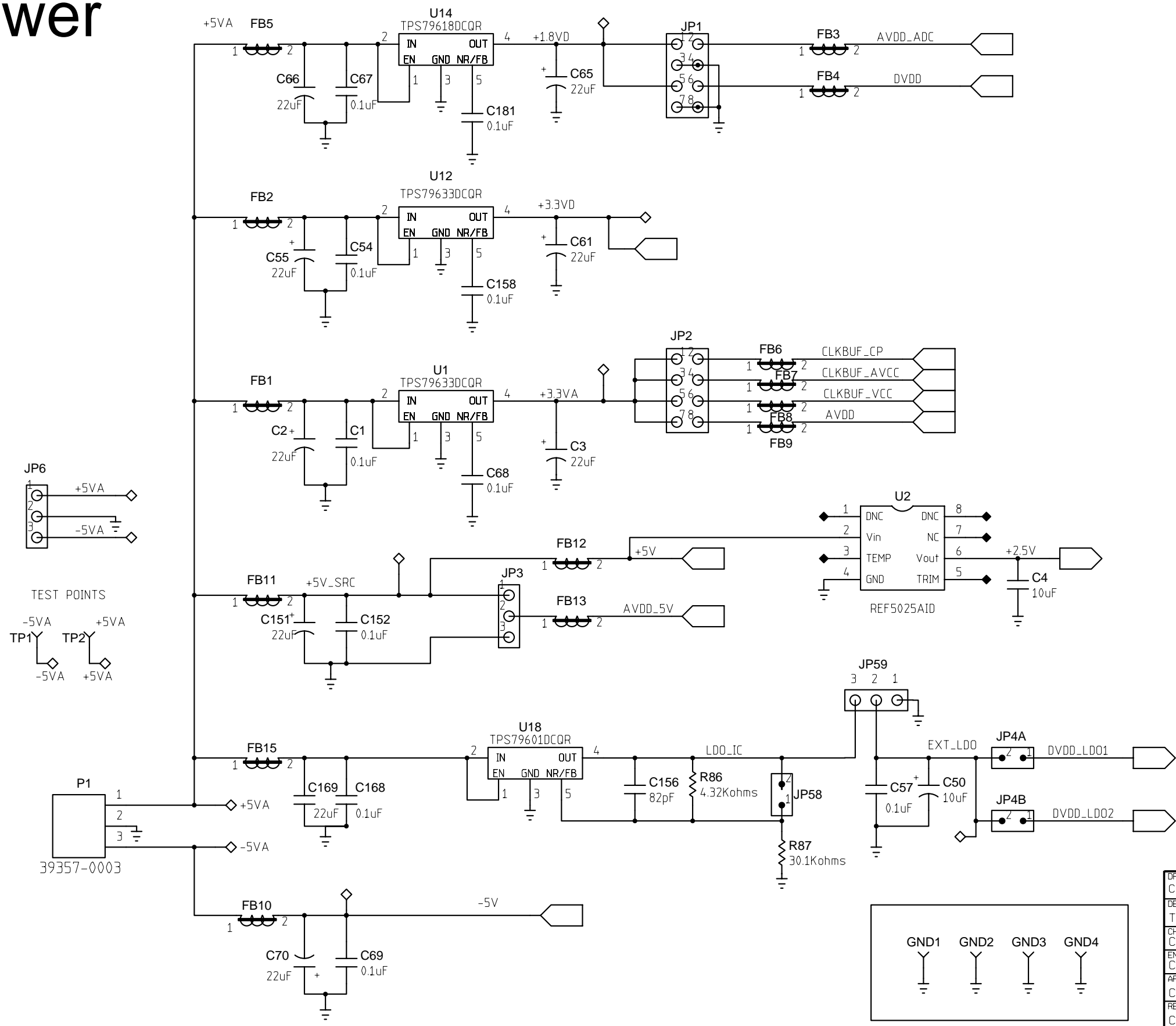
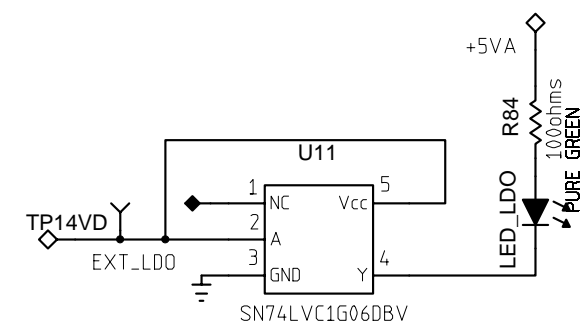
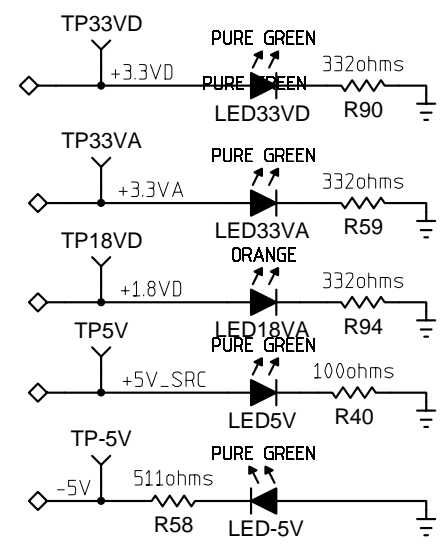



# Power



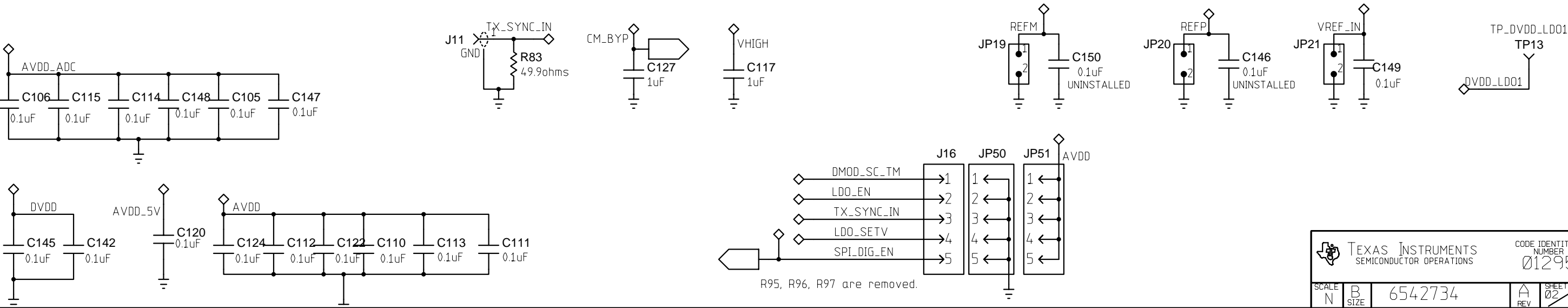
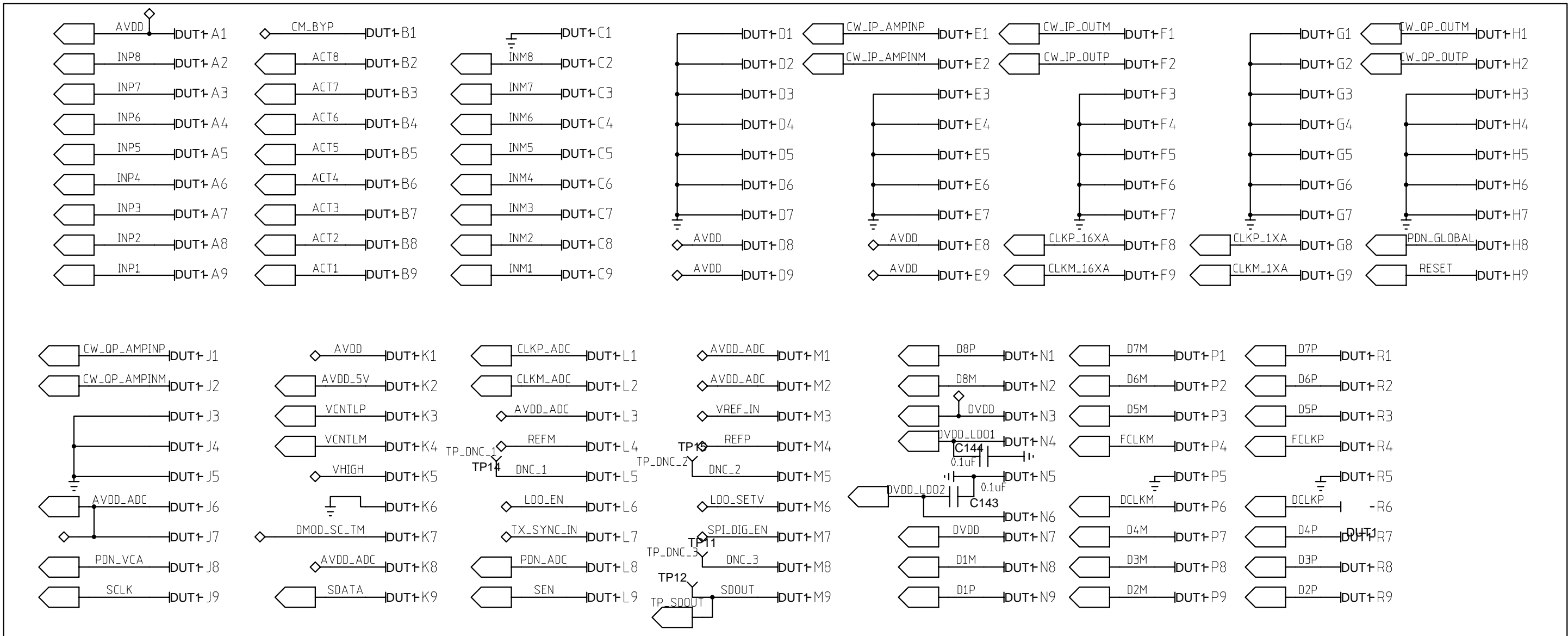
REV	REVISIONS
A	ECR XXXXXXXX10/04/2012, MPK



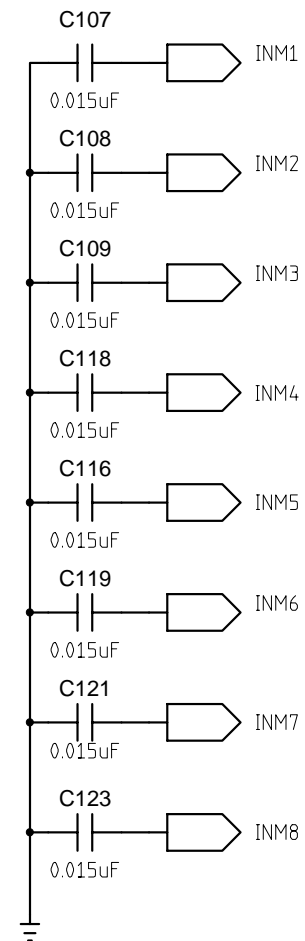
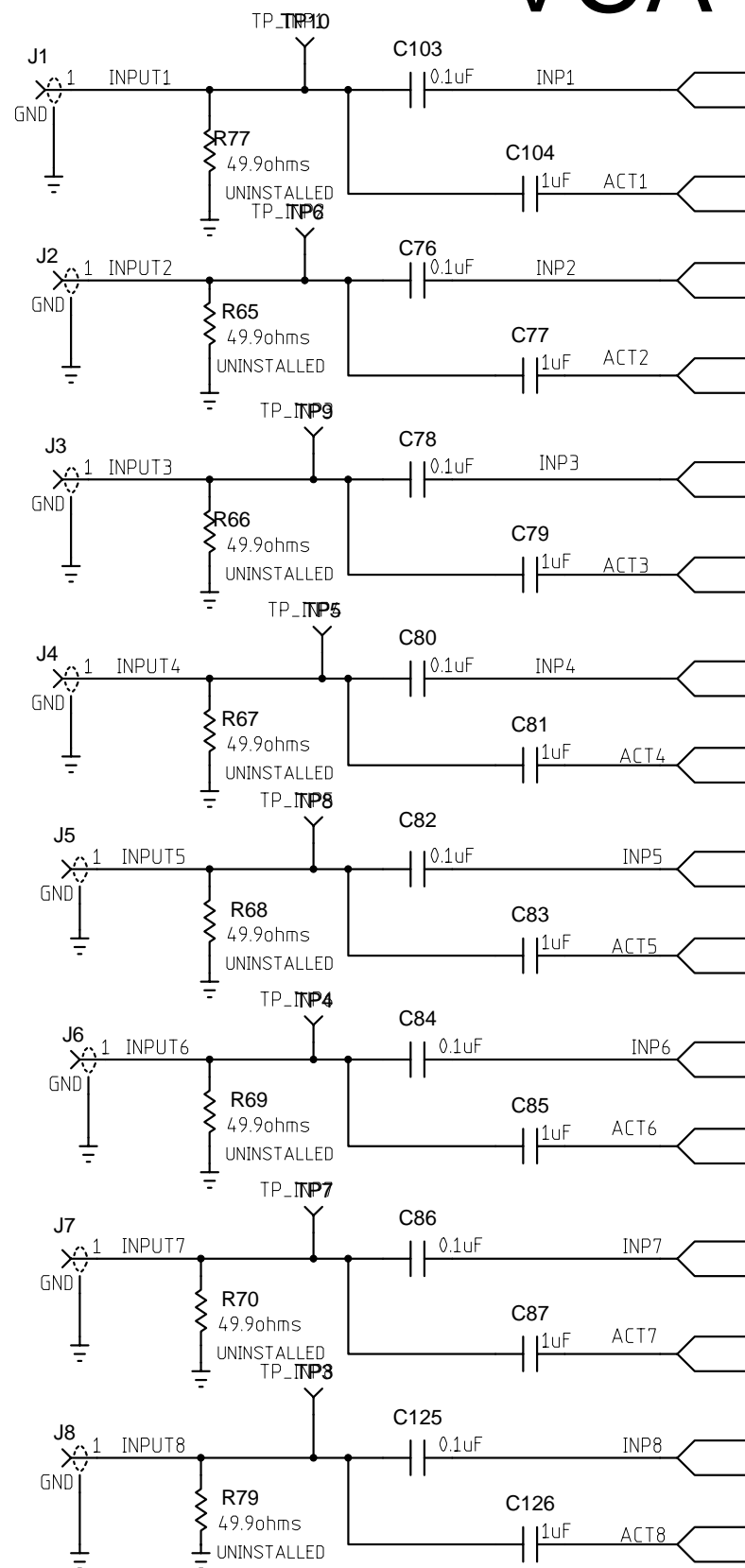
## Power Supply

DRAFTSMAN: C. Smyth	DATE 10/04/2012	 TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS	CODE IDENTITY NUMBER 01295			
DESIGNER: T. Reinert	DATE 10/04/2012		TITLE: SCHEMATIC, AFE5809 EVM			
CHECKER: C. Smyth	DATE 10/04/2012					
ENGINEER: C. Smyth	DATE 10/04/2012					
APPROVED: C. Smyth	DATE 10/04/2012					
RELEASED: C. Smyth	DATE 10/04/2012	SCALE N	B SIZE	6542734	A REV	SHEET 01 11

# AFE5807/08 DEVICE

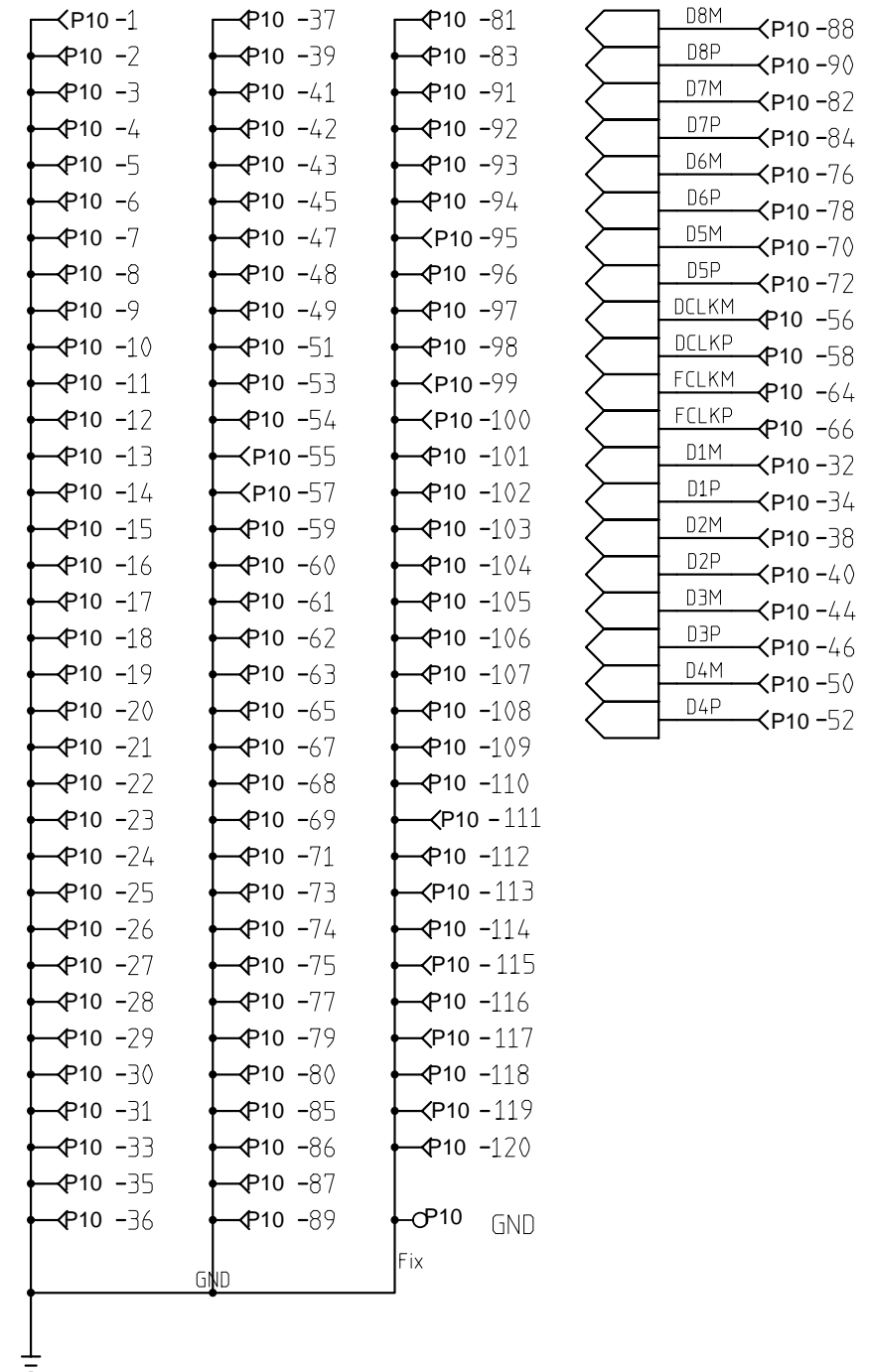


# VCA INPUT

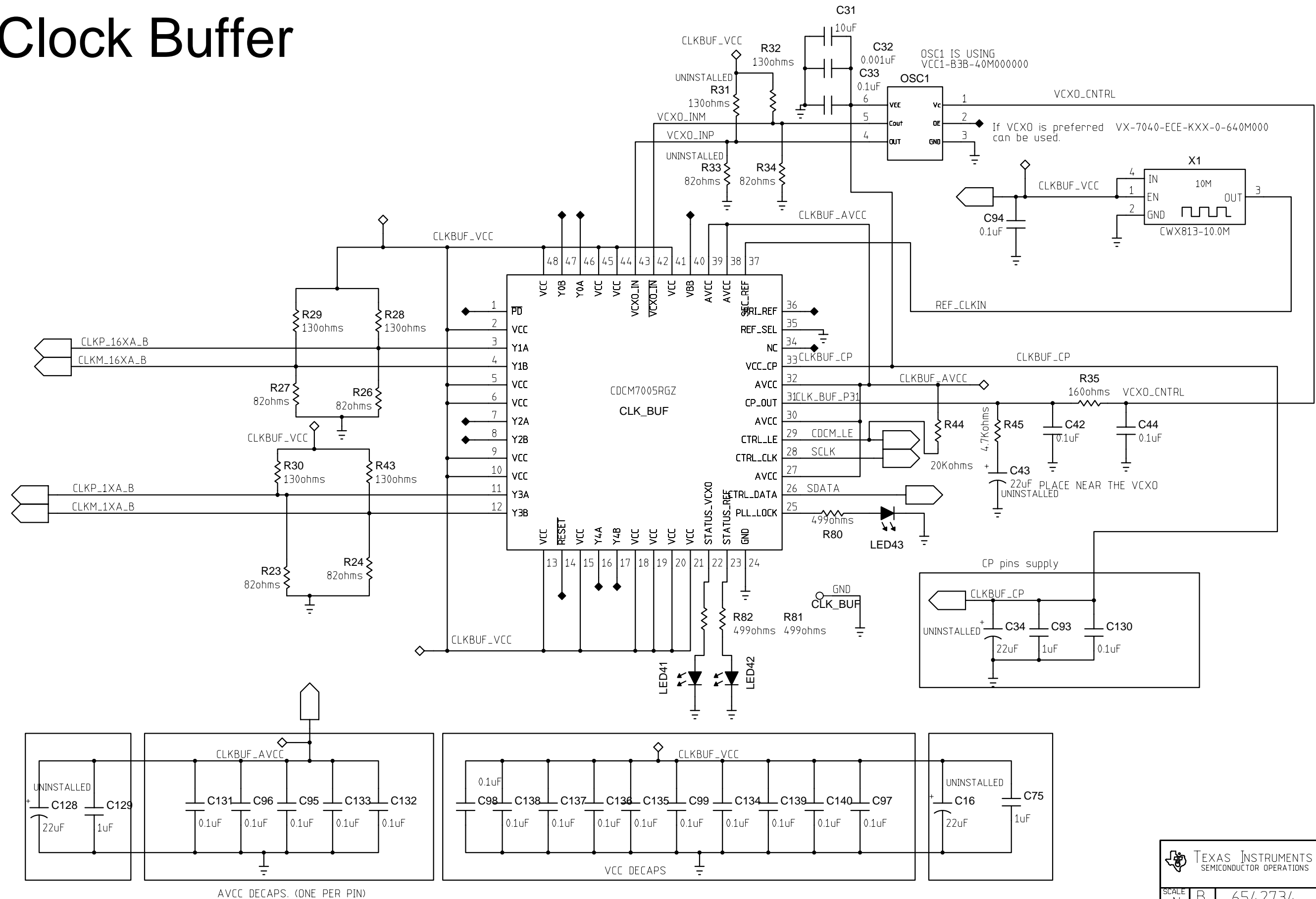


Priority of Close to Pins INPx  
C22-C29 1st  
C30-C37 2nd

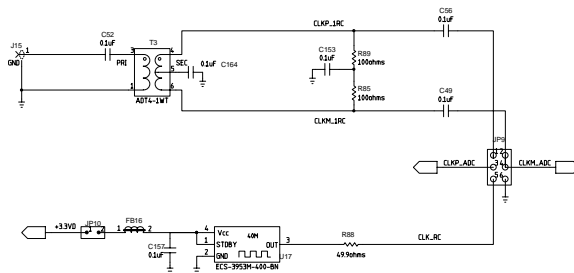
# ADC OUTPUT



# Clock Buffer

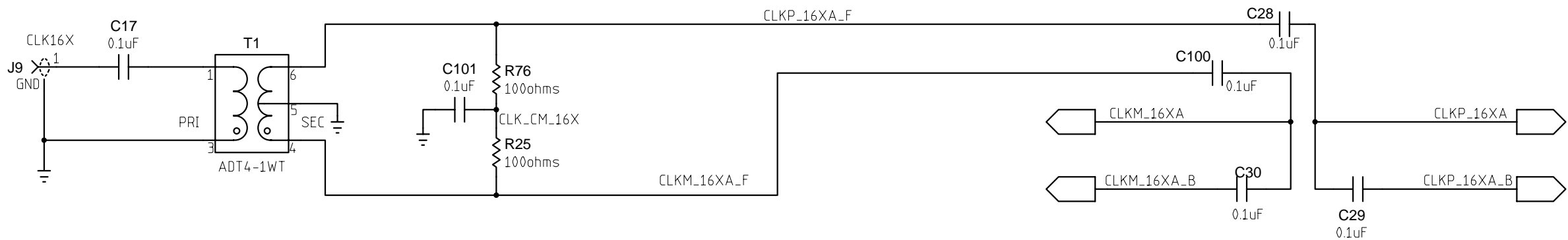


# ADC CLOCK

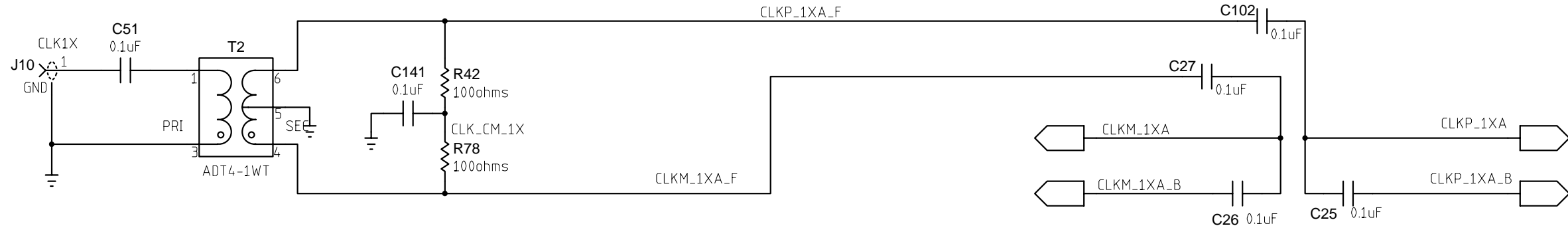


# CW CLK

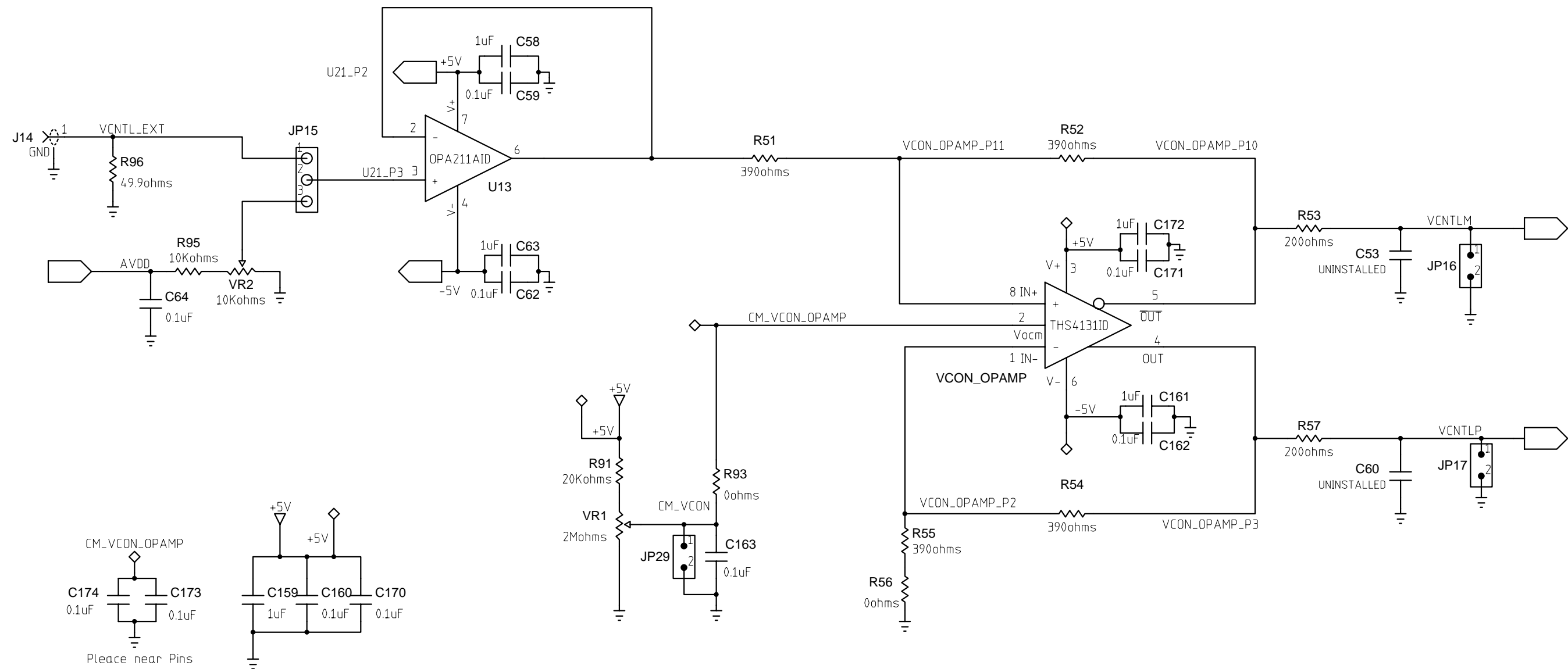
16X



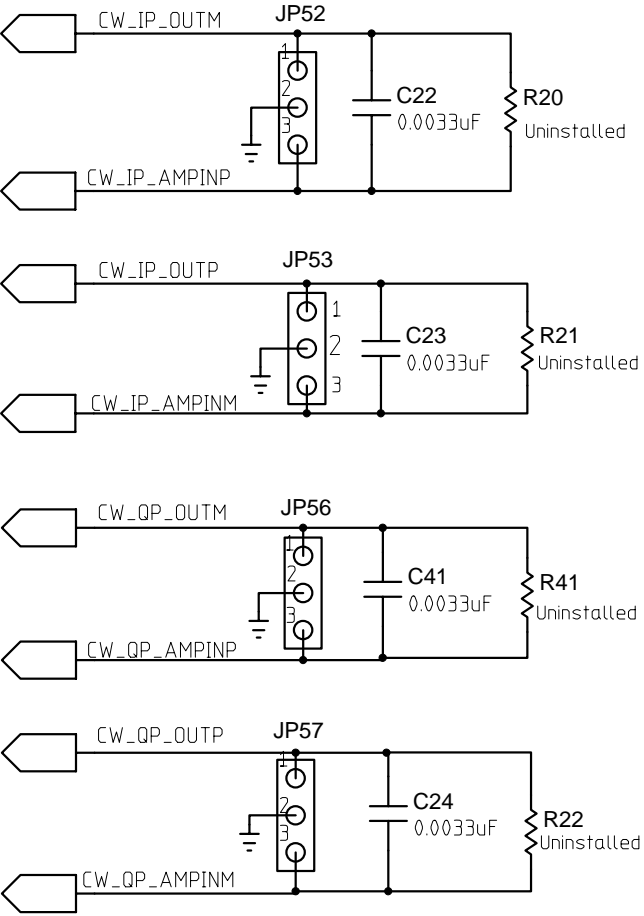
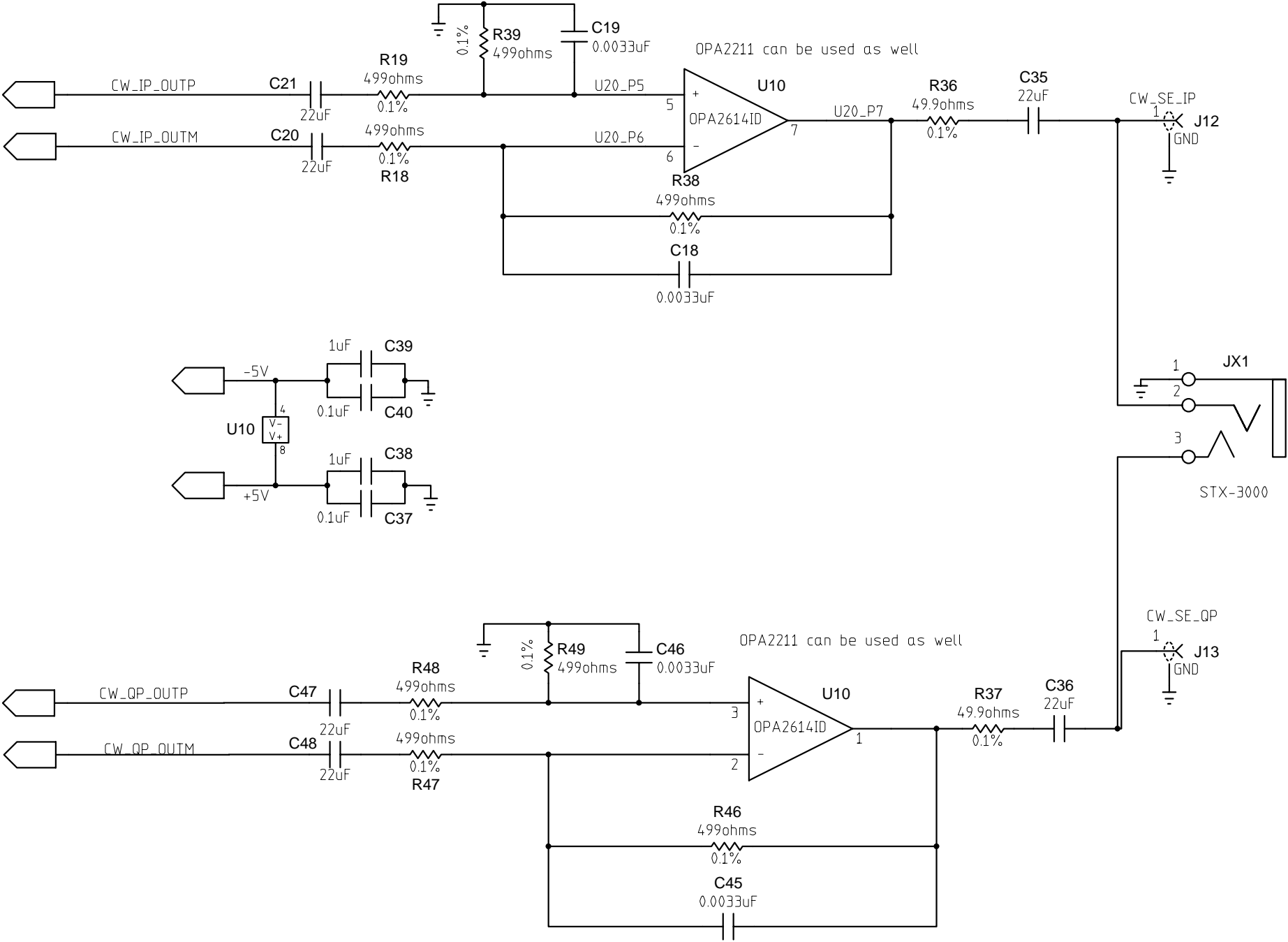
1X



# VCON SINGLE TO DIFFERENTIAL CONVERTER



# CW Mixer Out

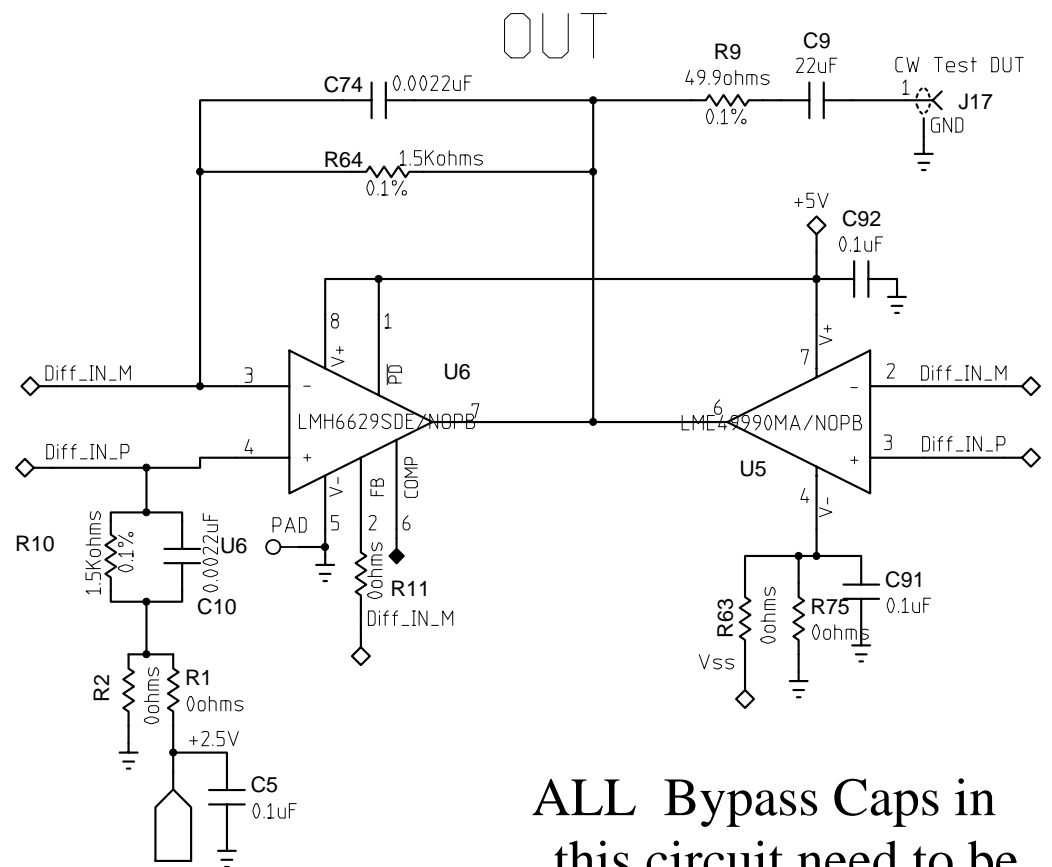
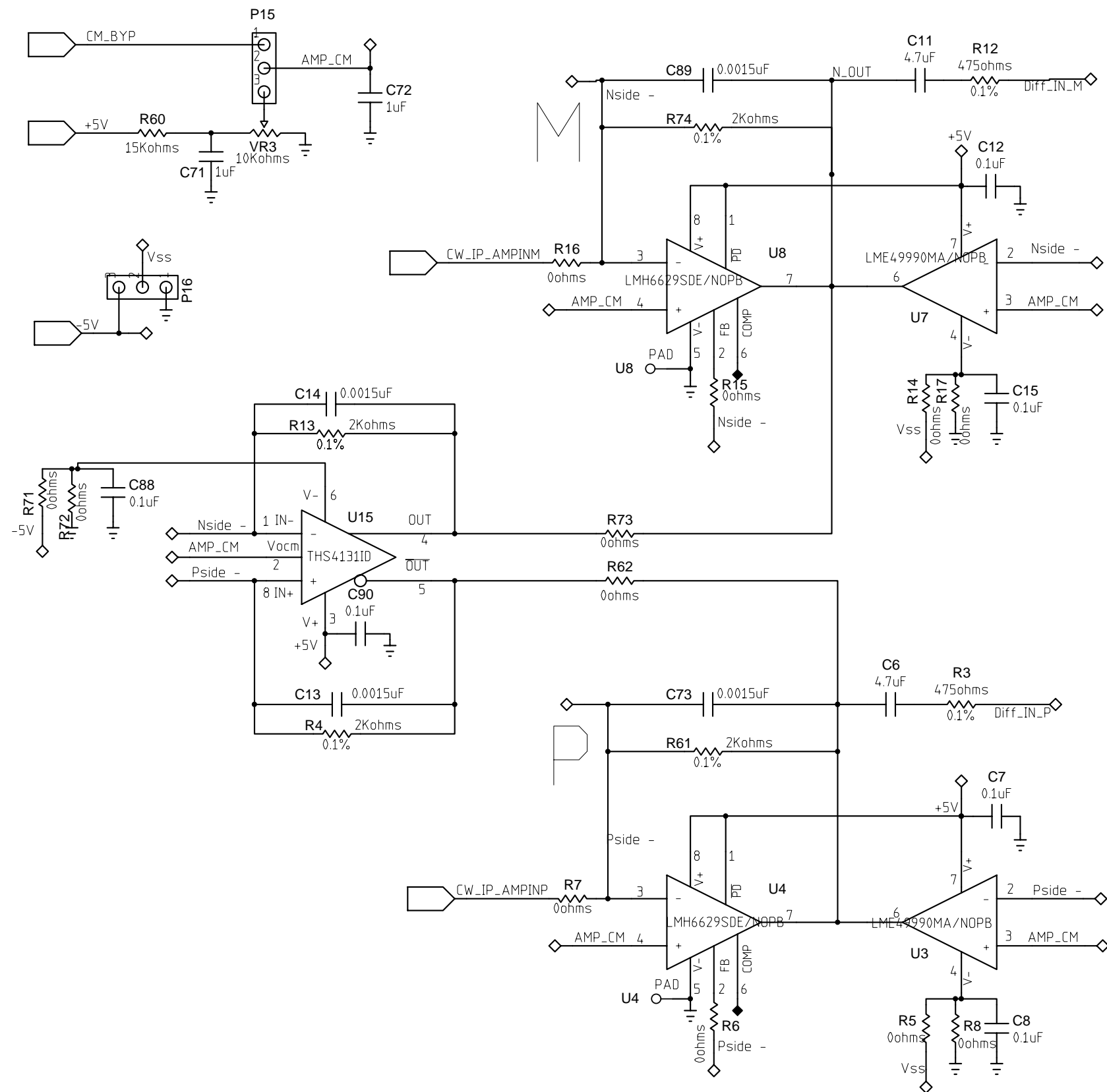




There are two ground planes here. We isolate the USB circuit from the rest of the board. The circuits are only coupled through the opto-isolators.



# CW Low Noise I/V Amp



ALL Bypass Caps in  
this circuit need to be  
tied close to the pin.

This Circuit provides 3  
options for populating  
Op-Amps for maximum flexibility

✱ Important

Make sure all the information is filled before releasing the schematic to Layout

- xx —————> Fill up by clicking on the text
- ☐ —————> Unselected
- ☒ —————> Selected ( Copy and paste this box on the item that has to be selected)
- P1

—————> For placement instruction .Place this note box number wherever it applies (Note description can be changed)
- R1

—————> For Routing instruction .Place this note box number wherever it applies (Note description can be changed)
- C1

—————> For current rating instruction .Place this note box number wherever it applies (Note description can be changed)

Board Specs

Cycle Time	xx	Controlled Impedence	<input checked="" type="checkbox"/>	
Number Of Layers	6	Impedance In Ohms	50	
Plating	HARD GOLD	<input type="checkbox"/>	BGA via Holes to be Filled with epoxy	<input type="checkbox"/>
	SOFT GOLD	<input checked="" type="checkbox"/>		
	HAL	<input type="checkbox"/>		

Thermal Keepout

Thermo Stream	<input type="checkbox"/>	Handler Mounting holes	<input type="checkbox"/>
Onley Peltier	<input type="checkbox"/>	Support Mounting holes	<input type="checkbox"/>
Both	<input type="checkbox"/>		

Critical Layout Instructions

Critical Layout Instructions can be enterd inside this box

☐

Net Classes and clearences specified for GND, PWR, LVDS, CMOS, etc. Use Refrence layout from Edge No XXXX

Otherwise stated, minimal trace width and trace clearance are 7 mil. Default trace width is based on 50ohm traces

R1

Planes with mutiple vias from Layer xx

R2

Thick trace width = xx

R3

LVDS pairs to have length matched max = xx

R4

Route all these traces on Layer xx

R5

Differential pair routing

R6

Routing needs to be symmetrical

R7

High instaneous current net

R8

xxxxxx-----

R9

xxxxxx-----

Current Rating for Critical Nets/Traces

Critical Voltage/Current Rating can be enterd inside this box

☐

Net Classes and clearences specified for HV, PWR etc. Use Refrence layout for Routing Edge No XXXX

Otherwise stated, net current is less than 200mA

C1

Low voltage current below 250mA

C2

Low voltage current below 500mA

C3

Low voltage current is up to 2A

C4

High voltage current up to 100mA instaneously, average current is below 10mA

C5

High voltage current up to 2A instaneously, average current is 50mA

C6

xxxxxx-----

C7

xxxxxx-----

C8

xxxxxx-----

C9

xxxxxx-----

Component Placement

Critical Placement Instructions can be enterd inside this box

Use Refrence layout for placement Board Edge Number xxxxx

Otherwise stated, placement follows Sch drawing locations

P1

Placement close to IC or DUT- Page 10 Caps.

P2

Placement close to socket

P3

Placement needs to be symmetrical

P4

xxxxxx-----

P5

xxxxxx-----

P6

xxxxxx-----

P7

xxxxxx-----

P8

xxxxxx-----

P8

xxxxxx-----

FAB VENDOR

TI - FAB vendor---xxxx

DFM is Provided Yes ☐

Design For Manufacture No ☐

We will select the FAB vendor ☐

MBU Ultrasound EVM SEED

Designer:Xiaochen Xu

Revision: A

Date 09/08/2012