

Layer Stack Up Detail for: TIDA-00496_F0.PcbDoc			
Layer Name	Layer Description	Copper Thickness	Dielectric Material
Top Solder Mask	<.6TS>		Solder Resist
Top Layer	<.6TL>	1.4mil	FR-408
L2_P1	<.6B1>	1.4mil	FR-408
L3_P2	<.6B2>	1.4mil	FR-408
Bottom Layer	<.6BL>	1.4mil	FR-408
Bottom Solder Mask	<.6BS>		Solder Resist

DESIGN INFORMATION

BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)  
2535.00mil X 3346.46mil

Number of Layers : 4  
MIN. TRACK WIDTH: 7 MIL  
MIN. CLEARANCE: 7.8 MIL  
MIN. VIA PAD SIZE: 26 MIL

MINIMUM ANNULAR RING 0.177mm (7MIL) EXTERNAL  
PER IPC-D-275 CLASS 2 LEVEL C  
REGISTRATION TOLERANCES: METAL +/- .5 MIL, HOLES +/- .3 MIL  
IT IS IMPEDANCE CONTROLLED BOARD

MATERIAL:  
☒ FR-408 ☐ FR-4 High Tg ☐ OTHER \_\_\_\_\_  
THICKNESS: ☒ 63 MIL (1.6mm) +/-10% ☐ OTHER \_\_\_\_\_  
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2  
☐ OTHER +/- \_\_\_\_\_  
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2  
☐ OTHER +/- \_\_\_\_\_  
COPPER THICKNESS (FINISHED):  
OUTER: ☒ 1.4MIL (1oz) ☐ 2MIL (1.4oz) ☐ 2.8MIL (2oz)  
INNER SIGNAL: ☒ 1.4MIL (1oz) ☐ 2.8MIL (2oz) ☐ N/A  
DRILLING:  
REFERENCE: ☒ AS SHOWN ☒ NC\_DRILL FILES  
PTH MIN COPPER THICKNESS: ☒ 1MIL ☐ OTHER \_\_\_\_\_  
BOARD FINISH:  
SILKSCREEN: ☒ TOP ☒ BOTTOM  
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER \_\_\_\_\_  
SOLDER RESIST COLOR:  
☒ GREEN ☐ BLUE ☐ OTHER \_\_\_\_\_  
SURFACE FINISH: ☒ IMMERSION GOLD (ENG) ☐ ENERPIG  
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER \_\_\_\_\_  
ARRAY/PANEL: ☐ CUT AND TRIM PER MECH LAYER 1  
☐ N.C. ROUTE ☒ V. SCORE  
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs  
TO MEET OR EXCEED THE REQUIREMENTS OF:  
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3  
☒ UL 94V-0 ☒ RoHS ☐ OTHER PER ORDER  
ADDITIONAL REQUIREMENTS:  
MICROSECTION: ☐ YES VIA TENTING: ☐ NONE ☒ REQUIRED  
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER  
MANUFACTURER'S UL: ☐ RAIL ☐ METAL ☒ SILK



PROJECT TITLE:  
IEEE1588 ethernet Brick\_Fiber

DESIGNED FOR:  
Public Release

FILE NAME:  
TIDA-00496\_F0.PcbDoc

ENGINEER:  
Srinivas Kalikuppa

LAYOUT BY:  
Avinash N

SCALE: 1:00

ALTUM DESIGNER VERSION:  
14.3.14.34663

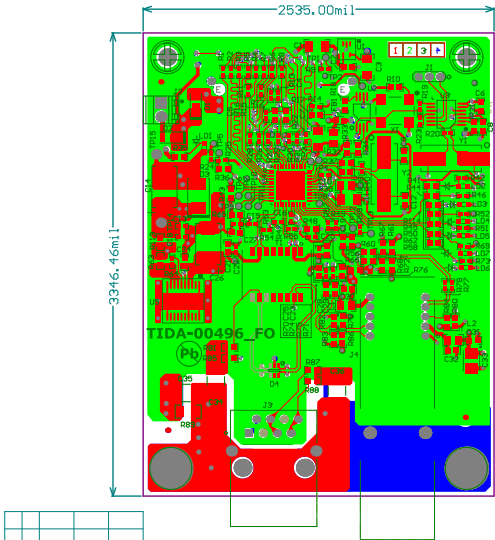
IMPEDANCE TABLE

LAYER	TRACE WIDTH	SPACING	IMPEDANCE	REFERENCE LAYER
TOP	7 MIL	16 MIL	100 OHM +/-10%	L2_P1
BOTTOM	7 MIL	16 MIL	100 OHM +/-10%	L3_P2

Symbol	Ht Count	Tool Size	Plated	Hole Type
B	107	12mil (0.305mm)	PTH	Round
A	96	16mil (0.406mm)	PTH	Round
C	49	20mil (0.508mm)	PTH	Round
H	10	97.89mil (0.81mm)	PTH	Round
G	3	32mil (0.813mm)	PTH	Round
D	2	33mil (0.838mm)	PTH	Round
F	8	35.039mil (0.89mm)	PTH	Round
I	2	40mil (1.016mm)	PTH	Round
M	2	44mil (1.118mm)	PTH	Round
K	2	55.118mil (1.4mm)	PTH	Round
E	2	57.087mil (1.45mm)	PTH	Round
J	2	62.205mil (1.58mm)	PTH	Round
O	2	125.984mil (3.2mm)	PTH	Round
L	2	127.953mil (3.25mm)	PTH	Round
	2	128mil (3.251mm)	PTH	Round
291 Total				

Drill Table

DRILL TOLERANCES:  
FOR PTH : +/-3MILS  
FOR NPTH : +/-2MILS  
FOR 12MIL DRILL VIA : +/-12MILS  
FOR 16MIL DRILL VIA : +/-16MILS



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00496_F0	REV: E1	SUN REV: Not In VersionControl	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME = <b>Top Layer</b>				
PLOT NAME = Multilayer Composite Print	GENERATED : 9/23/2015 2:39:00 PM	TEXAS INSTRUMENTS		