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IMPEDANCE TABLE

LAYER	TRACE WIDTH	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP	6 MILS	99 OHM	LAYER-2
Layer-3	4 MILS	99 OHM	LAYER-4
Layer-6	4.5 MILS	99 OHM	LAYER-4
Layer-8	4.5 MILS	99 OHM	LAYER-7
Layer-9	4 MILS	99 OHM	LAYER-6
Bottom	6 MILS	99 OHM	LAYER-6

2.76 (in)

5.30 (in)

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP	4.50 MILS	6.01 MILS	99 OHM	LAYER-2
BOTTOM	4.50 MILS	6.01 MILS	99 OHM	LAYER-6

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP	6.01 MILS	9.50 MILS	100 OHM	LAYER-2
Layer-3	4.01 MILS	11.50 MILS	100 OHM	LAYER-4

Notes :

All vias are landed on both the sides except thermal vias

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Routed Path Length	Hole Length
□	4	170.00mil (4.318mm)	NPTH	Round	Top Layer - Bottom Layer	-	-
○	2	125.20mil (3.180mm)	NPTH	Round	Top Layer - Bottom Layer	-	-
⊕	2	118.11mil (3.000mm)	NPTH	Round	Top Layer - Bottom Layer	-	-
✕	6	118.11mil (3.000mm)	PTH	Round	Top Layer - Bottom Layer	-	-
✳	1	80.00mil (2.032mm)	PTH	Round	Top Layer - Bottom Layer	-	-
◇	6	47.24mil (1.200mm)	PTH	Round	Top Layer - Bottom Layer	-	-
⊗	4	40.16mil (1.020mm)	NPTH	Round	Top Layer - Bottom Layer	-	-
▽	28	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer	-	-
⊞	4	40.00mil (1.016mm)	NPTH	Round	Top Layer - Bottom Layer	-	-
✳	55	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	-	-
⊕	4	33.47mil (0.850mm)	PTH	Round	Top Layer - Bottom Layer	-	-
⊕	1123	12.20mil (0.310mm)	PTH	Round	Top Layer - Bottom Layer	-	-
✕	27	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	-	-
✕	4	23.62mil (0.600mm)	PTH	Slot	Top Layer - Bottom Layer	27.56mil (0.700mm)	51.18mil (1.300mm)
▽	2	39.37mil (1.000mm)	PTH	Rectangle	Top Layer - Bottom Layer	118.11mil (3.000mm)	118.11mil (3.000mm)
⊕	1	39.37mil (1.000mm)	PTH	Rectangle	Top Layer - Bottom Layer	137.80mil (3.500mm)	137.80mil (3.500mm)
	1273 Total						

Slot definitions :

Routed Path Length = Calculated from tool start centre position to tool end centre position.

Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.80mil	1	
3	Top Layer	Copper	1.80mil		
4	Dielectric1	FR-4	3.87mil	4.02	
5	L2-GND	Copper	1.20mil		
6	Dielectric 2	FR-4	4.00mil	4.26	
7	L3-SIG1	Copper	1.20mil		
8	Dielectric 3	FR-4	8.70mil	4.06	
9	L4-GND	Copper	1.20mil		
10	Dielectric 4	FR-4	4.00mil	4.26	
11	L5-PWR/SIG	Copper	1.20mil		
12	Dielectric 5	FR-4	13.51mil	4.06	
13	L6-SIG2	Copper	1.20mil		
14	Dielectric 6	FR-4	4.00mil	4.26	
15	L7-PWR2	Copper	1.20mil		
16	Dielectric 7	FR-4	8.42mil	4.06	
17	L8-SIG3	Copper	1.20mil		
18	Dielectric 8	FR-4	4.00mil	4.26	
19	L9-GND	Copper	1.20mil		
20	Dielectric 9	FR-4	3.87mil	4.02	
21	Bottom Layer	Copper	1.80mil		
22	Bottom Solder	Solder Resist	0.80mil	1	
23	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL

MIN. CLEARANCE: 4 MIL

MIN. VIA PAD SIZE: 15.78MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

☐ FR-408 ☐ FR-4 High Tg ☒ OTHER FR-4

THICKNESS: ☐ 62 MIL (1.6mm) +/-10% ☒ OTHER 69.17MILS +/-10%

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2

☐ OTHER +/-

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2

☐ OTHER +/-

DRILLING:

REFERENCE: ☒ AS SHOWN ☒ NC\_DRILL FILES

PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:

SILKSCREEN: ☒ TOP ☒ BOTTOM

SILKSCREEN COLOR: ☒ WHITE ☐ OTHER

SOLDER RESIST COLOR: ☐ GREEN ☒ OTHER RED

☐ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG

☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER

ARRAY/PANEL: ☐ CUT AND TRM PER M1 BOARD OUTLINE

☐ N.C. ROUTE ☐ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3

☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: ☐ YES

BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WDE, XX MIL SPACE

TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: MMWAUEICBOOST

DESIGNED FOR: Public Release

FILE NAME: PROC074B-PCB.PcbDoc

ENGINEER: Chethan Kumar Y.B

LAYOUT BY: TESSOLUE

ALTIM DESIGNER VERSION: 17.1.9.592

SCALE: 1.00

ALL ARTWORK VIEWED FROM TOP SIDE

BOARD #: PROC074

REV: B

SUN REV: Not In VersionControl

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LAYER NAME = Drill Drawing

TID #: N/A

PLOT NAME = PROC074B.GDI

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TEXAS INSTRUMENTS

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