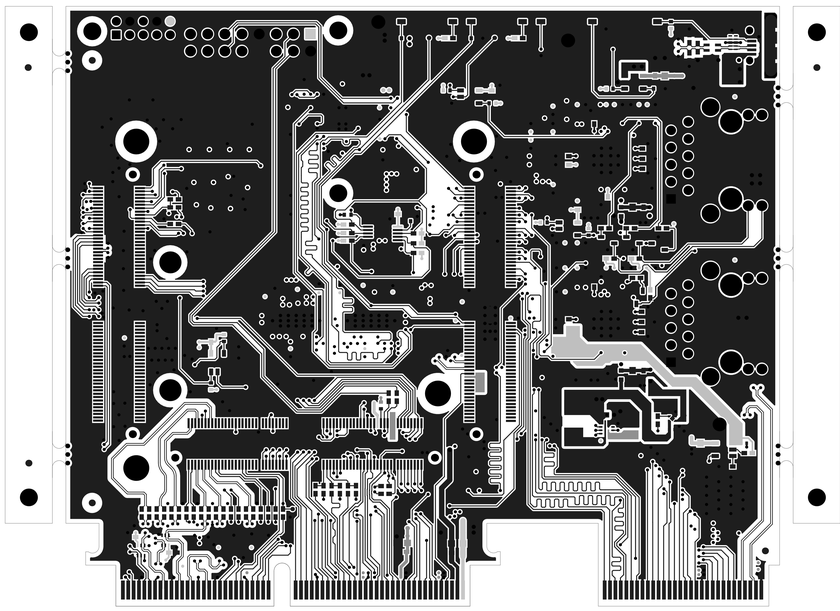

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465	
LAYER NAME = Top Layer	TID #:			
PLOT NAME = Top Layer	GENERATED : 01/10/2024 12:24:07			TEXAS INSTRUMENTS

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TEXAS INSTRUMENTS

PROJECT TITLE: AM261 HSEC Adapter Board

DESIGNED FOR: Public Release

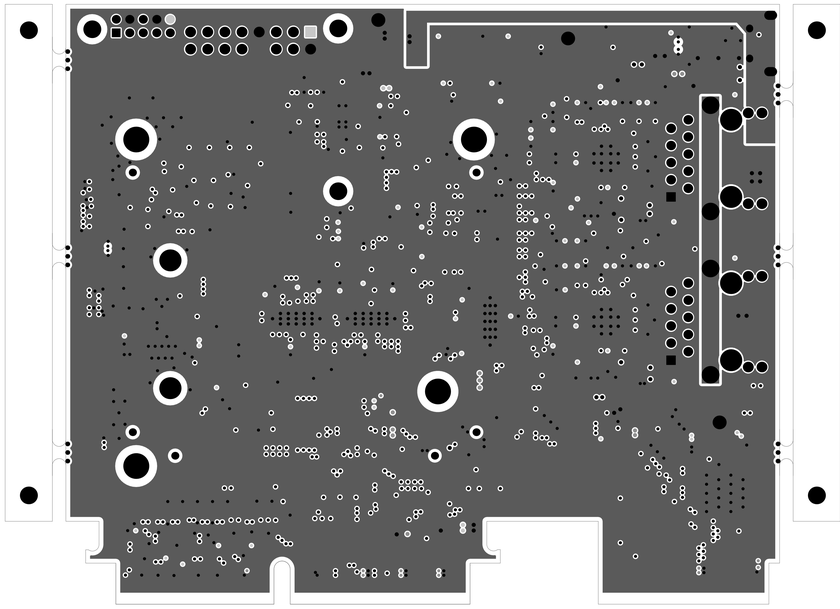
FILE NAME: PROC200E1.PcbDoc

ENGINEER:

LAYOUT BY: .PCB_Layout

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.0.1.36



PROJECT TITLE:
AM261 HSEC Adapter Board

DESIGNED FOR:
Public Release

FILE NAME:
PROC200E1.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465
LAYER NAME = M9 Title Sheet	TID #:		
PLOT NAME = GND1	GENERATED : 01/10/2024 12:24:07		TEXAS INSTRUMENTS

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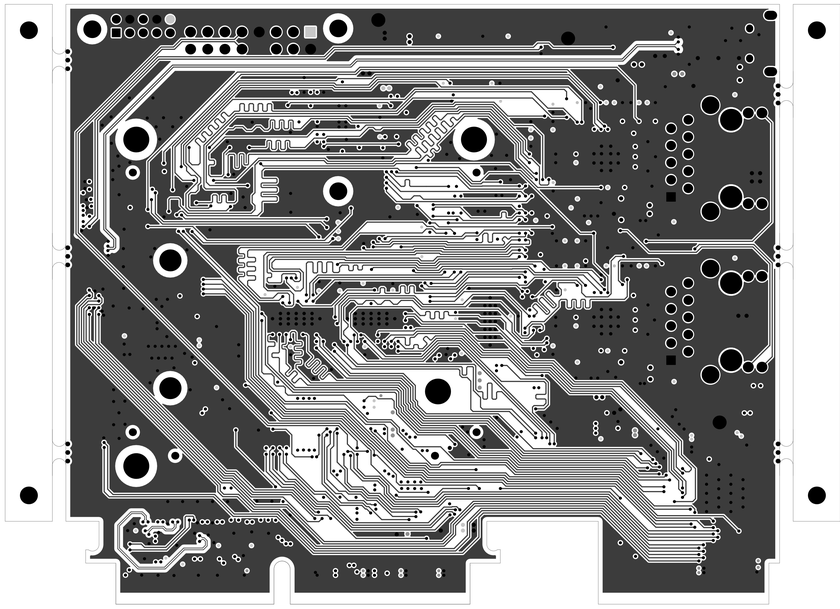
ENGINEER:	LAYOUT BY: .PCB_Layout
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.0.1.36



TEXAS INSTRUMENTS

PROJECT TITLE:
AM261 HSEC Adapter Board

DESIGNED FOR:
Public Release

FILE NAME:
PROC200E1.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465	
LAYER NAME = MS Title Sheet	TID #:			
PLOT NAME = SIG	GENERATED : 01/10/2024 12:24:07			TEXAS INSTRUMENTS

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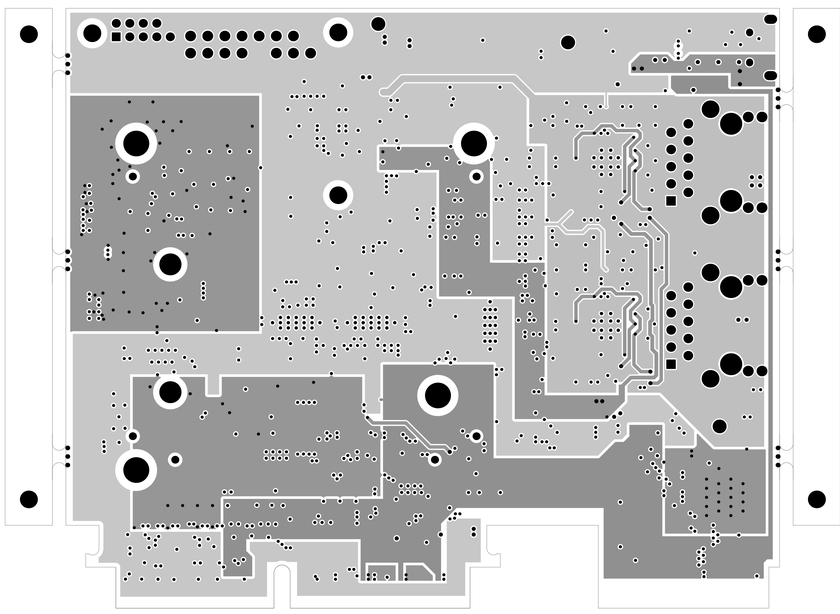
ENGINEER:	LAYOUT BY: .PCB_Layout
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.0.1.36



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465	
LAYER NAME = M9 Title Sheet (M1 Board Outline, PWR)	TID #:			
PLOT NAME = PWR	GENERATED : 01/10/2024 12:24:07			TEXAS INSTRUMENTS

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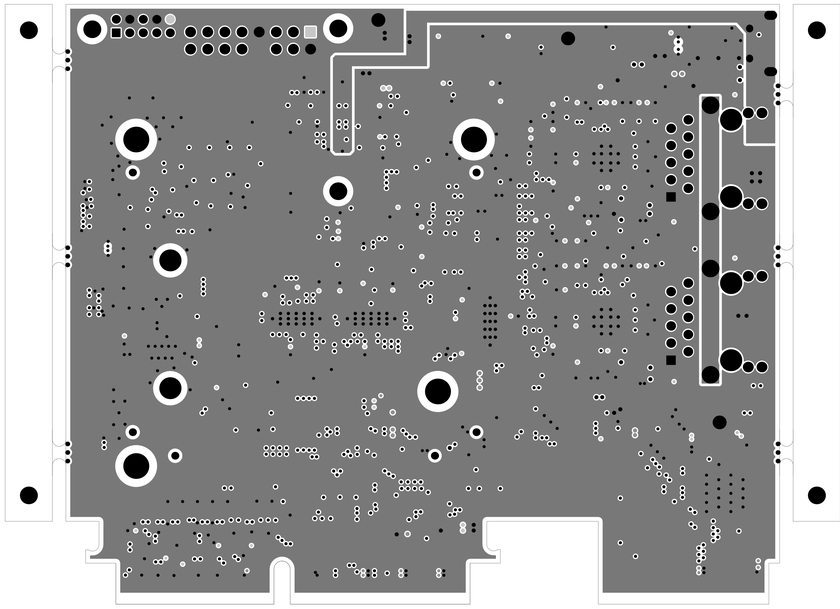
TEXAS INSTRUMENTS

PROJECT TITLE: AM261 HSEC Adapter Board

DESIGNED FOR: Public Release

FILE NAME: PROC200E1.PcbDoc

ENGINEER:	LAYOUT BY: .PCB_Layout
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.0.1.36



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465	
LAYER NAME = M9 Title Sheet	TID #:			
PLOT NAME = GND2	GENERATED : 01/10/2024 12:24:07			TEXAS INSTRUMENTS

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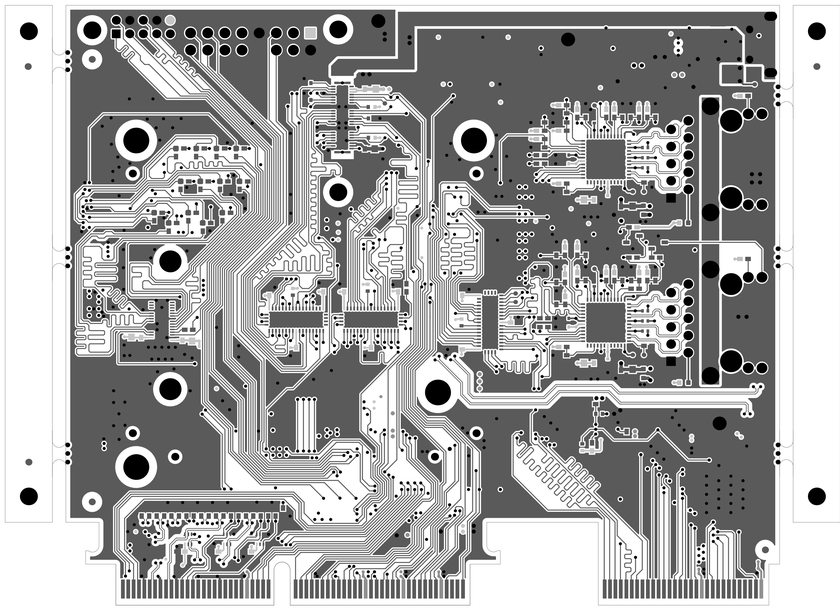
TEXAS INSTRUMENTS

PROJECT TITLE:
AM261 HSEC Adapter Board

DESIGNED FOR:
Public Release

FILE NAME:
PROC200E1.PcbDoc

ENGINEER:	LAYOUT BY: .PCB_Layout
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.0.1.36



TEXAS INSTRUMENTS

PROJECT TITLE:
AM261 HSEC Adapter Board

DESIGNED FOR:
Public Release

FILE NAME:
PROC200E1.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465	ENGINEER:	LAYOUT BY: .PCB_Layout
LAYER NAME = Bottom Sheet	TID #:				
PLOT NAME = Bottom Layer	GENERATED : 01/10/2024 12:24:08		TEXAS INSTRUMENTS	SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.0.1.36

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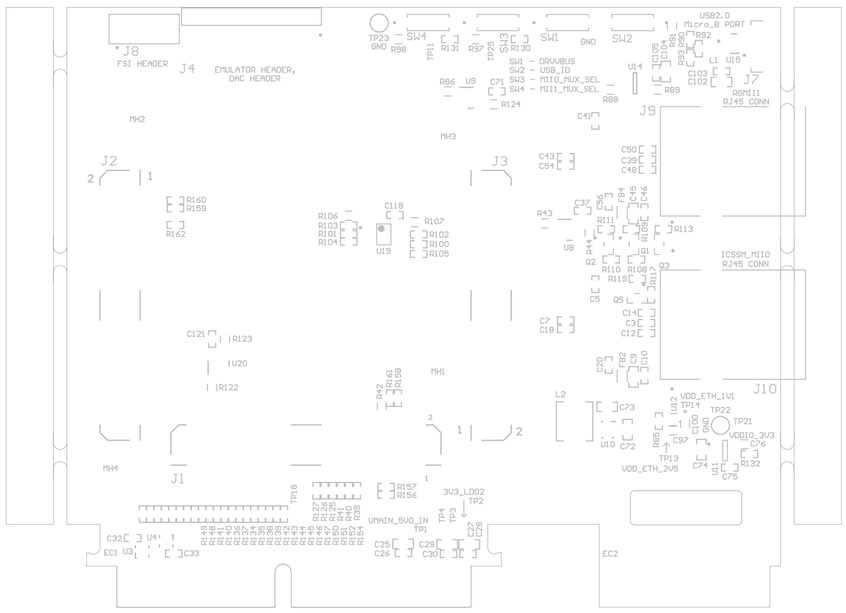

TEXAS INSTRUMENTS

PROJECT TITLE:
AM261 HSEC Adapter Board

DESIGNED FOR:
Public Release

FILE NAME:
PROC200E1.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465
LAYER NAME = M0 Title Sheet (M1 Board Outline)	TID #:		
PLOT NAME = Top Silkscreen Overlay	GENERATED : 01/10/2024 12:24:08		TEXAS INSTRUMENTS

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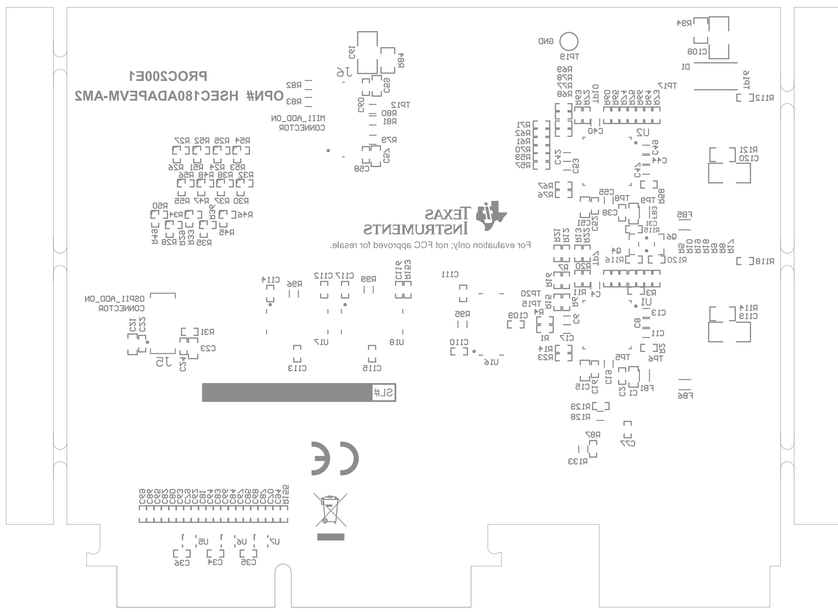
ENGINEER:	LAYOUT BY: .PCB_Layout
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.0.1.36



TEXAS INSTRUMENTS

PROJECT TITLE:
AM261 HSEC Adapter Board

DESIGNED FOR:
Public Release

FILE NAME:
PROC200E1.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465
LAYER NAME = M9 Title Sheet (M1 Board Outline)	TID #: Bottom Overlay		
PLOT NAME = Bottom Silkscreen Overlay	GENERATED : 01/10/2024 12:24:08		TEXAS INSTRUMENTS

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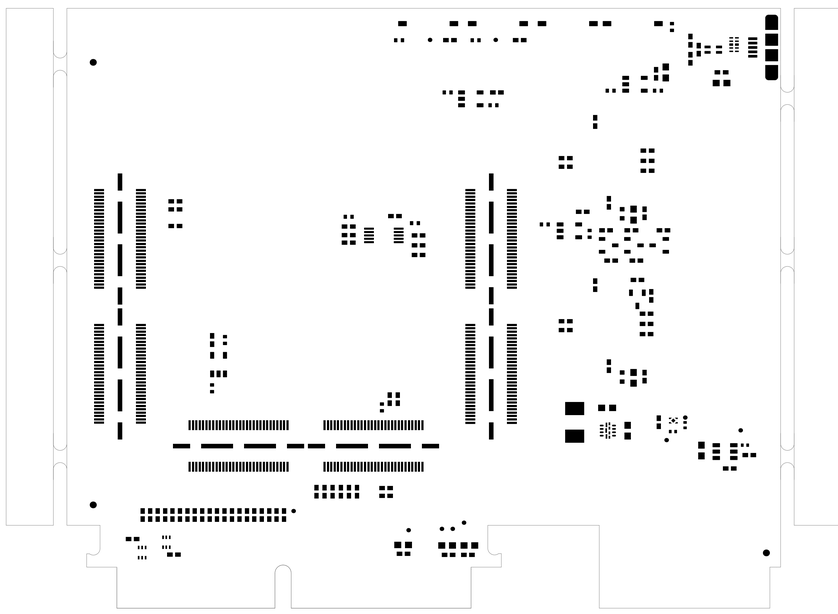
ENGINEER:	LAYOUT BY: .PCB_Layout
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.0.1.36



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465
LAYER NAME = Top Paste Sheet	TID #:		
PLOT NAME = Top Paste Mask Print	GENERATED : 01/10/2024 12:24:08		TEXAS INSTRUMENTS

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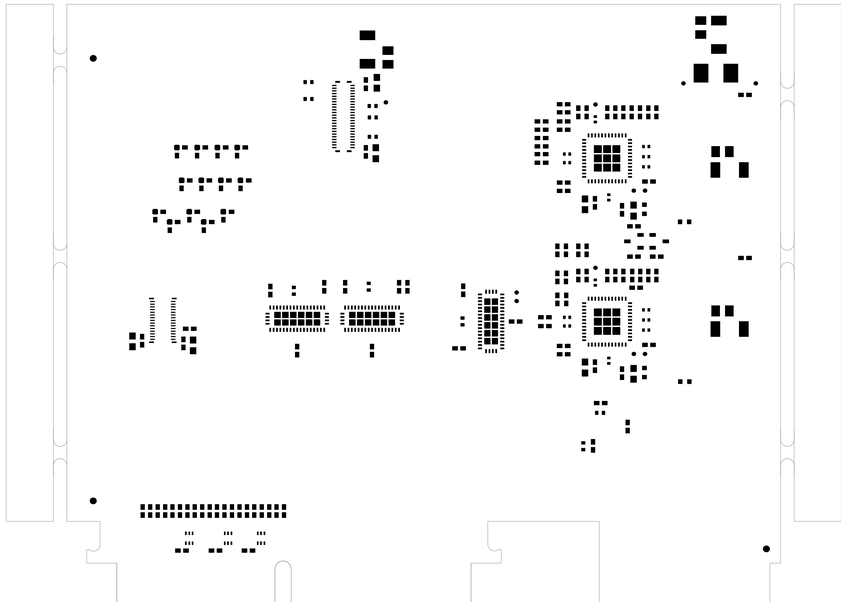
TEXAS INSTRUMENTS

PROJECT TITLE: AM261 HSEC Adapter Board

DESIGNED FOR: Public Release

FILE NAME: PROC200E1.PcbDoc

ENGINEER:	LAYOUT BY: .PCB_Layout
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.0.1.36



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465	
LAYER NAME = Bottom Paste	TID #:			
PLOT NAME = Bottom Paste Mask Print	GENERATED : 01/10/2024 12:24:08			TEXAS INSTRUMENTS

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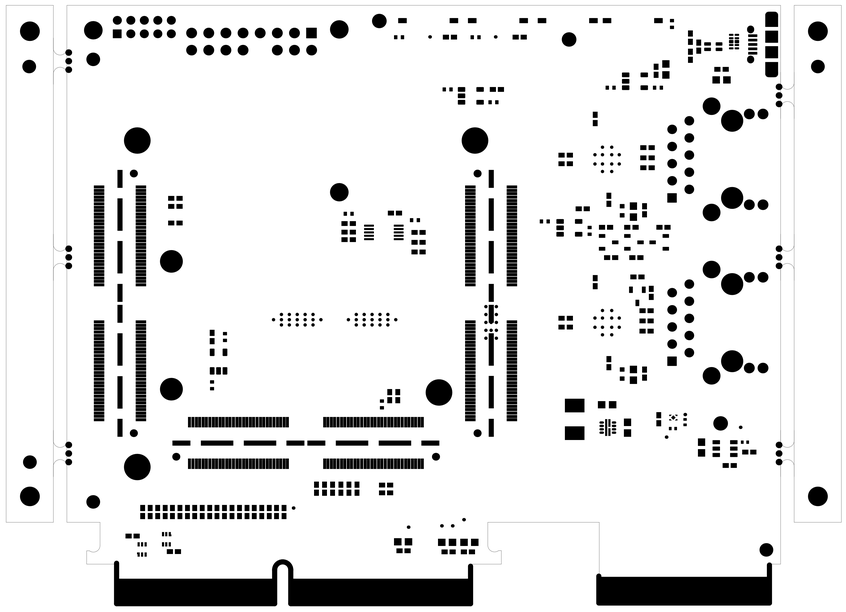
TEXAS INSTRUMENTS

PROJECT TITLE: AM261 HSEC Adapter Board

DESIGNED FOR: Public Release

FILE NAME: PROC200E1.PcbDoc

ENGINEER:	LAYOUT BY: .PCB_Layout
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.0.1.36



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465	
LAYER NAME = Top Solder	TID #:			
PLOT NAME = Top Solder Mask Print	GENERATED : 01/10/2024 12:24:08			TEXAS INSTRUMENTS

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TEXAS INSTRUMENTS

PROJECT TITLE: AM261 HSEC Adapter Board

DESIGNED FOR: Public Release

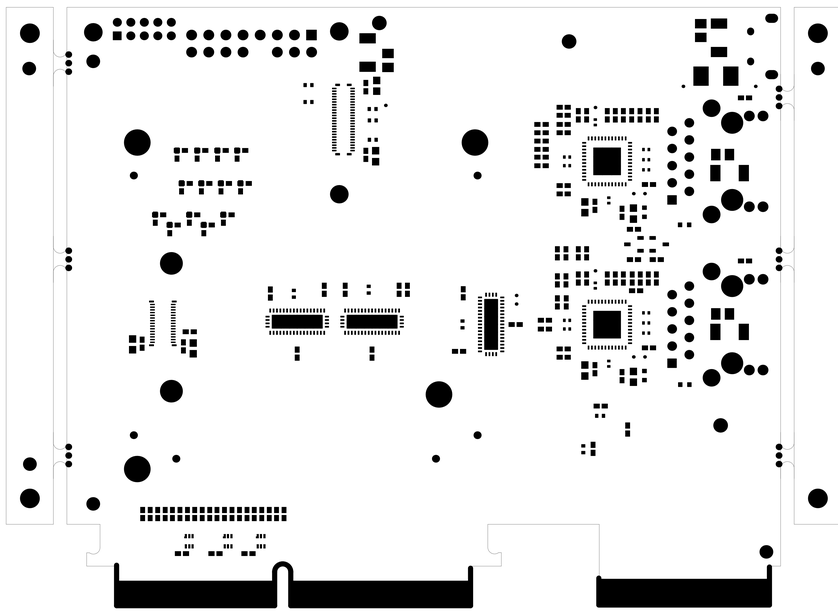
FILE NAME: PROC200E1.PcbDoc

ENGINEER:

LAYOUT BY: .PCB_Layout

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.0.1.36



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465
LAYER NAME = M1 Board Outline M9 Title Sheet	TID #: Bottom Solder		
PLOT NAME = Bottom Solder Mask Print	GENERATED : 01/10/2024 12:24:08		TEXAS INSTRUMENTS

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TEXAS INSTRUMENTS

PROJECT TITLE: AM261 HSEC Adapter Board

DESIGNED FOR: Public Release

FILE NAME: PROC200E1.PcbDoc

ENGINEER:	LAYOUT BY: .PCB_Layout
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.0.1.36

PROJECT TITLE:
AM261 HSEC Adapter Board

DESIGNED FOR:
Public Release

FILE NAME:
PROC200E1.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465
LAYER NAME = M1 Board Outline M9 Title Sheet	TID #:		
PLOT NAME = Board Outline	GENERATED : 01/10/2024 12:24:08		TEXAS INSTRUMENTS

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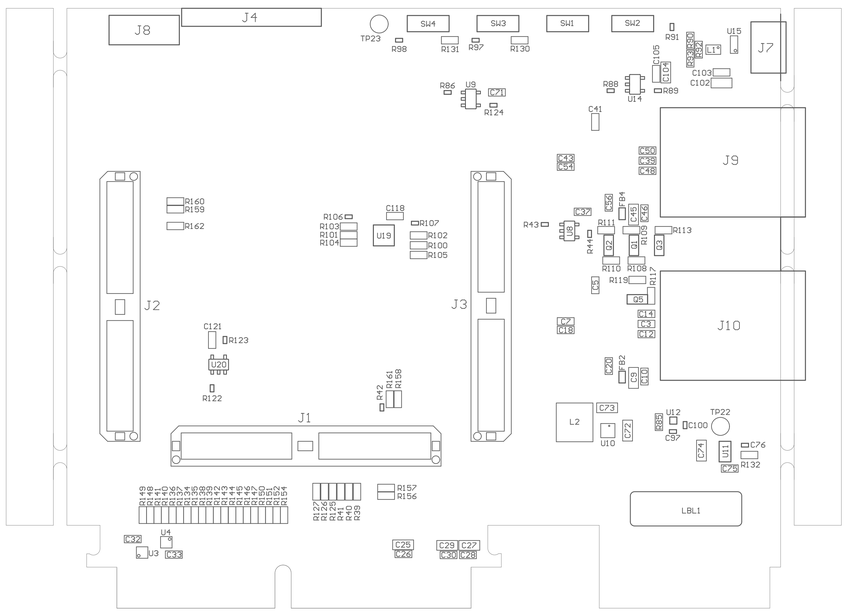
ENGINEER:

LAYOUT BY: .PCB_Layout

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.0.1.36

223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
221 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



ASSEMBLY VARIANT: [No Variations]

ACB 0 REWORK FROM WIDPFBODE TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465	
LAYER NAME = M9 Title Sheet (M1 Board Outline)	TID #:			
PLOT NAME = M5 Assembly Top (GENERATED)	GENERATED : 01/10/2024 12:24:08		TEXAS INSTRUMENTS	

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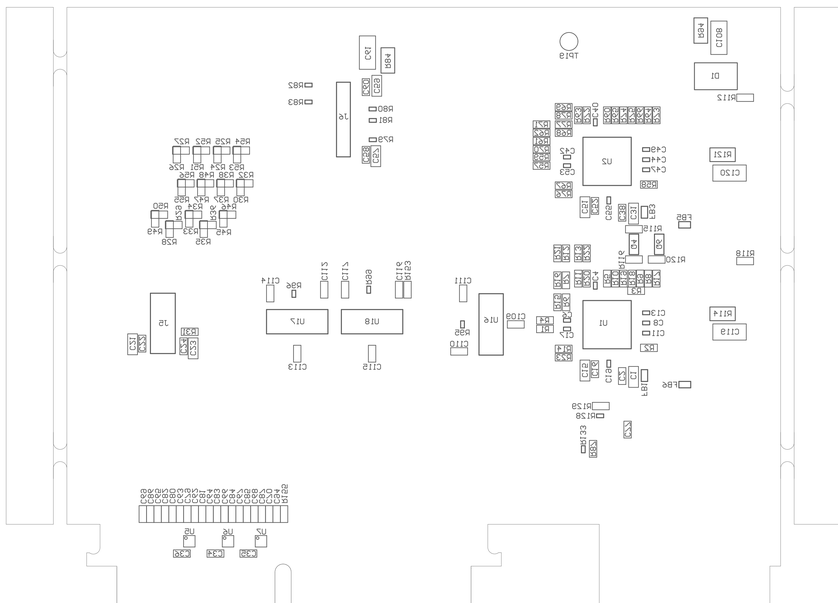
TEXAS INSTRUMENTS

PROJECT TITLE: AM261 HSEC Adapter Board

DESIGNED FOR: Public Release

FILE NAME: PROC200E1.PcbDoc

ENGINEER:	LAYOUT BY: .PCB_Layout
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.0.1.36



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

ALL ARTWORK VIEWED FROM TOP SIDE	E1	BOARD #: PROC200E1	BOARD REV: E1
LAYER NAME = M9 Title Sheet (M1 Board Outline)		TID #:	TID #
PLOT NAME: PROC200E1-M9-Assembly Bottom		GENERATED: 01/01/2024 12:24:08	PLOTTED BY: TEXAS INSTRUMENTS

PCB VIEWED FROM BOTTOM SIDE

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TEXAS INSTRUMENTS

PROJECT TITLE: AM261 HSEC Adapter Board

DESIGNED FOR: Public Release

FILE NAME: PROC200E1.PcbDoc

ENGINEER:

LAYOUT BY: .PCB_Layout

SCALE: 1.00

ALTIUM DESIGNER VERSION: 24.0.1.36

TEXAS INSTRUMENTS

PROJECT TITLE:
AM261 HSEC Adapter Board

DESIGNED FOR:
Public Release

FILE NAME:
PROC200E1.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465	ENGINEER:	LAYOUT BY: .PCB_Layout
LAYER NAME = Drill Guide	TID #:				
PLOT NAME = Drill Guide For (Top Layer - Bottom Layer): 01/10/2024 12:24:09	GENERATED BY:		TEXAS INSTRUMENTS	SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.0.1.36

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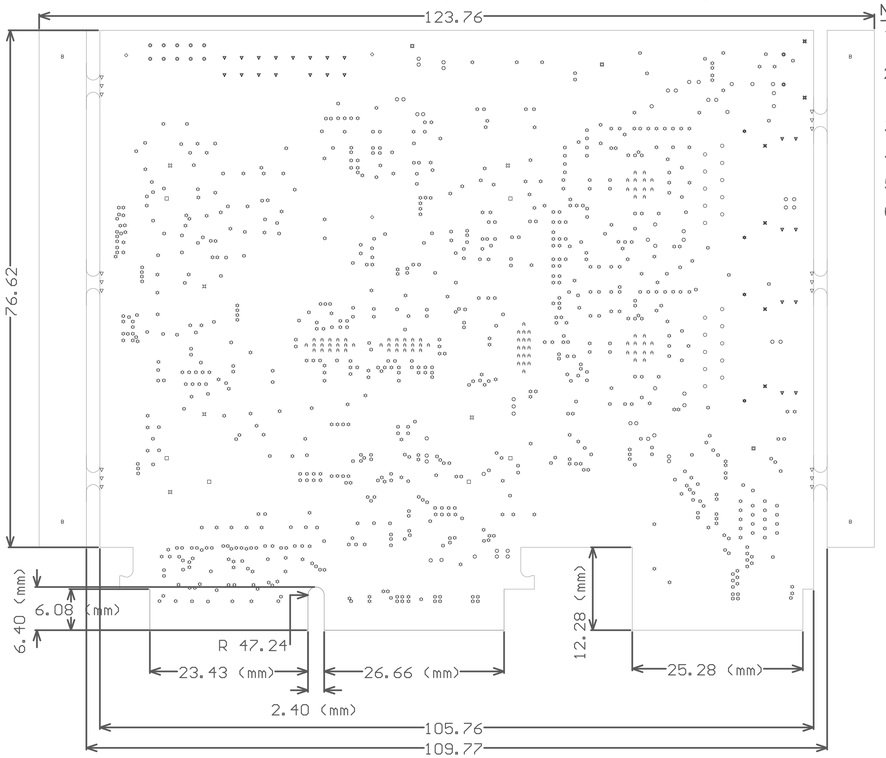
Symbol	Count	Hole Size	Hole Length	Plated	Hole Tolerance (+)	Hole Tolerance (-)	Hole Tolerance	Hole Type
A	75	7.87mil (0.200mm)	-	PTH				Round
	863	8.00mil (0.203mm)	-	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)	+/-3.00mil	Round
	55	12.00mil (0.305mm)	-	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)	+/-3.00mil	Round
	2	25.59mil (0.650mm)	29.53mil (0.750mm)	PTH				Slot
	10	31.50mil (0.800mm)	-	PTH				Round
	18	32.00mil (0.813mm)	-	NPTH	3.00mil (0.076mm)	3.00mil (0.076mm)	+/-3.00mil	Round
	20	35.43mil (0.900mm)	-	PTH				Round
	3	40.00mil (1.016mm)	-	PTH				Round
	23	40.16mil (1.020mm)	-	PTH				Round
	6	45.28mil (1.150mm)	-	NPTH	3.00mil (0.076mm)	3.00mil (0.076mm)	+/-3.00mil	Round
	2	51.18mil (1.300mm)	29.53mil (0.750mm)	PTH				Slot
	4	66.93mil (1.700mm)	-	PTH				Round
	3	102.99mil (2.616mm)	-	PTH				Round
B	4	108.00mil (2.743mm)	-	NPTH	3.00mil (0.076mm)	3.00mil (0.076mm)	+/-3.00mil	Round
	4	127.95mil (3.250mm)	-	NPTH				Round
	2	127.95mil (3.250mm)	-	PTH				Round
	4	159.00mil (4.039mm)	-	NPTH	3.00mil (0.076mm)	3.00mil (0.076mm)	+/-3.00mil	Round
	1098 Total							

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout



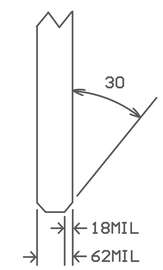
SCALE : NTS

NOTES:

1. BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
2. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED, PROVIDED NO ADJACENT COPPER IS EXPOSED & NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING/COVERING" REQUIREMENTS.
3. MANUFACTURER'S IDENTIFICATION,DATECODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE OF THE BOARD.
4. LAYER TO LAYER REGISTRATION SHALL BE WITHIN +/-2 MIL.
5. REFER IMPEDANCE TABLE FOR IMPEDANCE CONTROL TRACES ON LAYER 1, 3 & 6.
6. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS OTHERWISE SOLDER MASK OPENED IN GERBER. VIA HOLES SHALL BE FILLED WITH NON CONDUCTIVE INK AND COVERED WITH SOLDER MASK.

IMPEDANCE TABLE : 6

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP BOTTOM	5.66 MILS 5.66 MILS	- -	50 OHM 50 OHM	LAYER-2 (GND LAYER) LAYER-5(GND LAYER)
TOP	4 MILS	7 MILS	100 OHM	LAYER-2 (GND LAYER)
TOP	5 MILS	6.22 MILS	90 OHM	LAYER-2 (GND LAYER)
L3	6.66 MILS	-	50 OHM	LAYER-2 / LAYER-4
L3	4.2 MILS	6 MILS	100 OHM	LAYER-2 / LAYER-4
BOTTOM	4 MILS	7 MILS	100 OHM	LAYER-5(GND LAYER)
BOTTOM	5 MILS	6.22 MILS	90 OHM	LAYER-5(GND LAYER)
L3	5.7 MILS	6 MILS	90 OHM	LAYER-2 / LAYER-4



GOLD FINGER
SIDE VIEW

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	2.00mil	3.6	
1	Top Layer		1.85mil		
	Dielectric 1	FR-4	3.70mil	4.1	
2	GND1		1.26mil		
	Dielectric 2	FR-4	5.00mil	3.7	
3	SIG1		1.26mil		
	Dielectric 3	FR-4	32.00mil	3.7	
4	PWR		1.26mil		
	Dielectric 4	FR-4	5.00mil	3.7	
5	GND2		1.26mil		
	Dielectric 5	FR-4	3.70mil	4.1	
6	Bottom		1.85mil		
	Bottom Solder	Solder Resist	2.00mil	3.6	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.5 MIL
MIN. VIA PAD SIZE: 18 MIL
MINIMUM ANNULAR RING 0.127mm (5MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER BLUE
[ ] MATTE [X] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV
[X] OTHER HARD GOLD OVER NICKEL 30u/80u, ON EDGEFINGERS

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[X] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

[ ] OUTER LAYERS 6 MIL WIDE, 6 MIL SPACE
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE
[ ] INNER LAYERS 5 MIL WIDE, 7 MIL SPACE
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE
[ ] OUTER LAYERS 6.1 MIL WIDE, 6 MIL SPACE
TRACES REQUIRE 90 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: AM261 HSEC Adapter Board
DESIGNED FOR: Public Release
FILE NAME: PROC200E1.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE | BOARD #: PROC200 | REV: E1 | SVN REV: 465
LAYER NAME = M1 Board Outline / Mechanical Layer 1 Dimensions | TID #:
PLOT NAME = Drill Drawing For (Top Layer To Bottom Layer) | GENERATED 01/10/2024 12:24:13 | TEXAS INSTRUMENTS

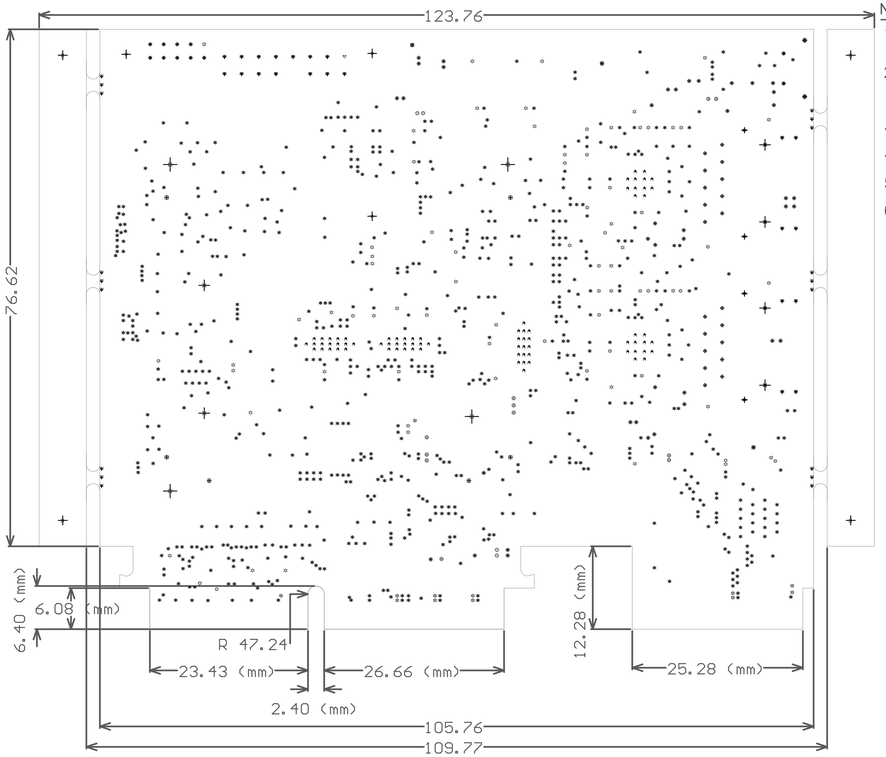
Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER:
LAYOUT BY: .PCB_Layout
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.0.1.36

Symbol	Count	Hole Size	Hole Length	Plated	Hole Tolerance (+)	Hole Tolerance (-)	Hole Tolerance	Hole Type
A	75	7.87mil (0.200mm)	-	PTH				Round
	863	8.00mil (0.203mm)	-	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)	+/-3.00mil	Round
	55	12.00mil (0.305mm)	-	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)	+/-3.00mil	Round
	2	25.59mil (0.650mm)	29.53mil (0.750mm)	PTH				Slot
	10	31.50mil (0.800mm)	-	PTH				Round
	18	32.00mil (0.813mm)	-	NPTH	3.00mil (0.076mm)	3.00mil (0.076mm)	+/-3.00mil	Round
	20	35.43mil (0.900mm)	-	PTH				Round
	3	40.00mil (1.016mm)	-	PTH				Round
	23	40.16mil (1.020mm)	-	PTH				Round
	6	45.28mil (1.150mm)	-	NPTH	3.00mil (0.076mm)	3.00mil (0.076mm)	+/-3.00mil	Round
	2	51.18mil (1.300mm)	29.53mil (0.750mm)	PTH				Slot
	4	66.93mil (1.700mm)	-	PTH				Round
	3	102.99mil (2.616mm)	-	PTH				Round
B	4	108.00mil (2.743mm)	-	NPTH	3.00mil (0.076mm)	3.00mil (0.076mm)	+/-3.00mil	Round
	4	127.95mil (3.250mm)	-	NPTH				Round
	2	127.95mil (3.250mm)	-	PTH				Round
	4	159.00mil (4.039mm)	-	NPTH	3.00mil (0.076mm)	3.00mil (0.076mm)	+/-3.00mil	Round
	1098 Total							

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

SCALE : NTS

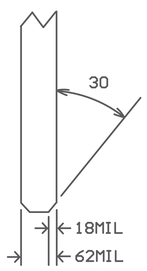


NOTES:

1. BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
2. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED, PROVIDED NO ADJACENT COPPER IS EXPOSED & NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING/COVERING" REQUIREMENTS.
3. MANUFACTURER'S IDENTIFICATION,DATECODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE OF THE BOARD.
4. LAYER TO LAYER REGISTRATION SHALL BE WITHIN +/-2 MIL.
5. REFER IMPEDANCE TABLE FOR IMPEDANCE CONTROL TRACES ON LAYER 1, 3 & 6.
6. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS OTHERWISE SOLDER MASK OPENED IN GERBER. VIA HOLES SHALL BE FILLED WITH NON CONDUCTIVE INK AND COVERED WITH SOLDER MASK.

IMPEDANCE TABLE : 6

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP BOTTOM	5.66 MILS 5.66 MILS	- -	50 OHM 50 OHM	LAYER-2 (GND LAYER) LAYER-5(GND LAYER)
TOP	4 MILS	7 MILS	100 OHM	LAYER-2 (GND LAYER)
TOP	5 MILS	6.22 MILS	90 OHM	LAYER-2 (GND LAYER)
L3	6.66 MILS	-	50 OHM	LAYER-2 / LAYER-4
L3	4.2 MILS	6 MILS	100 OHM	LAYER-2 / LAYER-4
BOTTOM	4 MILS	7 MILS	100 OHM	LAYER-5(GND LAYER)
BOTTOM	5 MILS	6.22 MILS	90 OHM	LAYER-5(GND LAYER)
L3	5.7 MILS	6 MILS	90 OHM	LAYER-2 / LAYER-4



GOLD FINGER
SIDE VIEW

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	2.00mil	3.6	
1	Top Layer		1.85mil		
	Dielectric 1	FR-4	3.70mil	4.1	
2	GND1		1.26mil		
	Dielectric 2	FR-4	5.00mil	3.7	
3	SIG1		1.26mil		
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	Dielectric 4	FR-4	5.00mil	3.7	
5	GND2		1.26mil		
	Dielectric 5	FR-4	3.70mil	4.1	
6	Bottom		1.85mil		
	Bottom Solder	Solder Resist	2.00mil	3.6	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4.5 MIL
MIN. VIA PAD SIZE: 18 MIL
MINIMUM ANNULAR RING 0.127mm (5MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER BLUE
[ ] MATTE [X] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV
[X] OTHER HARD GOLD OVER NICKEL 30u/80u, ON EDGEFINGERS

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[X] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

[ ] OUTER LAYERS 6 MIL WIDE, 6 MIL SPACE
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE
[ ] INNER LAYERS 5 MIL WIDE, 7 MIL SPACE
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE
[ ] OUTER LAYERS 6.1 MIL WIDE, 6 MIL SPACE
TRACES REQUIRE 90 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: AM261 HSEC Adapter Board
DESIGNED FOR: Public Release
FILE NAME: PROC200E1.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465
LAYER NAME = M1 Board Outline, M2 Board Dimensions	TID #:		
PLOT NAME = Fab Drawing	GENERATED : 01/10/2024 12:24:17	TEXAS INSTRUMENTS	

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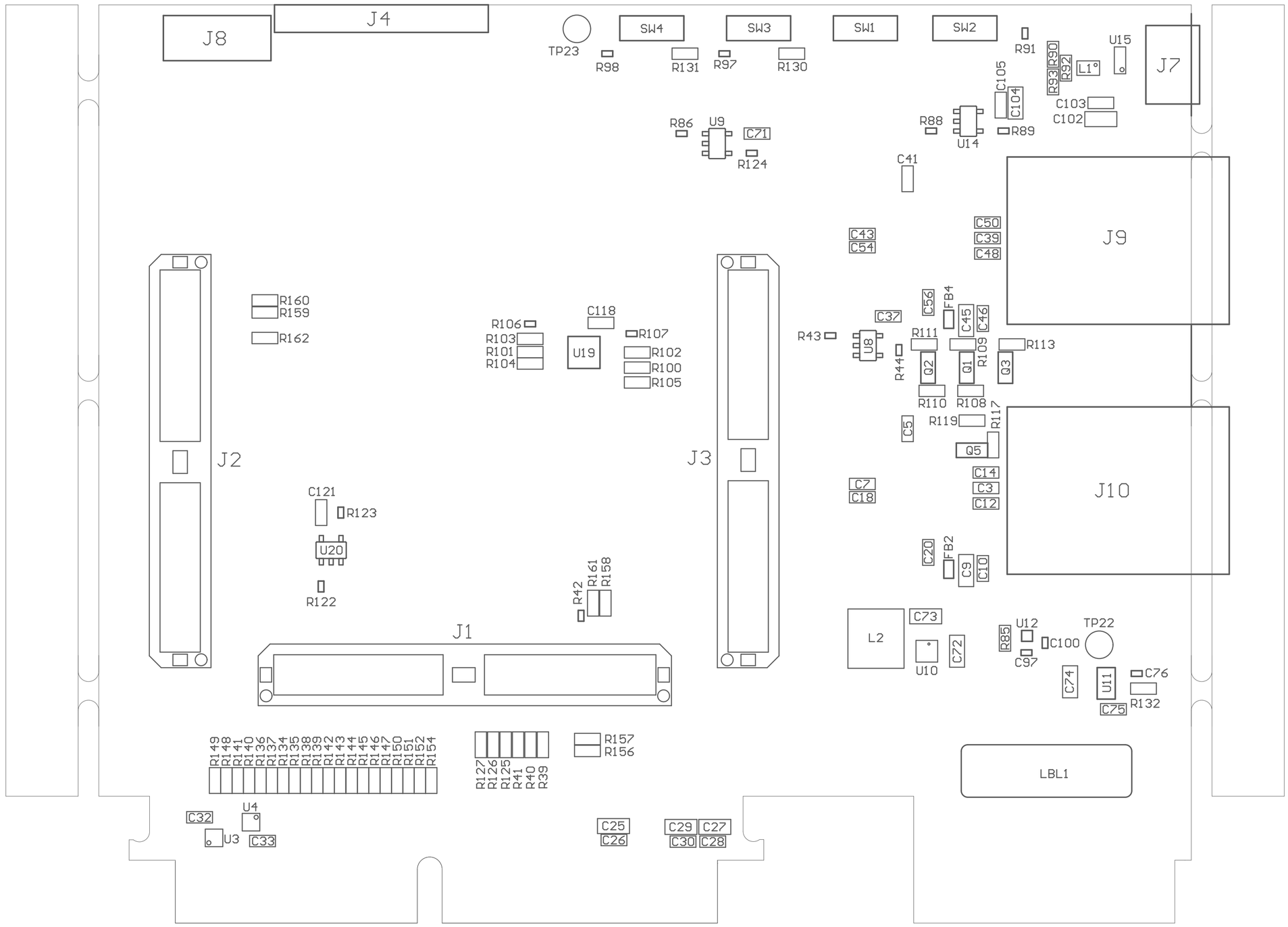
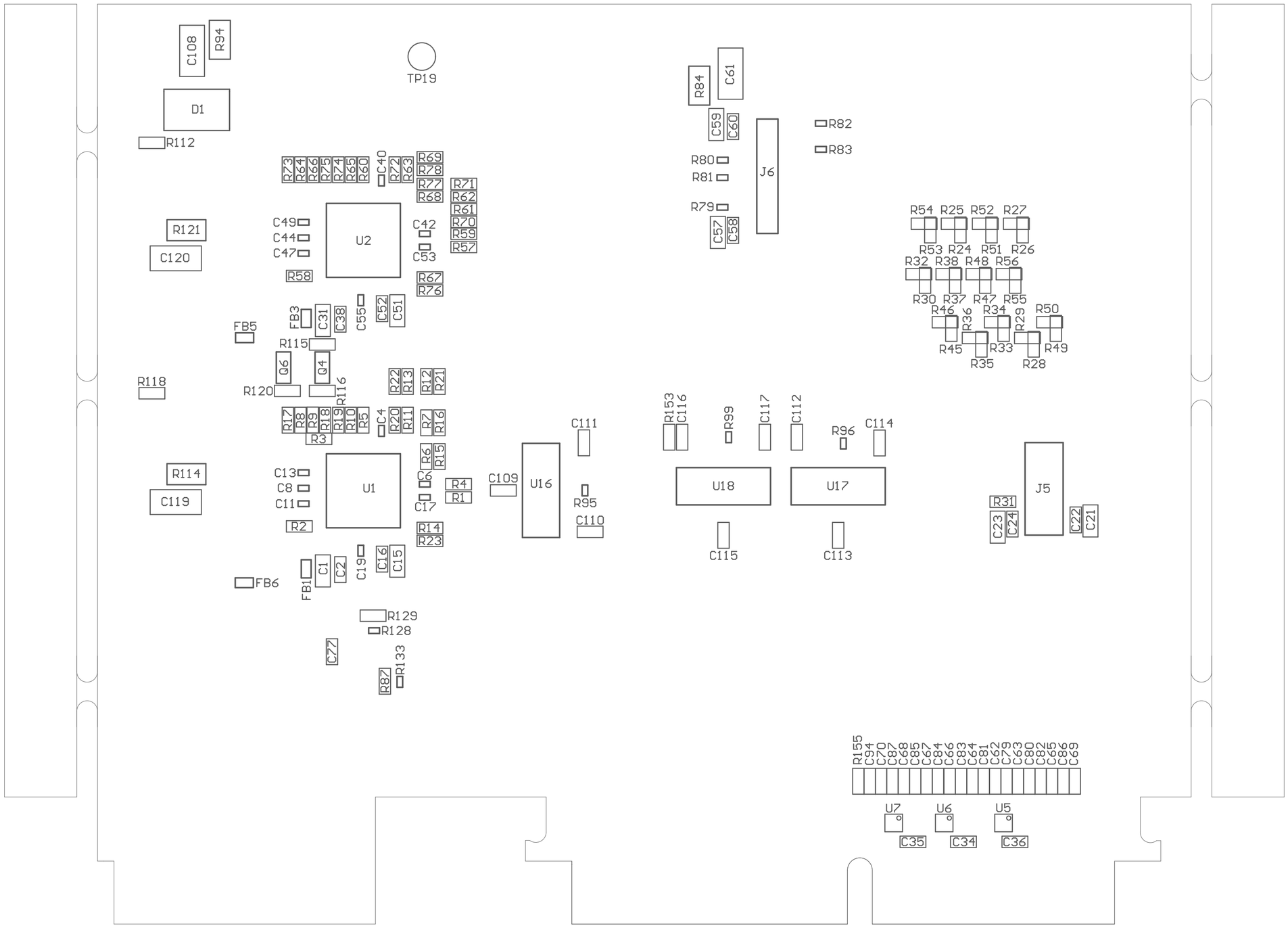
ENGINEER:
LAYOUT BY: .PCB_Layout
SCALE: 1.00
ALTIUM DESIGNER VERSION: 24.0.1.36

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



ASSEMBLY VARIANT: [No Variations]

PCB VIEWED FROM TOP SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465
TID #: M1 Board Outline			
GENERATED : PLOT NAME = TOP Assembly Drawing	01/10/2024 12:24:19		TEXAS INSTRUMENTS



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB VIEWED FROM BOTTOM SIDE	BOARD #: PROC200	REV: E1	SVN REV: 465
	TID #:		
PLOT NAME = BTM Assembly Drawing	GENERATED : 01/10/2024 12:24:19		TEXAS INSTRUMENTS