

AM275x EVM

TABLE OF CONTENTS

PAGE	CONTENTS
01	TABLE OF CONTENTS
02	REVISION HISTORY
03	LINK TO DESIGN COLLATERALS AND FAQs
04	BLOCK DIAGRAM AM275x EVM
05	BLOCK DIAGRAM XDS110 DEBUGGER
06	POWER ARCHITECTURE BLOCK DIAGRAM
07	POWER SEQUENCE
08	I2C TREE
09	GPIO MAPPING TABLE
10	USB TYPE-C POWER
11	USB TYPE-C POWER CONNECTOR
12	PERIPHERAL POWER SUPPLY
13	PRE REGULATOR SUPPLIES - LDOs
14	SOC POWER SUPPLY PMIC - 1
15	SOC POWER SUPPLY PMIC - 2
16	SOC POWER SUPPLIES, SUPPLY RAILS AND SOC GROUND VSS
17	SOC POWER SUPPLIES - DECAPS 1
18	SOC POWER SUPPLIES - DECAPS 2
19	SOC WKUP /MCU DOMAIN & OSCILLATOR
20	CDCE CLOCK GENERATION, SOC & ETHERNET PHY CLOCK BUFFER
21	SOC RESET -1
22	SOC RESET -2
23	BOOT MODE SWITCHES & BOOTMODE PINS
24	HYPERRAM DEVICE INTERFACE AND RESET
25	SOC OSPI INTERFACE AND OSPI DEVICE INTERFACE & RESET
26	SOC MMC0 INTERFACE AND FET SELECTION
27	eMMC FLASH + RESET
28	SD CARD - LOAD SWITCH, LOAD SWITCH RESET LOGIC
29	SOC PERIPHERALS 1 - McASP
30	SOC PERIPHERALS 2 - GENERAL
31	SOC PERIPHERAL 3 - ETHERNET INTERFACE AND USB
32	McASP4 FET SELECTION AND MLB HEADER
33	SoC ADC0 INTERFACE AND HEADER
34	AUDIO REFERENCE CLOCKS
35	Ethernet PHY power supply (VDD_2V5)
36	CPSW3G RGMII_1 ETHERNET CONNECTOR 1 & RESET
37	CPSW3G RGMII_2 ETHERNET CONNECTOR 2 & RESET
38	USB0 TYPE-C DRP
39	AUDIO - STEREO LINEOUT - 1
40	AUDIO - STEREO LINEOUT - 2
41	AUDIO - MICROPHONE/LINE IN 1

PAGE	CONTENTS
42	AUDIO - MICROPHONE/LINE IN 2
43	AUDIO EXPANSION CONNECTOR 1 & DECAPS
44	AUDIO EXPANSION CONNECTOR 2 & DECAPS
45	CAN TRANSCEIVER
46	BOOTMODE IO EXPANDER AND BUFFERS
47	IO EXPANDER AND USER TEST LEDS
48	TEMPERATURE SENSOR AND BOARD ID EEPROM
49	CURRENT MONITORING DEVICES 1
50	CURRENT MONITORING DEVICES 2
51	FT4232 UART TO USB BRIDGE
52	FT4232 UART BUFFERS
53	XDS110 DEBUGGER
54	XDS110 JTAG BUFFER
55	XDS110 TEST AUTOMATION BUFFERS
56	JTAG 20 PIN cTI CONNECTOR
57	ASSEMBLY NOTES AND MOUNTING HARDWARE

BOARD REVISION	E1
SCHEMATIC VERSION	1.0

Note:
Verify the DNI components configuration with respect to the EVM schematics (Use PDF) after completion of design before board assembly

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Title TABLE OF CONTENTS		
Size	PROC190E1	Rev
C		E1
Date:	Monday, September 02, 2024	Sheet 1 of 57

REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	28-05-2024	Initial Draft			
0.2	05-06-2024	Internally reviewed and comments updated	Venkatesh K J	Pandiyarajan	
0.3	06-06-2024	Modified PMIC section as per TI requirements	Venkatesh K J	Pandiyarajan	
0.4	12-06-2024	Implemented review comments from TI	Venkatesh K J	Pandiyarajan	
0.5	20-06-2024	Implemented review comments from TI 1. Updated I2C address of PMIC 2. Resetstatz for warm reset control	Venkatesh K J	Pandiyarajan	
0.6	26-06-2024	Implemented review comments from TI 1. Current sensing for VDD_CANUART AND VDDSHV_CANUART 2. Decap under BGA package change from 0402 to 0201	Venkatesh K J	Pandiyarajan	
0.7	19-07-2024	Implemented reiew comments form TI 1. Implementation of SYNC1_OUT function 2. Addition of OR logic for IVS/3V3 IO voltage control of MMC0 3. PMIC OPN changed to TPS6522435RAHRQ1	Venkatesh K J	Pandiyarajan	
0.8	09-08-2024	Implemented review comments from TI 1. Added optional routing path for CS in OSPI devices having CS on A3 rather than C2. 2. Changed PCM audio device input cap from 2.2uf to 22uf	Venkatesh K J	Pandiyarajan	
0.9	20-08-2024	Updated VDD_CORE decaps with alternate MPN based on TI PDN suggestion.	Venkatesh K J	Pandiyarajan	
1.0	28-08-2024	1. Capacitor line items optimized to reuse VDD_CORE decap values. 2. Schematic Baselined	Venkatesh K J	Pandiyarajan	

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Title REVISION HISTORY

Size	Rev
C	E1
Date: Monday, September 02, 2024	Sheet 2 of 57

LINK TO DESIGN COLLATERALS

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am62x-am62ax-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review>

FAQs

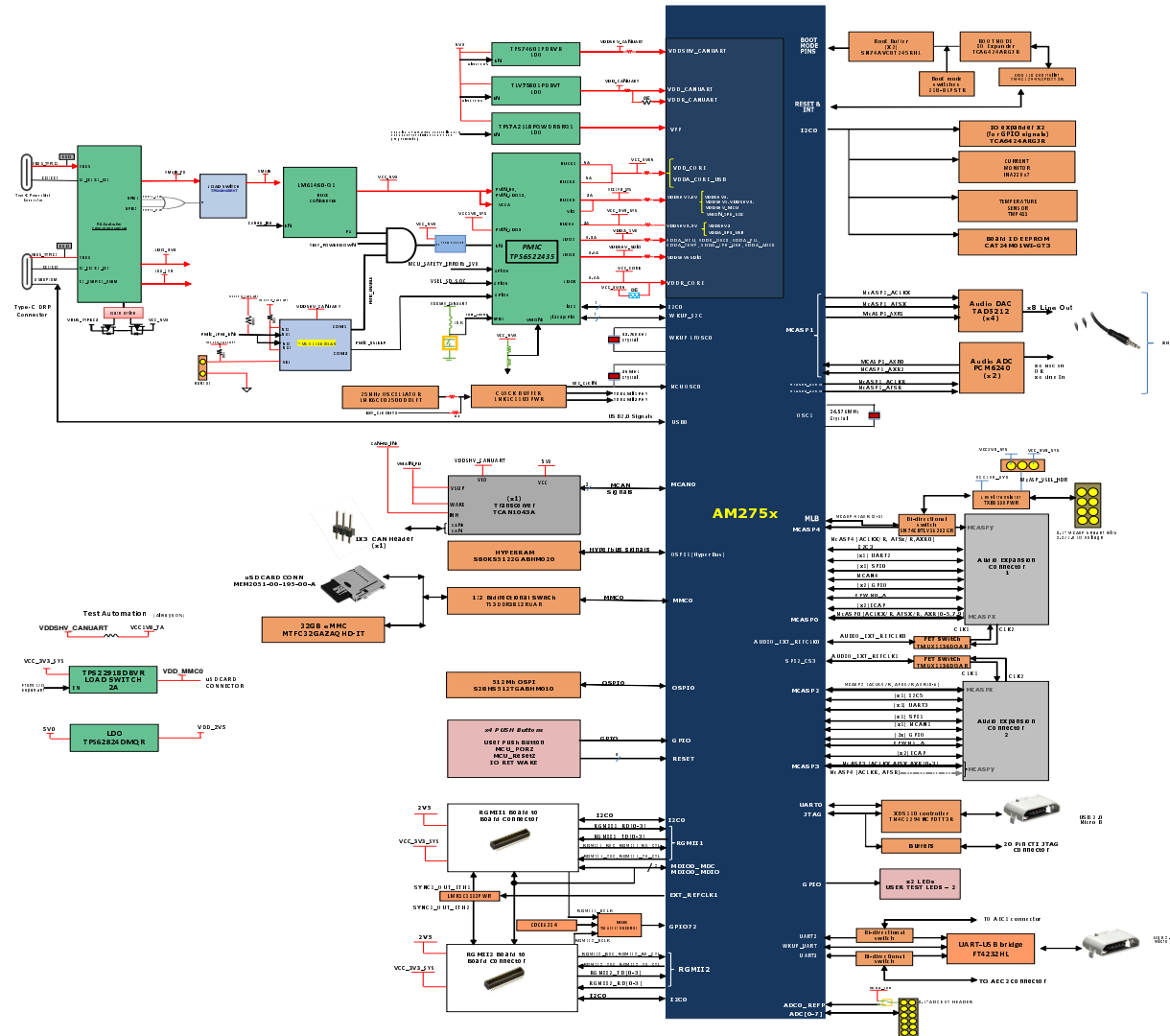
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Title LINK TO DESIGN COLLATERALS

Size	PROC190E1		Rev
C			E1
Date:	Monday, September 02, 2024	Sheet 3 of 57	

BLOCK DIAGRAM AM275x EVM



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Title BLOCK DIAGRAM AM275x_SKEWM

Size PROC190E1

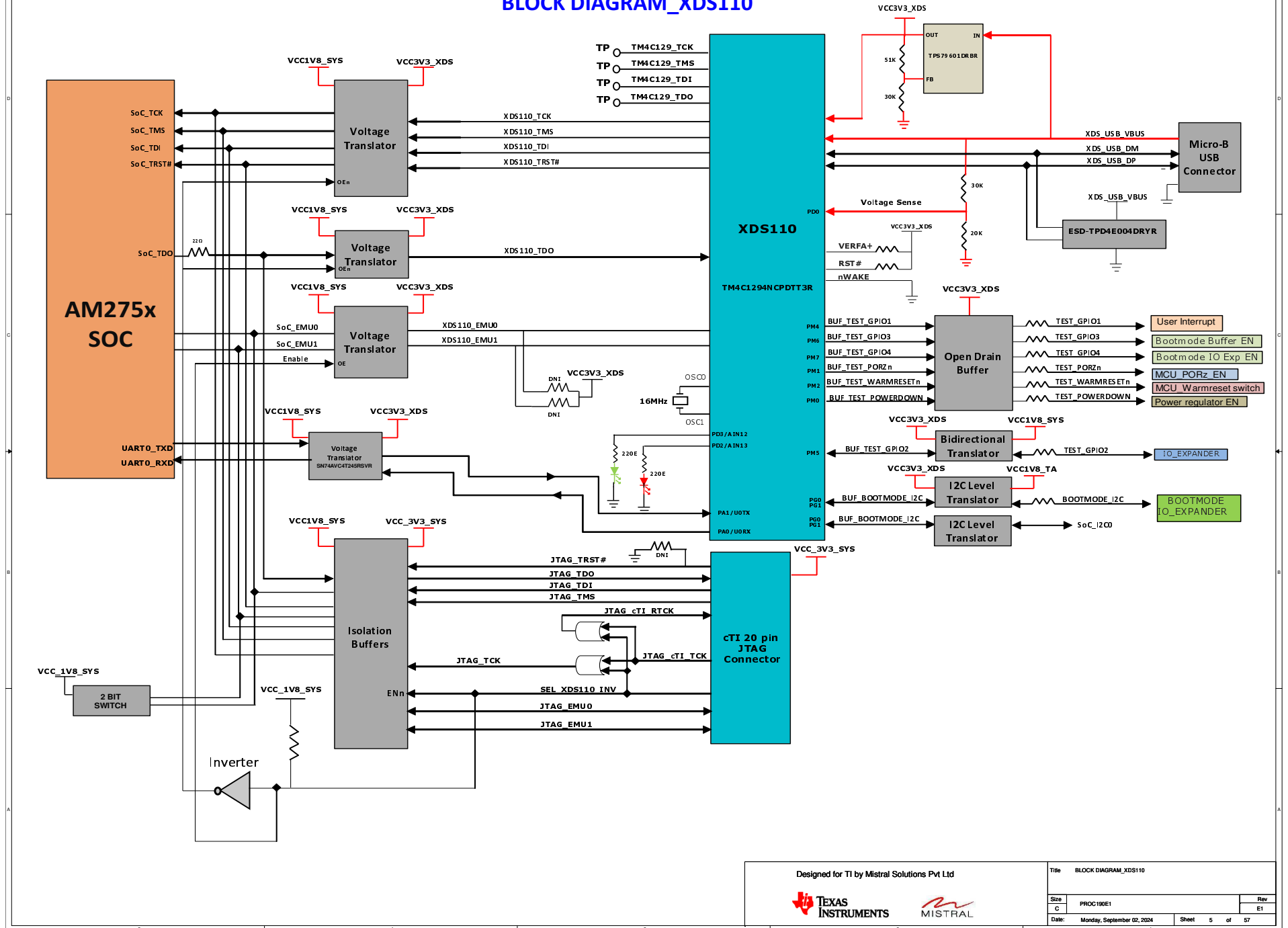
C

Date: Thursday, September 05, 2024

Rev E1

Sheet 4 of 57

BLOCK DIAGRAM_XDS110



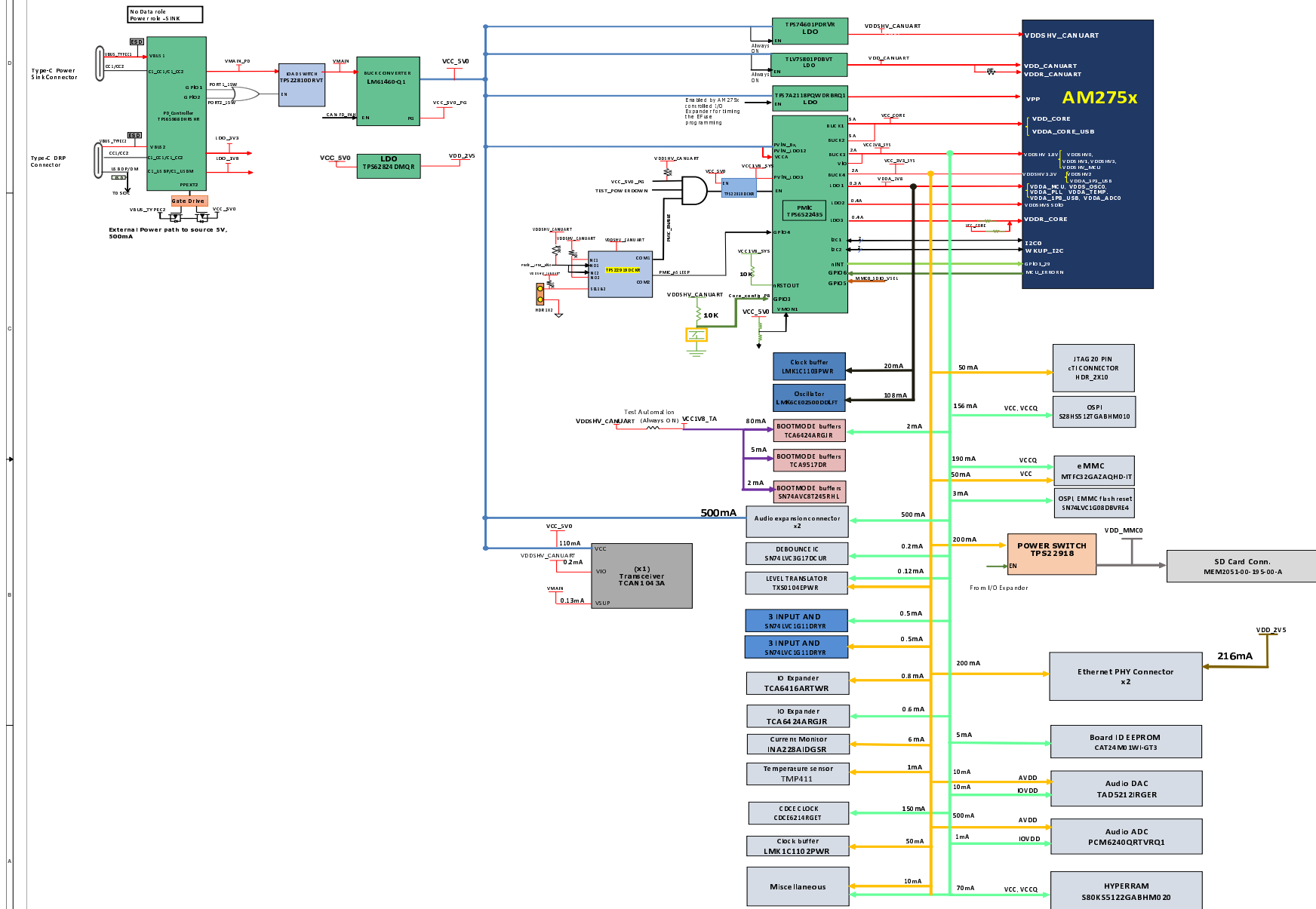
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Title BLOCK DIAGRAM_XDS110

Size	Rev
C	PROC190E1
Date:	Monday, September 02, 2024
Sheet	5 of 57

POWER ARCHITECTURE BLOCK DIAGRAM



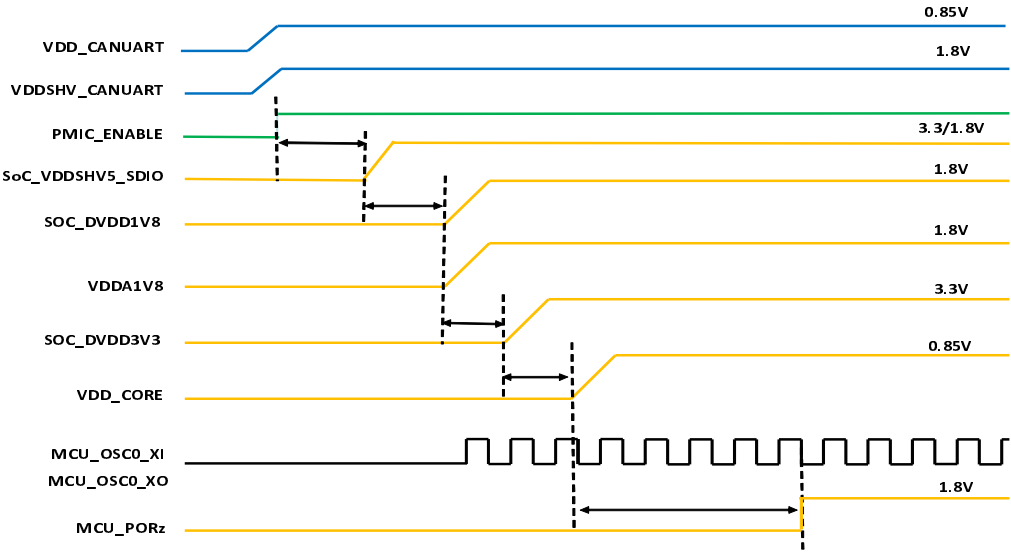
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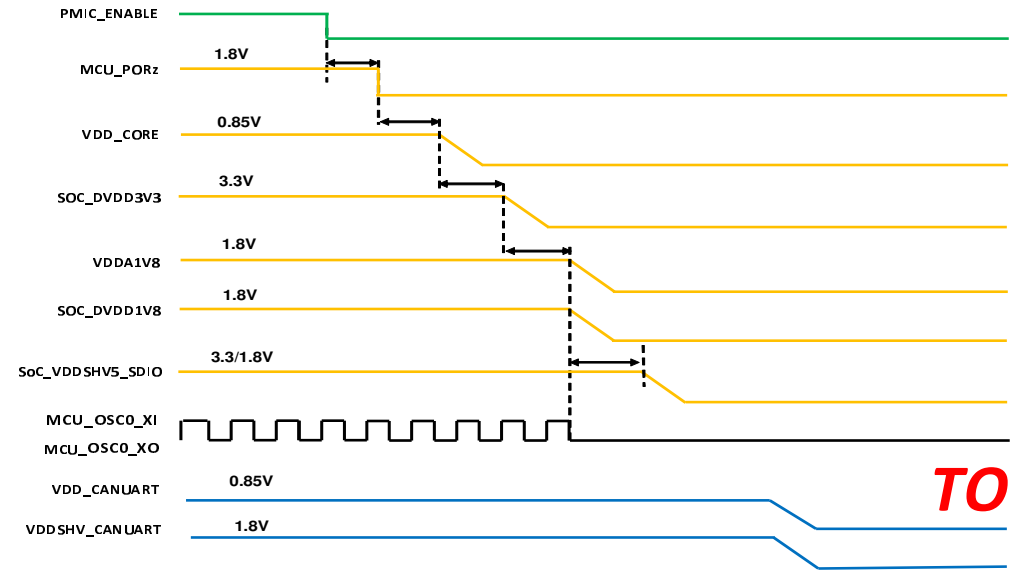
Title	POWER ARCHITECTURE BLOCK DIAGRAM
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Size	PROC190E1	Rev
C		E1
Date:	Monday, September 02, 2024	Sheet 6 of 57

POWER UP SEQUENCE



POWER DOWN SEQUENCE



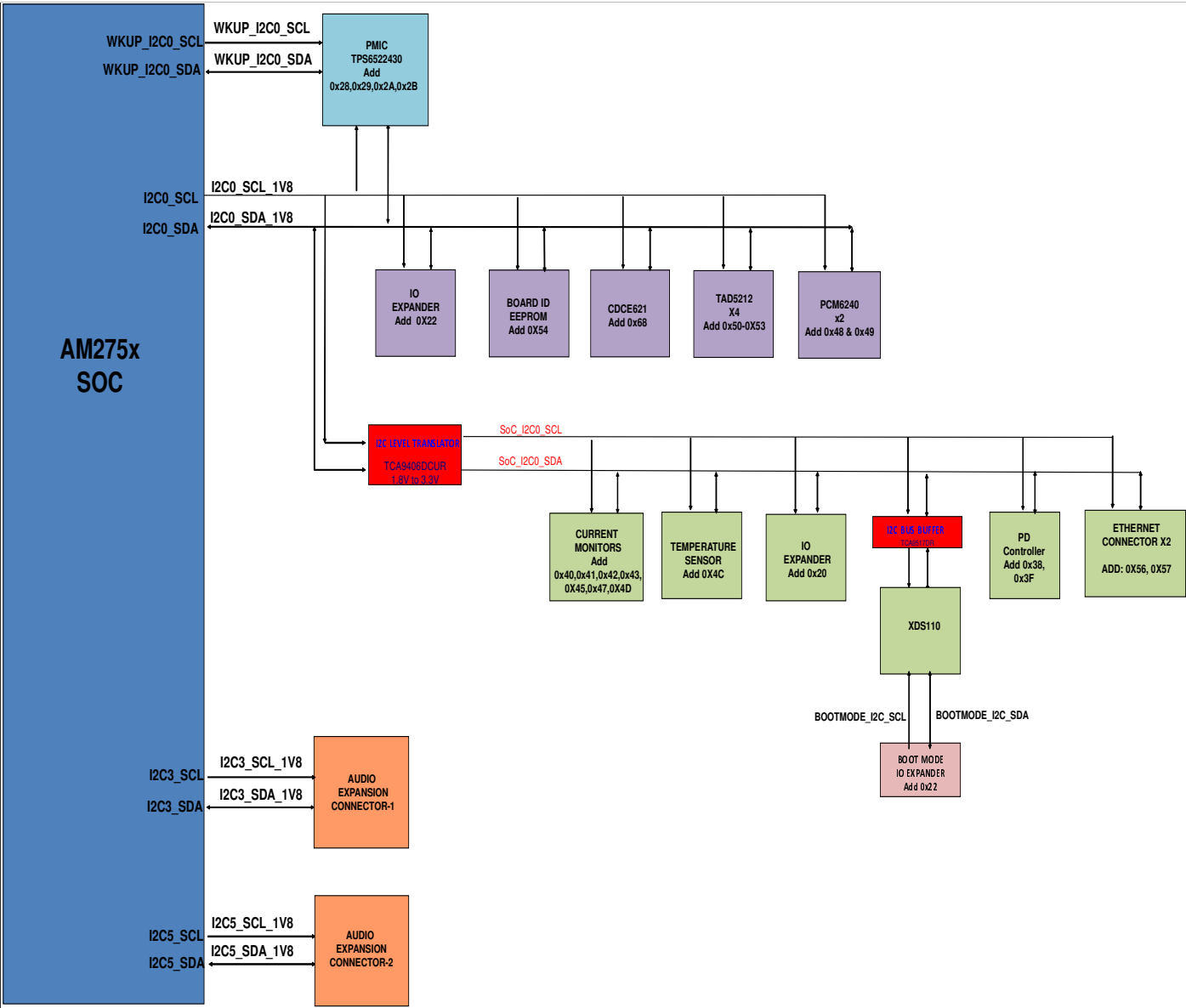
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Title POWER SEQUENCE		
Size	PROC190E1	Rev
C		E1
Date:	Thursday, September 05, 2024	Sheet 7 of 57

I2C TREE



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Title I2C TREE		
Size	PROC190E1	Rev
C		E1
Date:	Monday, September 02, 2024	Sheet 8 of 57

GPIO MAPPING TABLE

SL.No	GPIO DESCRIPTION	GPIO NETNAME	Functionality	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN	VOLTAGE RAIL CONNECTED
									ON SOC SIDE	ON KEVM
1	User_Test_LED_1	SOC_GPIO1_49	GPIO	GPIO1_38	MCASP1_AXR3	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD1V8
2	User_interrupt	GPIO_MCU_SoC_INTn	GPIO	MCU_GPIO0_2	MCU_GPIO0_2	INPUT	NA	NA	VDDSHV_MCU	SoC_DVDD1V8
3	PMIC SD/DDR voltage select, and EMMC/SD FET path select	VSEL_SD_SOC	VOLTAGE SELECTION	MCU_GPIO0_0	WKUP_TIMER_IO0	OUTPUT	NA	NA	VDDSHV_MCU	SoC_DVDD1V8
4	Push button IORET WAKE	IORET_WAKE	GPIO	MCU_GPIO0_16	MCU_GPIO0_16	INPUT	HIGH	LOW	VDDSHV_CANUART	SOC_VDDSHV_CANUART
5	AEC conn 1 GPIO_0	AEC1_GPIO0_0	GPIO	MCU_GPIO0_15	MCU_GPIO0_15	NA	NA	NA	VDDSHV_CANUART	SOC_VDDSHV_CANUART
6	AEC conn 1 GPIO_1	AEC1_GPIO0_1	GPIO	GPIO0_12	OSPI0_CSn1	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
7	For PMIC interrupt	MCU_INTn	Interrupt	GPIO1_29	I2C1_SDA	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD1V8
9	User Interrupt	GPIO1_23_INTn	INTERRUPT	MCU_GPIO0_1	WKUP_TIMER_IO1	INPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD1V8
	IO Expander Interrupt									
9	AEC conn 2 GPIO_0	AEC2_GPIO0_0	GPIO	MCU_GPIO0_4	MCU_GPIO0_4	NA	NA	NA	VDDSHV_MCU	SoC_DVDD1V8
10	AEC conn 2 GPIO_1	AEC2_GPIO0_1	GPIO	MCU_GPIO0_3	MCU_GPIO0_3	NA	NA	NA	VDDSHV_MCU	SoC_DVDD1V8
IO EXPANDER -01										
1	RGMII2_RST	GPIO_CPSW2_RST	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	LOW		VCC_3V3_SYS
2	RGMII1_RST	GPIO_CPSW1_RST	ENABLE	IO EXPANDER-P11		OUTPUT	HIGH	LOW		VCC_3V3_SYS
3	MMC0 FET selection	MMC0_FET_EN	Peripheral selection	IO EXPANDER-P02		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	McASP4 FET selection	McASP4_FET_SEL	Peripheral selection	IO EXPANDER-P03		OUTPUT	LOW	HIGH		VCC_3V3_SYS
5	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	ENABLE	IO EXPANDER-P05		INPUT	HIGH	LOW		VCC_3V3_SYS
6	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P12		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER -02										
1	PCM1 RESET	GPIO_PCM1_RST	ENABLE	IO EXPANDER-P20		OUTPUT	HIGH	LOW		VCC1V8_SYS
2	PCM2 RESET	GPIO_PCM2_RST	ENABLE	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC1V8_SYS
3	Test GPIO from the XDS IC	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC1V8_TA
4	Audio ext refclk2 selection	AUDIO_EXT_REFCLK2_S0	Clock selection	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC1V8_SYS
5	Audio ext refclk2 selection	AUDIO_EXT_REFCLK2_S1	Clock selection	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC1V8_SYS
6	AEC 1 & 2 connector refclk selection	AEC1_REFCLK_SEL	Clock selection	IO EXPANDER-P26		OUTPUT	HIGH	LOW		VCC1V8_SYS
7	AEC 1 & 2 connector refclk selection	AEC2_REFCLK_SEL	Clock selection	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC1V8_SYS
8	eMMC flash reset	GPIO_eMMC_RSTn	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	LOW		VCC1V8_SYS
9	TCAN1043A enable	IO_MCAN0_EN	ENABLE	IO EXPANDER-P11		OUTPUT	HIGH	LOW		VDDSHV_CANUART
10	TCAN1043A STB control	IO_MCAN0_STB#	MODE SELECTION	IO EXPANDER-P13		OUTPUT	HIGH	LOW		VDDSHV_CANUART
11	UART2 FET selection	UART2_FET_SEL	Peripheral selection	IO EXPANDER-P14		OUTPUT	LOW	HIGH		VCC1V8_SYS
12	UART3 FET selection	UART3_FET_SEL	Peripheral selection	IO EXPANDER-P15		OUTPUT	LOW	HIGH		VCC1V8_SYS
13	PCM6240_INT	PCM1_INT_1V8	INTERRUPT	IO EXPANDER-P16		INPUT	NA	HIGH		VCC1V8_SYS
14	PCM6240_INT	PCM2_INT_1V8	INTERRUPT	IO EXPANDER-P17		INPUT	NA	HIGH		VCC1V8_SYS
15	uSD interface voltage enable	MMC0_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	LOW		VCC1V8_SYS
16	VPP supply enable	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	LOW	HIGH		VCC1V8_SYS

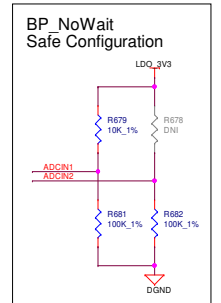
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Title GPIO MAPPING TABLE

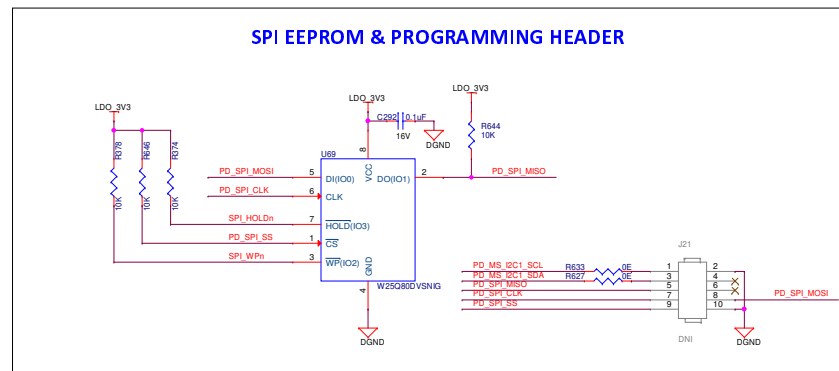
Size	PROC190E1	Rev	E1
C			
Date:	Monday, September 02, 2024	Sheet	9 of 57

TYPE-C DUAL PD CONTROLLER

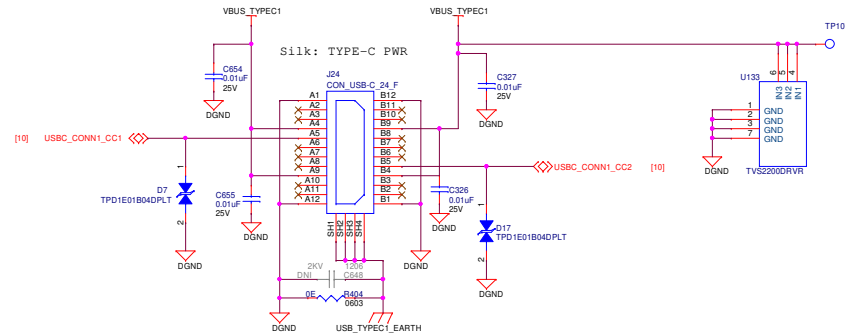


I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

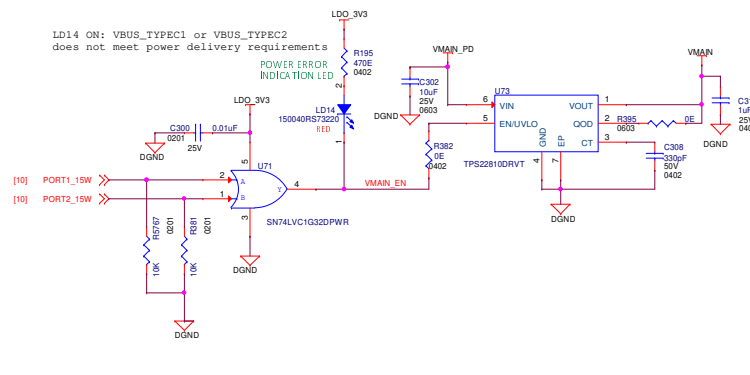
SPI EEPROM & PROGRAMMING HEADER



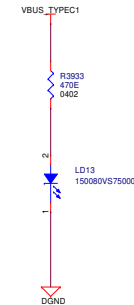
USB TYPE-C POWER CONNECTOR



LOAD SWITCH FOR VMAIN



POWER INDICATION LED: VBUS_TYPEC1



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Title USB TYPE-C POWER CONNECTOR

Size	Rev
C	E1
Date: Monday, September 02, 2024	Sheet 11 of 57

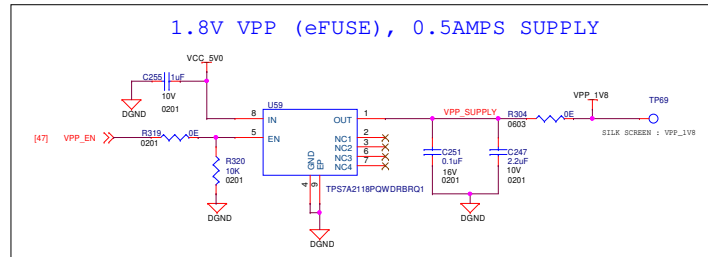
5V, 6.0 AMPS SUPPLY

[illegible]

TP1 TP2 TP77 TP40 TP85 TP42 TP44 TP4

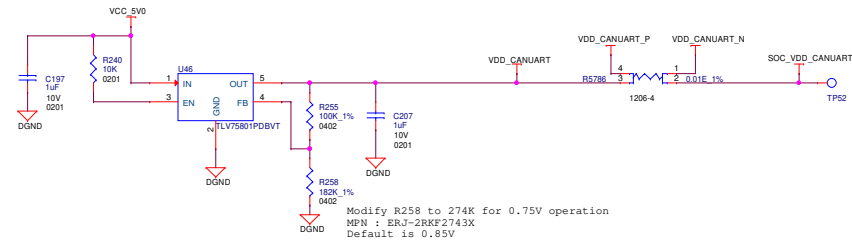
DGND DGND DGND DGND DGND DGND DGND DGND

PRE REGULATOR SUPPLY - LDOs

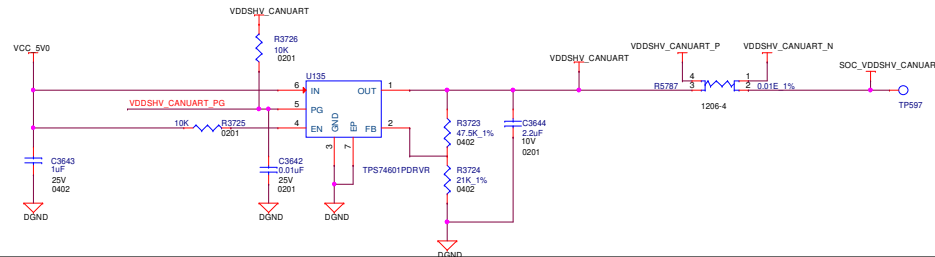


D-NOTE:U59 only needed for eFUSE ROM programming. If no OTP operation, VPP can be left unconnected.

VDD_CANUART (0.85V), 0.5 AMPS SUPPLY



VDDSHV_CANUART (1.8V), 1 AMPS SUPPLY



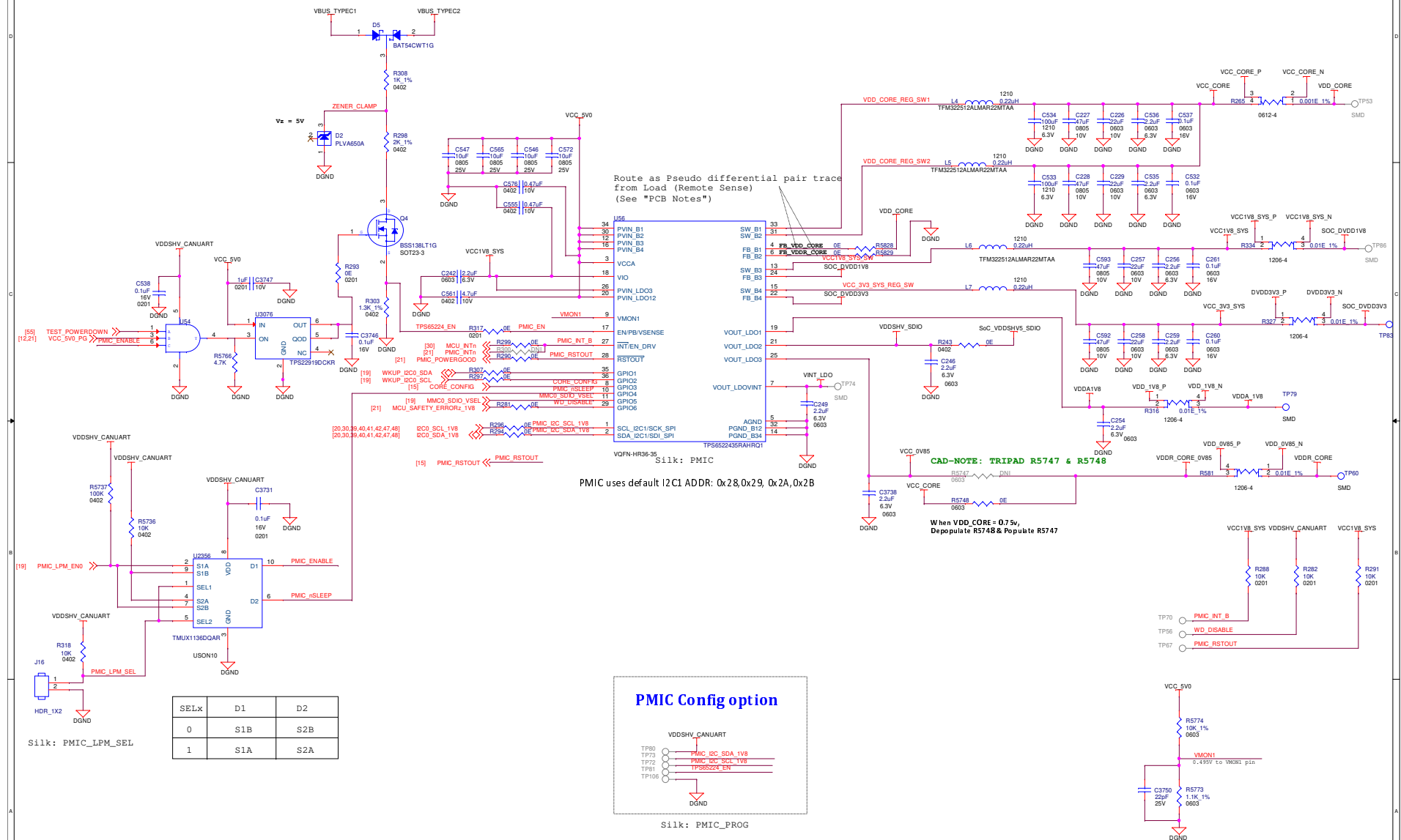
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Title SOC POWER SUPPLIES - LDOs & VCC_3V3_SYS LOAD SWITCH

Size	Rev
C	PROC190E1
Date:	Monday, September 02, 2024
Sheet	13 of 57

SOC POWER SUPPLY PMIC - 1



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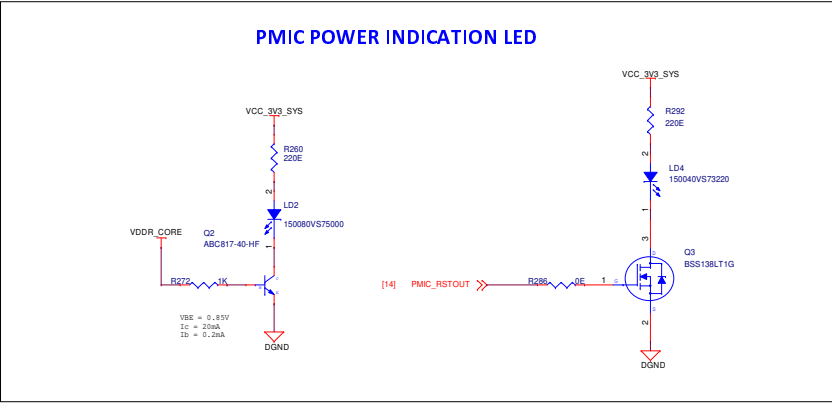


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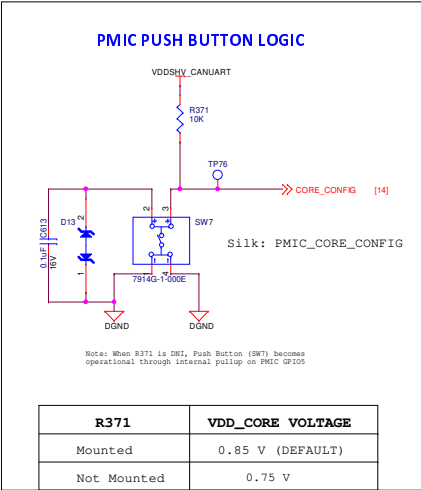
Size	PROC190E1	Rev	
C		E1	
Date:	Monday, September 02, 2024	Sheet	14 of 57

SOC POWER SUPPLY PMIC - 2

PMIC POWER INDICATION LED

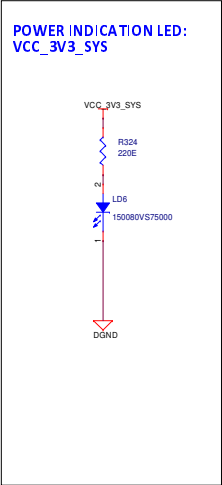


PMIC PUSH BUTTON LOGIC



R371	VDD_CORE VOLTAGE
Mounted	0.85 V (DEFAULT)
Not Mounted	0.75 V

POWER INDICATION LED:
VCC_3V3_SYS



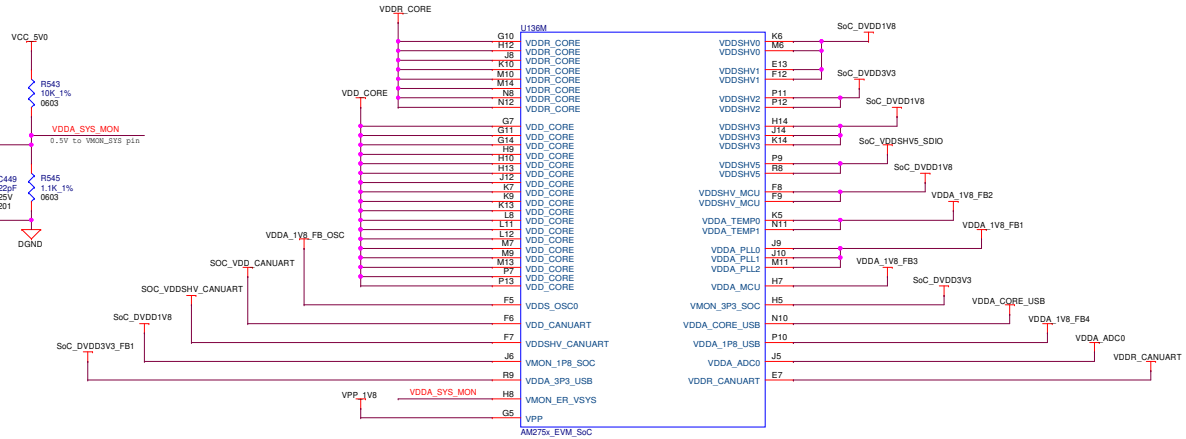
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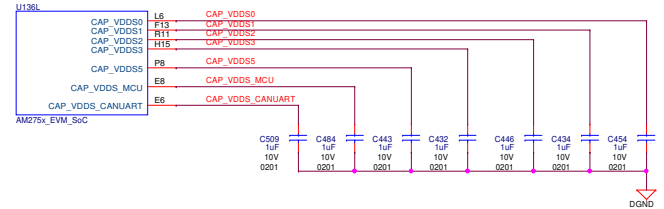
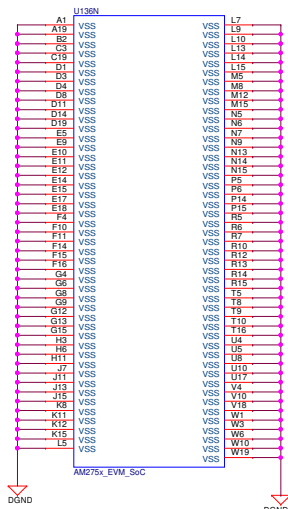
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Size	PROC190E1	Rev
C		E1
Date:	Monday, September 02, 2024	Sheet 15 of 57

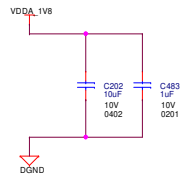
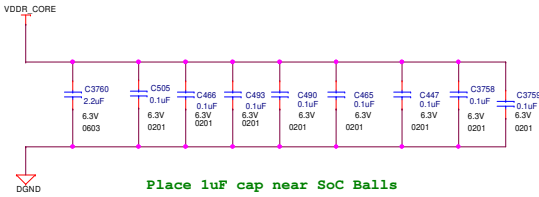
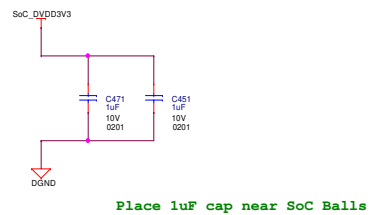
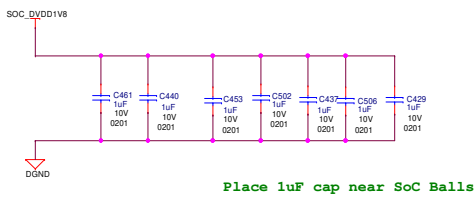
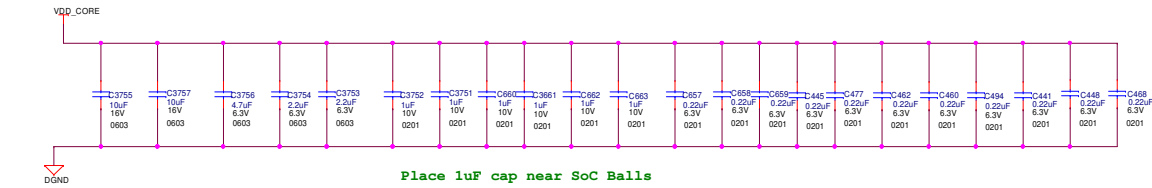
SOC POWER SUPPLIES AND SUPPLY RAILS



SOC VSS

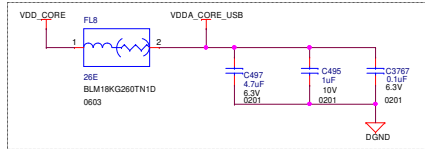


SOC POWER SUPPLIES - DECAPS 1

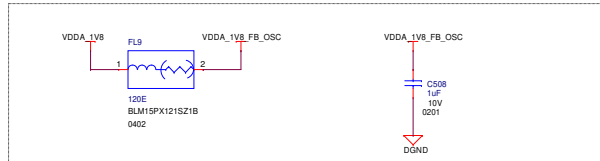


SOC POWER SUPPLIES - DECAPS 2

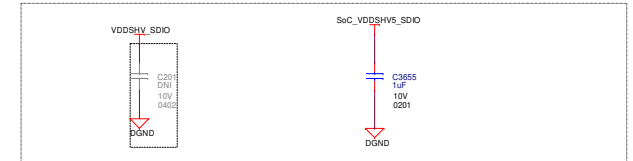
Peripherals - Core SUPPLY



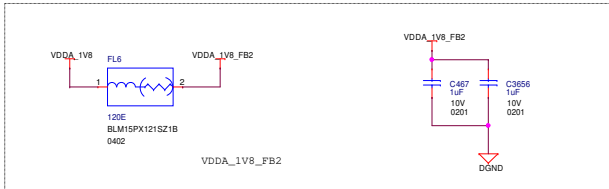
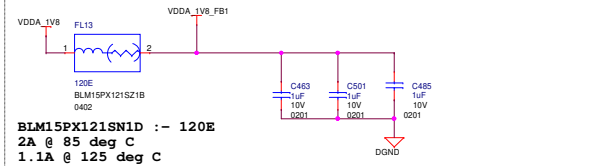
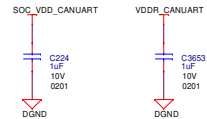
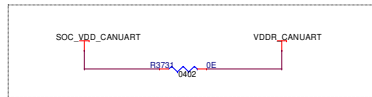
Peripherals - 1.8V Analog SUPPLY



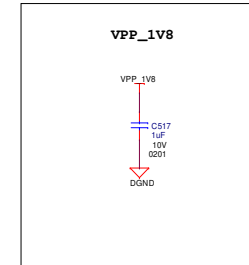
3.3V/1.8V MMC0 SUPPLY



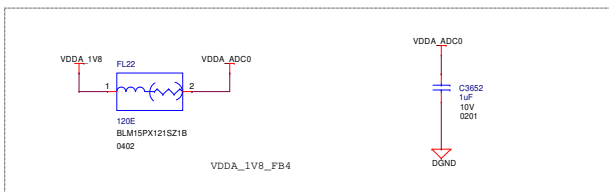
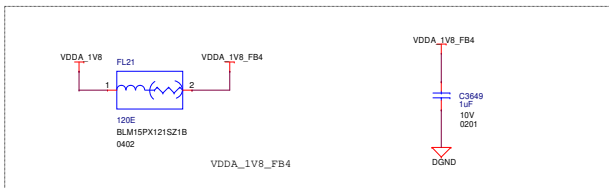
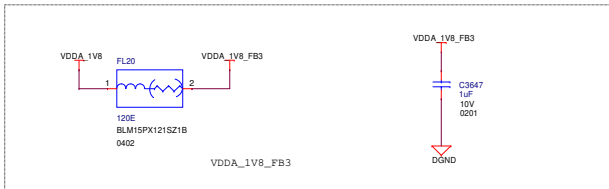
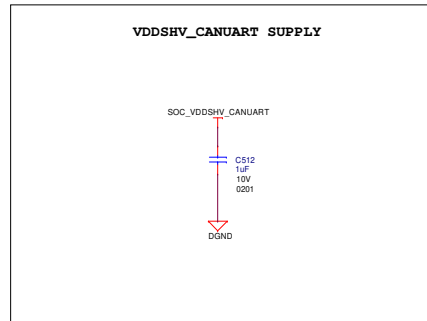
VDDR_CANUART SUPPLY



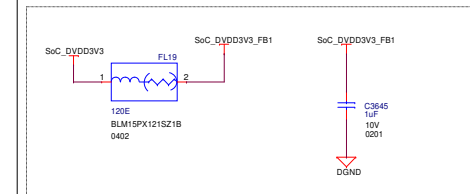
VPP_1V8



VDDSHV_CANUART SUPPLY



Peripherals - 3.3V Analog SUPPLY



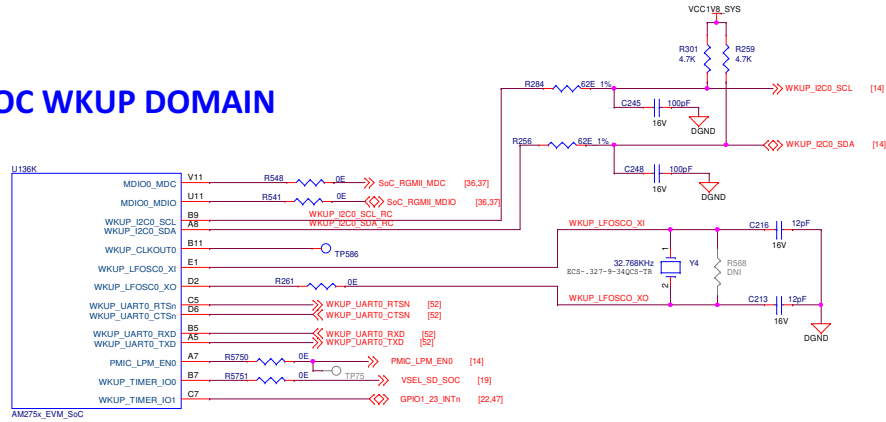
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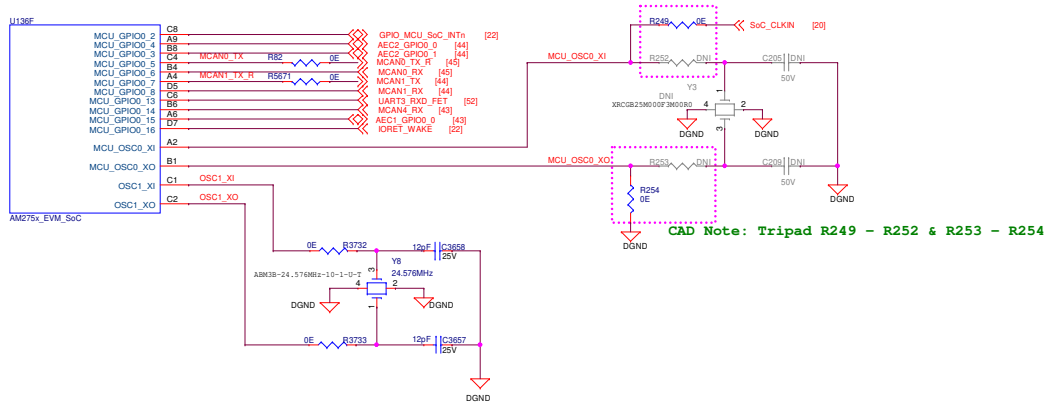
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Size	Rev
C	PROC190E1
Date:	Monday, September 02, 2024
Sheet	18 of 57

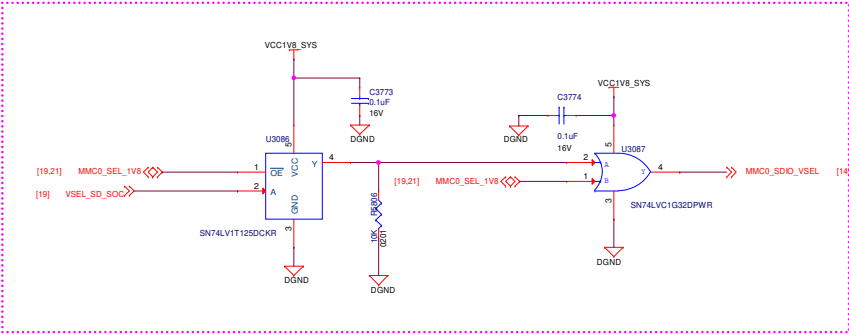
SOC WKUP DOMAIN



SOC GPIO



CAD Note: Tripad R249 - R252 & R253 - R254



MMC0_SEL_1V8	VSEL_SD_SOC	MMC0_SDIO_VSEL	VDDSHV_SDIO	
0	0	0	3V3	3V3 IO routed to uSD
0	1	1	1V8	1V8 IO routed to uSD
1 (DEFAULT)	X	1	1V8	1V8 IO routed to EMMC

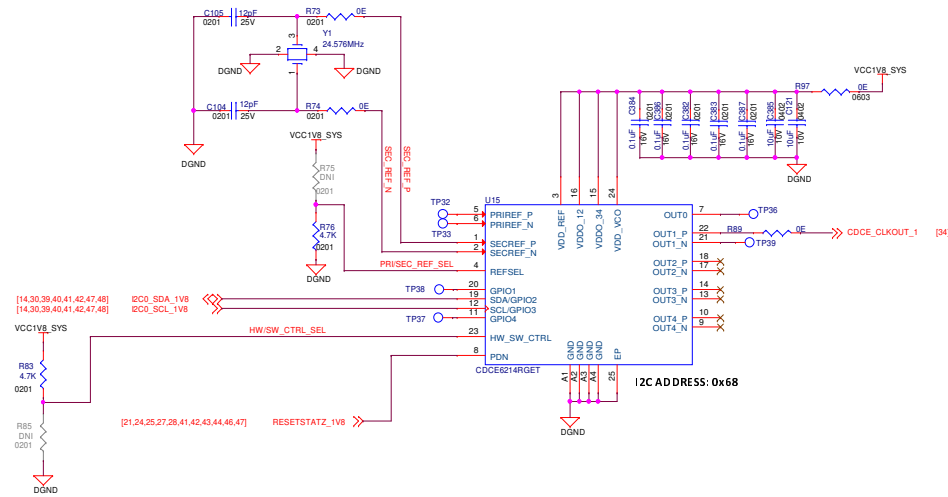
Designed for TI by Mistral Solutions Pvt Ltd



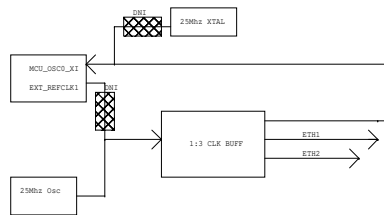
Title SOC WKUP & CLOCK

Size	PROC190E1	Rev
C		E1
Date:	Monday, September 02, 2024	Sheet 19 of 57

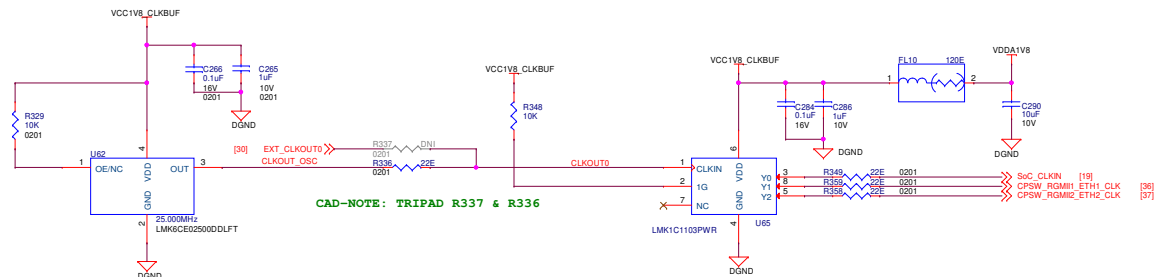
CDCE CLOCK GENERATION



OSCILLATOR



SOC & ETHERNET PHY CLOCK BUFFER



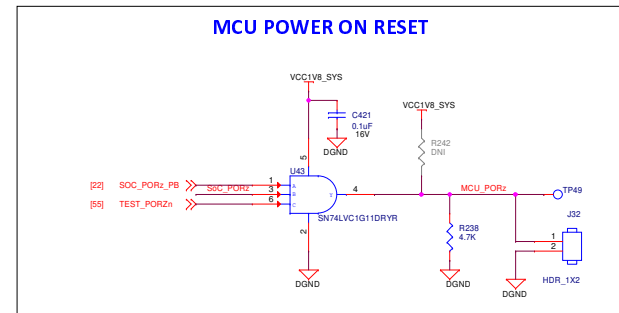
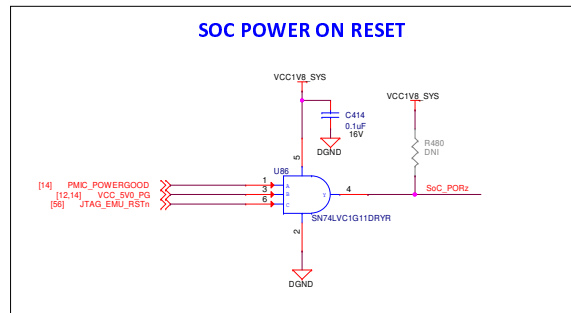
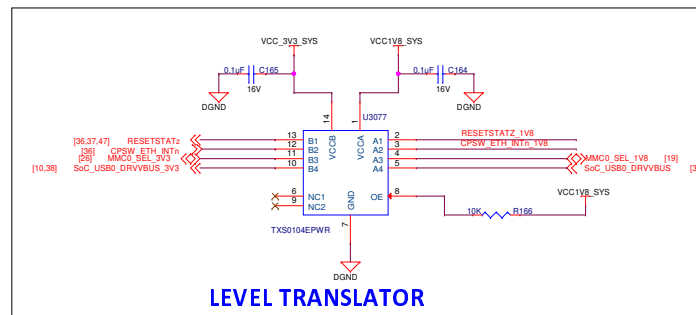
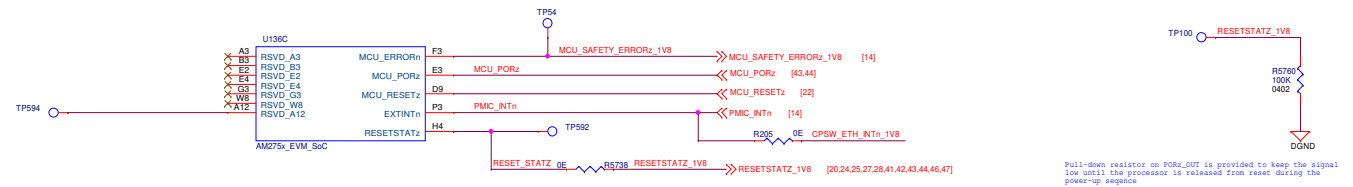
Designed for TI by Mistral Solutions Pvt Ltd



Title CDCE CLOCK GENERATION

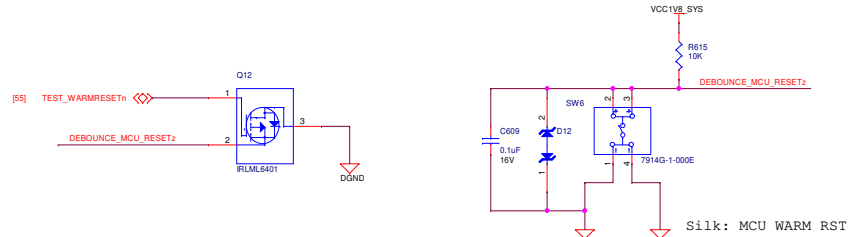
Size	Rev
C	PROC190E1
Date:	Monday, September 02, 2024
Sheet	20 of 57

SOC - RESET

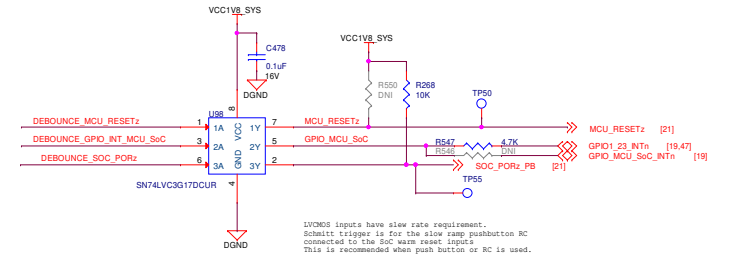


SOC RESET - 2

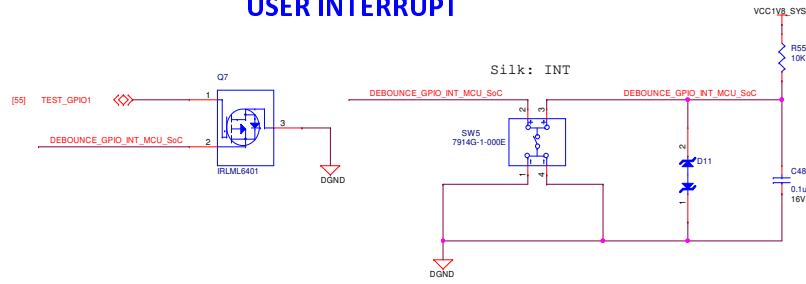
MCU WARM RESET



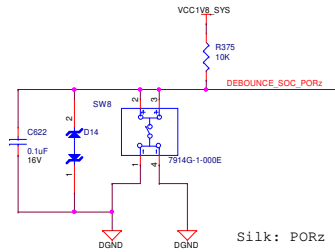
RESET & INT DEBOUNCE CIRCUIT



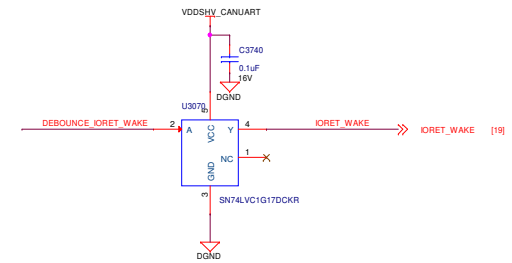
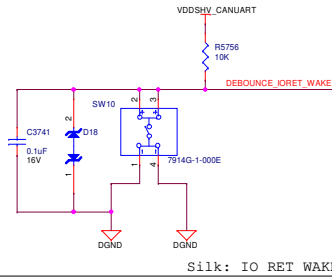
USER INTERRUPT



SOC PORz



IO RET WAKE



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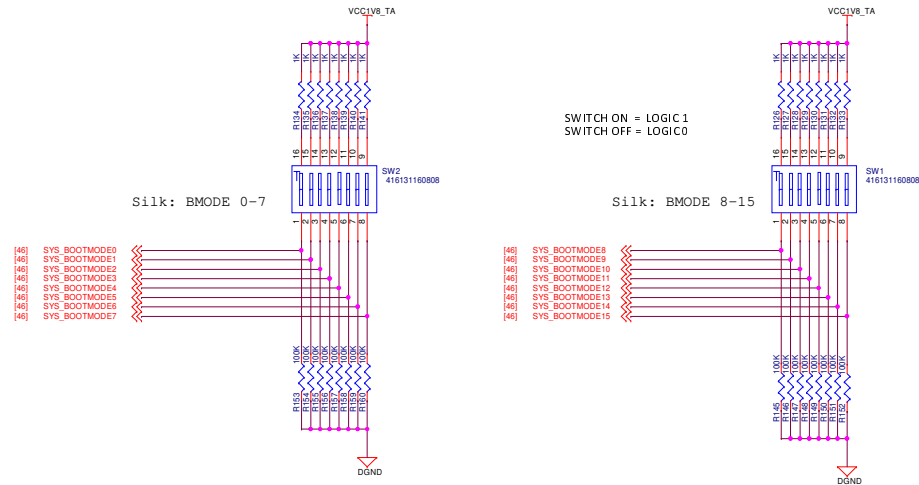
Title SOC RESET - 2

Size	Rev
C	PROC190E1
Date:	Monday, September 02, 2024

Sheet 22 of 57

BOOT MODE SWITCHES

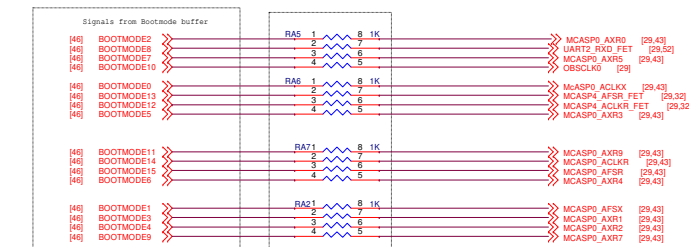
D-Note: VCC1V8_TA supply is used for test automation.
Connect SOC_VDD01V8 in the custom board design when buffers are not used



BOOT MODES SUPPORTED

1. OSPI
2. MMC0 - SD CARD
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. USB0 MS

BOOTMODE PINS



D-Note :
Connect SIG_BOOTMODE signals when
bootmode buffers are not used

D-NOTE:

1. 1K Resistor at the output of the buffer is recommended when the bootmode pins are used for alternate functions
2. Replace 1K Resistor at the output of the buffer with resistor of value 0E when bootmode buffers are not used

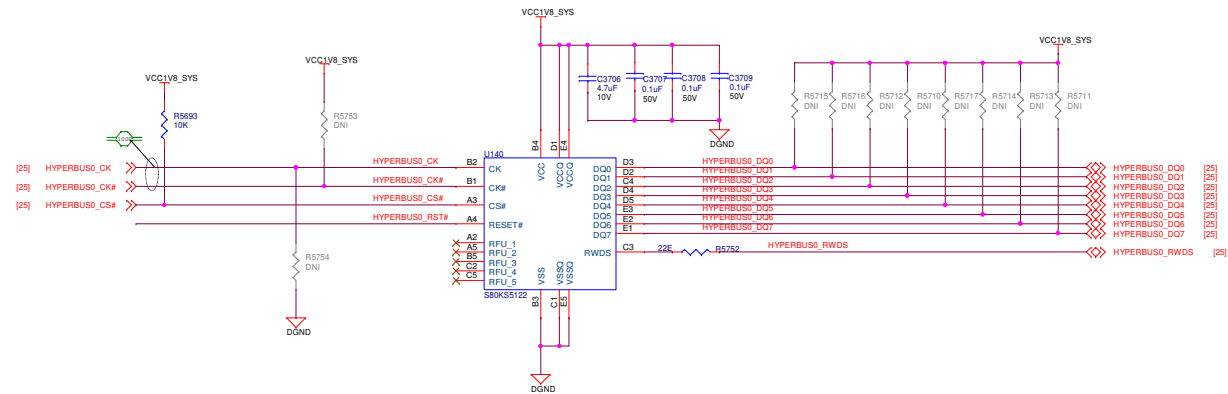
Designed for TI by Mistral Solutions Pvt Ltd



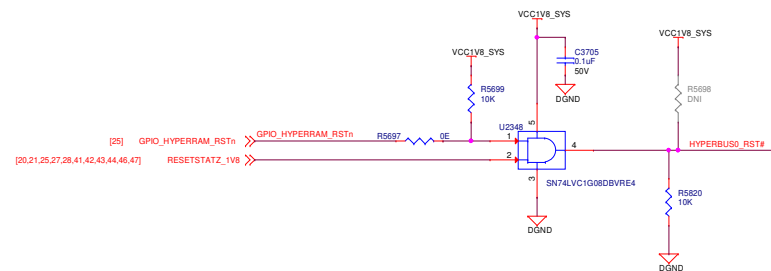
Title BOOT MODE SWITCHES

Size	Rev
C	E1
Date: Monday, September 02, 2024	Sheet 23 of 57

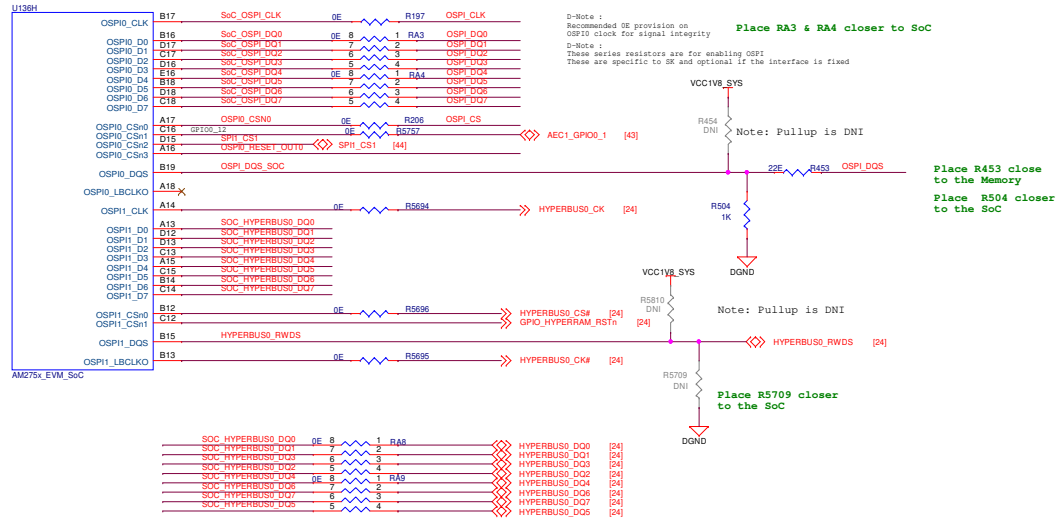
HYPERRAM DEVICE



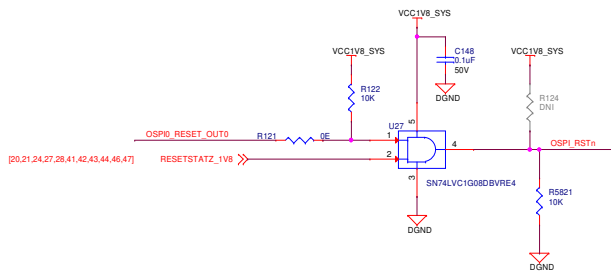
HYPERRAM RESET



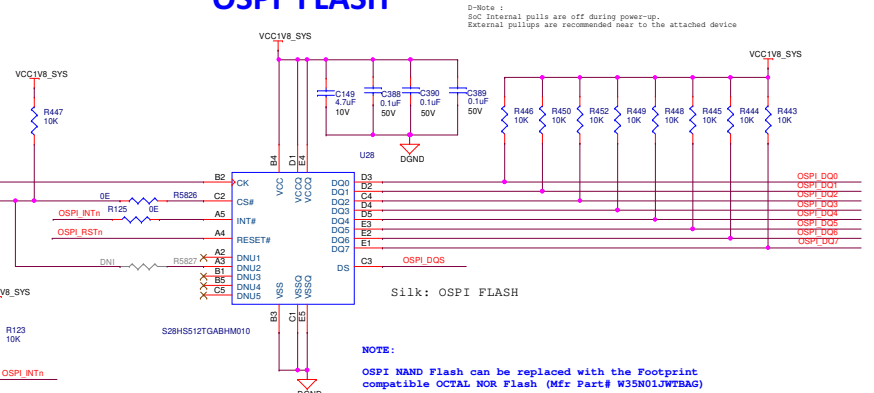
OSPI INTERFACE



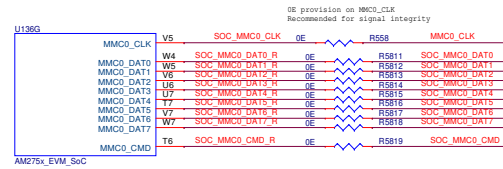
OSPI FLASH RESET



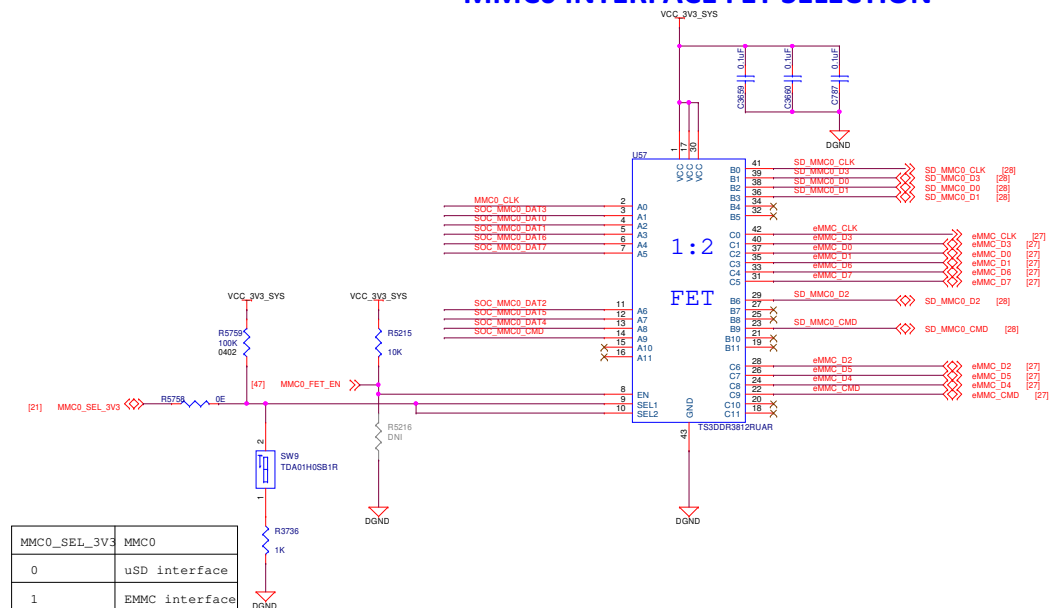
OSPI FLASH



MMIO INTERFACE

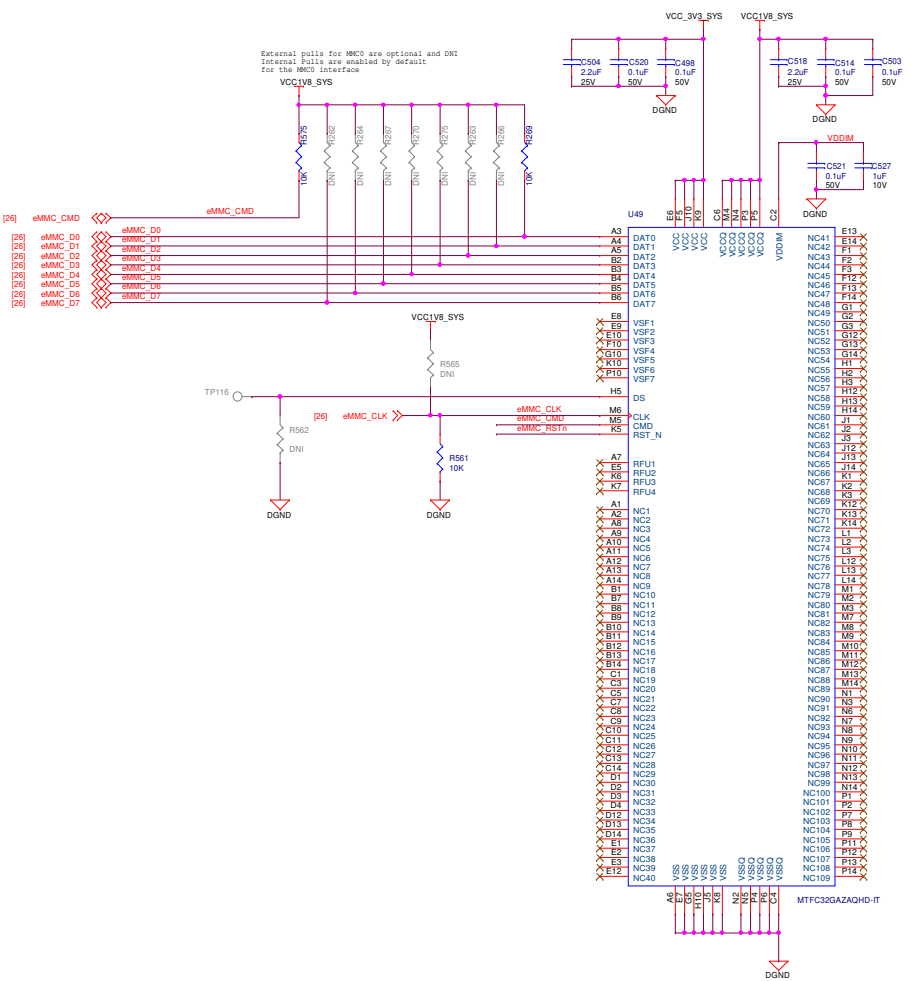
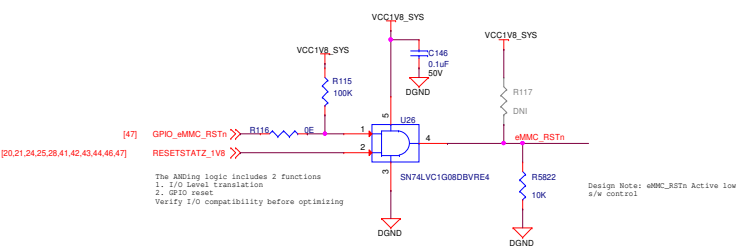


MMCO INTERFACE FET SELECTION



eMMC FLASH

eMMC FLASH RESET

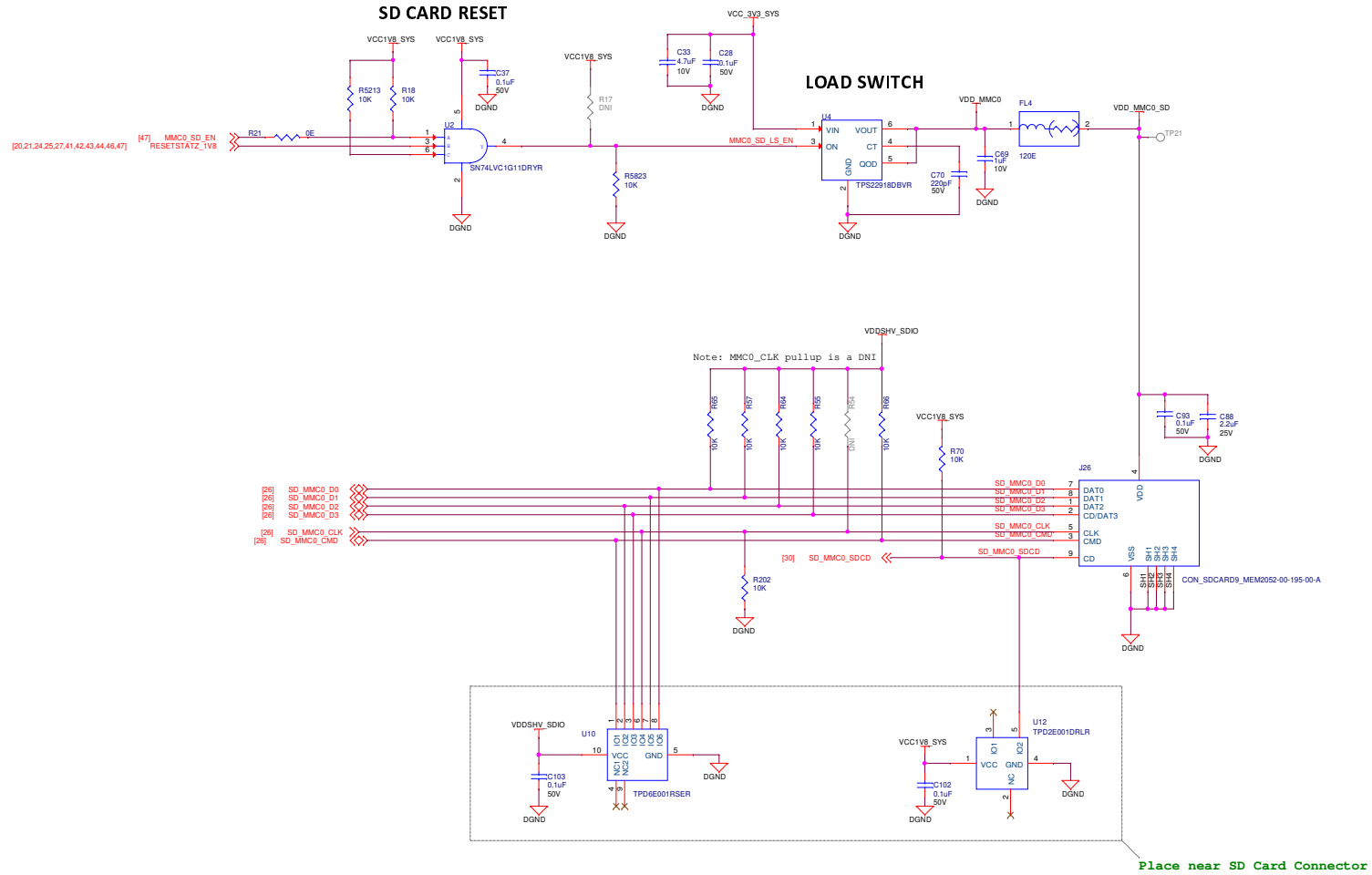


Designed for TI by Mistral Solutions Pvt Ltd



Title eMMC FLASH AND RESET		
Size	PROC190E1	Rev
C		E1
Date:	Monday, September 02, 2024	Sheet 27 of 57

SD CARD INTERFACE



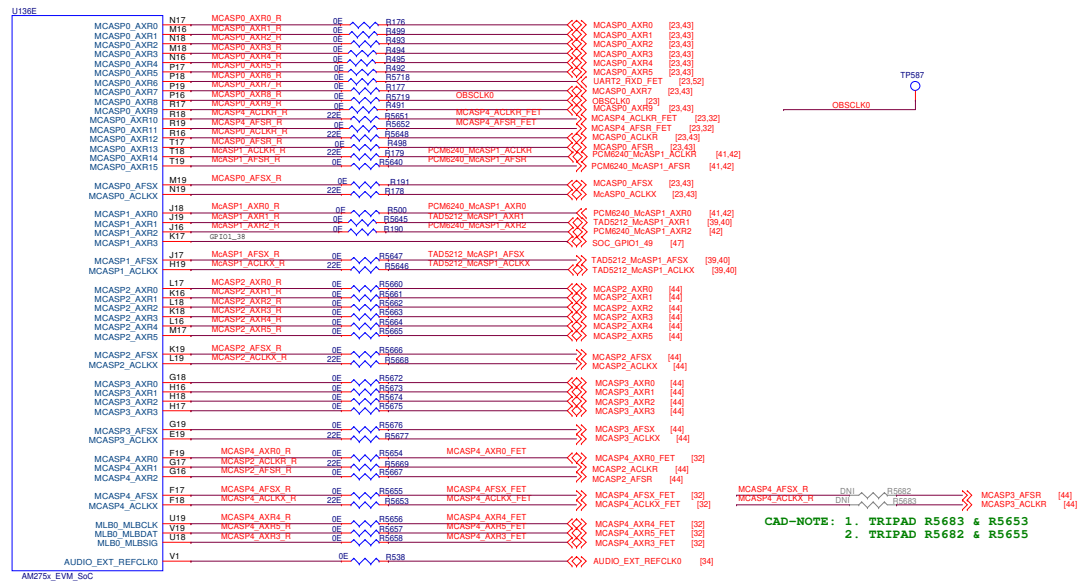
Place near SD Card Connector

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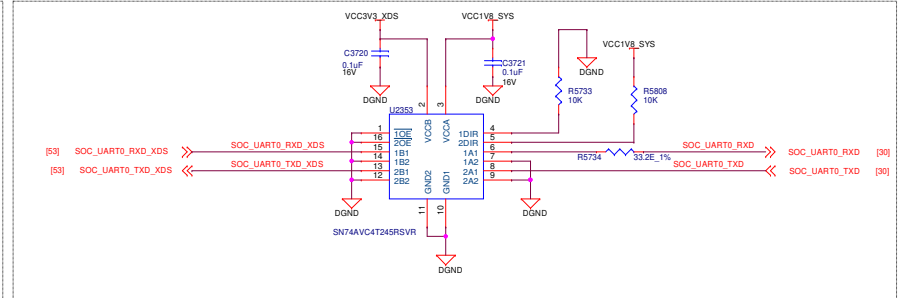
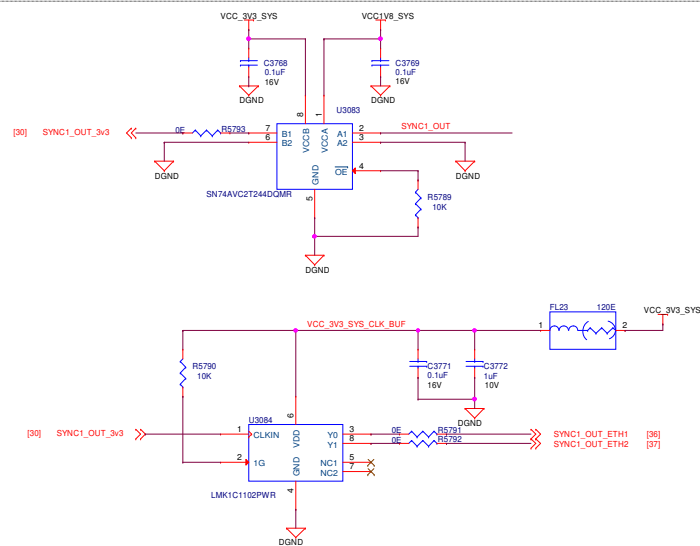
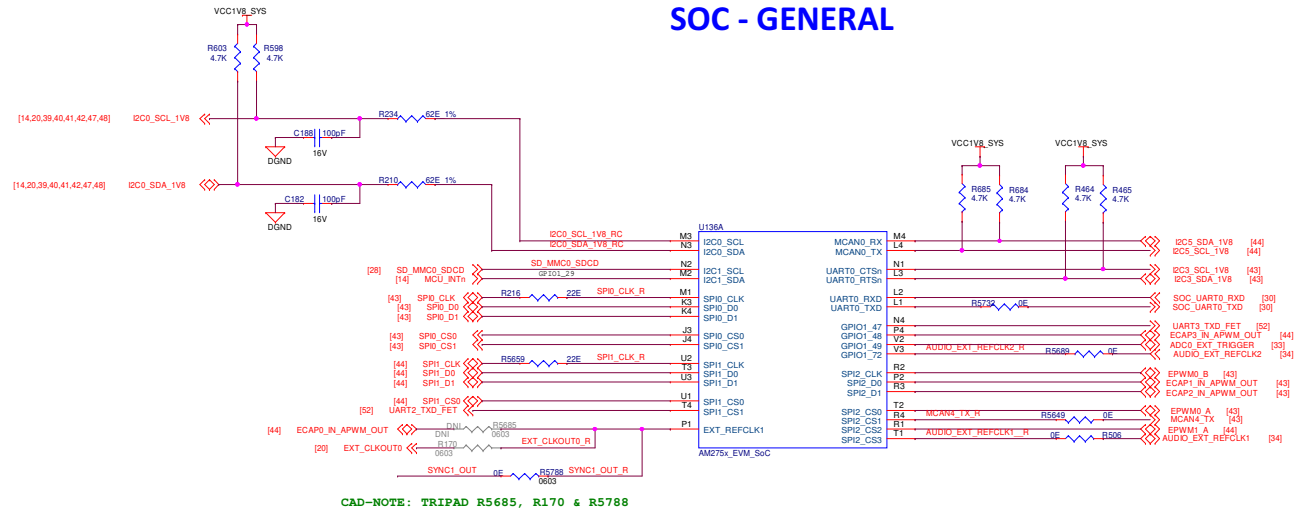


Title					SD CARD INTERFACE				
Size		PROC190E1						Rev	
C								E1	
Date:			Monday, September 02, 2024			Sheet		28 of 57	

SOC McASP



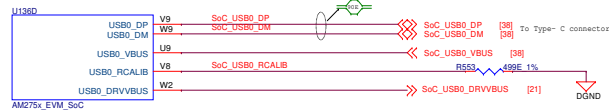
SOC - GENERAL



SOC CPSW3G ETHERNET INTERFACE



SOC - USB



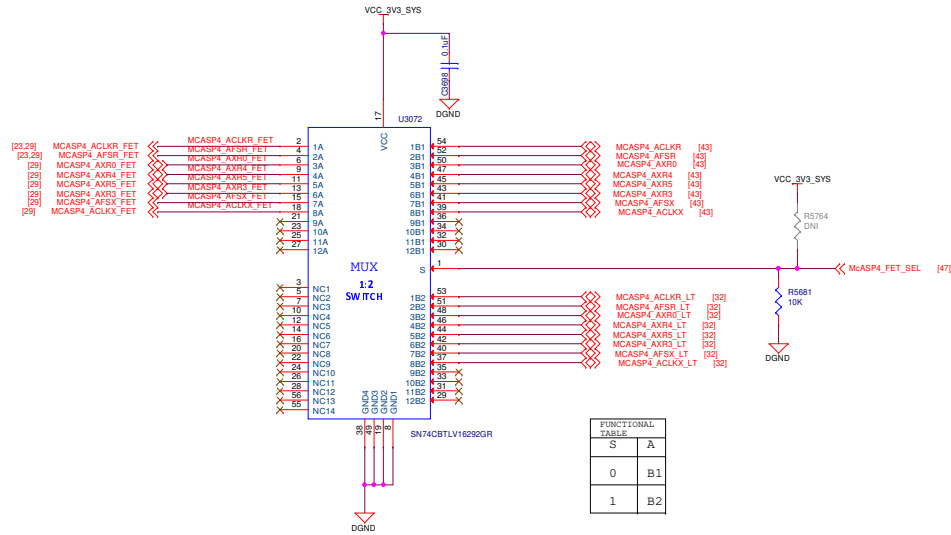
Designed for TI by Mistral Solutions Pvt Ltd



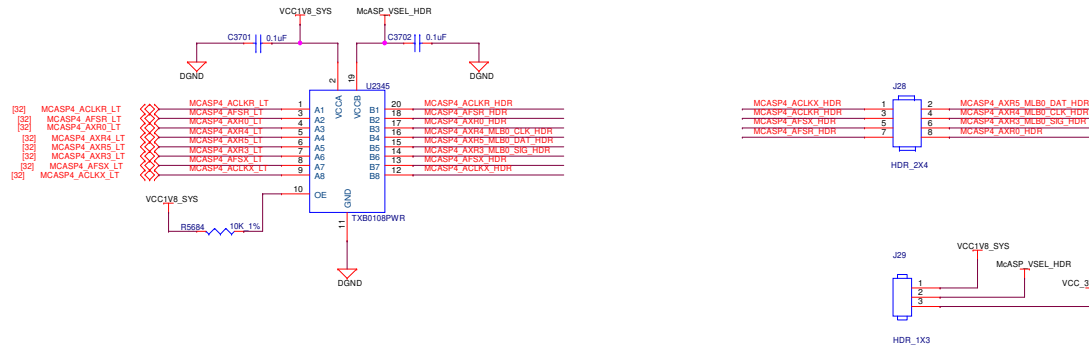
Title SOC PERIPHERALS 3

Size	Rev
C	PROC190E1
Date:	Monday, September 02, 2024
Sheet	31 of 57

McASP4 FET SELECTION



FUNCTIONAL TABLE	
S	A
0	B1
1	B2



McASP HEADER 3.3/1.8 VOLTAGE SELECTION

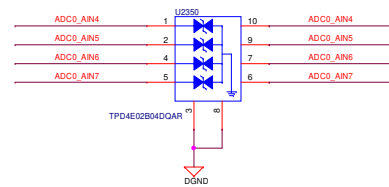
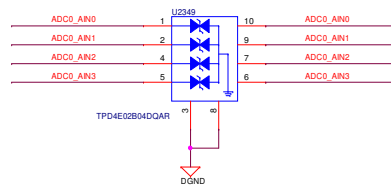
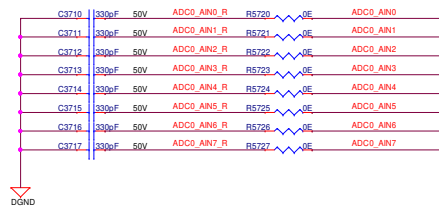
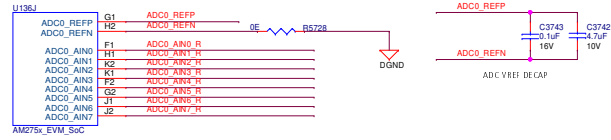
Designed for TI by Mistral Solutions Pvt Ltd



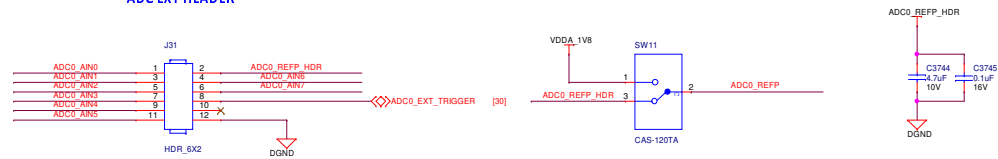
Title: McASP4 FET SELECTION & MLB HEADER

Size	Rev
C	PROC190E1
Date:	Monday, September 02, 2024
Sheet	32 of 57

SOC ADC



ADC EXT HEADER



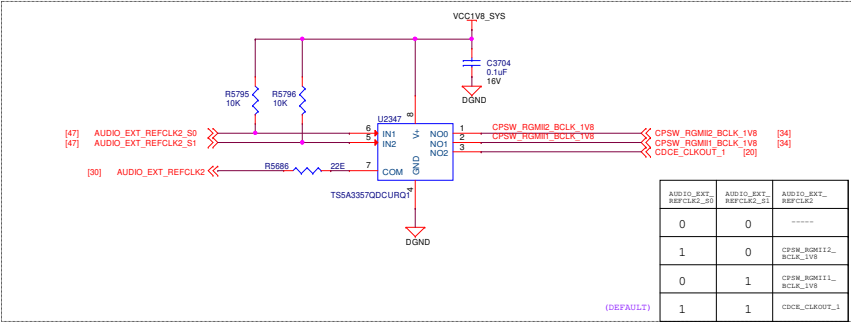
Designed for TI by Mistral Solutions Pvt Ltd



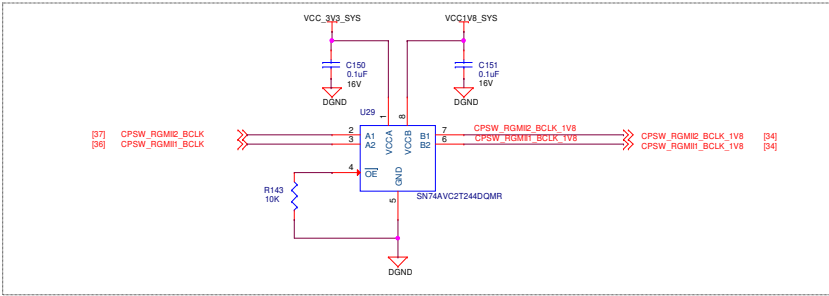
Title Soc ADC0 INTERFACE AND HEADER

Size	Rev
C	PROC190E1
Date:	Monday, September 02, 2024
Sheet	33 of 57

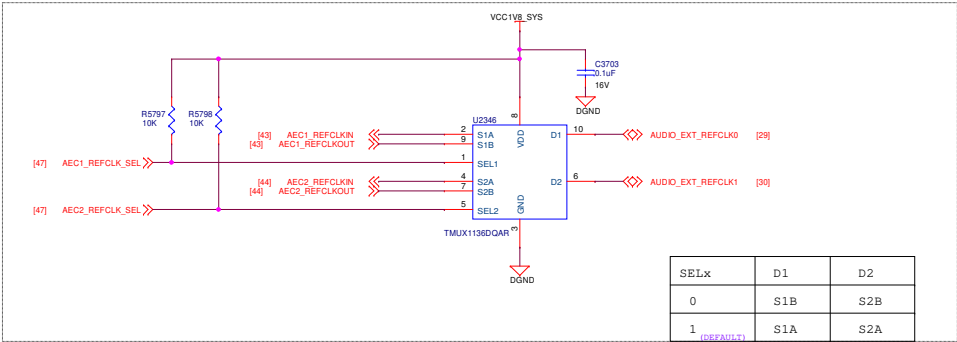
AUDIO_EXT_REFCLK2_SELECTION



ETHERNET_BCLK LEVEL TRANSLATOR



AUDIO EXPANSION REFCLK



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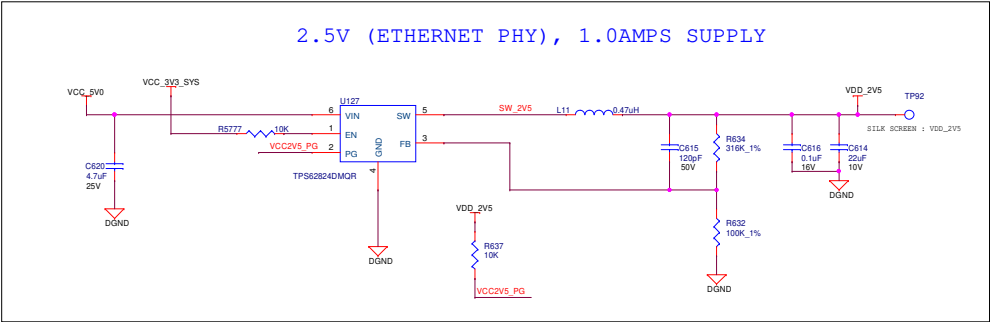


Title AUDIO REFERENCE CLOCK

Size	PROC190E1	Rev
C		E1

Date: Monday, September 02, 2024 Sheet 34 of 57

POWER SUPPLY (CORE) FOR ETHERNET PHY



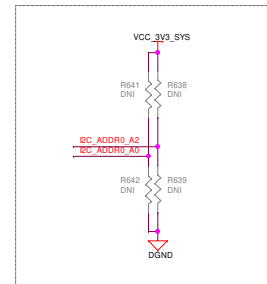
Designed for TI by Mistral Solutions Pvt Ltd



Title ETHERNET PHY POWER SUPPLY

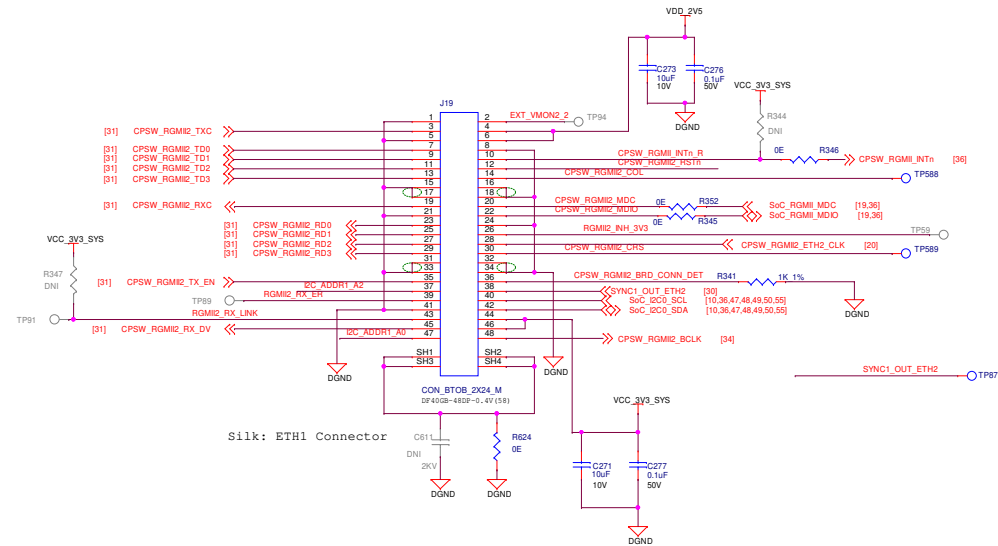
Size	PROC190E1	Rev
C		E1
Date:	Monday, September 02, 2024	Sheet 35 of 57

A vertical bar divided into four segments labeled A, B, C, and D from bottom to top. Segment B contains a right-pointing arrow.

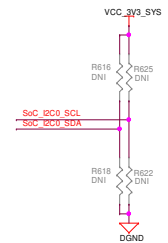
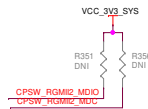
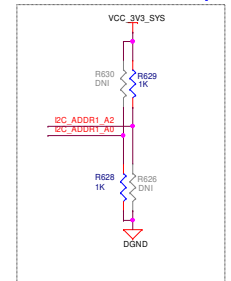


A B

ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 2

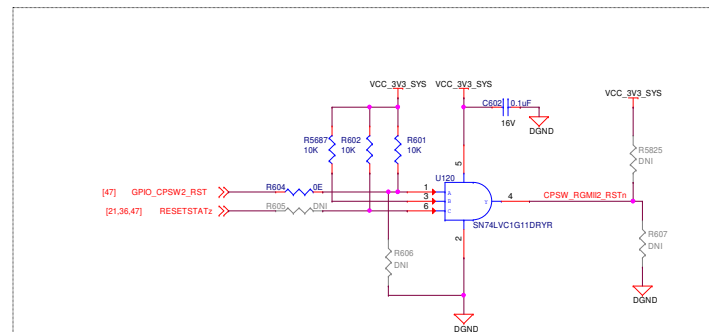


I2C Address Strap



CAD Note: Thevenin's termination should be placed at the J19 Connector

CPSW3G RGMII 2 RESET



Note: Verify the resistor mounting configuration for resistors that are marked as DNI

Designed for TI by Mistral Solutions Pvt Ltd

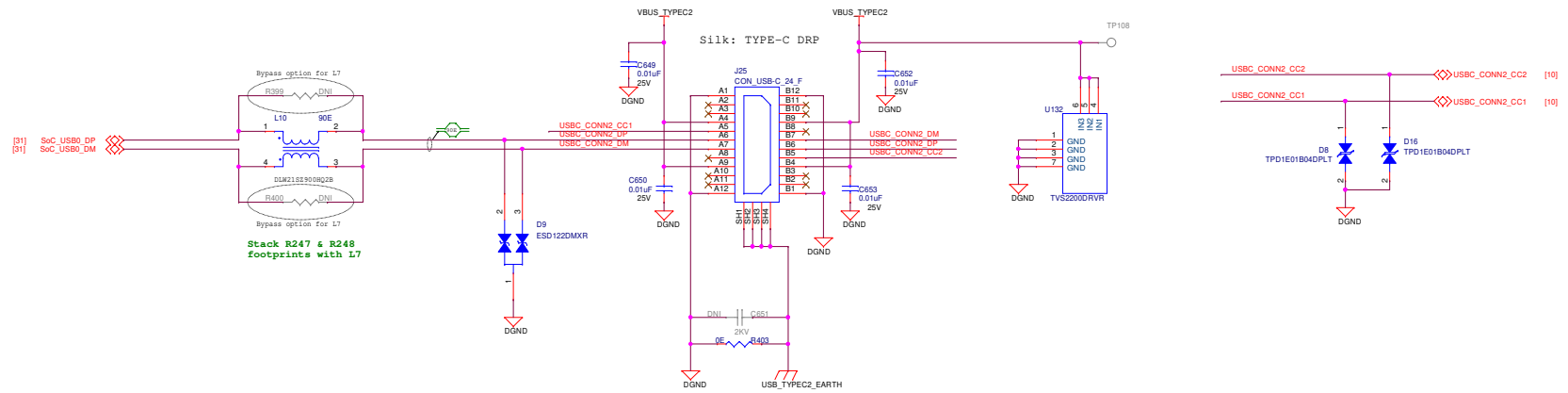


Title: ETHERNET EXPANSION CONNECTOR CPSW3G RGMII 2

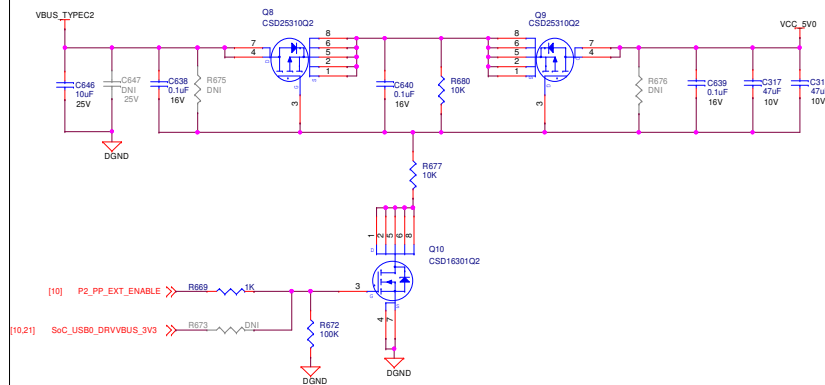
Size	Rev
C	PROC190E1
Date:	Monday, September 02, 2024

Sheet 37 of 57

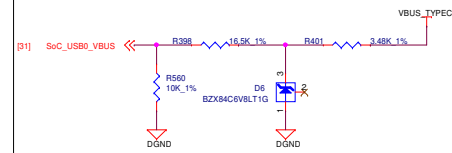
USB0 TYPE-C DRP



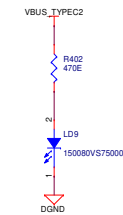
EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



Note: Refer data sheet USB VBUS Design Guidelines section.

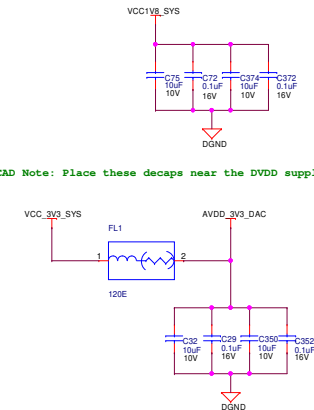


POWER INDICATION LED: VBUS_TYPEC2



[illegible]

CAD Note: Place these decaps near the DVDD supply pin of DAC's



CAD Note: Place these decaps near the AVDD supply pin of DAC's

[illegible]

CAD Note: Place these decaps near the DVDD supply pin of DAC's

[illegible][illegible]

I2C address selection device 1

VCC_I2V8_IOVDD

R23 DNI

R20 DNI

PCM1_ADDR_1

PCM1_ADDR_0

R22 10K

R26 10K

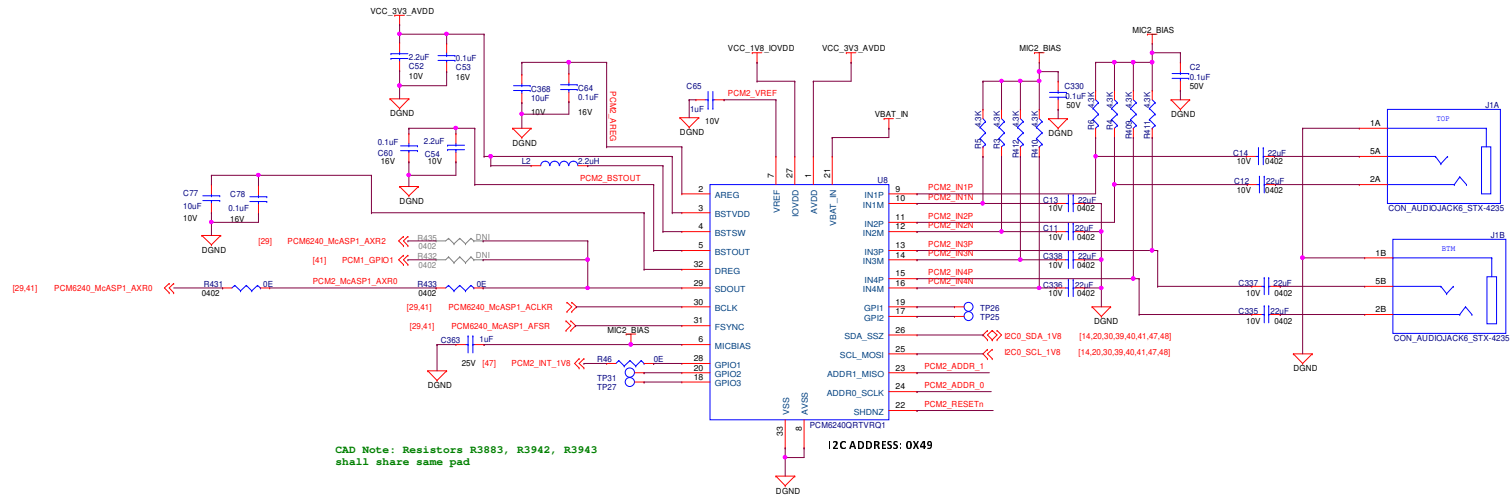
GND



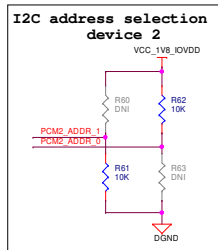
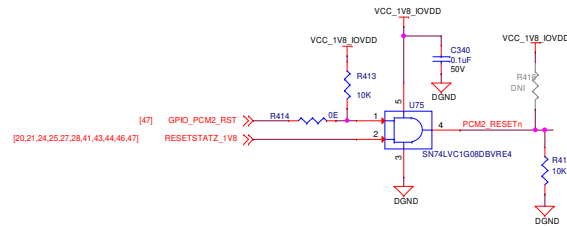
TEXAS
INSTRUMENTS

Sheet 41 of 57

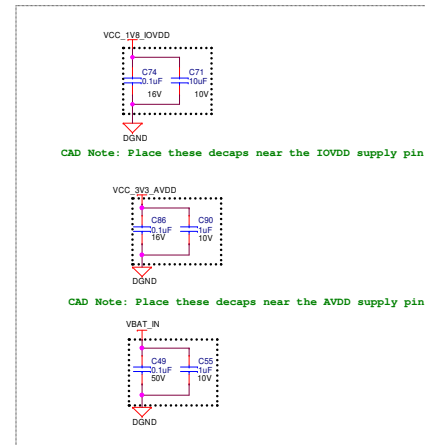
AUDIO - MICROPHONE/LINE IN 2



PCM2 RESET



ADC Supply & Decaps



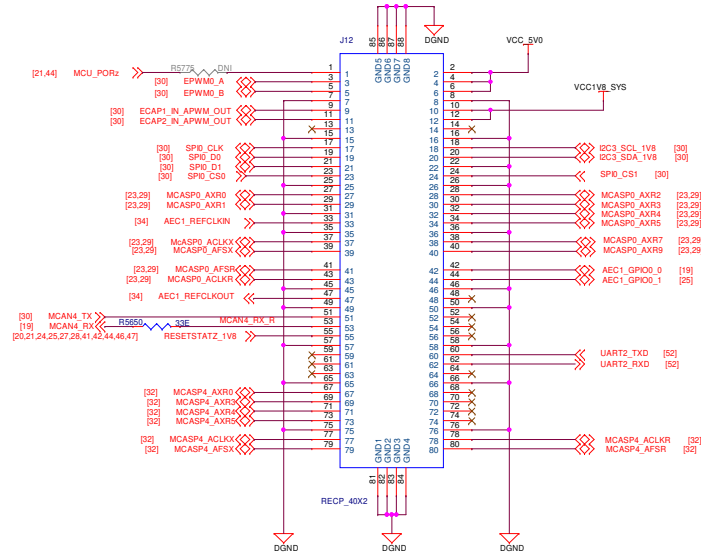
Designed for TI by Mistral Solutions Pvt Ltd



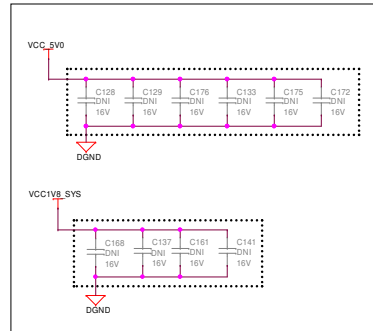
Title AUDIO - MICROPHONE/LINE IN 2

Size	PROC190E1	Rev
C		E1
Date:	Monday, September 02, 2024	Sheet 42 of 57

AUDIO EXPANSION CONNECTOR #1



AUDIO EXPANSION DECAPS



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Title AUDIO EXPANSION CONNECTOR #1

Size	Rev
C	PROC190E1
Date:	Monday, September 02, 2024
Sheet	43 of 57



TEXAS
INSTRUMENTS

Title	AUDIO EXPANSION CONNECTOR #2
-------	------------------------------

Size	
------	--

C	PROC190E1
Date:	Monday, September 02, 2024

Sheet 44 of 57

Rev

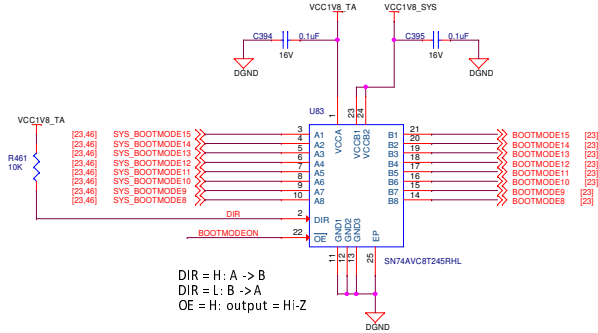
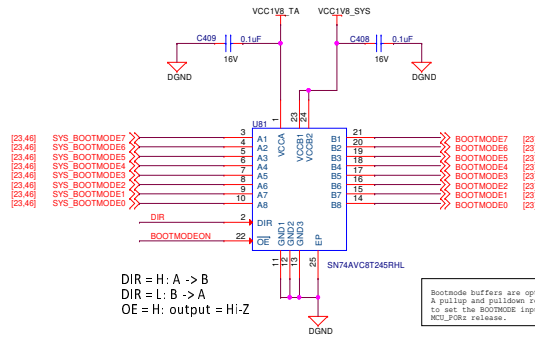
A vertical bar divided into four segments labeled A, B, C, and D from bottom to top. Segment B contains a right-pointing arrow.



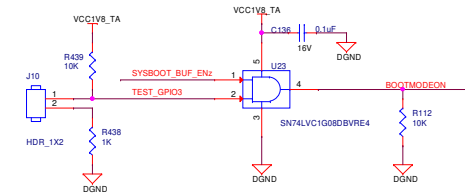
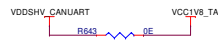
Size	PROC190E1	Rev
C		E1
Date:	Monday, September 02, 2024	Sheet 45 of 57

BOOTMODE BUFFERS AND IO EXPANDERS

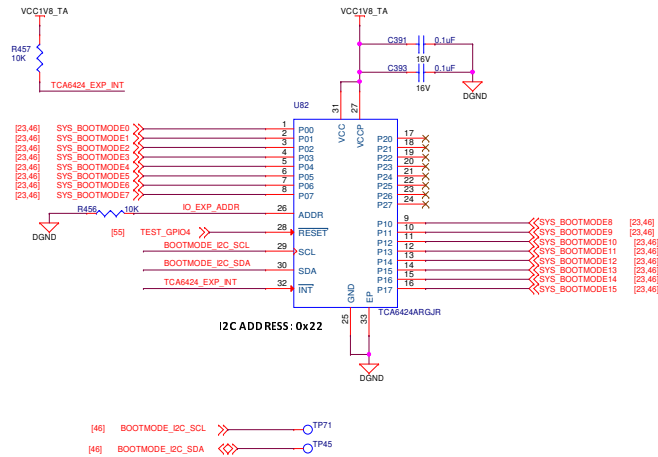
BOOT MODE BUFFERS



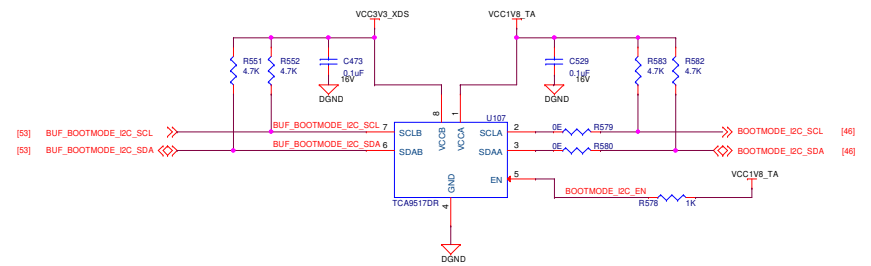
TEST AUTOMATION SUPPLY



BOOTMODE IO EXPANDER



BOOTMODE I2C BUS BUFFER



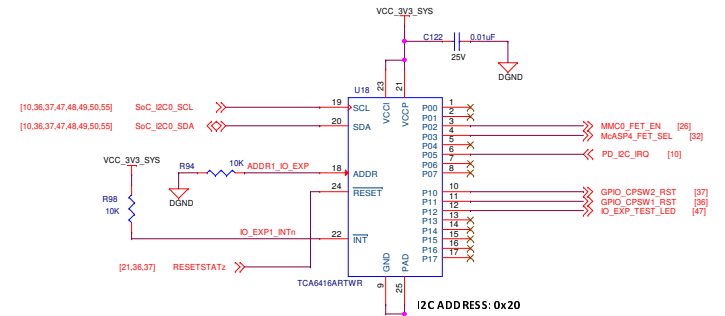
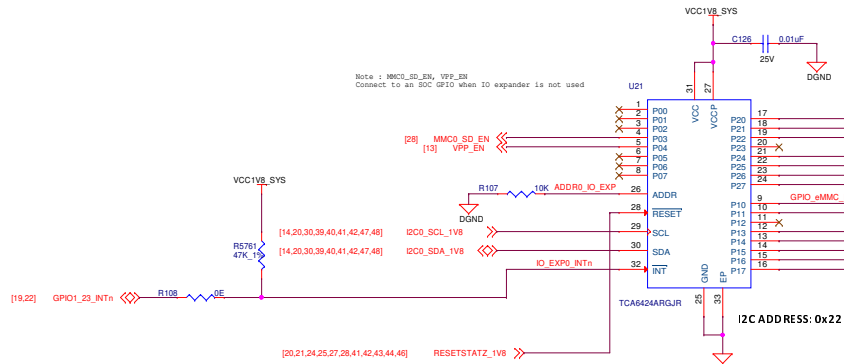
Designed for TI by Mistral Solutions Pvt Ltd



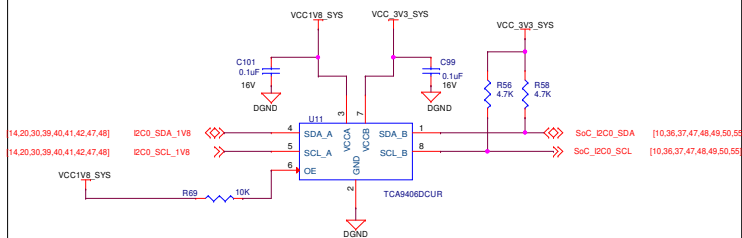
Title BOOT MODE BUFFER & IO EXPANDERS

Size	Rev
C	E1
Date: Monday, September 02, 2024	Sheet 46 of 57

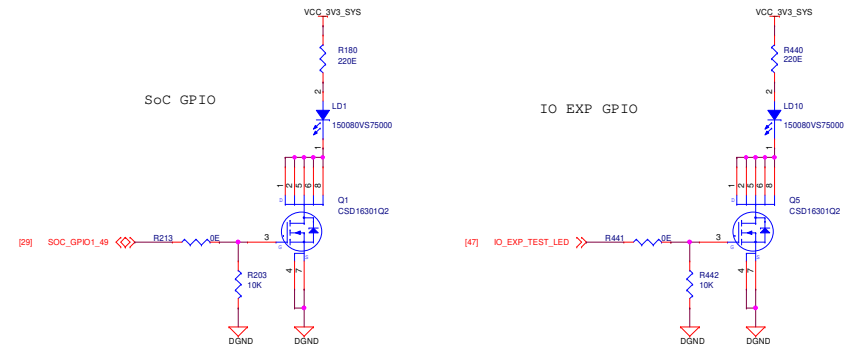
IO EXPANDER



I2C LEVEL TRANSLATOR



USER TEST LEDS



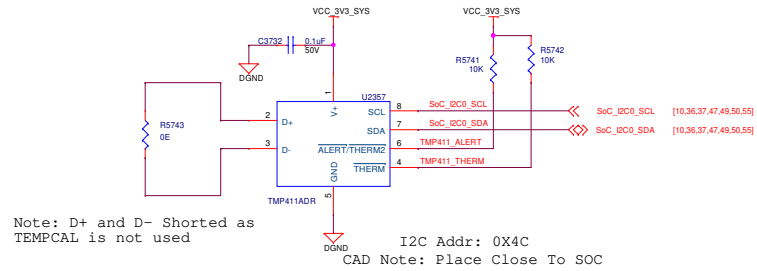
Designed for TI by Mistral Solutions Pvt Ltd



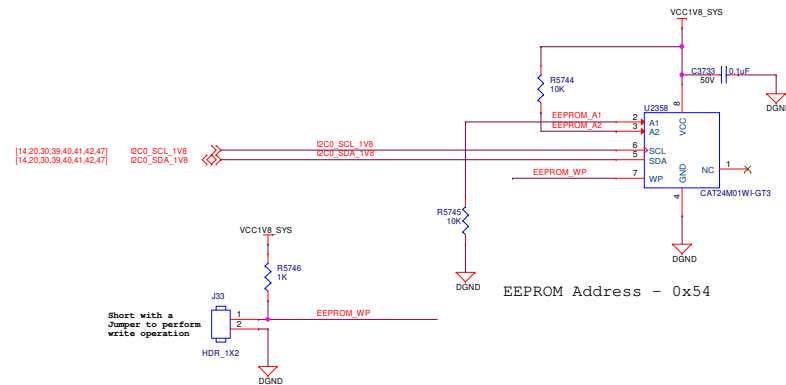
Title IO EXPANDER & USER TEST LEDS

Size	PROC190E1	Rev
C		E1
Date:	Monday, September 02, 2024	Sheet 47 of 57

TEMPERATURE SENSORS



BOARD ID EEPROM



PROC180E1

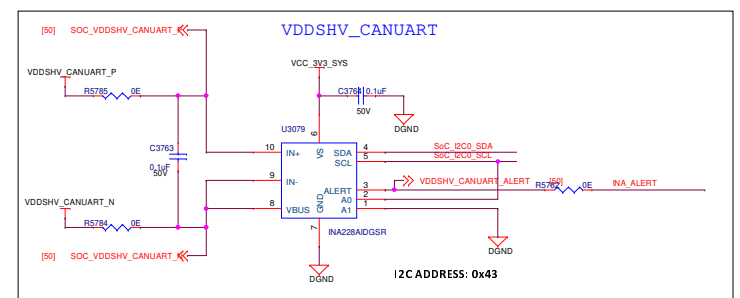
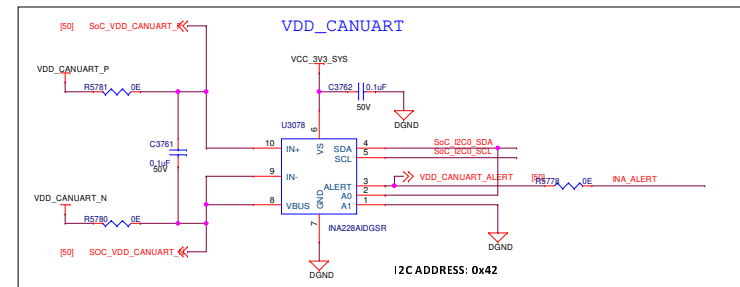
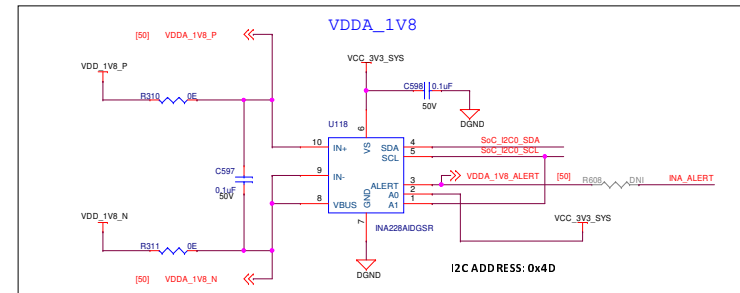
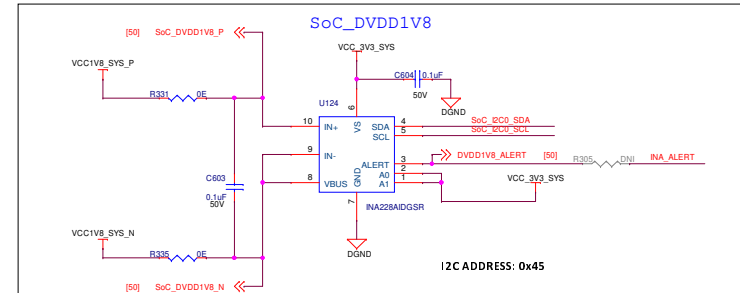
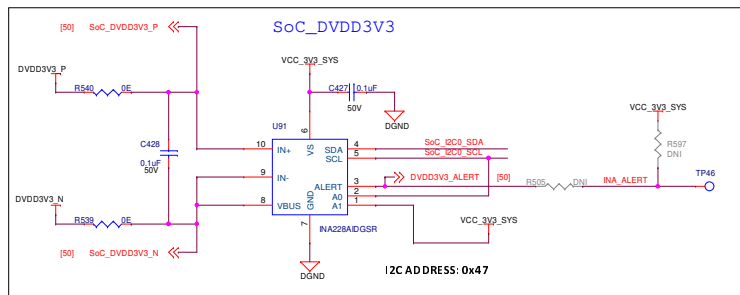
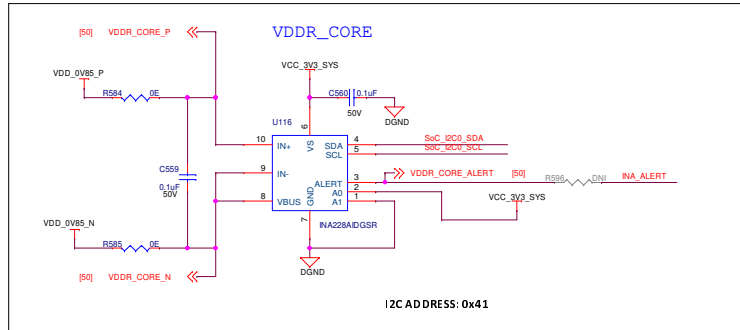
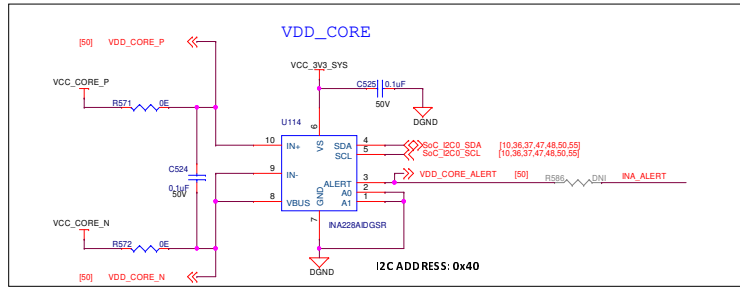
Designed for TI by Mistral Solutions Pvt Ltd



Title TEMPERATURE SENSORS & BOARD ID EEPROM

Size	Rev
C	E1
Date:	Monday, September 02, 2024
Sheet	48 of 57

CURRENT MONITORING DEVICES - 1



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_OV85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	47
VCC_1V8	SoC_DVDD1V8	45
VDDA_1V8	VDDA_1V8	4D
VDD_CANUART	SOC_VDD_CANUART	42
VDDSHV_CANUART	SOC_VDDSHV_CANUART	43

Note: The design supports current/voltage measurements using either INA228 or INA231. INA228 will be populated on the the SK (Implemented via stacked PCB footprint).

PROC180E1

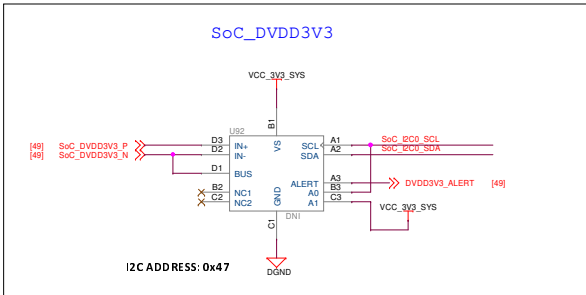
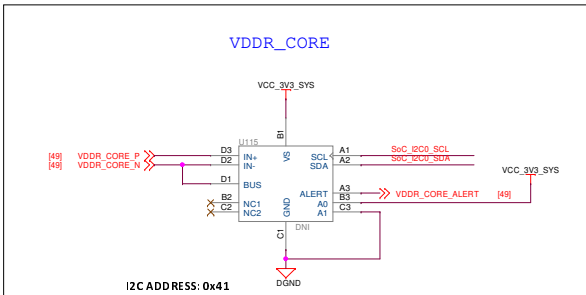
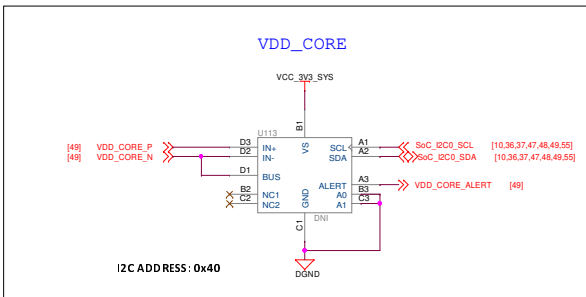
Designed for TI by Mistral Solutions Pvt Ltd



Title CURRENT MONITORING DEVICES - 1

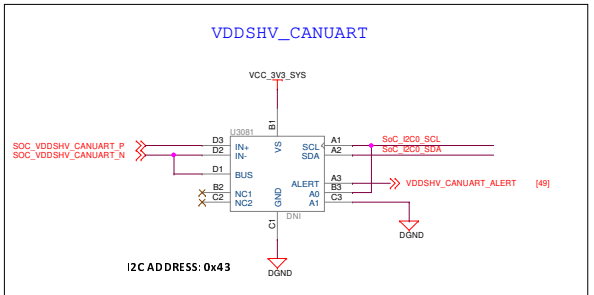
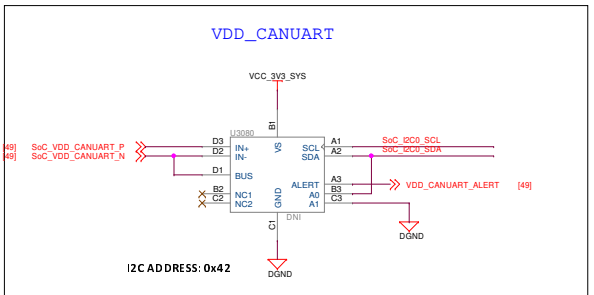
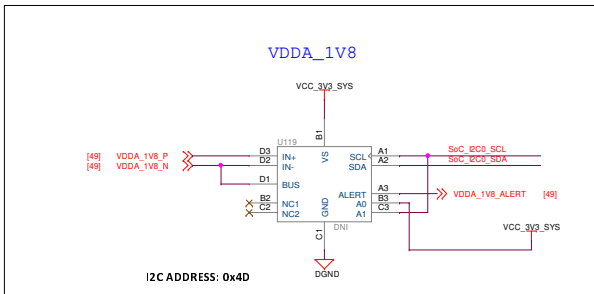
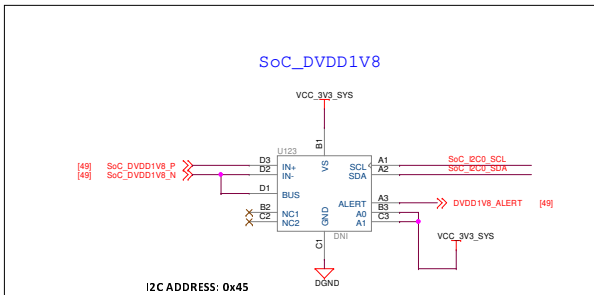
Size	Rev
C	PROC180E1
Date:	Monday, September 02, 2024
Sheet	49 of 57

CURRENT MONITORING DEVICES - 2



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	47
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VDD_CANUART	SOC_VDD_CANUART	42
VDDSHV_CANUART	SOC_VDDSHV_CANUART	43

Note: The design supports current/voltage measurements using either INA228 or INA231. INA228 will be populated on the the SK (Implemented via stacked PCB footprint).



PROC180E1

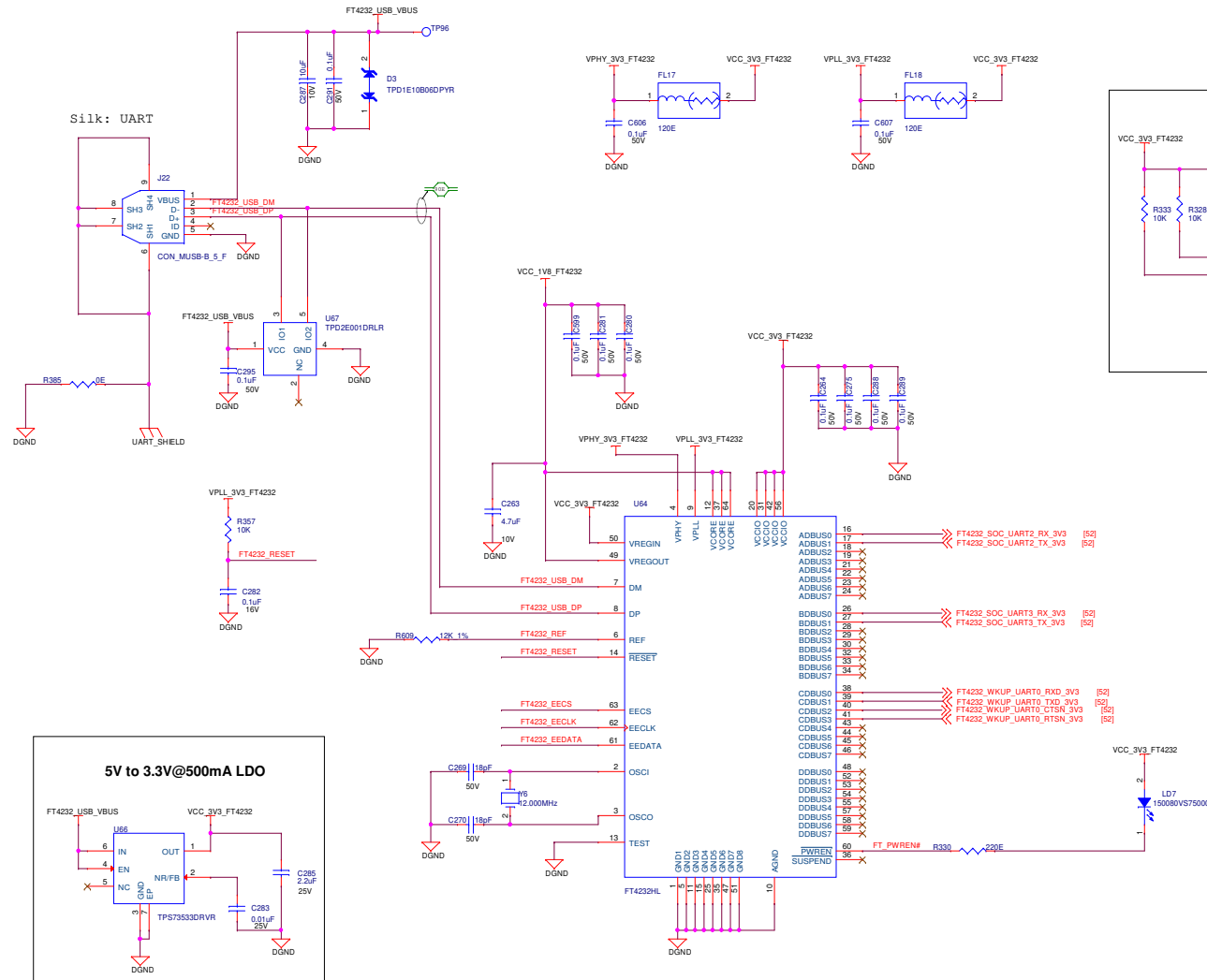
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Title CURRENT MONITORING DEVICES - 2

Size	Rev
C	PROC180E1
Date:	Monday, September 02, 2024
Sheet	50 of 57

USB TO UART BRIDGE



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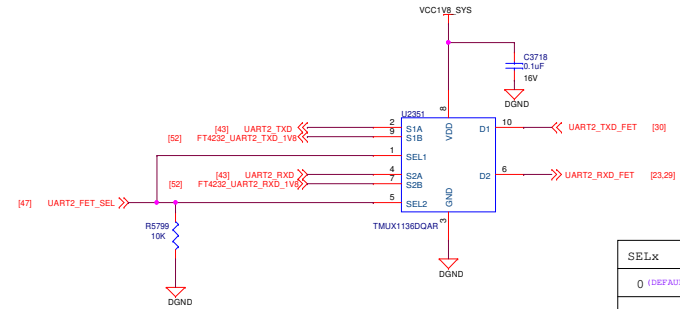
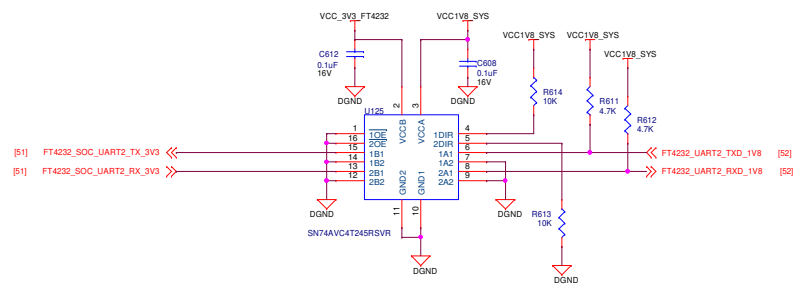


Title FT4232 UART to USB BRIDGE

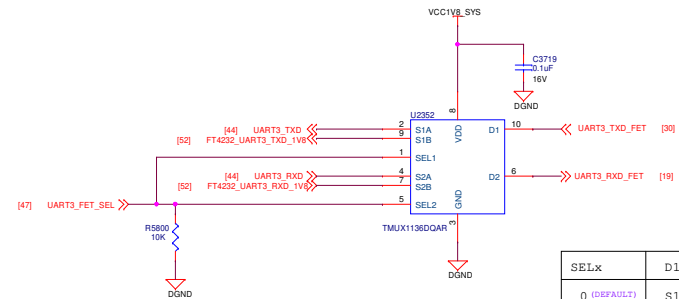
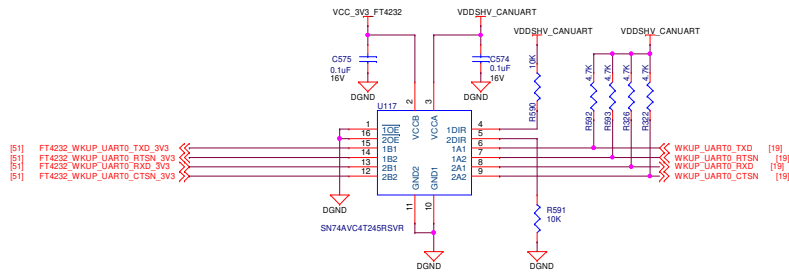
Size	Rev
C	PROC190E1
Date:	Monday, September 02, 2024

Sheet 51 of 57

FT4232 UART BUFFERS



SELx	D1	D2
0 (DEFAULT)	S1B	S2B
1	S1A	S2A



SELx	D1	D2
0 (DEFAULT)	S1B	S2B
1	S1A	S2A

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Title FT4232 UART BUFFERS

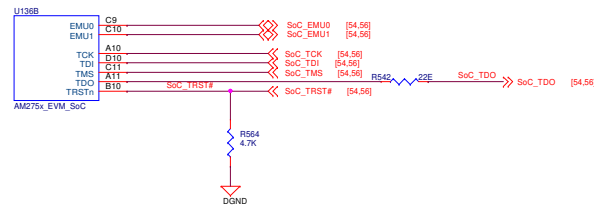
Size	Rev
C	E1

Date: Monday, September 02, 2024 Sheet 52 of 57

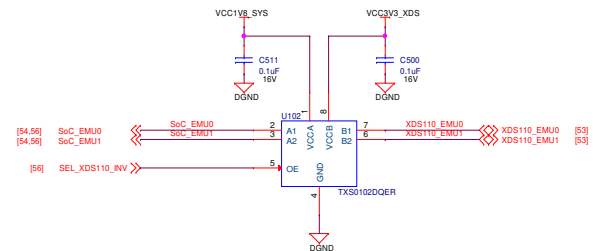
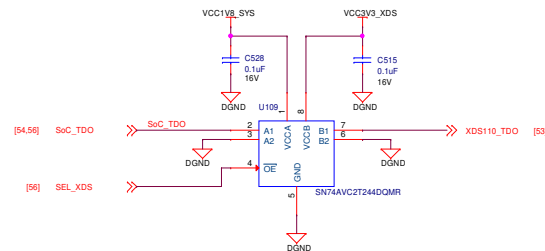
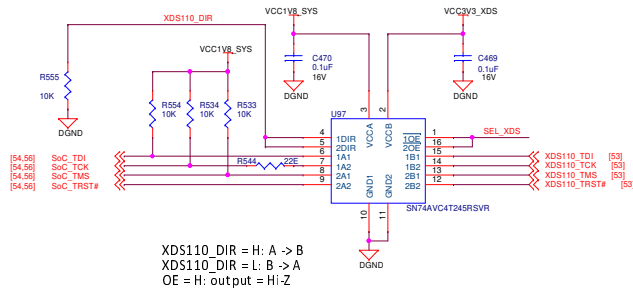
XDS110 DEBUGGER

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SOC_GPIO0_90 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

SOC - JTAG



XDS110 JTAG BUFFER



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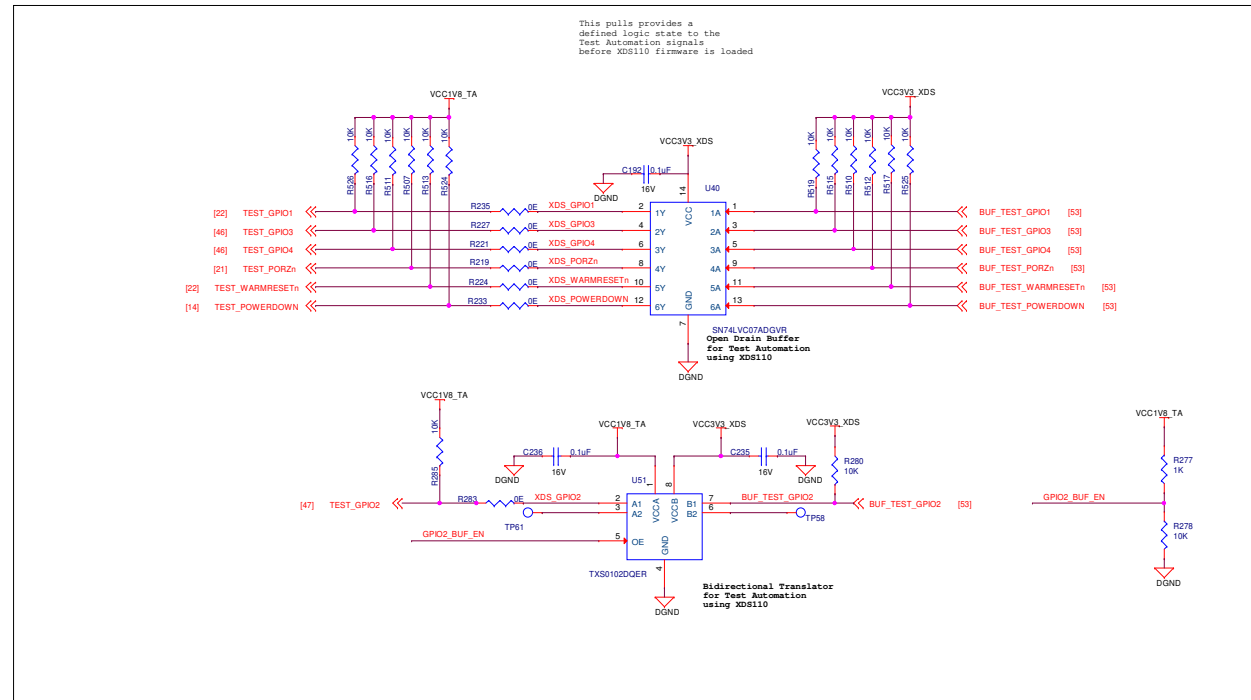


Title XDS110 JTAG BUFFER

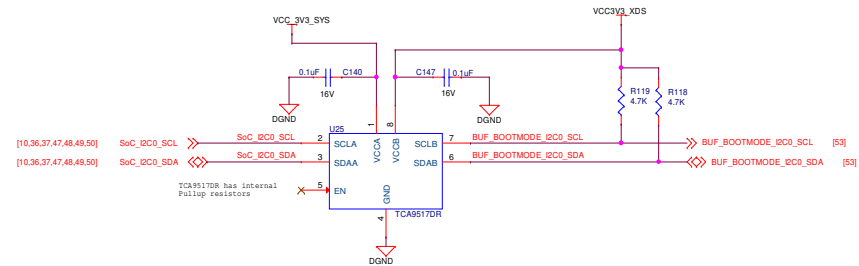
Size	Rev
C	PROC190E1
Date:	Monday, September 02, 2024

Sheet 54 of 57

XDS110 TEST AUTOMATION BUFFERS



SOC I2C BUS BUFFER



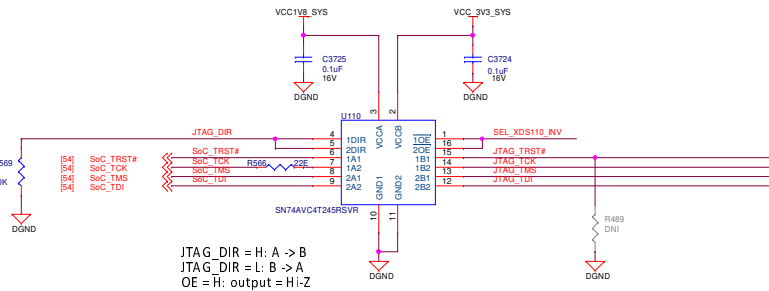
Designed for TI by Mistral Solutions Pvt Ltd



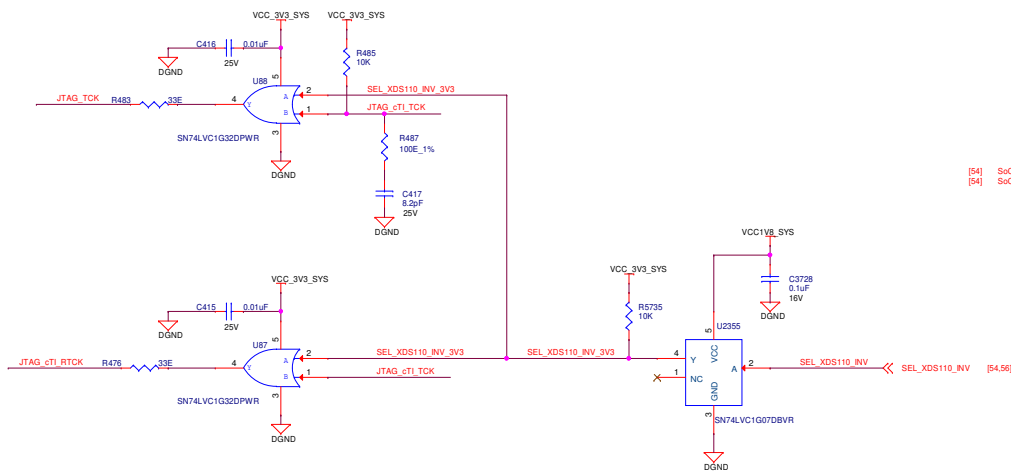
Title XDS110 TEST AUTOMATION BUFFERS

Size	Rev
C	E1
Date: Monday, September 02, 2024	Sheet 55 of 57

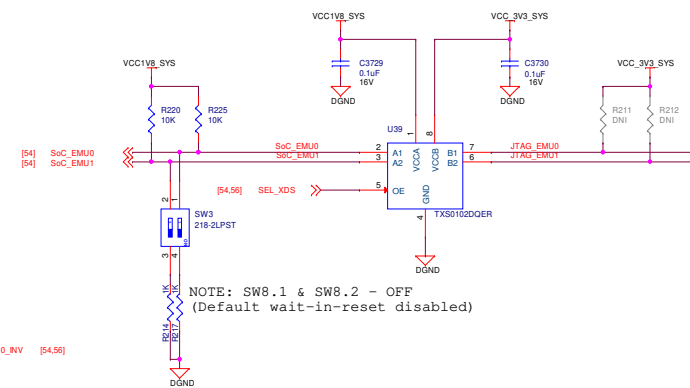
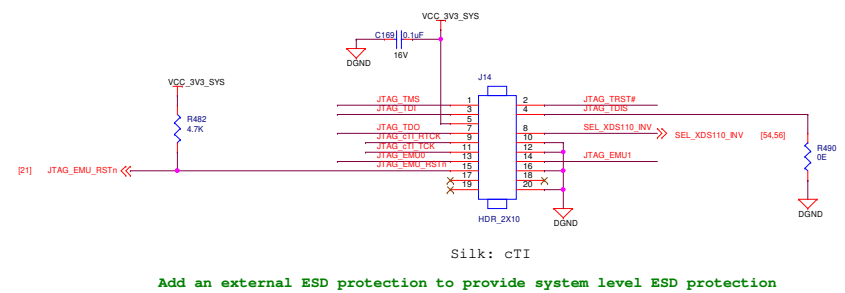
JTAG BUFFERS



JTAG CLOCK BUFFER



cTI20 JTAG CONNECTOR



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Title JTAG 20 PIN cTI CONNECTOR		
Size	PROC190E1	Rev
C		E1
Date: Monday, September 02, 2024	Sheet 56	of 57

MOUNTING HARDWARE

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

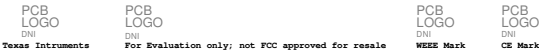
FIDUCIALS



JUMPERS



LOGOs



LABELS

Board Serial No.



Assembly Revision



EVM Orderable No.



Orderable Part Numbers

Variant	Label Text
001	AUDIO-AM275-EVM

BARE PCB



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Title MOUNTING HARDWARE

Size	Rev
C	E1
Date:	Monday, September 02, 2024
Sheet	57 of 57