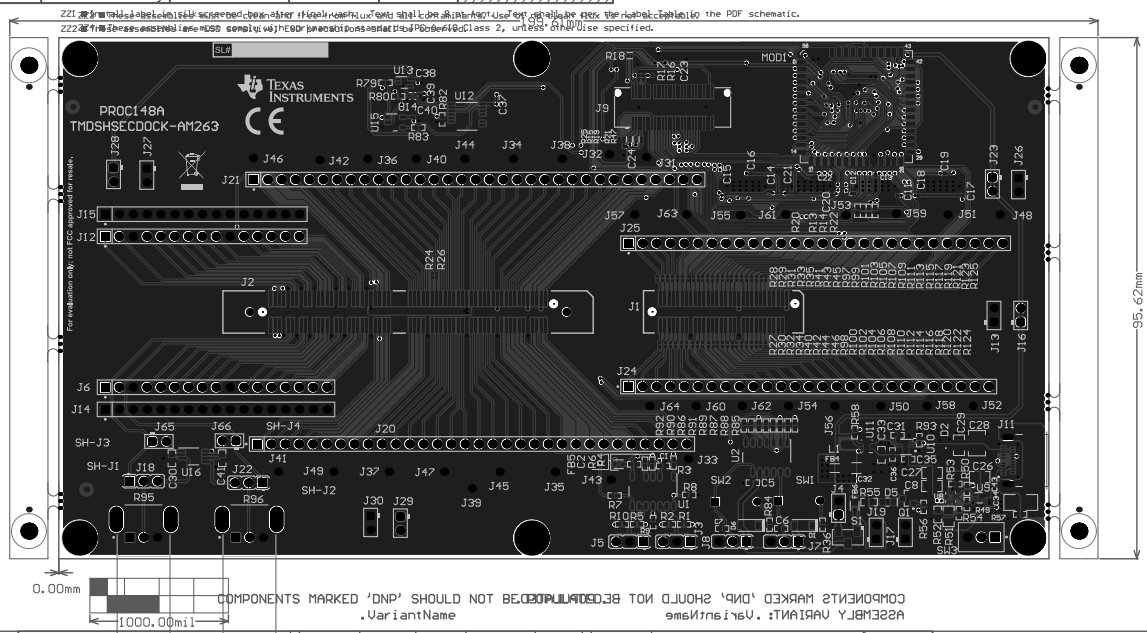
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	3.70mil	4.1	
2	GND01		1.38mil		
	Dielectric 1	FR-4	48.00mil	4.8	
3	PWR/GND02		1.38mil		
	Dielectric 3	FR-4	3.70mil	4.1	
4	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

IMPEDENCE TABLE :

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP	4 MILS	5 MILS	120OHM	LAYER-3
TOP/BOT	4 MILS	-	50 OHM	LAYER-2 /LAYER-3



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
.VariantName

ALL ARTWORK VIEWED FROM TOP SIDE	[illegible]	[illegible]	[illegible]	[illegible]
LAYER NAME = [illegible]	TID #:	TID #:	.TIDDIT.	:# DIT
PLOT NAME = [illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should [illegible] validate and test your design implementation to confirm the system functionality for your application.

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 4 MIL
MIN. VIA PAD SIZE: 18 MIL
MINIMUM ANNULAR RING 0.12mm (5MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[ ] MATTE [X] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] Breakaway Tabs

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[X] 8MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: .PRJ_Title
DESIGNED FOR: .PRJ_Customer
FILE NAME: PROC148A.PcbDoc
ENGINEER: .PRJ_Engineer
LAYOUT BY: .PCB_Layout
SCALE: 1.00
ALTIUM DESIGNER VERSION: 22.8.2.66