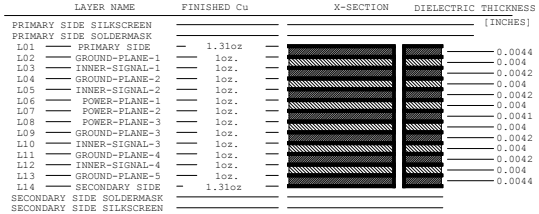
REVISIONS		
REV #	DESCRIPTION	DATE
REV #	CCN #	DDMMYY

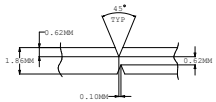
FABRICATION NOTES:

1. FABRICATE PCB IN ACCORDANCE WITH IPC-6012C, CLASS 2; PER IPC-6011. PCB SHALL BE MANUFACTURED USING I-SPEED OR EQUIVALENT.
2. MATERIALS:
   1. LAMINATE AND PREPREG (B-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/126. (MIN.TG 170)
   2. COPPER FOIL TO BE IN ACCORDANCE WITH IPC-MF-150. UNLESS OTHERWISE SPECIFIED, ALL COPPER WEIGHT FOR INNER LAYERS AND EXTERNAL LAYERS FOLLOW THE STACKUP PDF. THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 6012B TABLE NO.3-7 AND 3-8.
3. ALL HOLES SHALL BE LOCATED WITHIN 0.150MM DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.125MM.
4. BOW AND TWIST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTH.
5. CONDUCTOR WIDTH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCASE FOR MATCHING IMPEDANCE MISTRAL SHALL APPROVE THE MODIFIED WIDTHS AND SPACING. TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
6. AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
7. FINISH:
   1. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG, ELECTROLESS NICKEL/IMMERSION GOLD, ELECTROLESS NICKEL SHALL BE 3-6 MICRONS, TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.04-0.06 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
   2. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-SM-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. VIA HOLES THAT HAVE MASK OPEN SHALL BE FILLED WITH NON CONDUCTIVE INK, ALL OTHER VIA HOLES SHALL BE FILLED WITH NON CONDUCTIVE INK AND COVERED WITH SOLDER MASK, ONLY SOLDERMASK IMAGES THAT ARE 0.08(0.003") PER SIDE SHALL BE REDUCED IF REQUIRED. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED. DEFAULT COLOUR OF SOLDER MASK SHALL BE GREEN.
   3. SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERABLE AREAS.
   4. SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 200M [0.00079"],
   5. ALL HOLES SURROUNDED BY LAND <=0.010" SHALL BE COMPLIANT TO IPC6012, CLASS 2.
8. MARKING:
   1. BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, UL FILE NUMBER, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
9. TEST REQUIREMENTS:
   1. 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-D-356 NET LIST FOR OPENS AND SHORTS.
10. THIEVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
11. TEAR DROPS SHALL BE ADDED ON INTERNAL AND EXTERNAL LAYER FOR ALL THE VIA'S AND THROUGH HOLE PADS.
12. FINISHED PCB THICKNESS SHALL BE 0.0732" +/-10%.
13. MIN TRACE WIDTH/SPACING ON BOARD IS 0.003"/0.003".
14. ALL THE IMPEDANCE SHALL BE MATCHED AS PER IMPEDANCE TABLE WITH +/-10% TOLERANCE.
15. ALL UNCONNECTED VIA'S SHALL BE SUPPRESSED IN INTERNAL LAYERS.

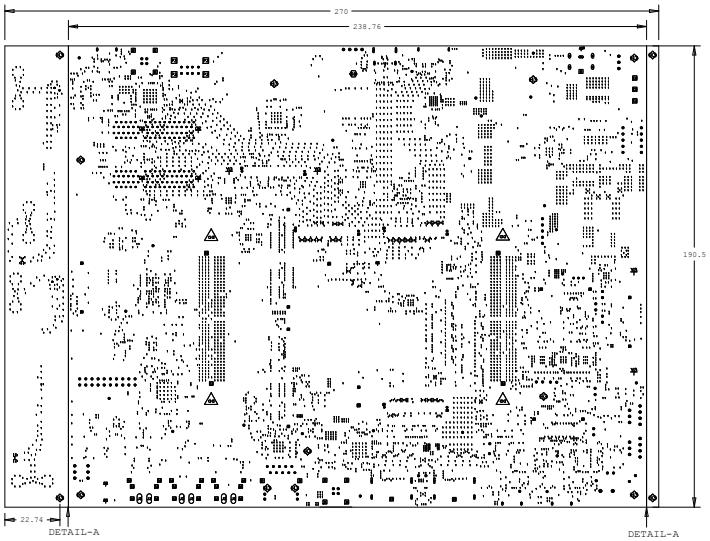
LAYER STACKUP



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	8.0	+3.0/-4.0	PLATED	6593
•	12.0	+3.0/-4.0	PLATED	10
•	28.0	+3.0/-3.0	PLATED	132
•	32.0	+2.0/-2.0	PLATED	8
•	32.0	+3.0/-3.0	PLATED	3
•	36.0	+3.0/-3.0	PLATED	18
•	40.0	+3.0/-3.0	PLATED	94
•	44.0	+2.0/-2.0	PLATED	27
•	56.0	+3.0/-3.0	PLATED	2
■	60.0	+3.0/-3.0	PLATED	18
■	66.0	+3.0/-3.0	PLATED	11
■	68.0	+3.0/-3.0	PLATED	3
■	90.0	+3.0/-3.0	PLATED	4
⊖	118.0	+3.0/-3.0	PLATED	1
•	34.0	+2.0/-2.0	NON-PLATED	8
■	40.0	+3.0/-3.0	NON-PLATED	13
■	44.0	+2.0/-2.0	NON-PLATED	1
■	52.0	+3.0/-3.0	NON-PLATED	1
■	58.0	+3.0/-3.0	NON-PLATED	6
▰	60.0	+3.0/-0.0	NON-PLATED	1
▰	62.0	+2.0/-2.0	NON-PLATED	1
▰	66.0	+3.0/-3.0	NON-PLATED	2
▰	92.0	+2.0/-2.0	NON-PLATED	4
⊕	108.0	+3.0/-3.0	NON-PLATED	4
⊕	126.0	+3.0/-3.0	NON-PLATED	14
⚠	250.0	+4.0/-4.0	NON-PLATED	4
▮	52.0x24.0	+3.0/-3.0	PLATED	6
▮	56.0x20.0	+3.0/-3.0	PLATED	2
▮	62.0x24.0	+2.0/-2.0	PLATED	2
▮	70.0x26.0	+2.0/-2.0	PLATED	4
▮	80.0x40.0	+3.0/-3.0	PLATED	4
▮	82.0x24.0	+2.0/-2.0	PLATED	2
▬	82.0x32.0	+3.0/-0.0	PLATED	1
▮	90.0x26.0	+2.0/-2.0	PLATED	4
▯	158.0x78.0	+3.0/-3.0	NON-PLATED	6



DETAIL-A(V-GROOVE DETAILS)
SCALE:NTS



IMPEDANCE SPECIFICATIONS

SL#	TYPE	LAYER	TRACEWIDTH(Mils)	SPACING(Mils)	IMPEDANCE(Ohms)	REF LAYER
01	EDGE COUPLED MICROSTRIP	L1/L4	5	6	120	L4/L11
02	EDGE COUPLED MICROSTRIP	L1/L4	4.7	5.6	100	L2/L13
03	EDGE COUPLED MICROSTRIP	L1/L4	6.3	5.7	90	L2/L13
04	EDGE COUPLED MICROSTRIP	L1/L4	7.4	5.8	85	L2/L13
05	MICROSTRIP	L1/L4	9		50	L2/L13
06	EDGE COUPLED STRIPLINE	L3	3	5	100	L2,L4
07	EDGE COUPLED STRIPLINE	L10	3	5	100	L9,L11
08	EDGE COUPLED STRIPLINE	L12	3	5	100	L11,L13
09	EDGE COUPLED STRIPLINE	L3	3.8	5	90	L2,L4
10	EDGE COUPLED STRIPLINE	L5	3.8	5	90	L4,L6
11	EDGE COUPLED STRIPLINE	L12	3.8	5	90	L11,L13
12	EDGE COUPLED STRIPLINE	L12	4.3	5	85	L11,L13
13	STRIPLINE	L3/L5	3.8		50	L2,L4/L4,L6
14	STRIPLINE	L10/L12	3.8		50	L9,L11 /L11,L13

SIGNATURES		DATE
LAYOUT BY	JA	180719
REVIEWED BY	ZA	180719
APPROVED BY	AMB	180719

TEXAS INSTRUMENTS

PROC079

J7X COMMON PROCESSOR BOARD

SIZE D | Rev E3 | SCALE: NONE | SHEET 1 OF 21