

J721E SOM - DUAL TPS65941x PMICs

TABLE OF CONTENTS

PAGE	CONTENTS
01	TABLE OF CONTENTS
02	REVISION HISTORY
03	SoM: SYSTEM BLOCK DIAGRAM
04	SoM: 2-Ph DUAL PMIC PDN-0A Diagram
05	SoM: I2C Tree Diagram
06	SoM: I2C Address Table
07	SoC: GPIO MAPPING TABLE
08	SoC: MLB, CSI & DSI INTERFACES
09	SoC: SERDES INTERFACES
10	SoC: MMC & UFS INTERFACES
11	SoC: EMIF & LPDDR4
12	SoC: MCU FLASH
13	FLASH: OSPI-FLASH, HYPER-FLASH & RAM
14	SOC: MCU & MAIN GENERAL IO, OSC CLKS
15	SOC: GENERAL & USB
16	SOC: MCU RGMII, MCU ADC & MAIN RGMII
17	SOC: PRG0 & PRG1
18	SOC: ANALOG POWER 1
19	SOC: DIGITAL POWER 2
20	SOC: DIGITAL POWER 3
21	SOC: GROUND
22	SOM: PMIC A
23	SOM: PMIC B
24	SOM: LOAD SWITCHES & POWER_SUPPLY 3
25	SOM: SOM to COMM PROC SERDES CONNECTORS
26	SOM: SOM to COMM PROC PRIMARY CONN #1
27	SOM: SOM to COMM PROC PRIMARY CONN #2
28	EVM: BOARD ID EEPROM & TEMP SENSORS
29	EVM: SOC CURRENT SENSE RESISTORS
30	EVM: PERIPHERAL CURRENT SENSE RESISTORS

PAGE	CONTENTS
31	EVM: ALTERNATE POWER SUPPLY OPTIONS A-D
32	EVM: ALTERNATE LPDDR4x POWER RESOURCE OPTION
33	EVM: NOTES, HARDWARE & LABELS
34	EVM: SI_SIM_COUPON BD
35	Recommended 3-Ph DUAL PMIC PDN-0B

Project :

J7 EVM




Title
TABLE OF CONTENTS

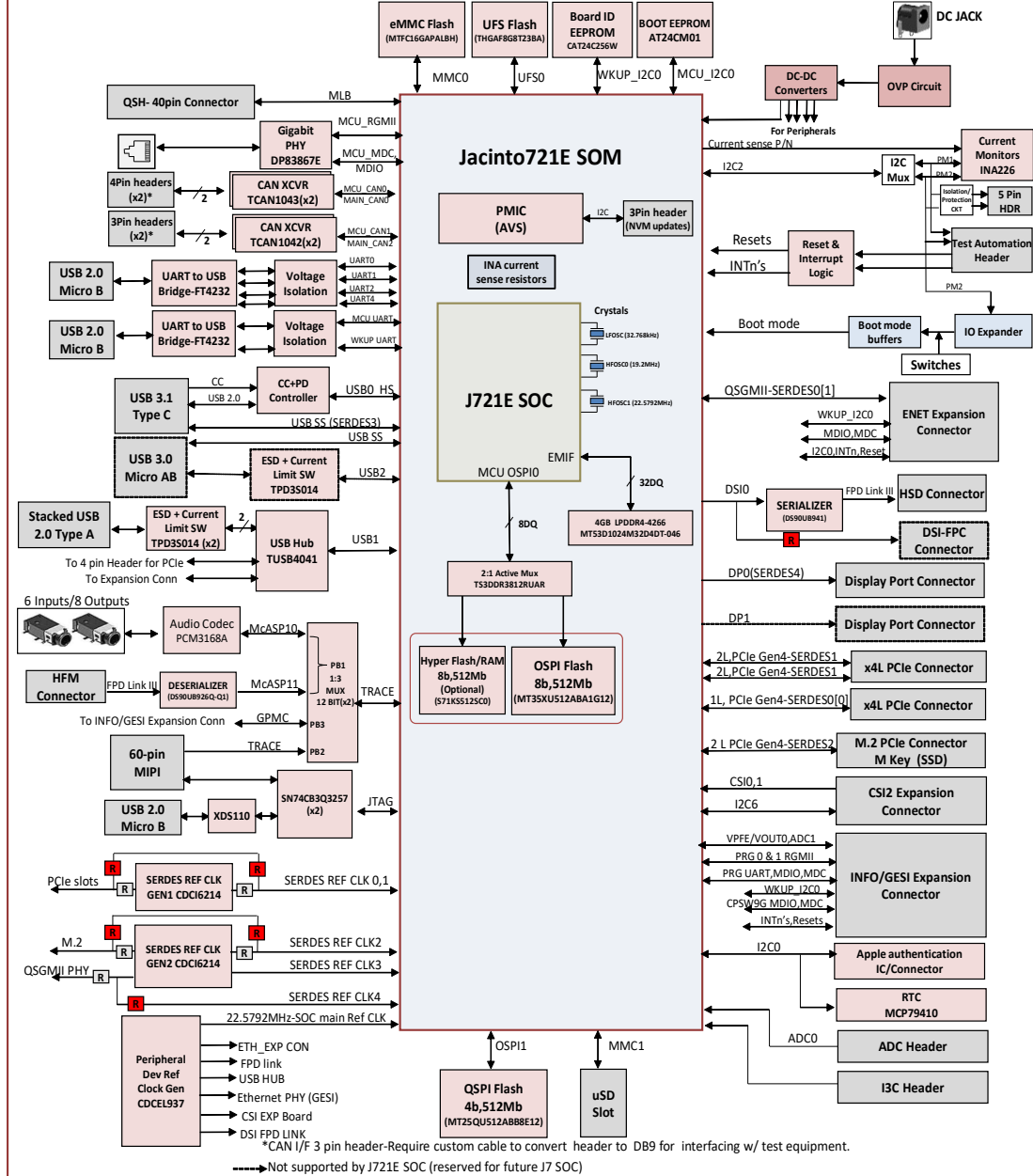
Size	PROC078 001 J721EXSOMG01EVM	Rev
C		E7B
Date:	Tuesday, November 03, 2020	Sheet 1 of 35

REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E7A	21 NOV 2019	Drafted from PROC078E7 SCH Released on 10th OCT 2019 DNI'd the PU Resistor R117 from MCU_PERIPH_RSTz R509 and R510 moved to Mount list (DNI property removed) Hardware Schematic page updated	Mistral Design Team		
E7B	3 NOV 2020	Added "Not Recommended for New Designs" banners to original 2-Phase Dual PMIC PDN diagram (pg 4). Added "Not Recommended for New Designs" & "ALL New Designs use..." banners to SoM PMIC A (pg 22). Added new recommended 3-Phase Dual PMIC PDN-0B diagram with PDN differences high-lighted (pg 35). Updated Analog Power 1 SCH layout & Notes to clarify analog supply filtering recommendations (pg18).	TI EVM Design Team		

Project : J7 EVM				Title REVISION HISTORY	
Size	PROC078 001 J721EXSOMG01EVM			Rev	
C				E7B	
Date:	Friday, November 13, 2020	Sheet	2	of	35

Common Processor Board



Project :

J7 EVM



Title
BLOCK DIAGRAM

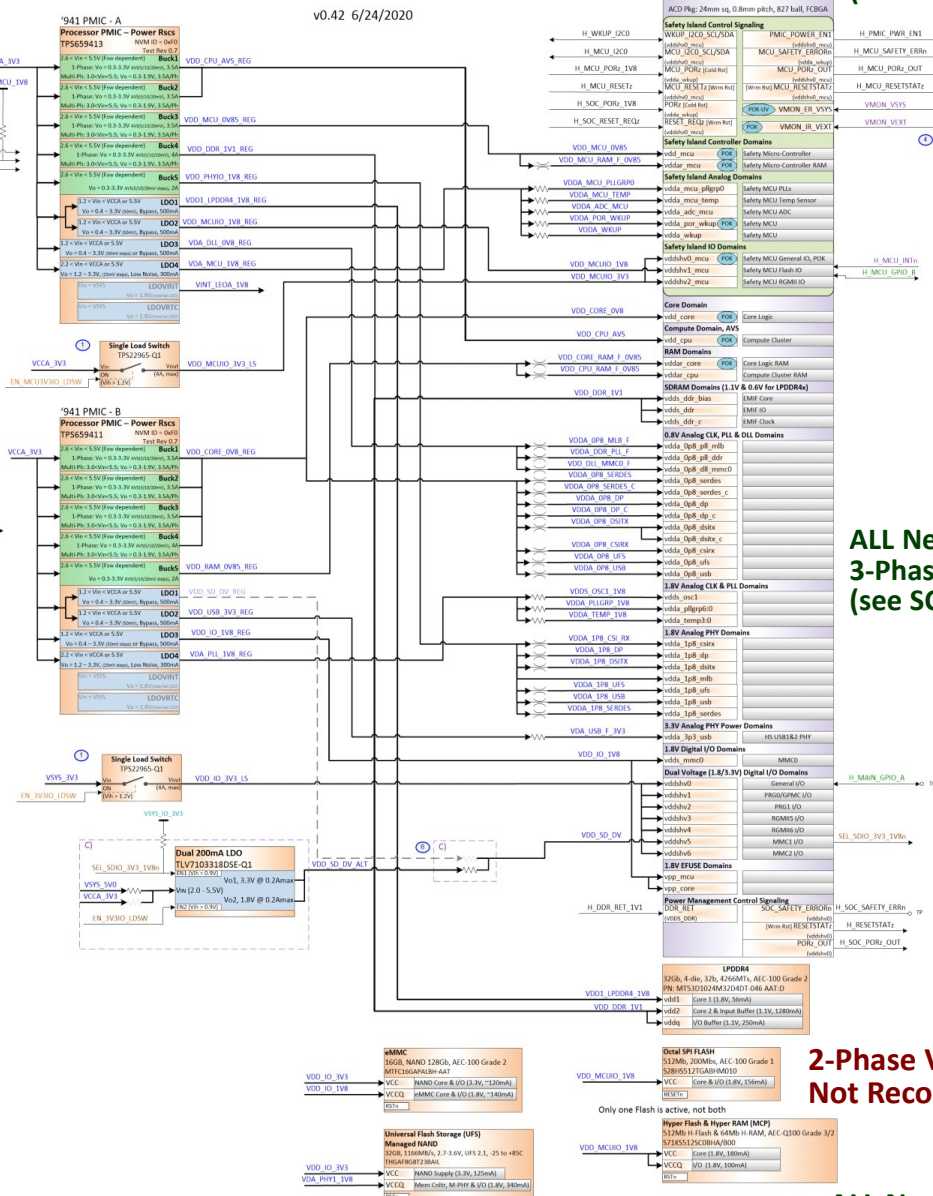
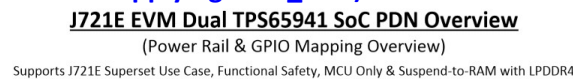
Size	PROC078 001 J721EXSOMG01EVM	Rev
C		ETA
Date:	Tuesday, November 03, 2020	Sheet 3 of 35

2-Phase VDD_CPU PDNs Not Recommended for New Designs

**ALL New Designs should use
3-Phase Buck supplying VDD_CPU
(see SCH's last page)**

**ALL New Designs should use
3-Phase Buck supplying VDD_CPU
(see SCH's last page)**

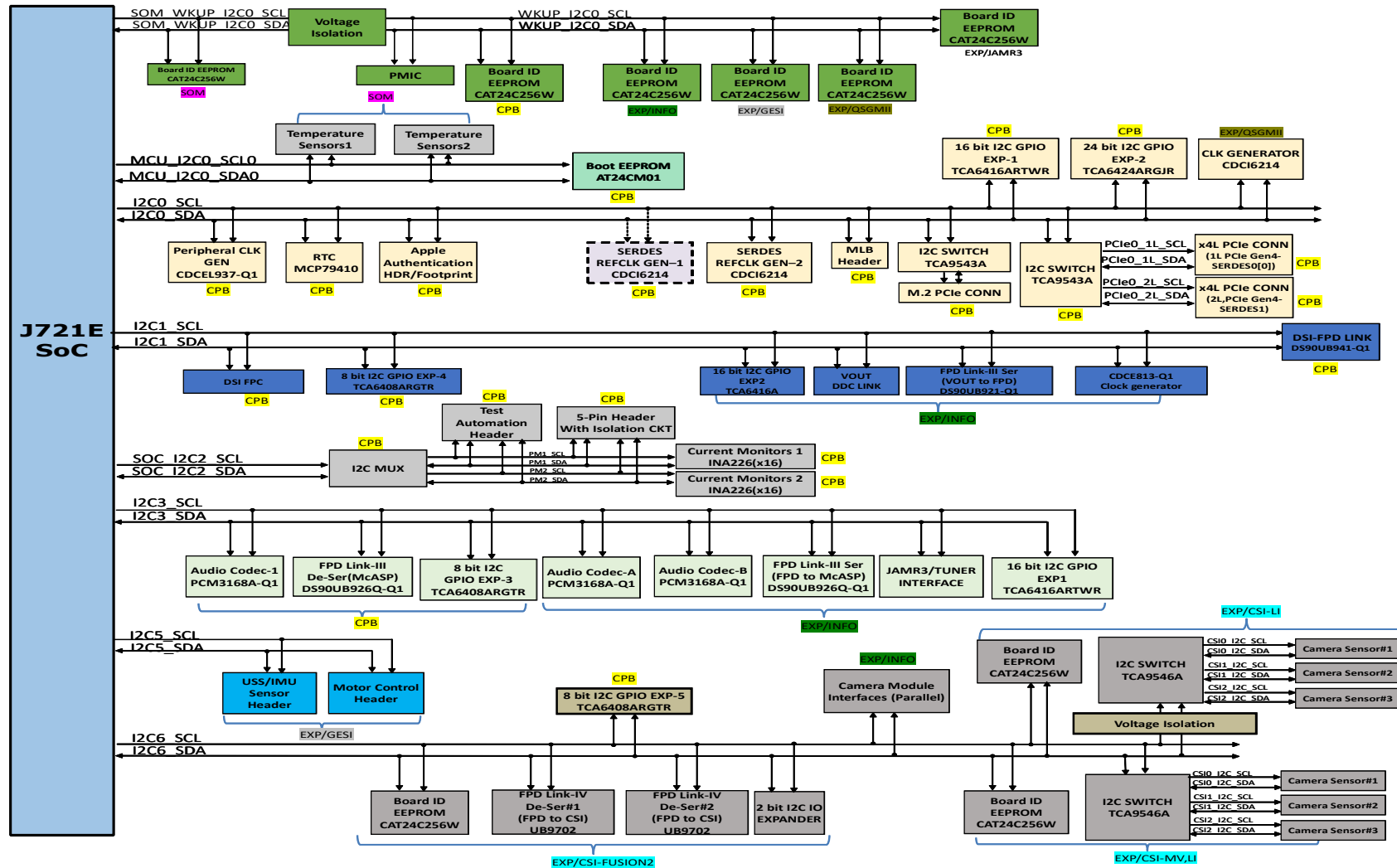
**ALL New Designs should use
3-Phase Buck supplying VDD_CPU
(see SCH's last page)**



**TEXAS
INSTRUMENT**

Title		2-Phase DUAL PMIC PDN-QA DIAGRAM	
Size	PROC078 001 J721EXSOMG01EVM	Revised By	
C		EW	
Date: Friday, December 04, 2020	Sheet 4 of 35		

SoM I2C TREE DIAGRAM



SoM I2C ADDRESS TABLE

J7ES EVM I2C Table				
Board	I2C Port	Device/Function	Part#	I2C Address
EVM/SoM	WKUP_I2C0	PMIC-A	TPS659413	0x48, 0x49, 0x4A & 0x4B
EVM/SoM	WKUP_I2C0	PMIC-B	TPS659411	0x4C, 0x4D, 0x4E & 0x4F
EVM/SoM	WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x50
EVM/CPB	WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x53
EXP/INFO	WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x52
EXP/GESI	WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x52
EXP/QSGMII	WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x54
EXP/JAMR3	WKUP_I2C0	Board ID EEPROM	CAT24C256W	0x51
EVM/CPB	MCU_I2C0	BOOT EEPROM	AT24CM01	0x50,51
EVM/SoM	MCU_I2C0	Temperature Sensors 1	TMP100NA/3K	0x48
EVM/SoM	MCU_I2C0	Temperature Sensors 2	TMP100NA/3K	0x49
EVM/CPB	SoC_I2C0	Peripheral Clock Generator	CDCEL937-Q1	0x6D
EVM/CPB	SoC_I2C0	RTC Module	MCP79410	0x57,6F
EVM/CPB	SoC_I2C0	Apple Authentication Header/Footerprint	2214BR-10G	0x10, 0x11
EVM/CPB	SoC_I2C0	SERDES REF CLK GEN - 2	CDCI6214	0x76
EVM/CPB	SoC_I2C0	16 bit I2C GPIO Expander-1	TCA6416ARTWR	0x20
EVM/CPB	SoC_I2C0	24 bit I2C GPIO Expander-2	TCA6424ARGJR	0x21
EVM/CPB	SoC_I2C0	I2C MUX for both x2LANE and x1LANE PCIe Interface	TCA9543APWR	0x70
EVM/CPB	SoC_I2C0	I2C MUX for M.2 PCIe Connector (2 L PCIe Gen4-SERDES2)	TCA9543APWR	0x71
EVM/CPB	SoC_I2C0	MLB Physical Interface Board	<connector interface>	
EXP/QSGMII	SoC_I2C0	Clock Generator on Quad ENET Board	CDCI6214	TBD
EVM/CPB	SoC_I2C1	8 bit I2C GPIO Expander-4	TCA6408ARGTR	0x20
EVM/CPB	SoC_I2C1	FPD Link-IV Serializer (DSI)	DS90UH981-Q1	0x0E
EXP/INFO	SoC_I2C1	Vout DDC link	CONNECTOR INTERFACE	
EXP/INFO	SoC_I2C1	I2C GPIO Expander(Video)	TCA6416ARTWR	0x21
EXP/INFO	SoC_I2C1	FPD Link-III Serializer (VOUT to FPD)	DS90UB921-Q1	0x1A
EXP/INFO	SoC_I2C1	CDCI (clock generator)	CDCE813-Q1	0x65
EVM/CPB	SoC_I2C1	DSI FPC	CONNECTOR INTERFACE	TBD
EVM/CPB	SoC_I2C2	Current Monitors 1(PM1_I2C)	INA226	0x40-0x4F
EVM/CPB	SoC_I2C2	Current Monitors 2(PM2_I2C)	INA226	0x40-0x4F
EVM/CPB	SoC_I2C2	Test Automation Header	<connector interface>	

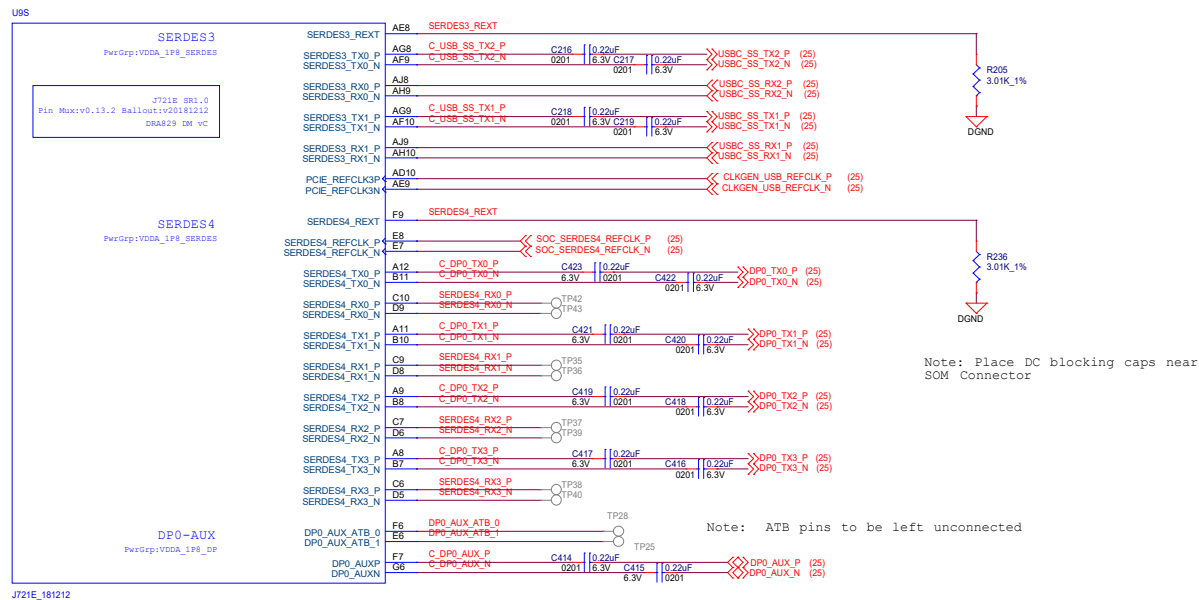
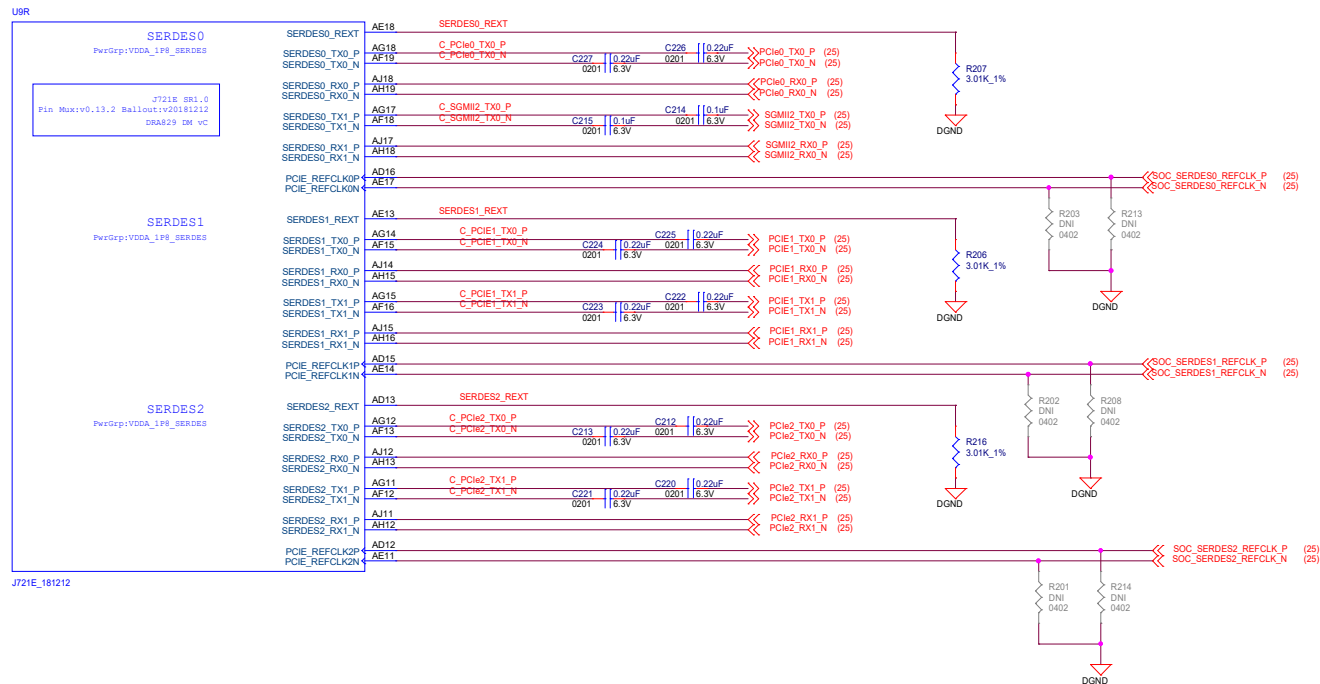
J7ES EVM I2C Table				
Board	I2C Port	Device/Function	Part#	I2C Address
EVM/CPB	SoC_I2C3	8 bit I2C GPIO Expander-3	TCA6408ARGTR	0x20
EVM/CPB	SoC_I2C3	Audio Codec - 1	PCM3168A-Q1	0x44
EVM/CPB	SoC_I2C3	FPD Link-III De-serializer (McASP)	DS90UB926Q-Q1	0x2C
EXP/INFO	SoC_I2C3	Audio Codec - A	PCM3168A-Q1	0x47
EXP/INFO	SoC_I2C3	Audio Codec - B	PCM3168A-Q1	0x46
EXP/INFO	SoC_I2C3	FPD Link-III De-Serializer (FPD to McASP)	DS90UB926Q-Q1	0x3B
EXP/INFO	SoC_I2C3	I2C GPIO Expander (Audio)	TCA6416ARTWR	0x21
EXP/GESI	SoC_I2C3	I2C GPIO Expander1	TCA6416ARTWR	0x21
EXP/GESI	SoC_I2C5	I2C GPIO Expander2	TCA6416ARTWR	0x21
EXP/GESI	SoC_I2C5	USS/IMU Sensor control Header		TBD
EXP/GESI	SoC_I2C5	Booster Pack Header		TBD
EVM/CPB	SoC_I2C6	8 bit I2C GPIO Expander-5	TCA6408ARGTR	0x20
EXP/CSI-FUSION2	SoC_I2C6	I2C IO Expander	PCA9536DGKR	0x41
EXP/CSI-FUSION2	SoC_I2C6	Board ID EEPROM (Fusion2 Serial Capture)	CAT24C256W	0x52
EXP/CSI-FUSION2	SoC_I2C6	FPD-Link IV De-Serializer #1 (FPD to CSI)	UB9702	TBD
EXP/CSI-FUSION2	SoC_I2C6	FPD-Link IV De-Serializer #2 (FPD to CSI)	UB9702	TBD
EXP/CSI-LI	SoC_I2C6	Board ID EEPROM (Leopard Imaging Adapter)	CAT24C256W	0x52
EXP/CSI-LI	SoC_I2C6	I2C MUX Camera sensors	TCA9543APWR	0x70
EXP/CSI-MV	SoC_I2C6	Board ID EEPROM (Machine Vision Application)	CAT24C256W	0x52
EXP/CSI-MV	SoC_I2C6	I2C MUX Camera sensors	TCA9543APWR	0x70
EXP/CSI-MV	SoC_I2C6	Camera Sensor #1, #2 & #3	IMX264LQR-C	TBD
EXP/INFO	SoC_I2C6	Camera Sensor, Parallel	<connector interface>	TBD

GPIO MAPPING TABLE

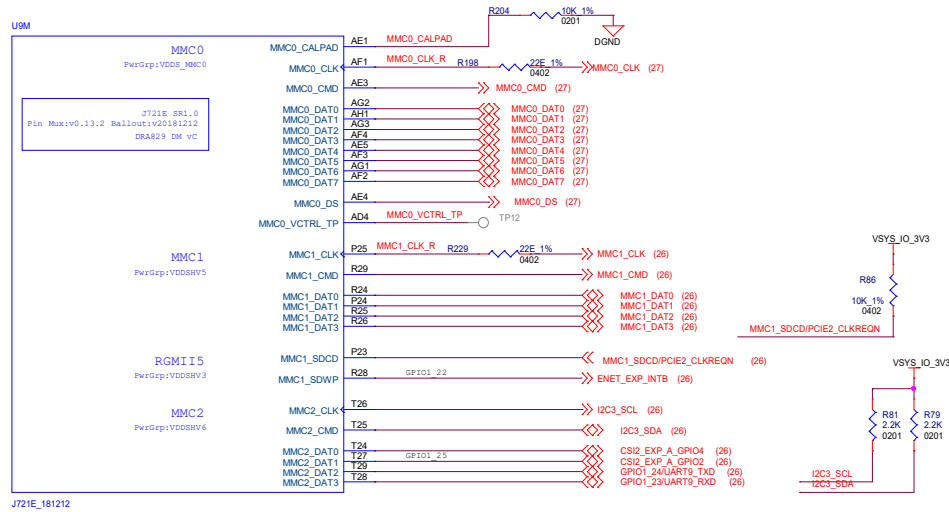
J721E SoM - GPIO Mapping Table						
Package Signal Name	GPIO	Net name	Input/Output	Default	State	Remarks
WKUP Domain						
WKUP_GPIO0_0	WKUP_GPIO0_0	MCU_MCAN0_EN	Output	BOOTMODE	Active High	MCU CAN0 Enable
WKUP_GPIO0_1	WKUP_GPIO0_1	BOOT_EEPROM_WP	Output	BOOTMODE	Active High	Boot EEPROM Write protect
WKUP_GPIO0_2	WKUP_GPIO0_2	MCU_CAN1_STB	Output	BOOTMODE	Active High	MCU CAN1 Standby
WKUP_GPIO0_3	WKUP_GPIO0_3	GPIO_MCU_RGMII1_RST#	Output	PU	Active low	MCU_RGMII1_Reset
WKUP_GPIO0_6	WKUP_GPIO0_6	WKUP_GPIO0_6	I/O	Test Point	NA	Terminated with Test point
WKUP_GPIO0_7	WKUP_GPIO0_7	SYS_IRQz	Input	PU	Active low	Push-button Interrupt, User Defined/Wake S2R ('0'>'1' - interrupt pending, '1' - normal operation)
WKUP_GPIO0_8	WKUP_GPIO0_8	OSPI/HYPER_MUX_SEL	Output	DIP_SEL	NA	Flash Memory Selection ('0' - OSPI0, '1' - Hyperflash + HyperRam)
WKUP_GPIO0_9	WKUP_GPIO0_9	PMIC_MCU_INT#	Input	PU	Active low	Interrupt from PMIC
WKUP_GPIO0_17	WKUP_GPIO0_17	MCU_OSPI0_ECC_FAIL	Output	NA	Active High	OSPI_ECC_FAIL (Mux option w/ HYPERBUS_CKn), MCU_OSPI0_ECC_FAIL is DNI resistor option.
MCU_SPI0_CLK	WKUP_GPIO0_52	WKUP_GPIO0_52	I/O	BOOTMODE	NA	Terminated with Test point
MCU_SPI0_CS0	WKUP_GPIO0_55	MCU_RGMII1_INT#	Input	PU	Active Low	MCU Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
MCU_SPI0_D0	WKUP_GPIO0_53	SYS_MCU_PWRDN	Output	PD	Active low	System Power Down ('0' - normal operation, '1' - system power down)
MCU_SPI0_D1	WKUP_GPIO0_54	MCU_CAN0_STBz	Output	PD	Active low	MCU CAN0 Standby
Main Domain						
EXTINTN	GPIO0_0	SOC_EXTINTN	Input	PU	Active low	Push-button Interrupt, User Defined
PRGO_PRU0_GPO5	GPIO0_48	IMU_GPIO1	I/O	NA	NA	Used as GPIO1 for IMU Sensor
PRGO_PRU0_GPO17	GPIO0_60	CAN_STB	Output	PD	Active High	Standby signals for CAN Transceivers
PRGO_PRU0_GPO18	GPIO0_61	GPIO0_61	I/O	NA	NA	Routed to INFO/GESI expansion connector.
PRGO_PRU0_GPO19	GPIO0_62	GPIO_PRG1_RGMII_RST	Output	PU	Active low	Used as a reset signal for PRG1 Ethernet PHY Chips
PRGO_PRU1_GPO5	GPIO0_68	GPIO_LIN_EN	Output	PD	Active High	LIN transceiver enable
RGMII5_RD0	GPIO0_96	RMI18_PHY_RESET	Output	PU	Active low	Used as a reset signal for RMI18 PHY Chip
RGMII6_TX_CTL	GPIO0_97	C_MCASPI0_ACLKR	Input	PU	Active low	CSI2 IO expander Interrupt. ('0' -
RGMII6_RX_CTL	GPIO0_98	C_MCASPI0_AFSR	NA	PU	Active low	I2C0 IO expander interrupt. ('0' - interrupt pending, '1' - no interrupt)(I2C0_IOEXP_INT#) Note: GPIO only available from Trace/GPMC Mux
RGMII6_RXC	GPIO0_104	RMI18_PHY_INTn	Input	PU	Active Low	RMI18 PHY Interrupt
RGMII6_RD3	GPIO0_105	IMU_GPIO0	I/O	NA	NA	Used as GPIO0 for IMU Sensor
SPI1_CS1	GPIO0_117	SEL_SDIO_3V3_1V8n	Output	PU	Active low	SW controls & transition Sd card to high speed 1.8V signaling if card type supports
UART0_CTSN	GPIO0_123	BP_GPIO3	I/O	NA	NA	Boosterpack_GPIO3
UART0_RTSN	GPIO0_124	BP_GPIO4	I/O	NA	NA	Boosterpack_GPIO4
UART1_CTSN	GPIO0_127	GPIO0_127/EQEP0_S/MLB0_MLCLK	Output	PU	Active High	CP Board - MCAN2_STB; GESI - Boosterpack_GPIO2
UART1_RTSN	GPIO1_0	GPIO1_0/EQEP0_I/MLB0_MLBDAT	Output	PD	NA	CP Board - PM I2C Mux selection. ('0' - SOC I2C2_SCL/SDA -> PM1_SCL/SDA, '1' -
MCAN1_RX	GPIO1_3	USBC_DIR	Input	PU	NA	USB Type C Cable Orientation. Type-C plug
ECAP0_IN_APWM_OUT	GPIO1_11	GPIO1_11/MAIN_I3CO_SDA/PULLEN	Input	PU	Active High	Display IO expander Interrupt. ('0' - interrupt pending, '1' - no interrupt) (IOEXP4_INT#)
EXT_REFCLK1	GPIO1_12	GPIO1_12/MLB0_REFCLK	Input	PD	NA	CP Board Audio De-serializer UB926_GPIO1 (Tuner Unused GPIO)
TIMER_IO1	GPIO1_14	DSI_UB981_INTB	Input	PU	Active low	DSI FPD Link Serializer/Panel Interrupt.
MMC1_SDWP	GPIO1_22	ENET_EXP_INTB	Input	PU	Active low	Ethernet Expansion Interrupt. ('0' - interrupt pending, '1' - no interrupt)
MMC2_DAT3	GPIO1_23	GPIO1_23/UART9_RXD	Input	PU	Active low	Interrupt function. ('0' - interrupt pending, '1' - no interrupt)
MMC2_DAT2	GPIO1_24	GPIO1_24/UART9_TXD	Input	PU	Active low	Interrupt function. ('0' - interrupt pending, '1' - no interrupt)
MMC2_DAT1	GPIO1_25	CSI2_EXP_A_GPIO2	I/O	NA	NA	CSI2 Expansion Board Specific.
MMC2_DAT0	GPIO1_26	CSI2_EXP_A_GPIO4	I/O	NA	NA	CSI2 Expansion Board Specific.
I3CO_SCL	GPIO1_5	H_I3CO_SCL	I/O	NA	NA	CP Board Audio De-serializer UB926_GPIO2
I3CO_SDA	GPIO1_6	H_I3CO_SDA	I/O	NA	NA	CP Board Audio De-serializer UB926_GPIO3
PRG1_PRU0_GPO10	GPIO0_11	PRG1_UART0_RTS#	I/O	PD	NA	INFO Expansion Audio De-serializer UB926_GPIO1 (Tuner Unused GPIO)
PRGO_PRU0_GPO2	GPIO0_45	PRGO_RGMII1_RD2	I/O	NA	NA	INFO Expansion Audio De-serializer UB926_GPIO2
PRGO_PRU0_GPO3	GPIO0_46	PRGO_RGMII1_RD3	I/O	NA	NA	INFO Expansion Audio De-serializer UB926_GPIO3
PRGO_PRU1_GPO2	GPIO0_65	PRGO_RGMII2_RD2	I/O	NA	NA	INFO Expansion JAMR3_GPIO0 (Function to be determined)
PRGO_PRU1_GPO3	GPIO0_66	PRGO_RGMII2_RD3	I/O	NA	NA	INFO Expansion JAMR3_GPIO1 (Function to be determined)
PRGO_PRU1_GPO13	GPIO0_76	PRGO_RGMII2_TD2	I/O	NA	NA	INFO Expansion JAMR3_GPIO2 (Function to be determined)
PRGO_PRU1_GPO16	GPIO0_79	GPIO0_79/PRGO_RGMII2_TXC	Input	NA	NA	INFO Expansion FPD Link3 Display Serializer interrupt (CON_UB921_INTB)

[illegible][illegible][illegible]

SERDES



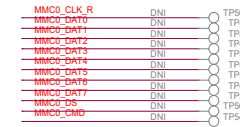
MMC Interface



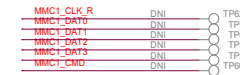
Via Probe Test Points

Place Near SOC

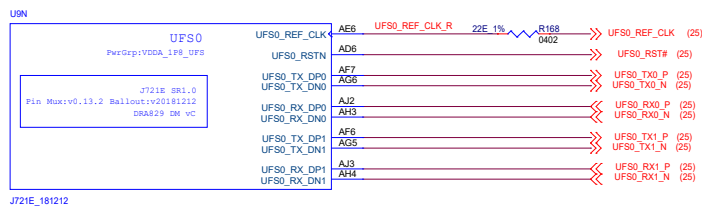
MMC0:

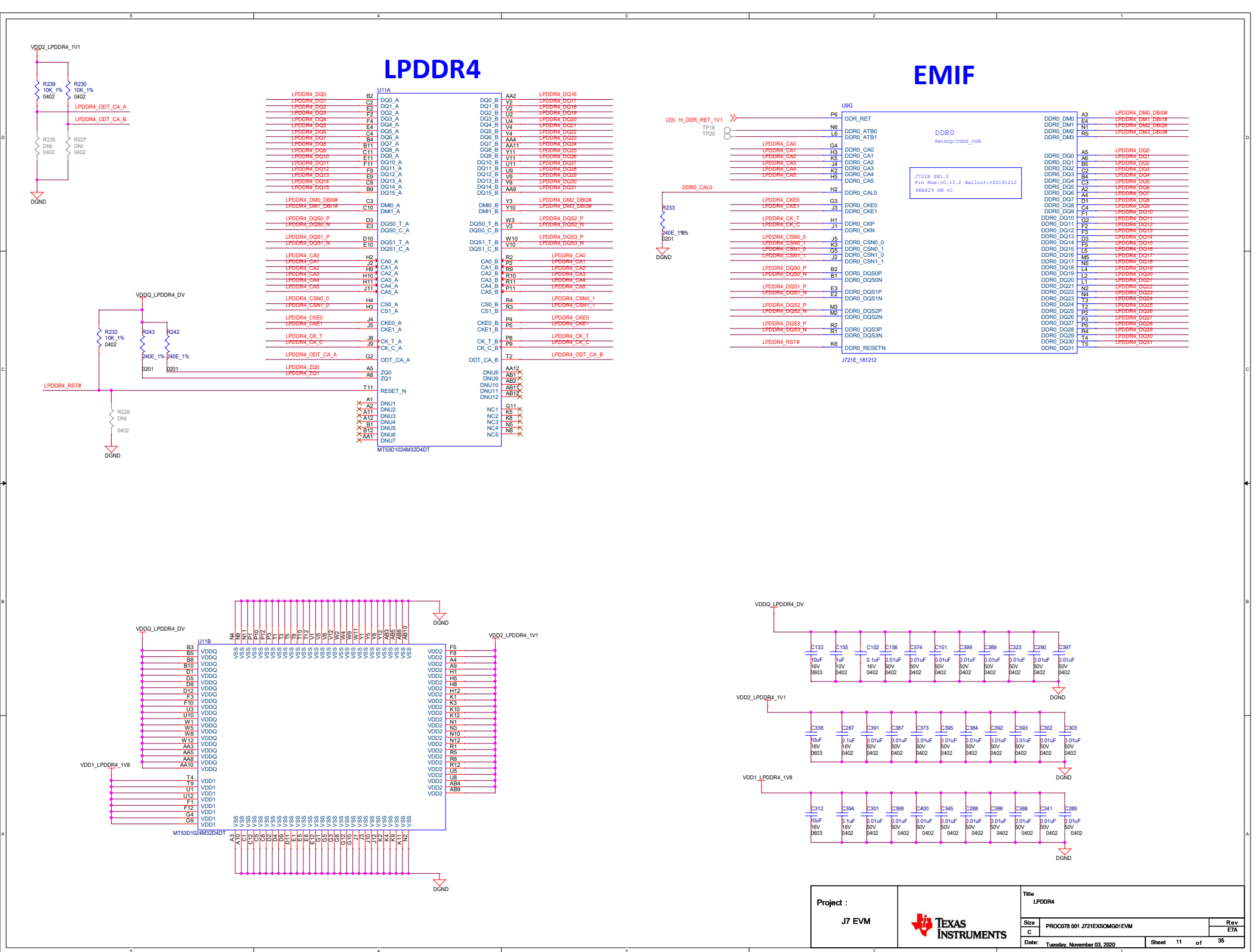


MMC1:



UFS Interface

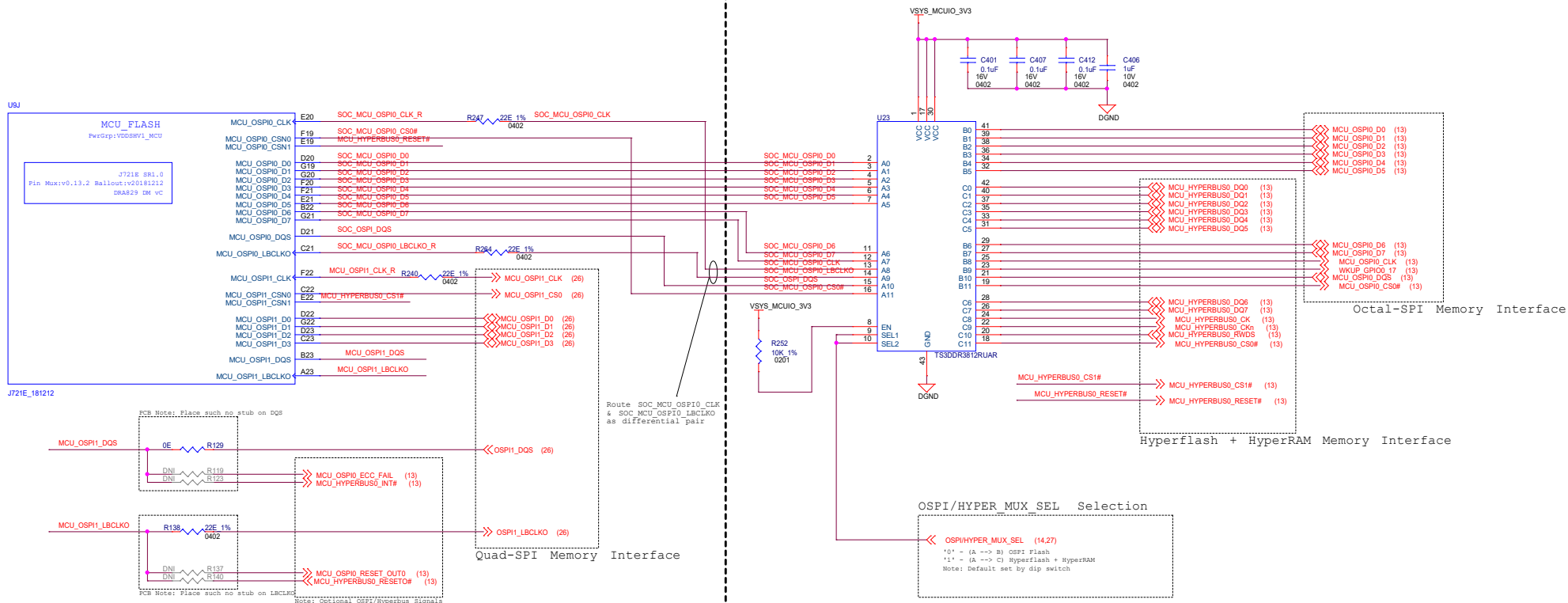




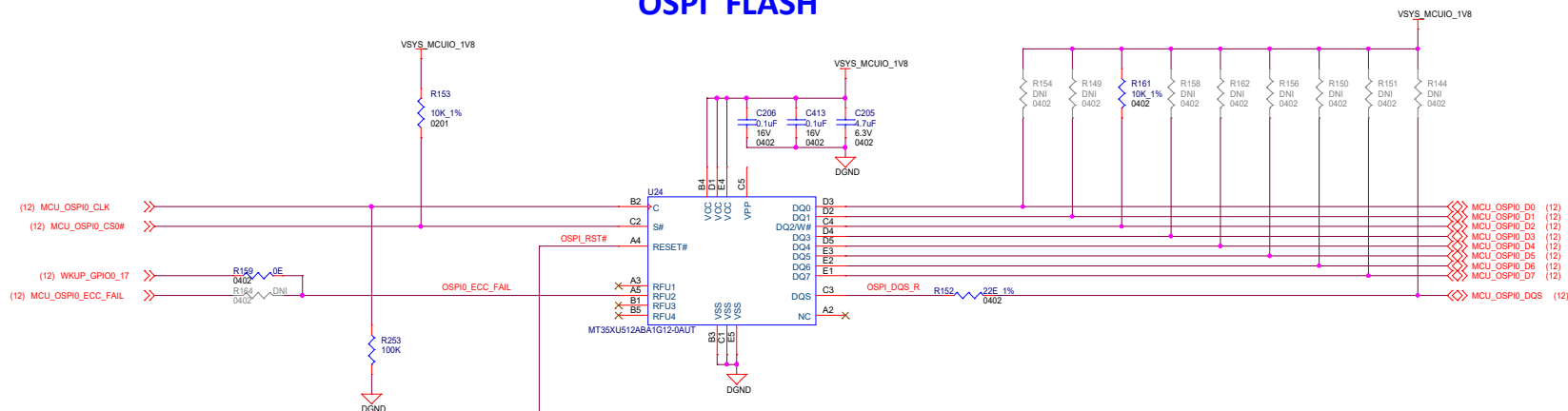
MCU FLASH

EVM development & evaluation test circuitry (TI EVM Only)

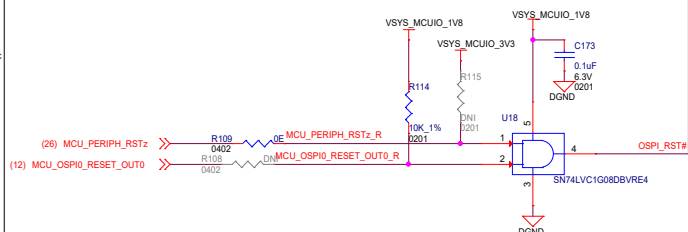
2:1 Mux for OSPI/HYBERBUS



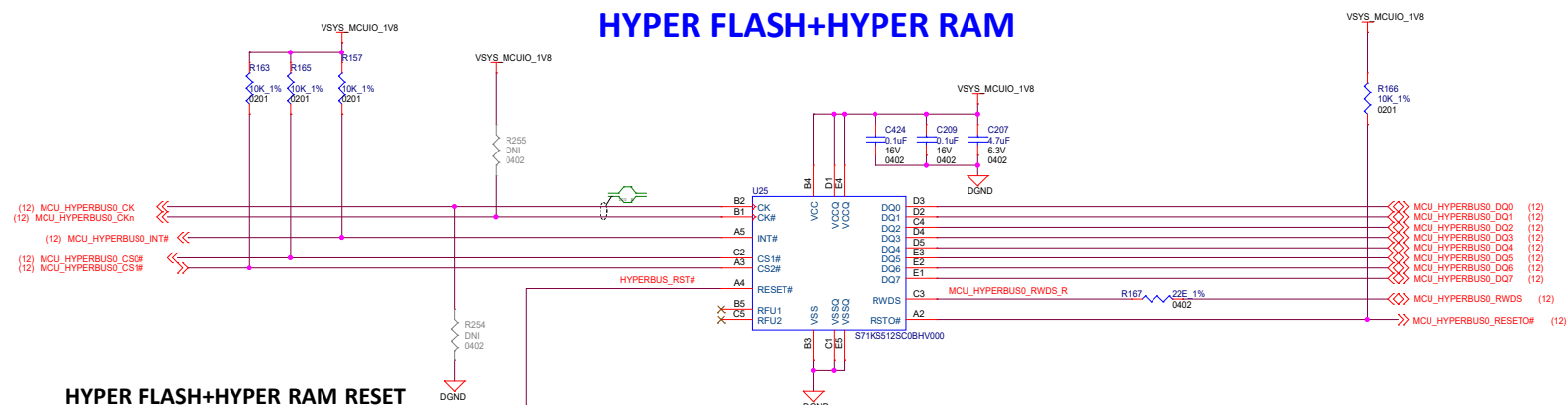
OSPI FLASH



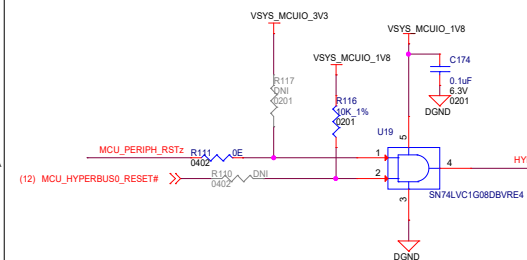
OSPI FLASH RESET



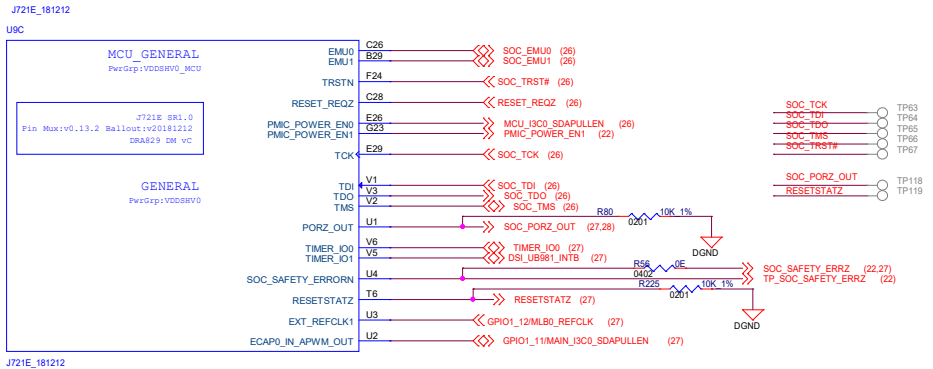
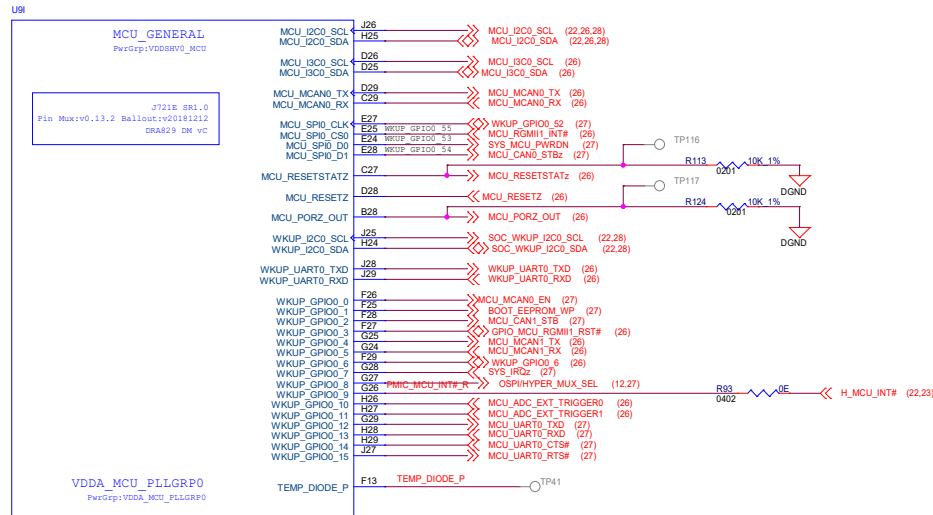
HYPER FLASH+HYPER RAM



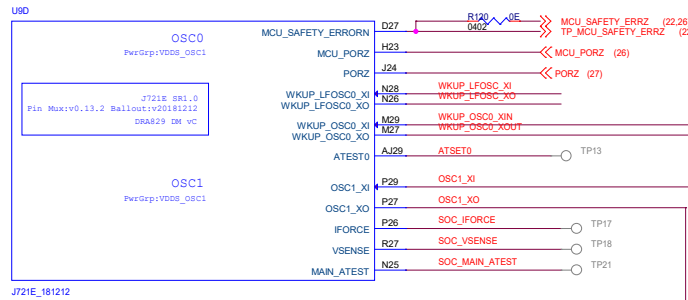
HYPER FLASH+HYPER RAM RESET



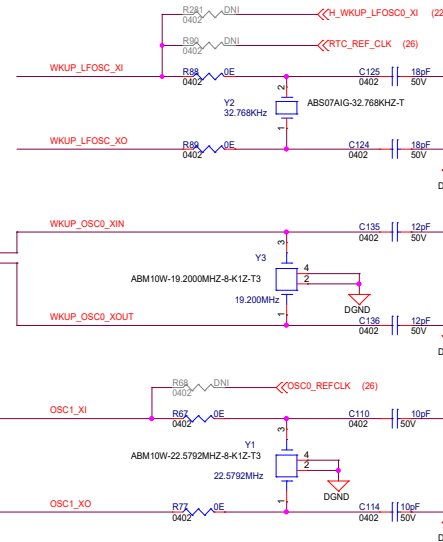
MCU & MAIN GENERAL IO, OSC CLKS



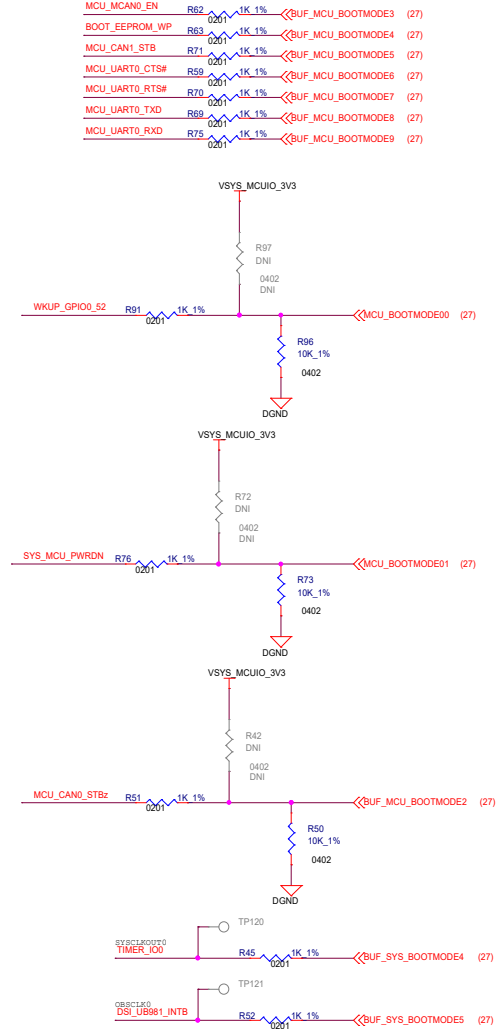
OSC



J721E_181212



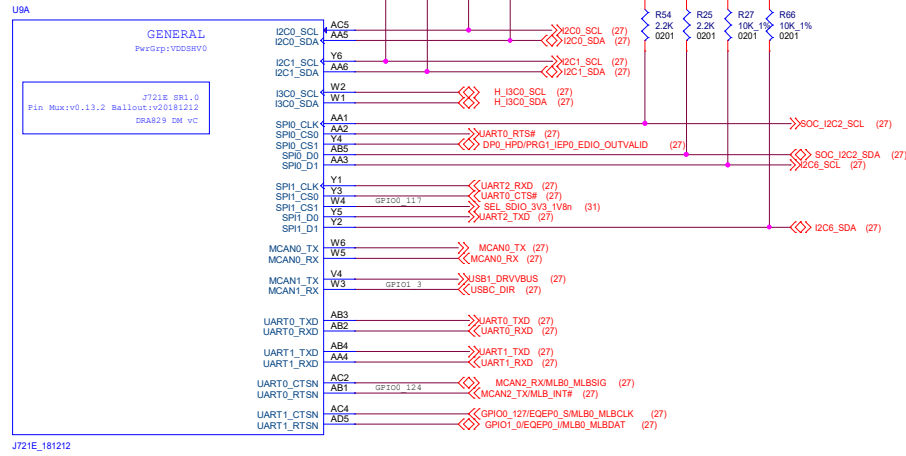
CLKS



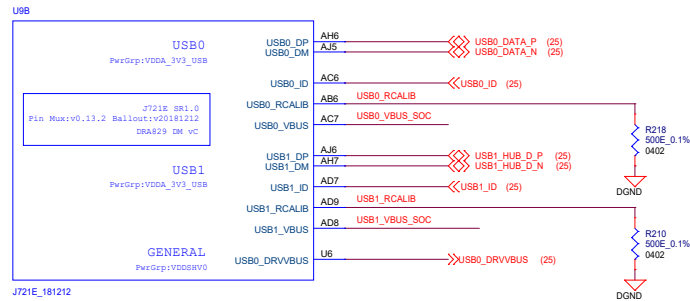
Project : J7 EVM		Title SOC_GENERAL&MCU_GENERAL	
C		Size PROC078 001 J721EXSOMG01EVM	Rev ETA
Date: Tuesday, November 03, 2020		Sheet 14	of 35



GENERAL

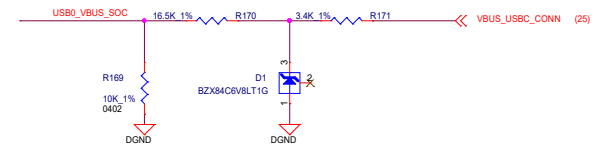


USB

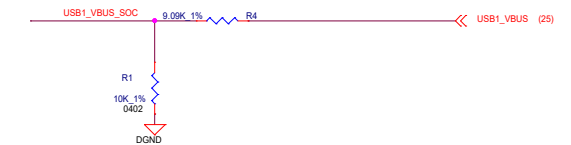


USB VBUS Resistor divider circuit

Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS



Note: Recommended VBUS circuit for embedded Hub



Project :

J7 EVM



Title
GENERAL_USB

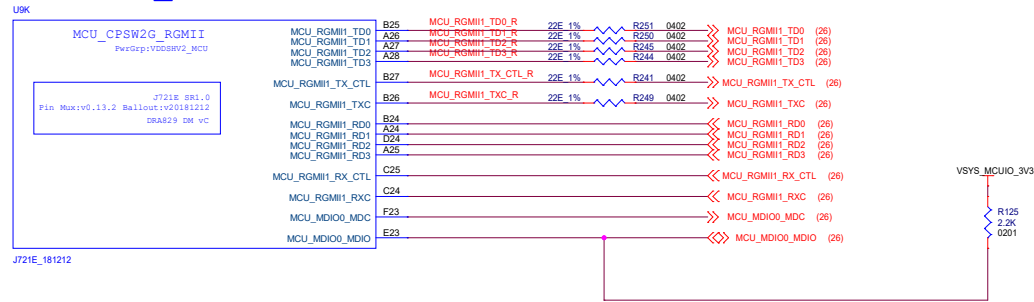
Size
C PROC078 001 J721EXSOMG01EVM

Date: Tuesday, November 03, 2020

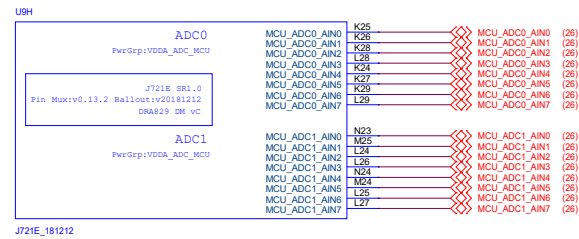
Rev
ETA

Sheet 15 of 35

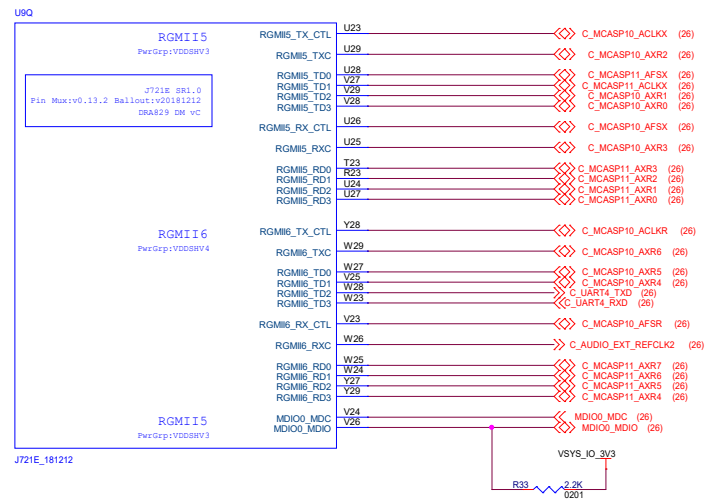
MCU_RGMII



MCU ADCs



MAIN RGMII



Project :

J7 EVM



Title
MCU_RGMII&MCU_ADC

Size
C PROC078 001 J721EXSOMG01EVM

Date: Tuesday, November 03, 2020

Sheet 16 of 35

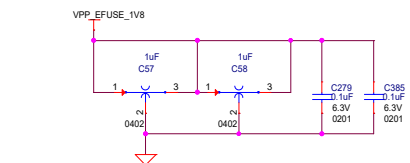
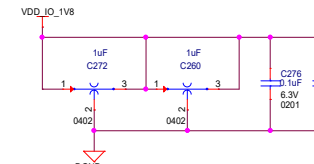
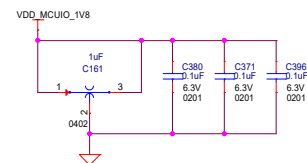
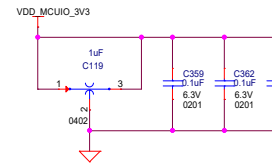
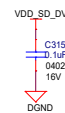
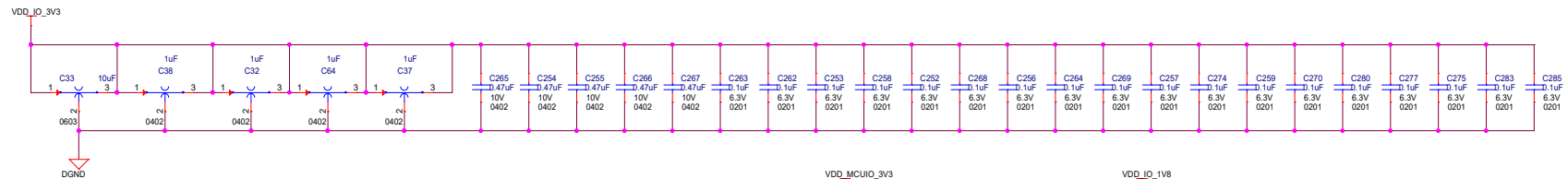
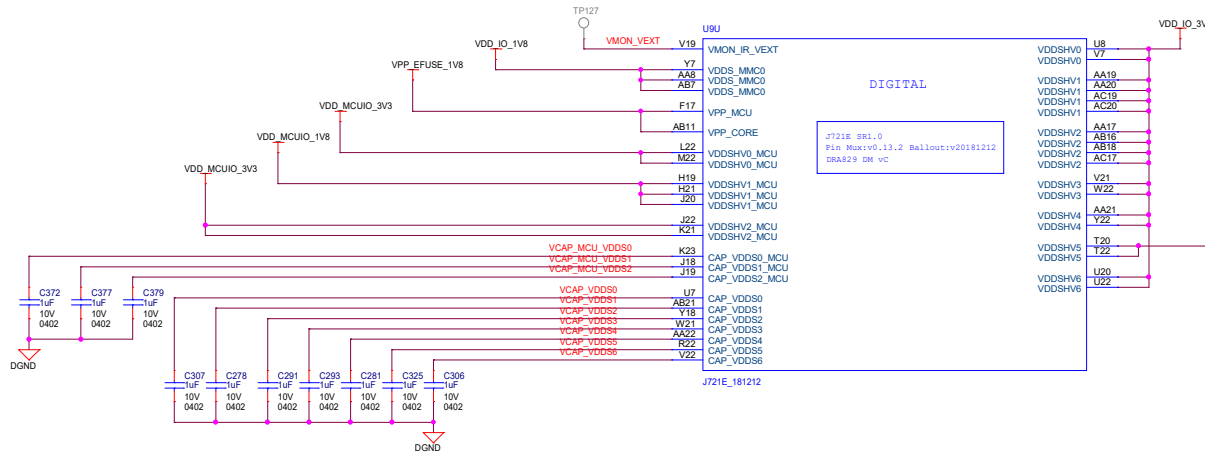
Rev
ETA

PRG0 & PRG1

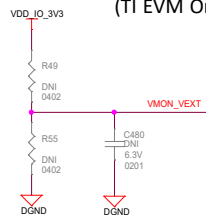


Title			
SOC POWER 1			
Size	PROC078 001 J721EXSOMG01EVM		Rev
C			ETB
Date:	Tuesday, November 03, 2020	Sheet	18 of 35

DIGITAL POWER 2



EVM development & evaluation test circuitry (TI EVM Only)



Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

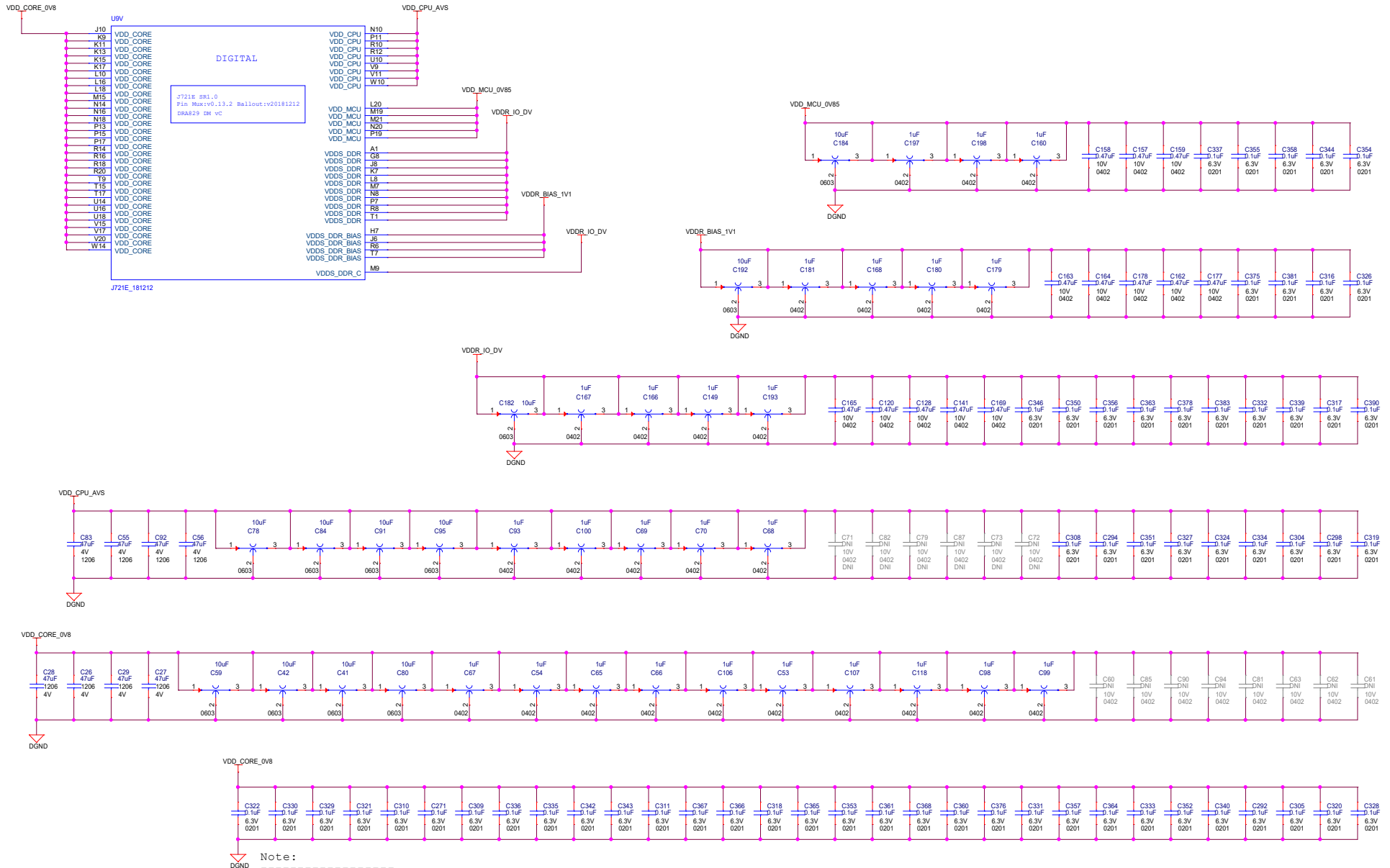
Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Project :
J7 EVM



Title		
SOC POWER 2		
Size	Rev	
C	PROC078 001 J721EXSOMG01EVM	ETA
Date:	Tuesday, November 03, 2020	Sheet 19 of 35

DIGITAL POWER 3



Note:

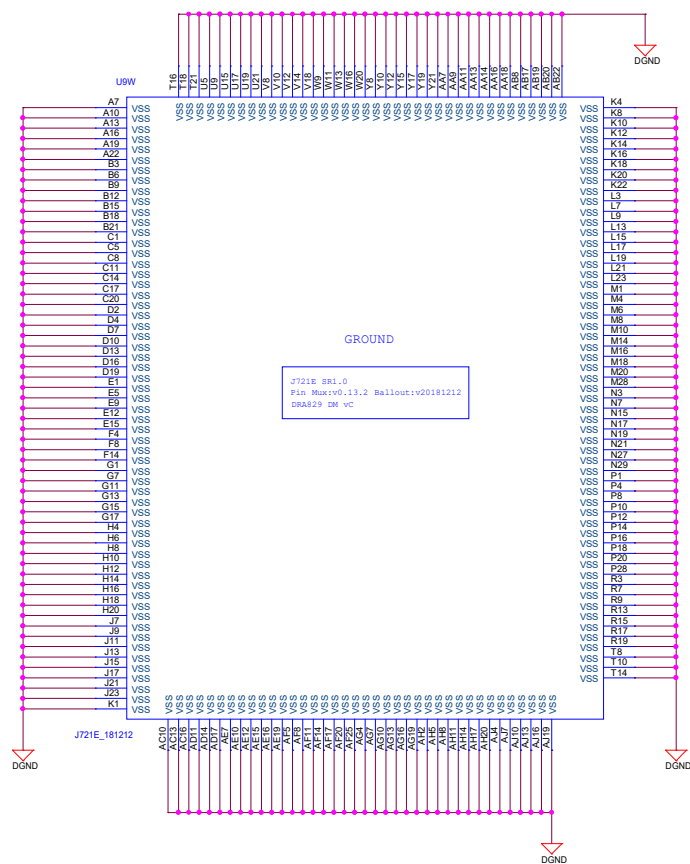
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Z_t).

Project :		Title	
J7 EVM		SOC POWER 3	
Size	PROC078 001 J721EXSOMG01EVM	Rev	ETA
C			
Date:	Tuesday, November 03, 2020	Sheet	20 of 35

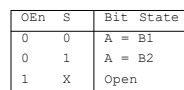


SOC GROUND

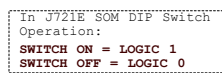


(TI EVM Only)

SW1.2	Port State	Function
Open	A = B1	SoC I2C to PMIC I2C
Close	A = B2	EXT I2C to PMIC I2C



SW3.1	SYS SAFETY ERRn
Open	MCU_SAFETY_ERRn
Closed	Active low, SoC ERRn or MCU ERRn



2-Phase VDD_CPU PDNs Not Recommended for New Designs

PMIC- A

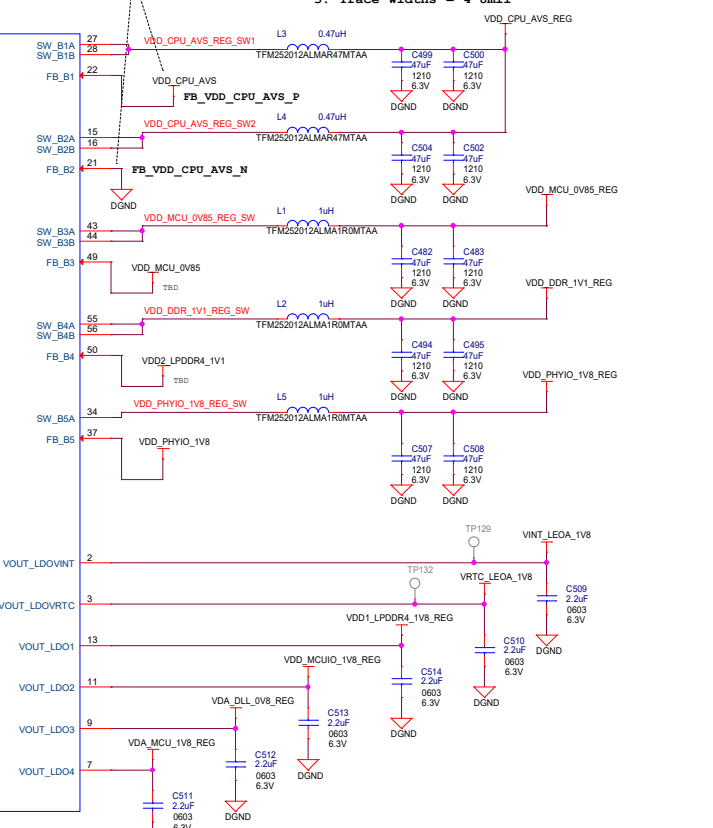
[illegible]

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:

1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace as close as possible, to power & Gnd via or across Decap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil. Try to keep traces near each other as best as possible, while

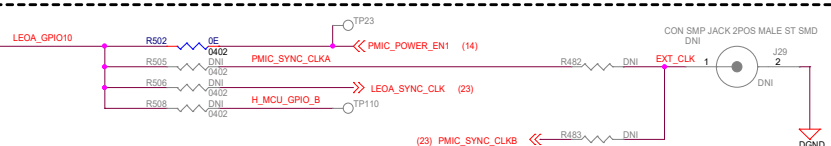
For single phase Buck converters, route remote sense feedback as follows:

1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace as close as possible, to a power via near in middle of SOC power ball group
3. Trace widths = 4-8mil"




2-Phase VDD_CPU PDNs Not Recommended for New Designs

**ALL New Designs should use
3-Phase Buck supplying VDD_CPU
(see SCH's last page)**



(EVM Bd Setting & Leo NVM Default):			
SW2	COM	GPIO: Type	NVM Funtion
-1 = Open (Low) = Closed(High)	LEOA_WDOG_DISABLE Alt_GPIO	In/Out	Disable WDOG Alt NVM
-2 = Open (Low) = Closed(High)	Enable WDOG Timer Disable WDOG Timer	In In	Enable WDOG Disable WDOG

Project : J7 EVM	 TEXAS INSTRUMENTS	Title POWER SUPPLY 1	
		Size C	PROC078 001 J721EXSOMG01EVM
		Rev E7B	
		Date: Friday, November 13, 2020	Sheet 22 of 35

PMIC - B

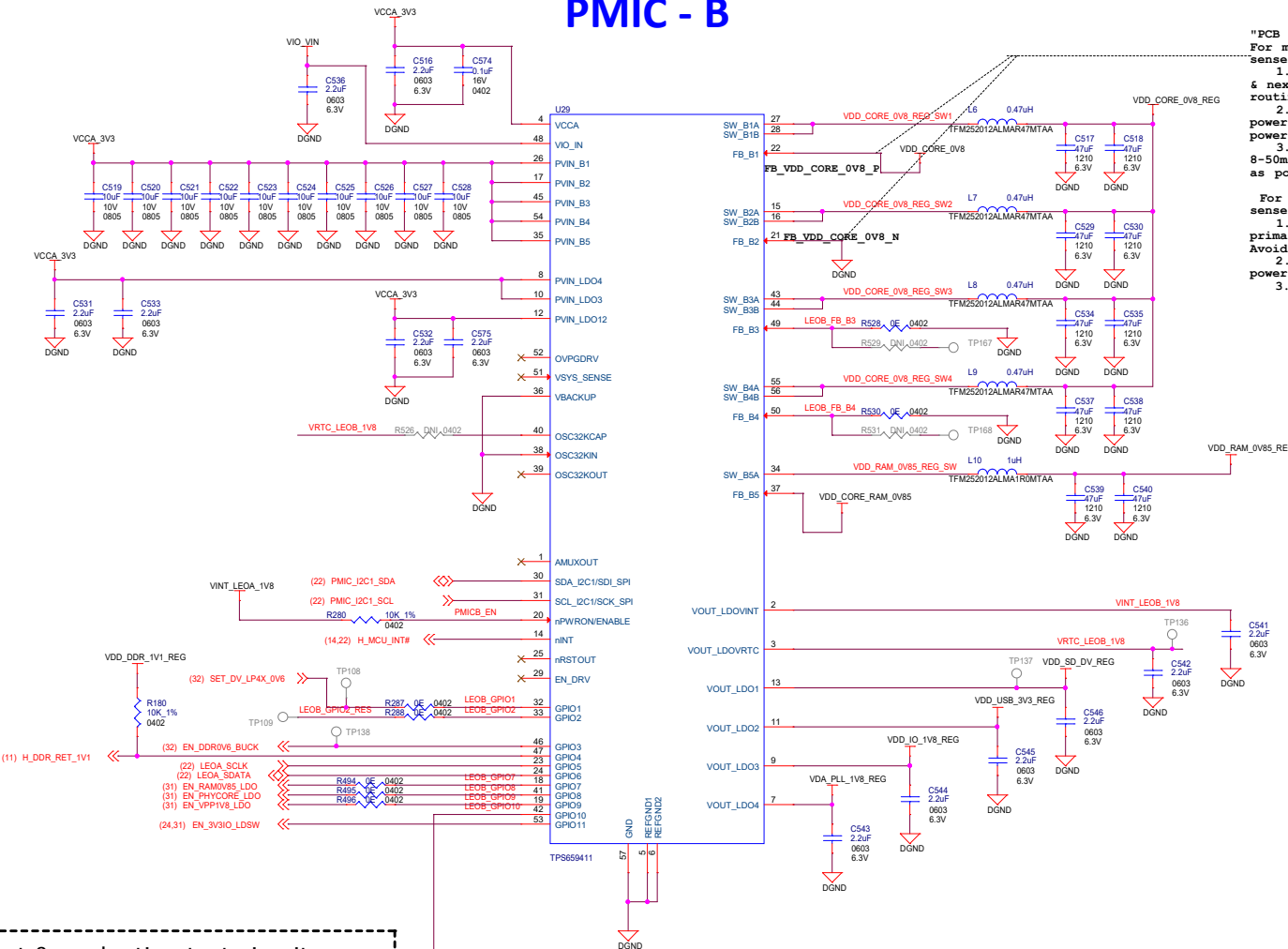
```

"PCB Notes:
For multi-phase Buck converter configs, route remote
sense feedback as follows:
- Pseudo differential pair traces on same layer
  & next to primarily power plane segment. Avoid
  routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to
  & Gnd vias or across Dcap in middle of SOC
  power rail group
3. Trace widths = 4-8mil & separation distance =
  8-50mil, try to keep traces near each other as best
  as possible while

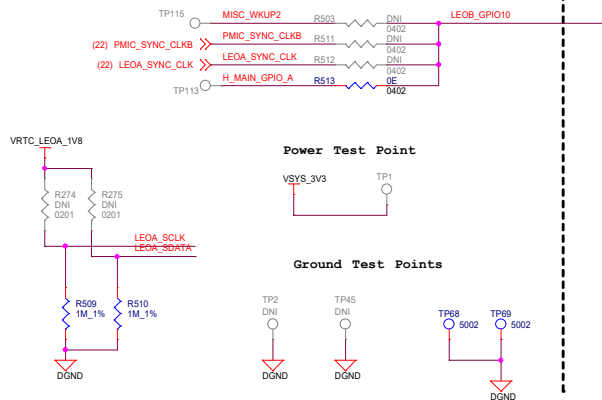
```

For single-phase Buck converters, route remote sense feedback as follows:

1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

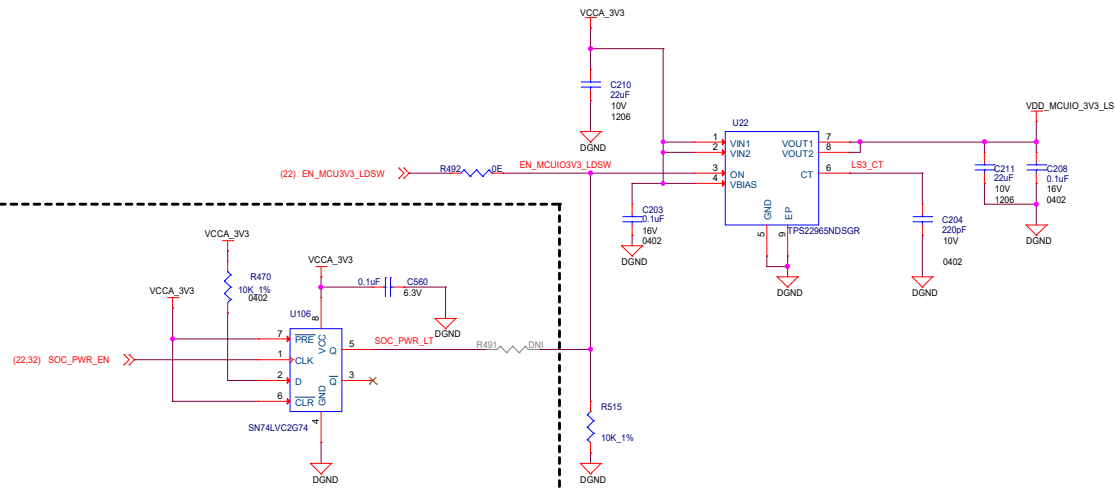


EVM development & evaluation test circuitry (TI EVM Only)

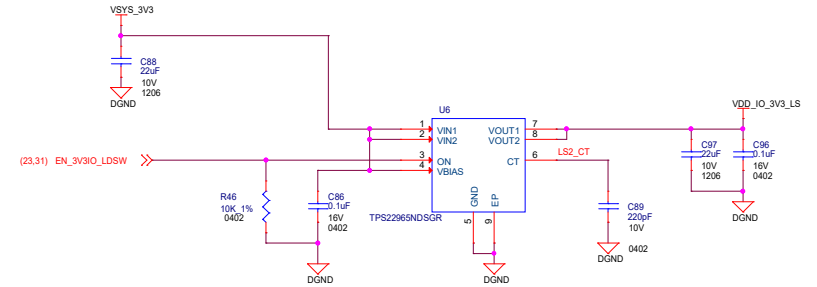


PMIC-B uses NVM to set I2C ADDR:
0x4C, 0x4D, 0x4E & 0x4F

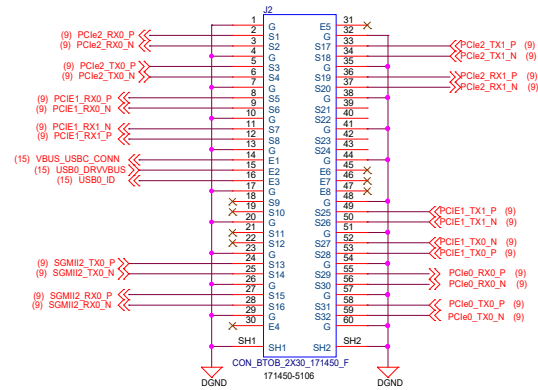
LOAD SWITCHES



EVM development & evaluation test circuitry
(TI EVM Only)



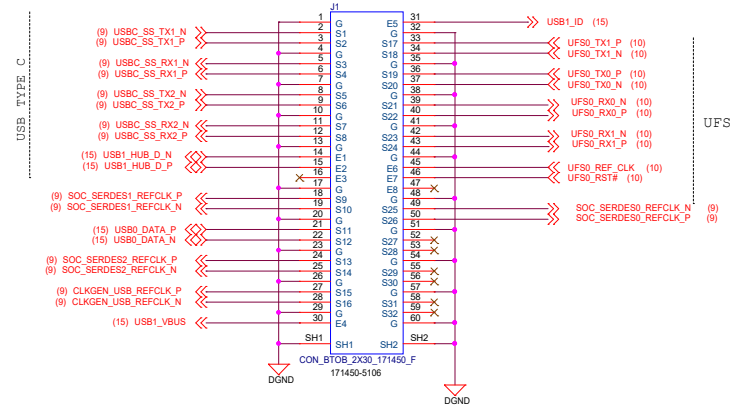
SOM to COMM PROC SERDES CONNECTORS



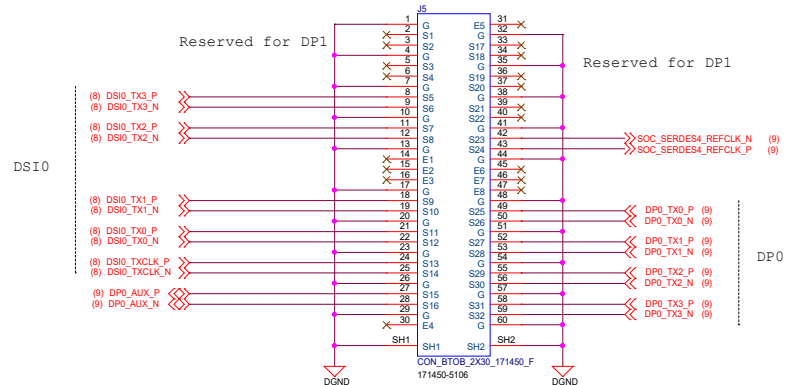
PCIe0-PCIe x1 Lane

PCIe1-PCIe x2 Lane

PCIe2-PCIe M.2



UFS



DP0

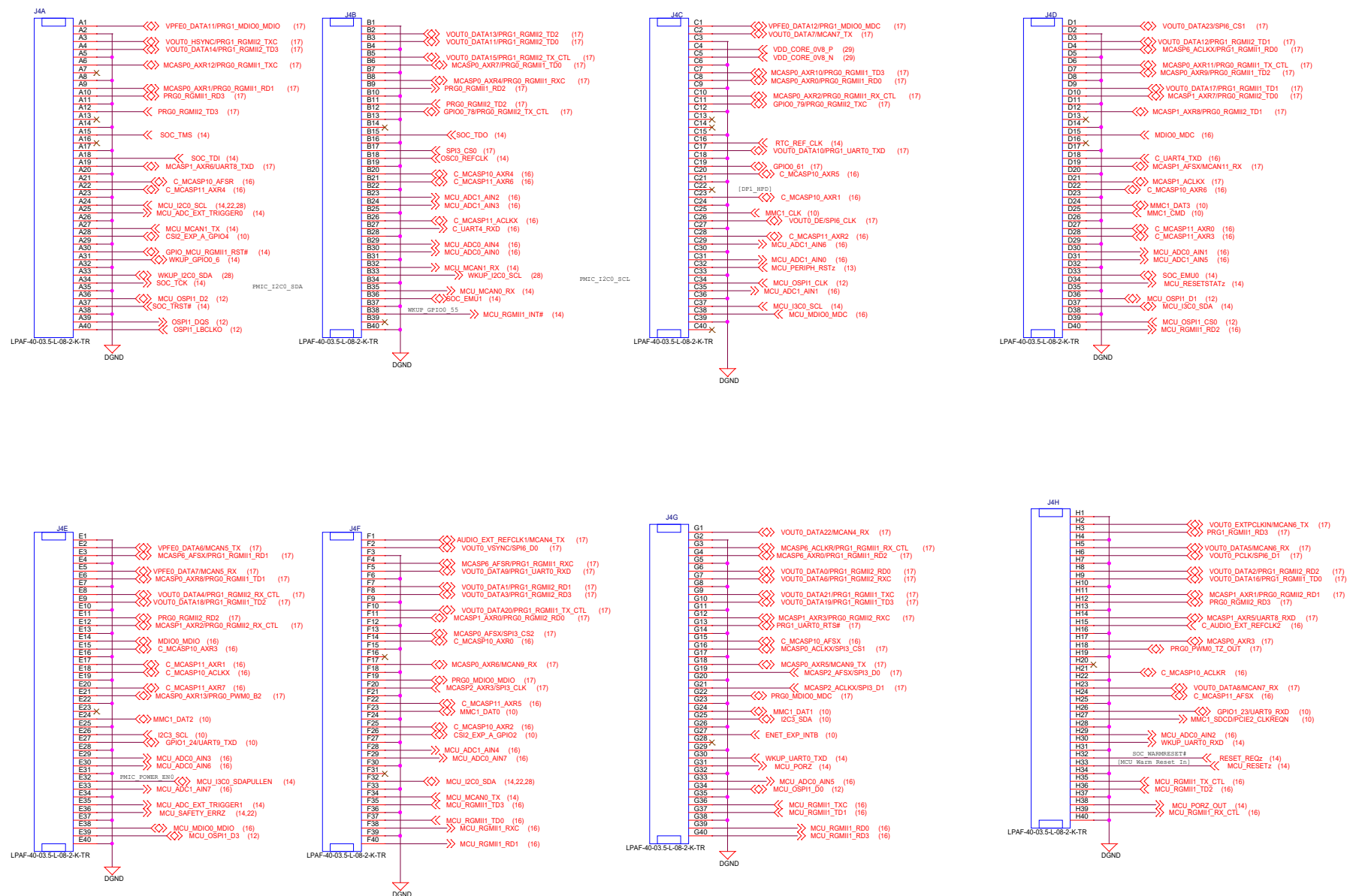
Project :

J7 EVM

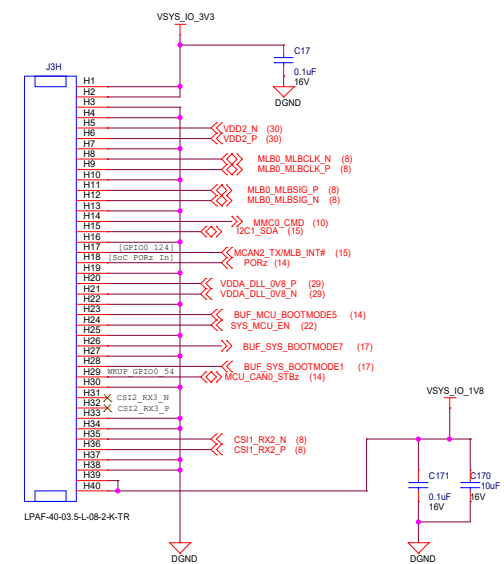
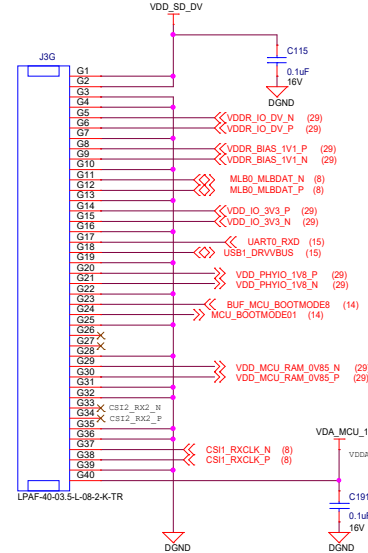
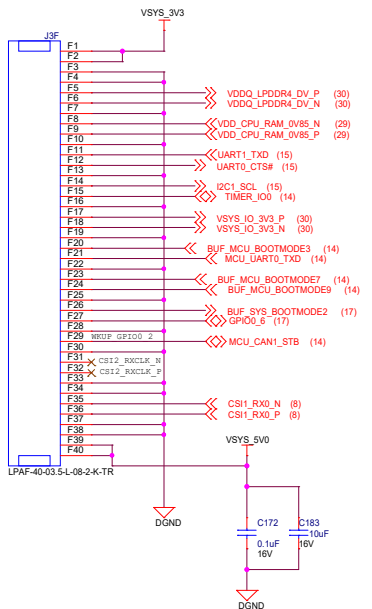
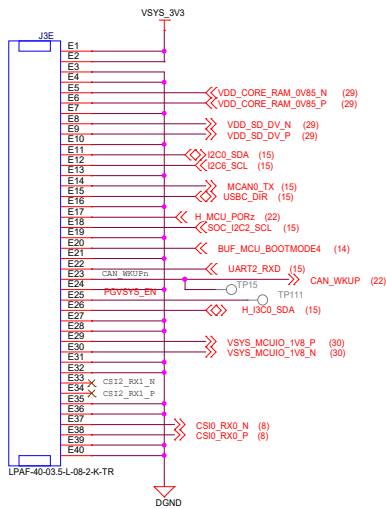
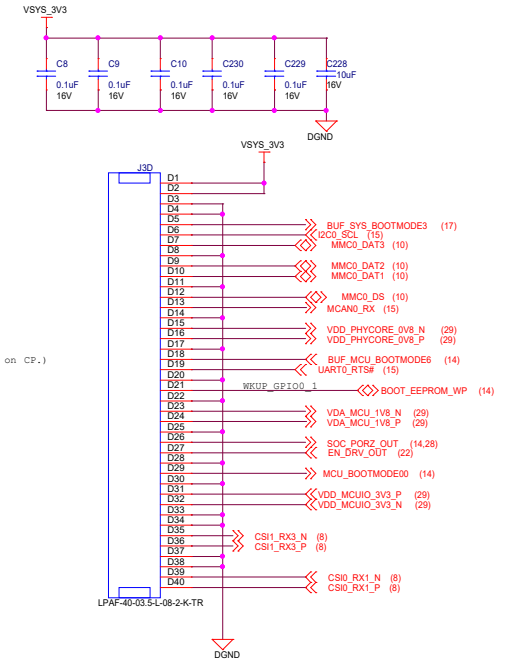
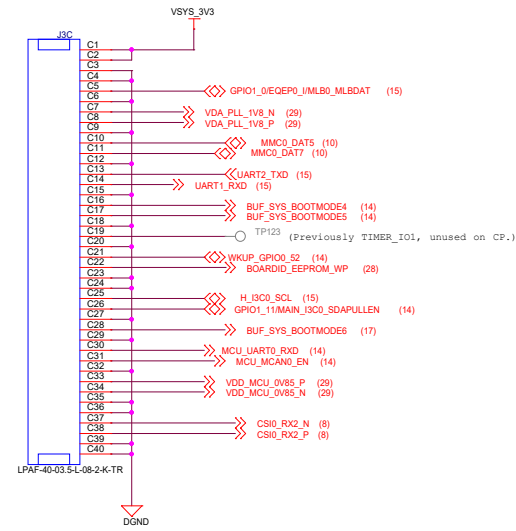
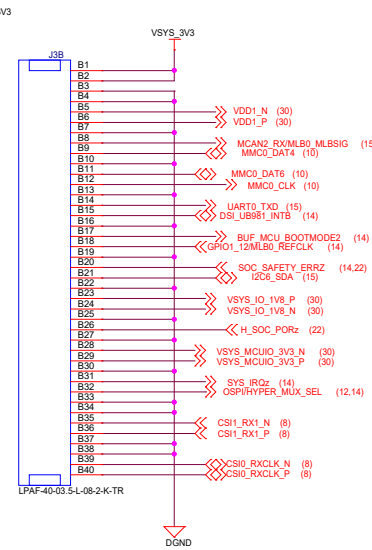
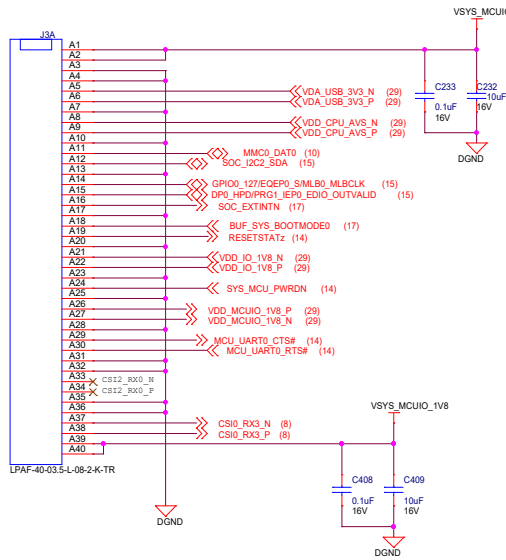


Title		
SOM B-B MOLEX CONNECTORS		
Size	Rev	
C	ETA	
Date: Tuesday, November 03, 2020		Sheet 25 of 35

SOM to COMM PROC PRIMARY CONN #1

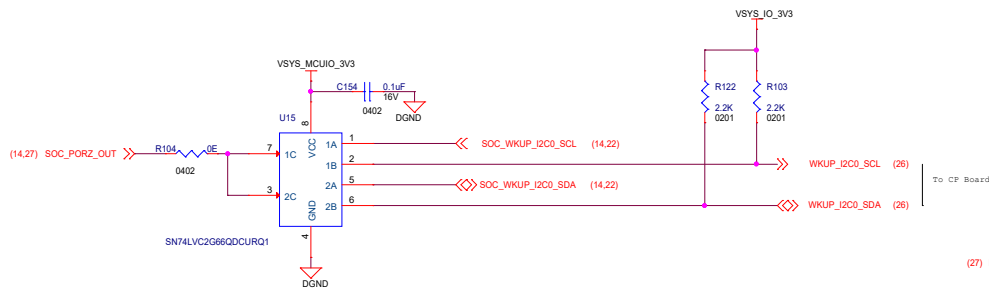


SOM to COMM PROC PRIMARY CONN #2

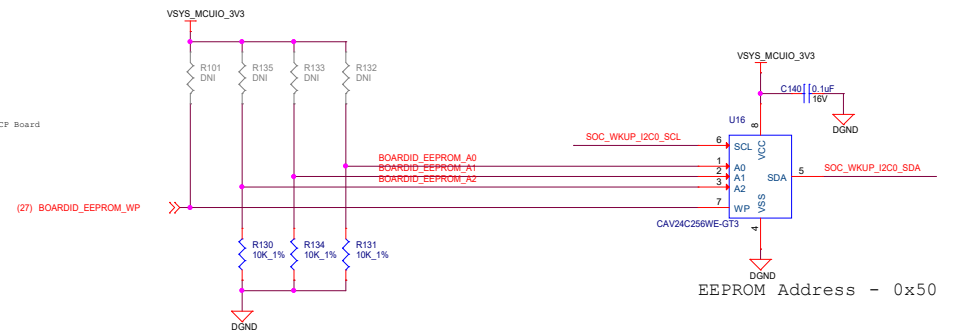


EVM development & evaluation test circuitry (TI EVM Only)

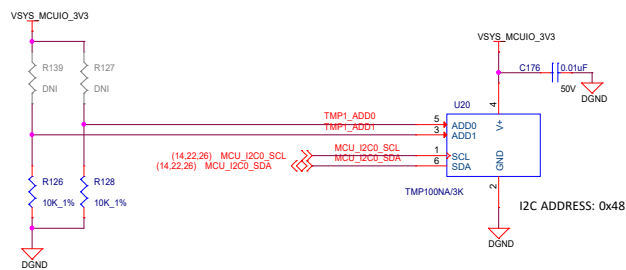
I2C for BOARD ID EEPROMs



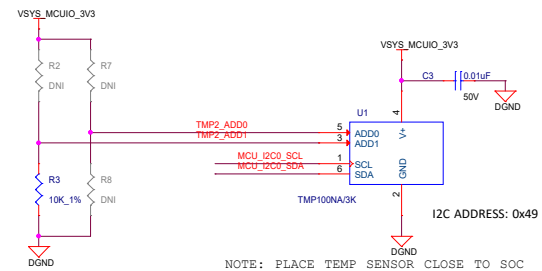
BOARD ID EEPROM (TI EVM Only)



TEMPERATURE SENSORS (TI EVM Only)



NOTE: PLACE TEMP SENSOR CLOSE TO Power Section



NOTE: PLACE TEMP SENSOR CLOSE TO SOC

Project :

J7 EVM



Title
CLOCK, Board ID EEPROM, TEMP SENSORS

Size
PROC078 001 J721EXSOMG01EVM

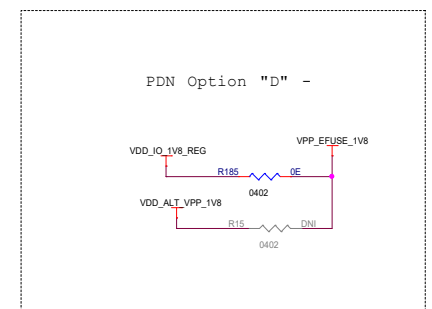
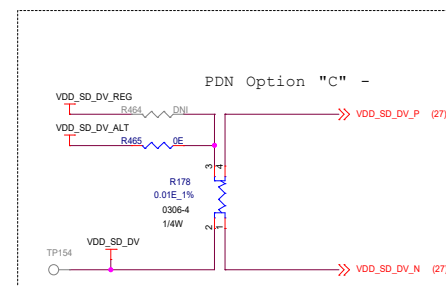
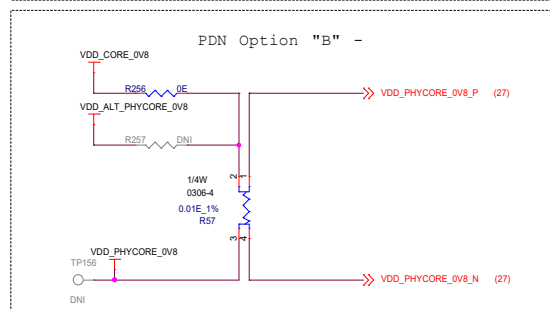
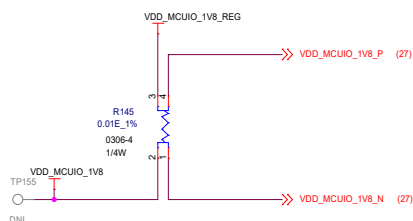
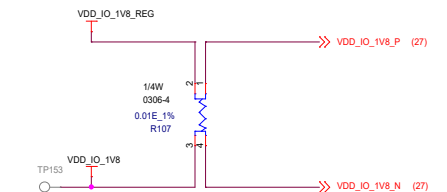
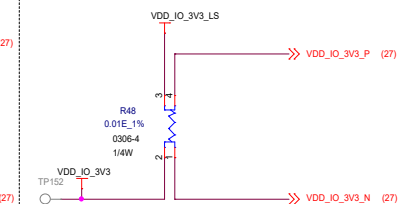
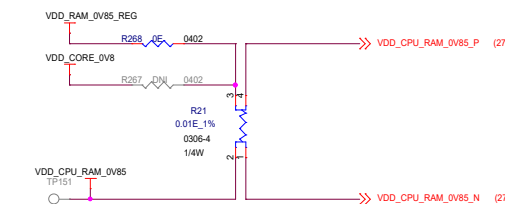
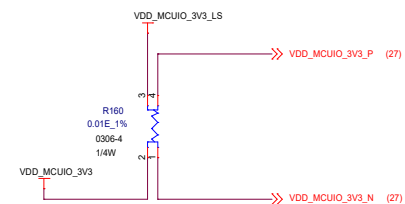
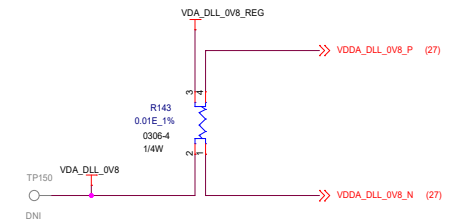
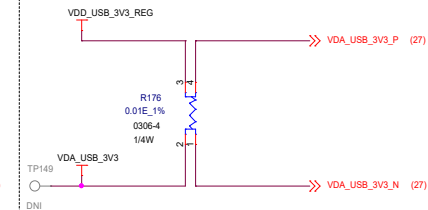
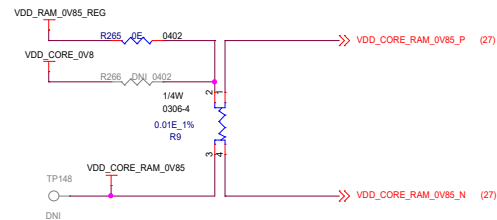
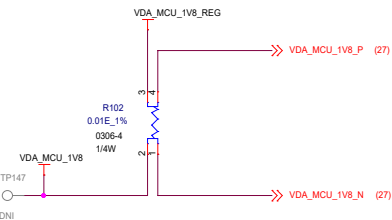
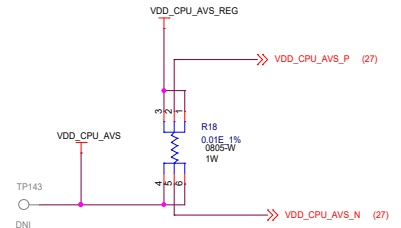
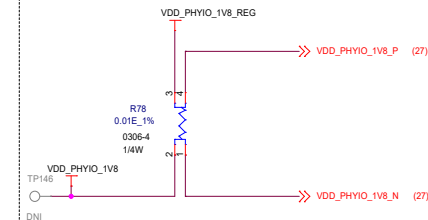
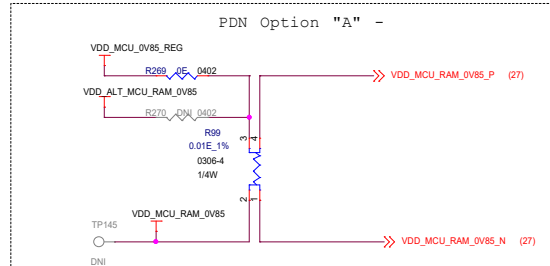
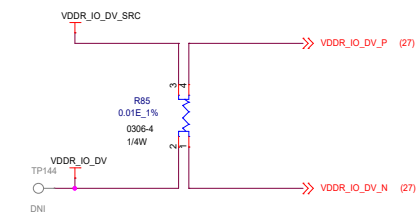
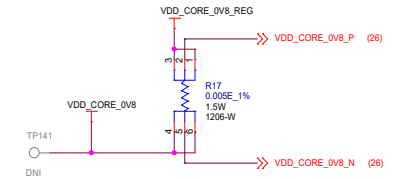
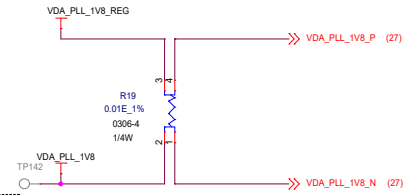
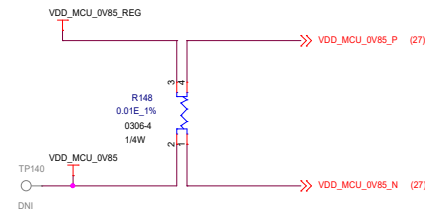
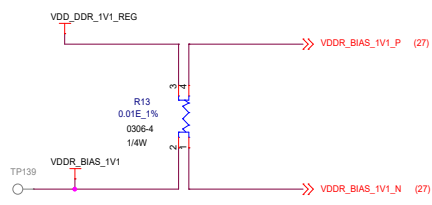
Date: Tuesday, November 03, 2020

Sheet 28 of 35

Rev
ETA

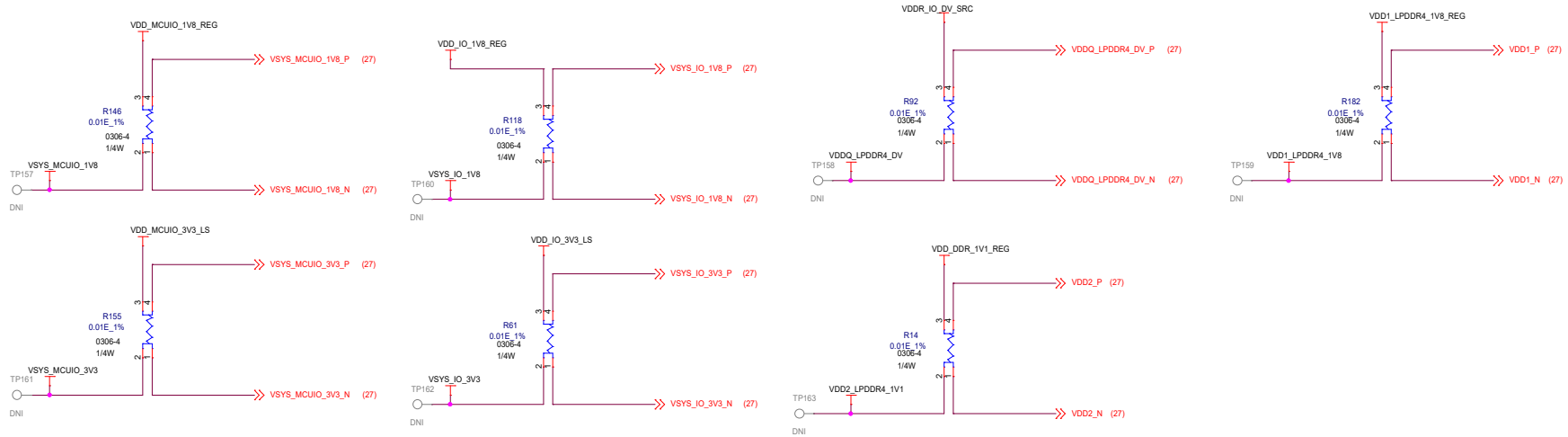
SOC Current Sense Resistors

EVM development & evaluation test circuitry (TI EVM Only)

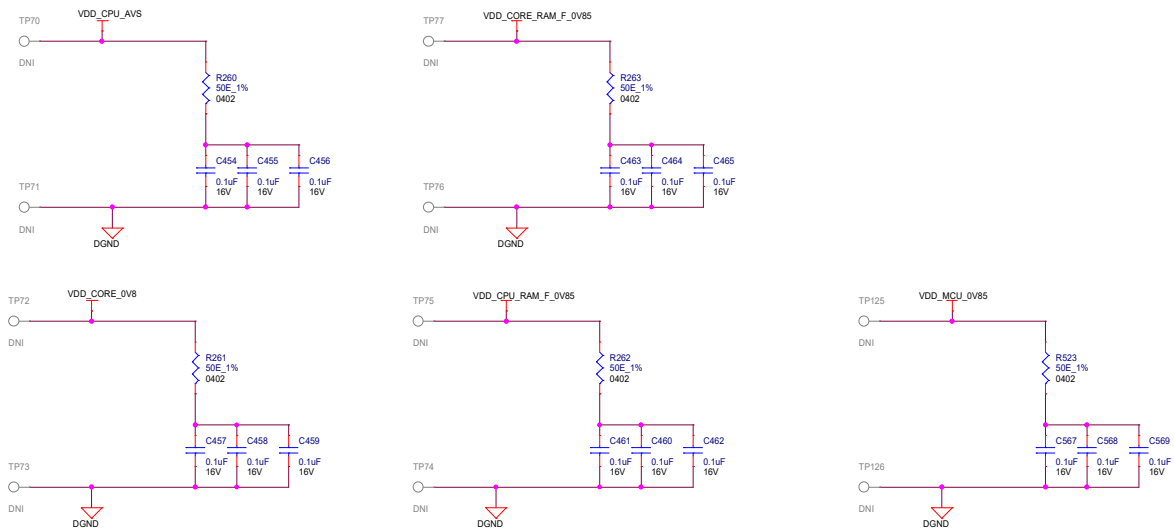


EVM development & evaluation test circuitry (TI EVM Only)

Peripheral Current Sense Resistors



Supply Rail Kelvin Sensing



ALTERNATE POWER SUPPLY OPTIONS A - D

EVM development & evaluation test circuitry

(TI EVM Only)

TI Internal Evaluations Only

Alternate power resources have been shown for functional & electrical testing on a few key SoC voltage domains.

PDN Options -

A) Evaluate common 0.85V Buck resource for both MCU CORE and MCU RAM array domains.

Evaluate common 0.85V Buck resource for both Main CORE and Main CORE & CPU RAM arrays.

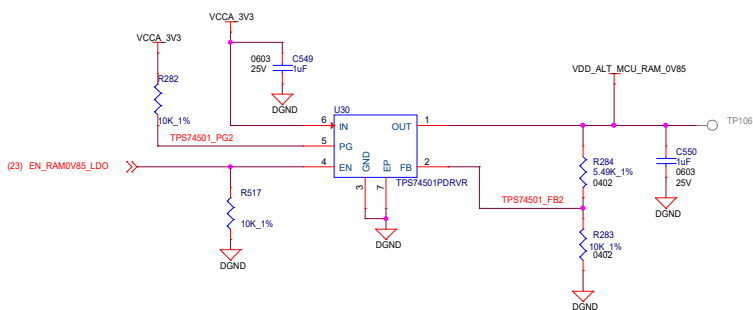
On EVM boards, PDN options for independent RAM domains are required to support RMA device testing & trouble-shooting.

B) Evaluate an independent low noise LDO for supplying VDD_PHYCORE_0V8 power rail & high speed SERDES (i.e. Sierra, Torrent) PHY Core domains.

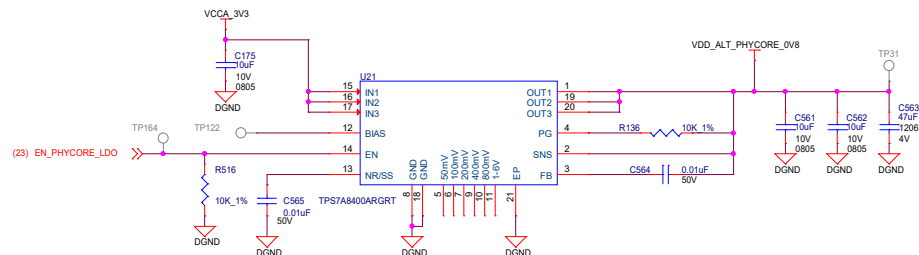
C) Evaluate a Dual LDO source for VDD_SD_DV that can change voltage level using GPIO control signal.

D) Evaluate a standard, low-impedance PMIC LDO or "Tri-State-able", high-impedance LDO for supplying VPP_EFUSE_1V8 power rail & domain.

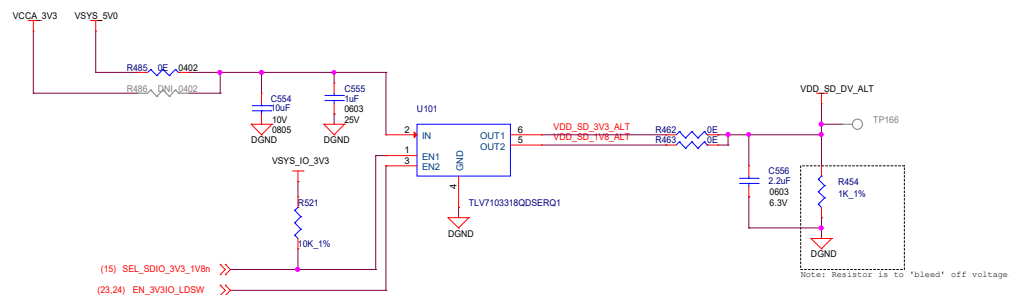
PDN Option - A: VDD_MCU_RAM_0V85_ALT rail's source



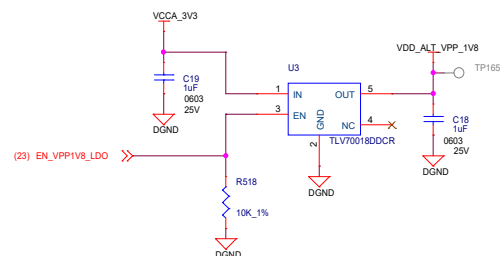
PDN Option - B: VDD_PHYCORE_0V8_ALT rail's source



PDN Option - C: VDD_SD_DV_ALT rail's source



PDN Option - D: VDD_VPP_1V8_ALT rail's source

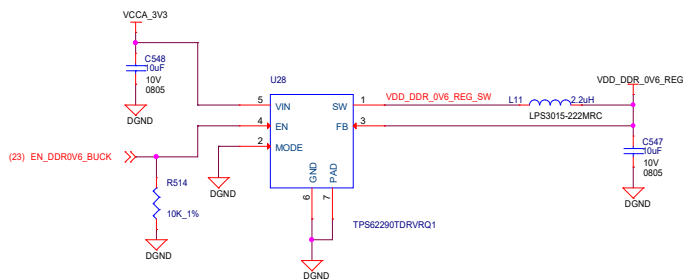


VDD_SD_DV_ALT	EN1	EN2	Comments
3.3V	HIGH	HIGH	Both enables driven high during power up seq to support initial 3.3V signaling per SD card protocol
1.8V	LOW	HIGH	SW controls & transition Sd card to high speed 1.8V signaling if card type supports

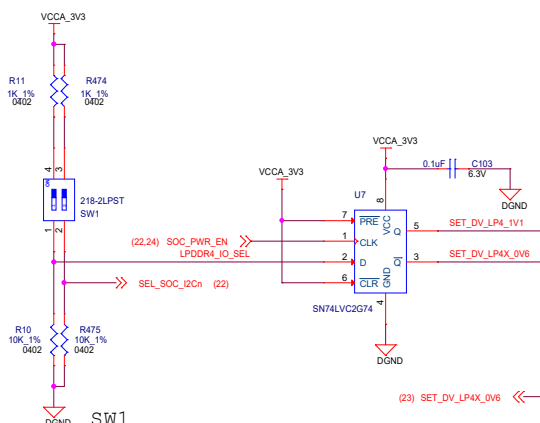
EVM development & evaluation test circuitry (TI EVM Only)

ALTERNATE LPDDR4X POWER SUPPLY OPTION

0.6V BUCK CONVERTER

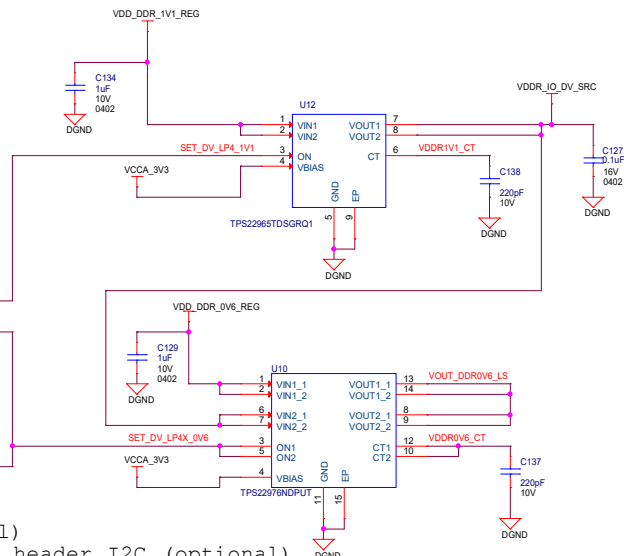


LP4 vs. LP4x SELECTION



- SW1
Pos1 - ON/High = LPDDR4 (default)
OFF/Low = LPDDR4x (optional)
Pos2 - ON/High = PMIC I2C to Ext header I2C (optional)
OFF/Low = PMIC I2C to SoC WKUP I2C (default)

LP4 vs. LP4x VIO ISOLATION



Project :

J7 EVM



Title
<Title>

Size	Rev
C	ETA
Date: Tuesday, November 03, 2020	Sheet 32 of 35

EVM Development & Evaluation test circuitry

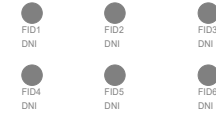
(TI EVM Only)

NOTES, HW & LABELS

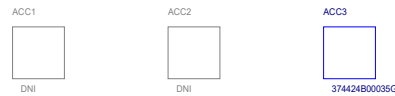
ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

FIDUCIALS



SOCKET, PROCESSOR & HEATSINK AS ACCESSORIES



BARE PCB



LABELS

Board Serial No.



EVM Orderable No.



Assembly Revision.



Orderable Part Numbers

Variant	Label Text
001 = Soldered GP SoC	J721EXSOMG01EVM
002 = Soldered HS SoC	J721EXSOMH01EVM
003 = Socketed SoC	J721EXSOMS01EVM

LOGOs



Project :

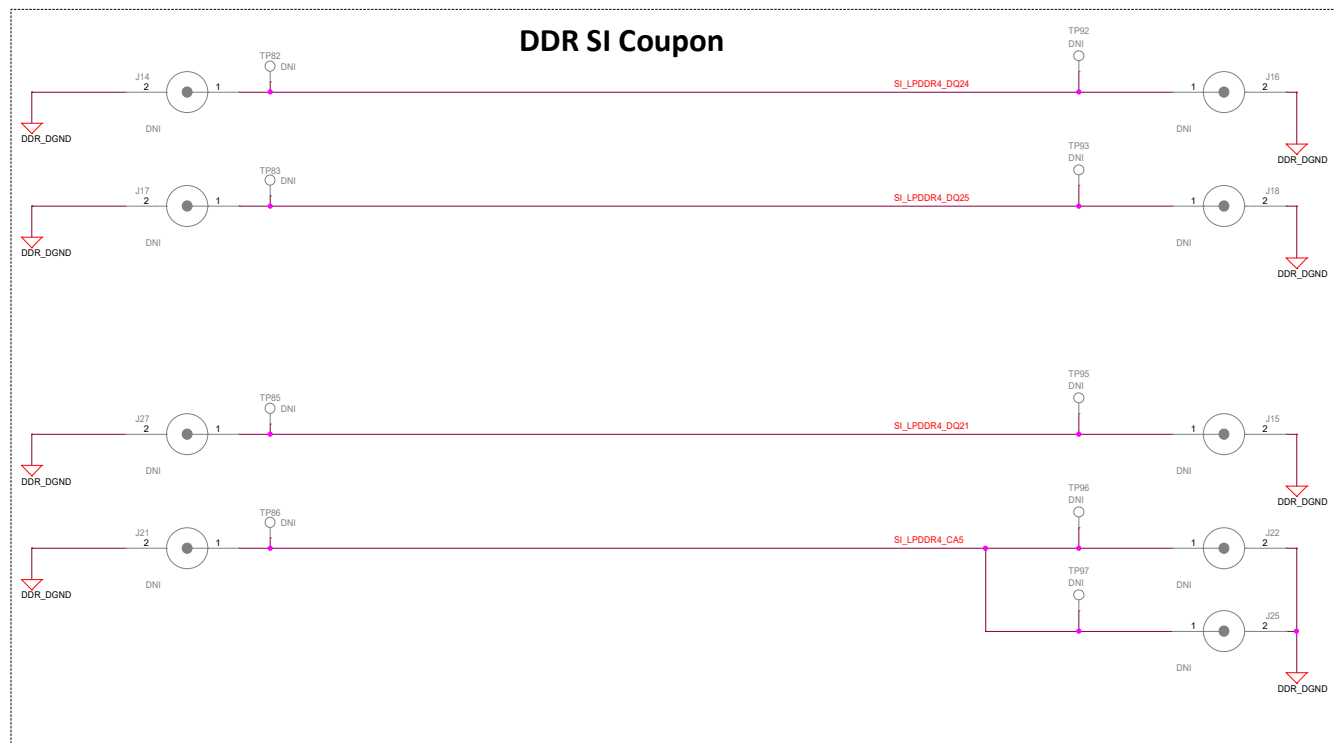
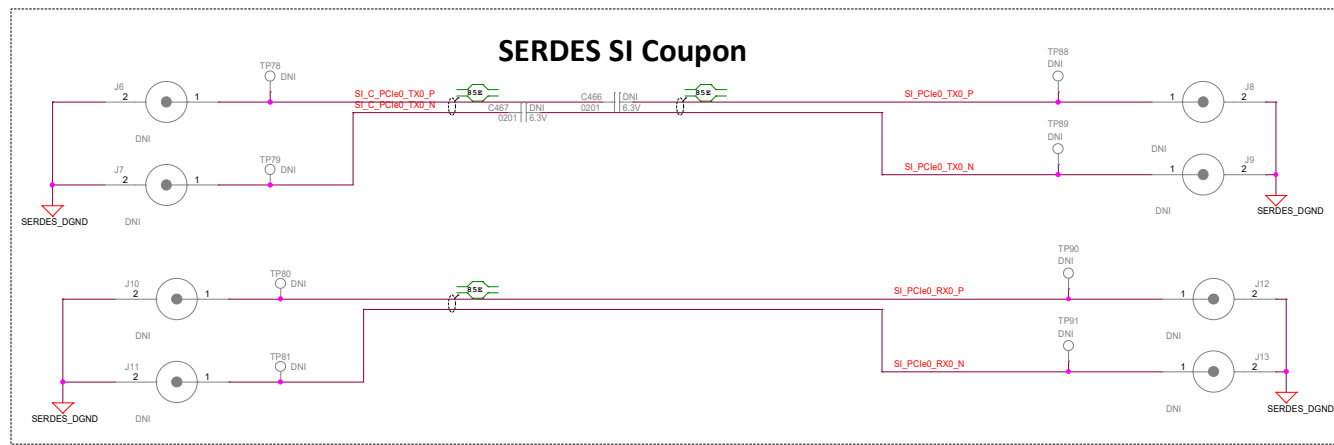
J7 EVM



Title
HARDWARE SCHEMATICS

Size	Rev
C	ETA
Date: Tuesday, November 03, 2020	Sheet 33 of 35

Note: Test coupon not part of EVM design, to be used for TI test only



ALL New Designs should use
3-Phase Buck supplying VDD_CPU
(Dual Leo PDN or Leo + Hera PDN)

ALL New Designs should use
3-Phase Buck supplying VDD_CPU
(Dual Leo PDN or Leo + Hera PDN)

3-Phase DUAL PMIC PDN Recommended for New Designs
(3-Phase Buck supplying VDD_CPU)

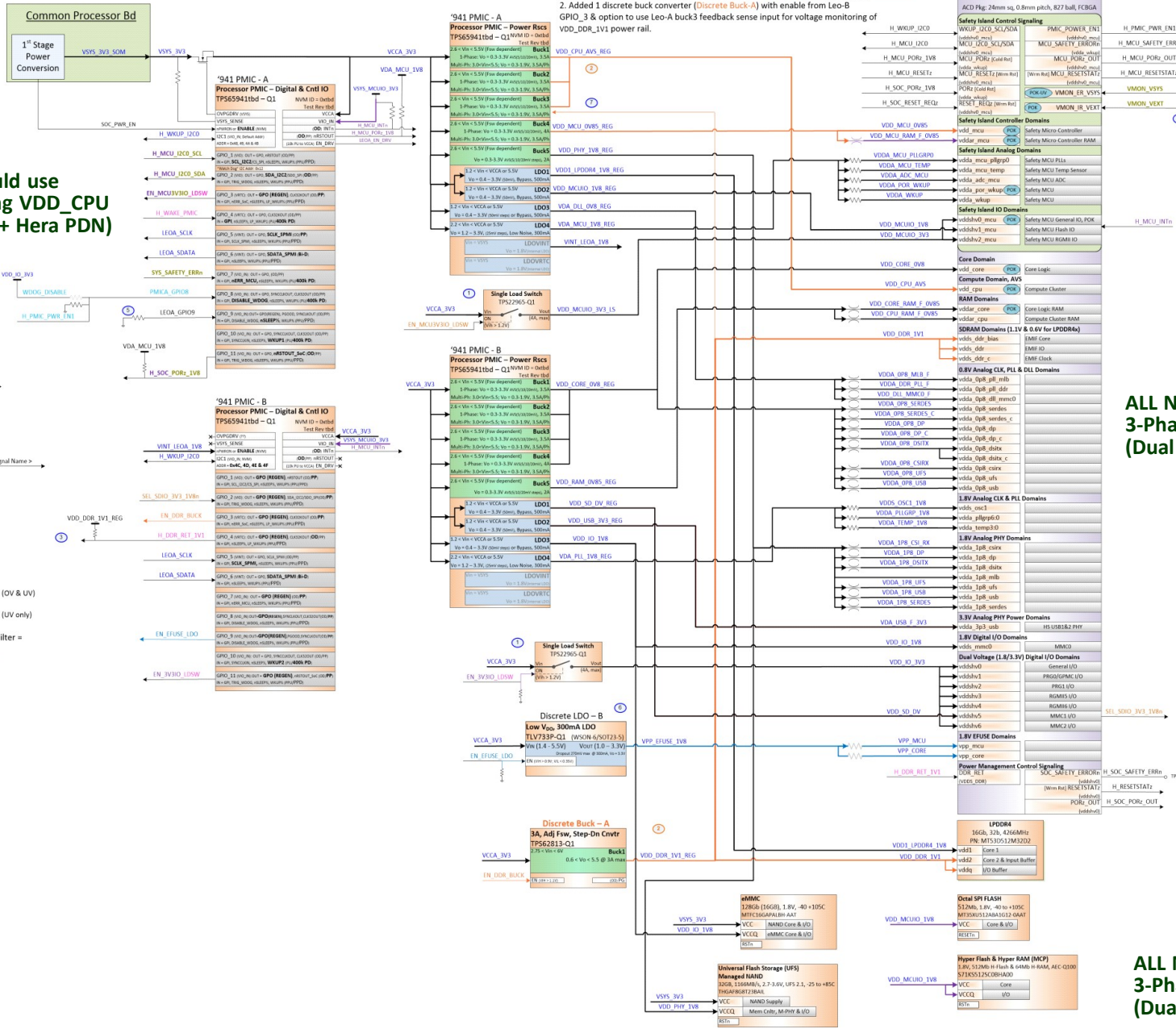
DRA829/TDA4VM 2-Phase vs. 3-Phase Dual Leo PDN-0B Differences

(Power Rail & GPIO Mapping Overview)

v0.9 10/14/2020

PDN Differences btw 2-Ph vs 3-Ph Dual Leo PDN

- 1. Changed 3 power rail mappings as high-lighted by "orange-colored" rails below.
- 2. Added 1 discrete buck converter (Discrete Buck-A) with enable from Leo-B GPIO, 3 & option to use Leo-A buck3 feedback sense input for voltage monitoring of VDD_DDR_V1 power rail.



ALL New Designs should use
3-Phase Buck supplying VDD_CPU
(Dual Leo PDN or Leo + Hera PDN)

ALL New Designs should use
3-Phase Buck supplying VDD_CPU
(Dual Leo PDN or Leo + Hera PDN)

ALL New Designs should use
3-Phase Buck supplying VDD_CPU
(Dual Leo PDN or Leo + Hera PDN)