

# AM625 / AM623 Starter Kit SK (EVM) WITH TPS6521904 PMIC

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### Revision Number

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REV	B
VER	0.15

### D-Note:

SK/EVM is an evaluation board or platform. The SK/EVM is not a reference design. In some cases, the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SoC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata and TRM when designing their custom board. The information found in the datasheet should always take precedence over the SK/EVM implementation.

### R-Note:

- \* Verify the DNI components configuration with respect to the SK schematics (use PDF) after completion of board design before board assembly.
- \* A standard 5% tolerance resistor can be used for most of the series and parallel pull resistors.
- \* Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build. (Refer FAQs listed for additional details).



Indicates circuit level change



Indicates that the value of the component has been updated.

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## REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	20 Jun 2025	- Drafted from PROC142A1 Schematics - Added optional clock path for EXP_CLKOUT0 signal on the Expansion header to support DANTE	Mistral Design Team	Pandiyarajan	
0.02	26 Jun 2025	Updated TIVA and XDS section as per TI requirement	Mistral Design Team	Pandiyarajan	
0.03	14 July 2025	Implemented the review comments shared by TI	Mistral Design Team	Pandiyarajan	
0.04	21 July 2025	- Replaced U13 with a dual-channel load switch - Changed the implementation of AUDIO_EXT_REFCLK1	Mistral Design Team	Pandiyarajan	
0.05	12 Aug 2025	- Added U113 regulator and corresponding components for VDD_CANUART implementation - Implemented partial IO support for FT4232 UART	Mistral Design Team	Pandiyarajan	
0.06	22 Sept 2025	- TP124 has been added to U12.B7 pin of the SoC - D16 and D17 ESD diodes have been added to J26 and J25 headers respectively - R785, R784 and R786 pulldown resistors have been added to AUDIO_EXT_REFCLK1_R, EXP_CLKOUT0 and AUDIO_EXT_REFCLK1 signals respectively	Mistral Design Team	Pandiyarajan	
0.07	07 Oct 2025	- Changed the supply from VCC3V3_EXP to VCC_3V3_SYS on U111 & R717 - Moved U112 and the corresponding components to the User Expansion Connector section & added the respective D-Notes	Mistral Design Team	Pandiyarajan	
0.08	03 Nov 2025	- R96 has been changed from 10k to 47k - VCCB of U106 has been changed from VCC3V3_TA to VCC_3V3_SYS - Pull-ups R787 & R788 have been added in the FT4232 UART buffers section - Pull-up resistor R789 has been added on TEST_GPI02_XDS signal	Mistral Design Team	Pandiyarajan	
0.09	04 Nov 2025	- U34 part number has been changed to TPS2051BD and the corresponding circuit has been updated - U114 and the corresponding circuit have been added for ESD protection of USB data lines - Y4 part number has been changed to ABM11W-25.0000MHZ-8-D1X-T3; C303 and C305 have been updated to 13pF	Mistral Design Team	Pandiyarajan	
0.10	11 Nov 2025	Implemented the review comments shared by TI	Mistral Design Team	Pandiyarajan	
0.11	09 Jan 2026	Mounted R6 (The production revision of Wi-Fi+BT module "M.2-CC3351" requires R6 resistor as confirmed by TI)	Mistral Design Team	Pandiyarajan	
0.12	23 March 2026	Below components have been updated based on TI review comments checklist: 1. Value of C232 is changed from 22uF to 4.7uF 2. C491, C534, C535, C536, C537 have been changed from 10pF to 47pF 3. R613, R743, R744, R746, R747 have been changed from 620E to 62E 4. Mounted R363 5. Added D-Notes	Mistral Design Team	Pandiyarajan	
0.13	31 March 2026	- Added D-notes - Added blocks to indicate value/circuit changes form rev A to B	Mistral Design Team	Pandiyarajan	
0.14	14 April 2026	Below components have been updated based on TI review comments checklist: 1. Tolerance of R502, R495, R461, R6, R305, R563, R560, R556, R552, R260, R259, R258, R255, R694, R693 and R400 resistors has been changed from 1% to 5% 2. Value of R304 has been changed from 47K to 10K 3. Value of R330 has been changed from 1.5K to 2.2K 4. Value of R614 & R617 has been changed from 1K to 470E 5. Value of R88 & R188 has been changed from 220E to 470E 6. Added and updated D-Notes	Mistral Design Team	Pandiyarajan	
0.15	23 April 2026	Updated D-Notes	Mistral Design Team	Pandiyarajan	

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## LINKS TO KEY COLLATERALS

<b>Hardware Design Guide:</b> <a href="https://www.ti.com/lit/an/sprad05b/sprad05b.pdf">https://www.ti.com/lit/an/sprad05b/sprad05b.pdf</a>
<b>Schematic Design checklist, General guidelines and Review Checklist for AM62x Processor Family:</b> <a href="https://www.ti.com/lit/pdf/sprado3">https://www.ti.com/lit/pdf/sprado3</a>
<b>PMIC Power Solutions Application Note:</b> <a href="https://www.ti.com/lit/an/slvafd0b/slvafd0b.pdf">https://www.ti.com/lit/an/slvafd0b/slvafd0b.pdf</a>
<b>DDR Board Design and Layout Guidelines:</b> <a href="https://www.ti.com/lit/an/sprad06/sprad06.pdf">https://www.ti.com/lit/an/sprad06/sprad06.pdf</a>
<b>SKs (Starter Kits) for Reference:</b> SK-AM62B, SK-AM62B-PI, SK-AM62-LP, SK-AM62-SIP, SK-AM62A-LP, SK-AM62P-LP
<b>Schematic Design guidelines combined for Sitara processor families :</b> <a href="https://www.ti.com/lit/pdf/sprad21">https://www.ti.com/lit/pdf/sprad21</a>

## LINKS TO KEY FAQs

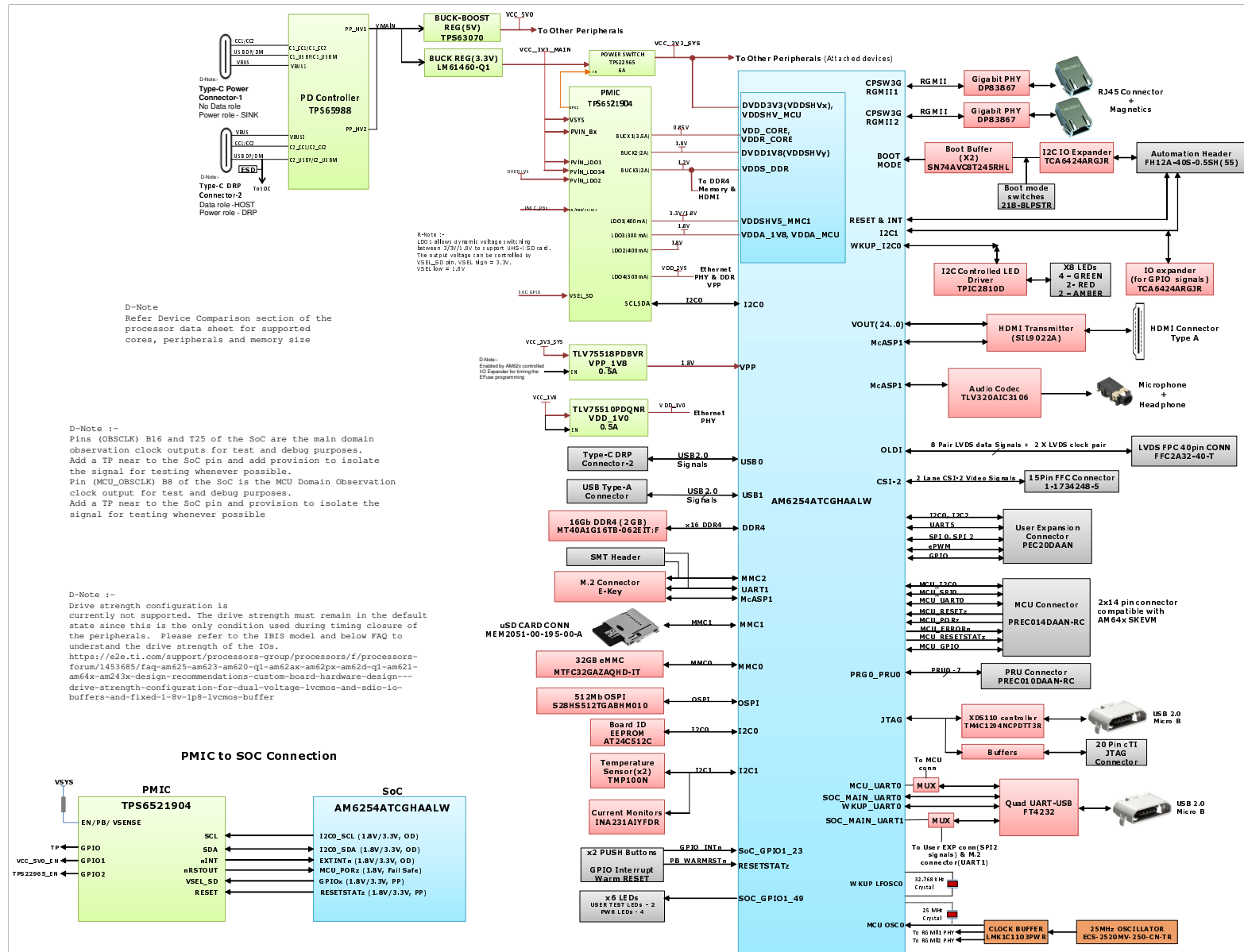
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## BLOCK DIAGRAM



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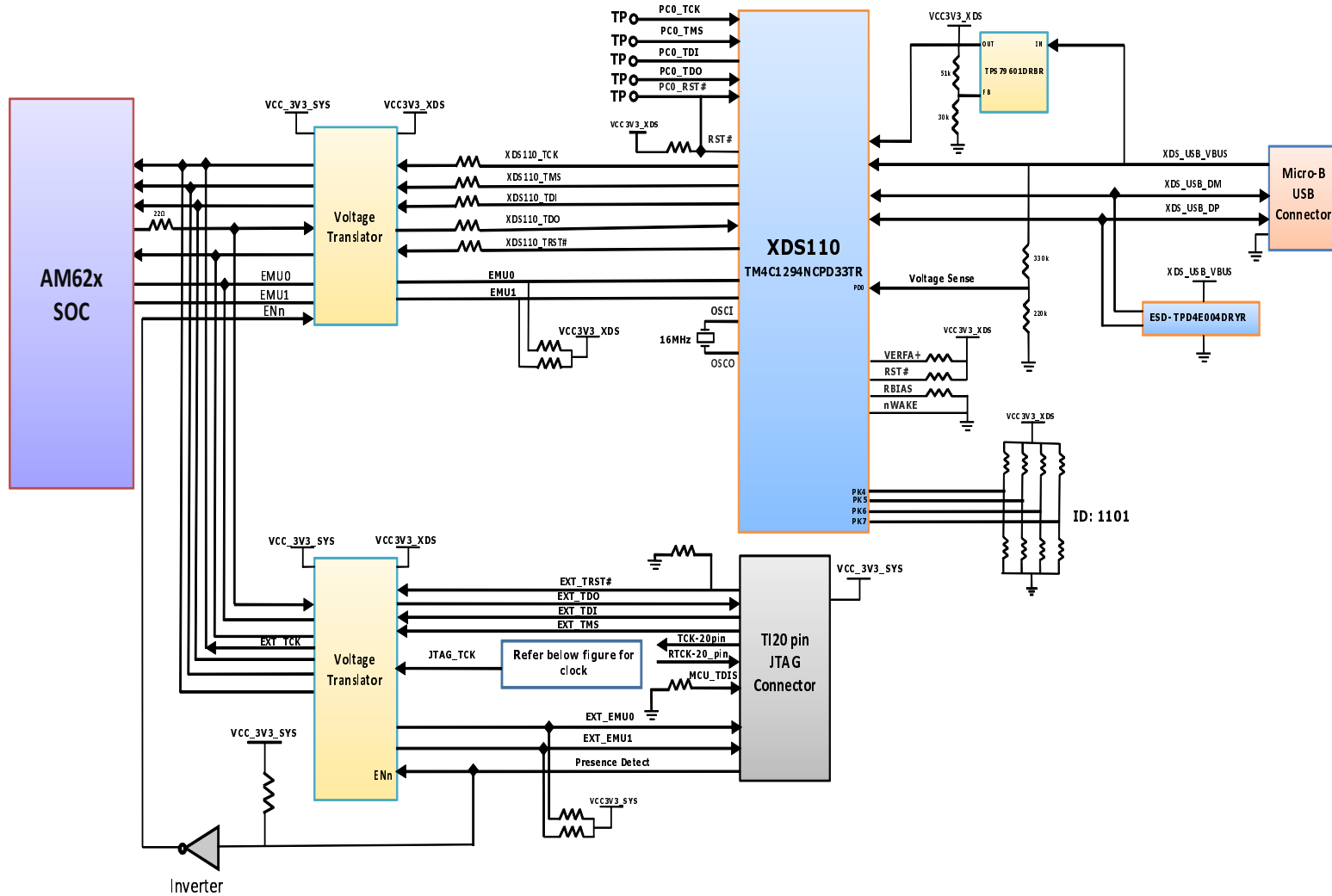
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## BLOCK DIAGRAM\_XDS110

### D-Note:

Please follow SK-AM62P-LP implementations for latest updates on XDS110



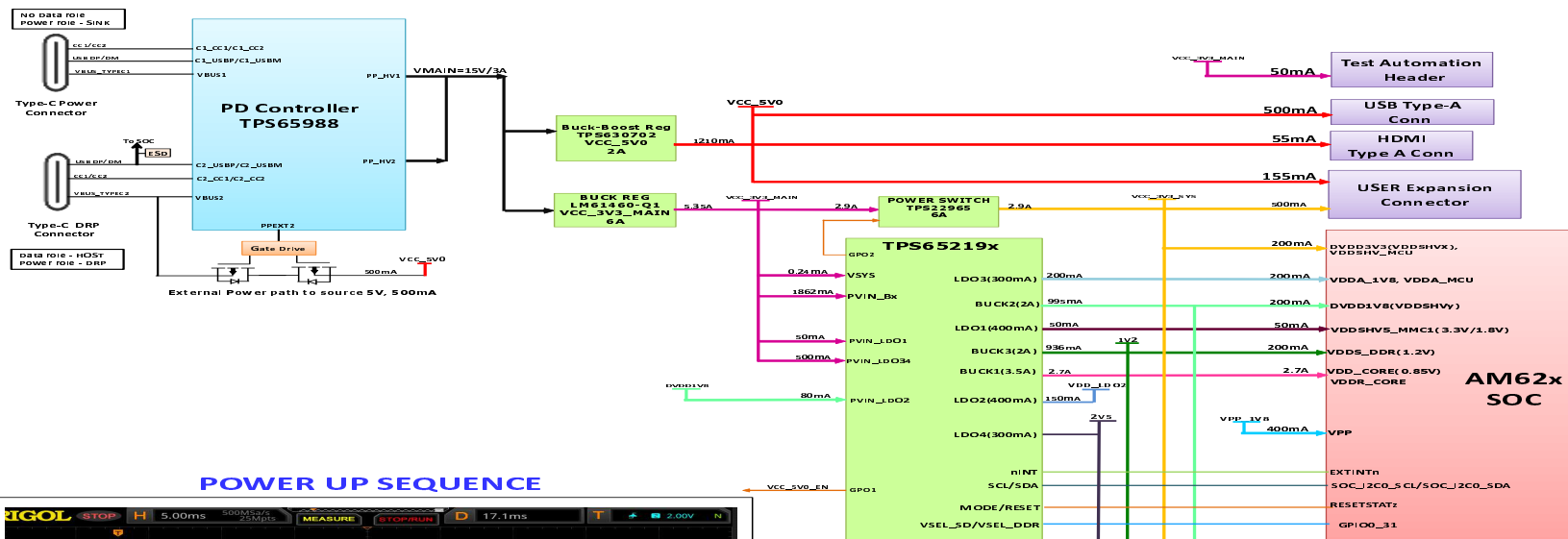
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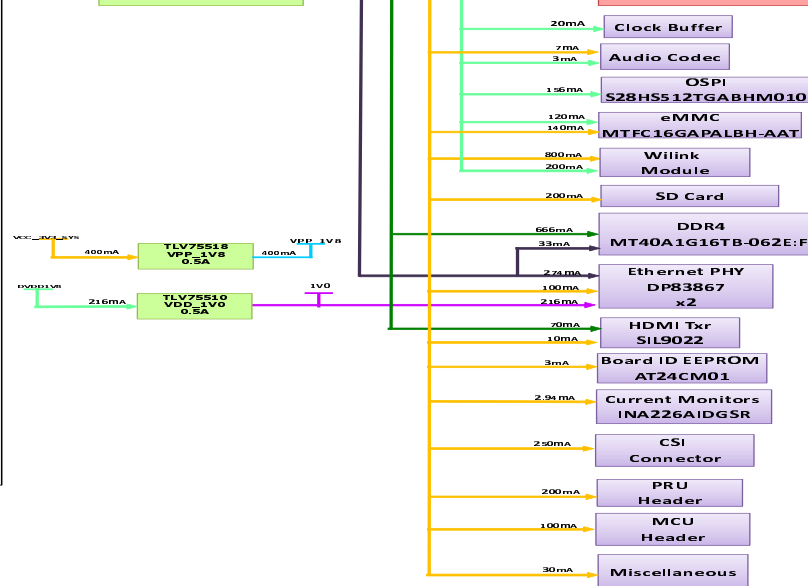
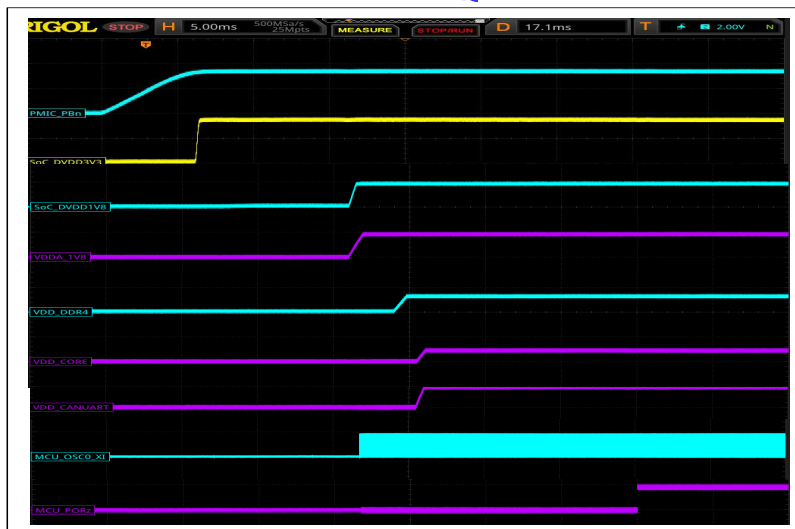
Title BLOCK DIAGRAM XDS110 DEBUGGER

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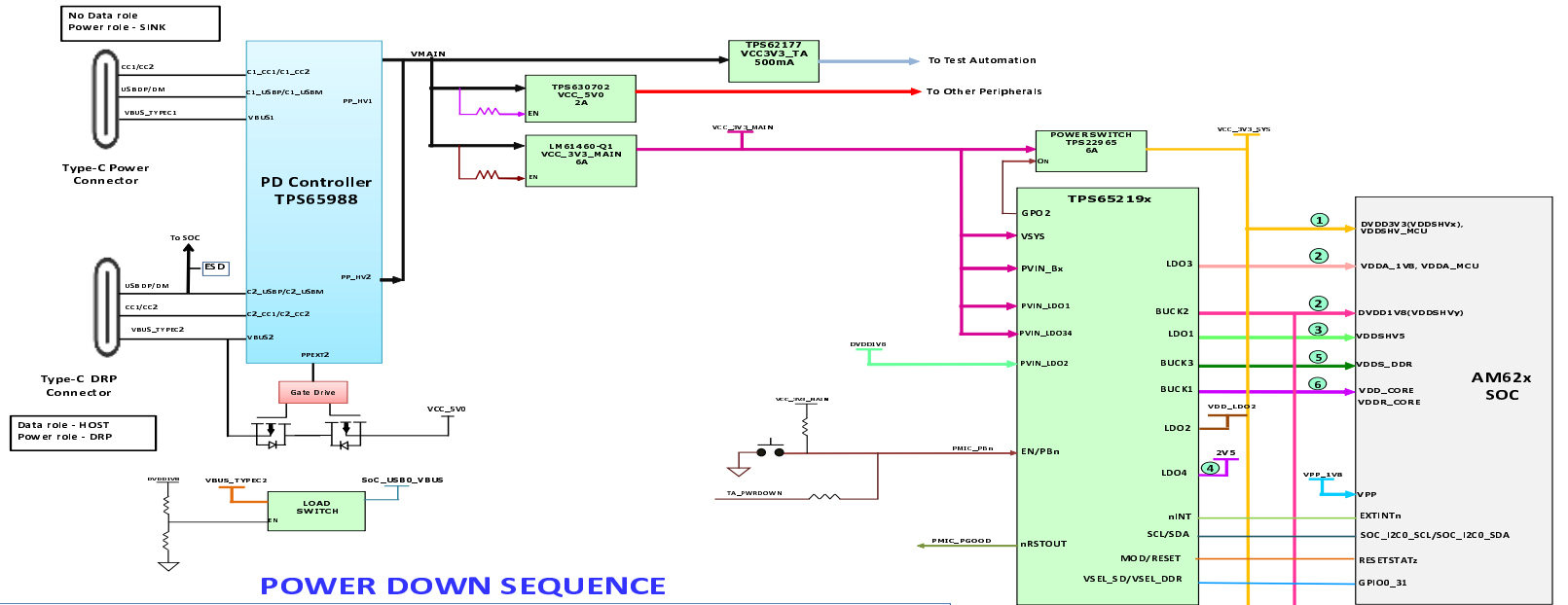
## POWER BLOCK DIAGRAM



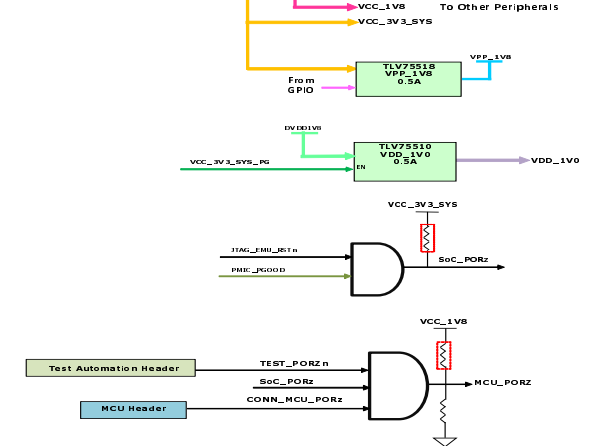
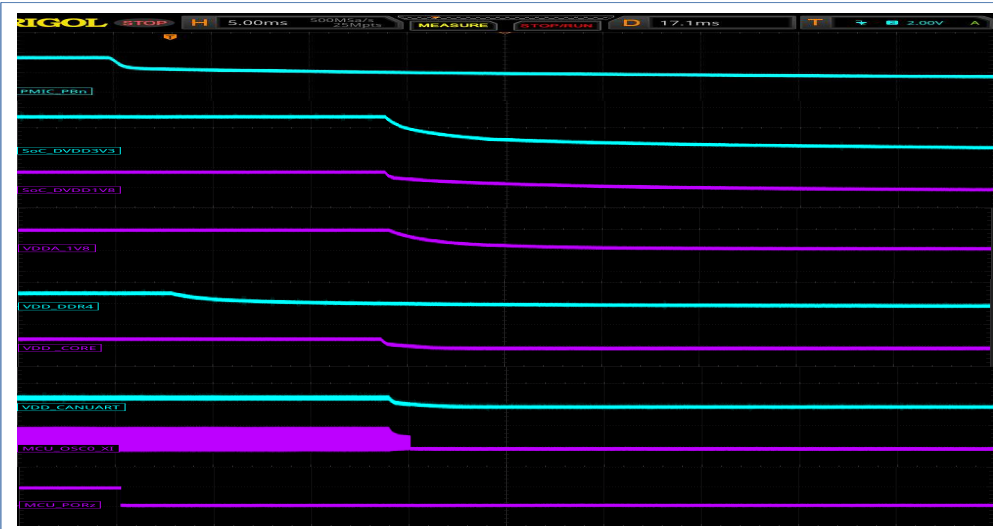
## POWER UP SEQUENCE



## POWER SEQUENCE



## POWER DOWN SEQUENCE



## I2C TREE

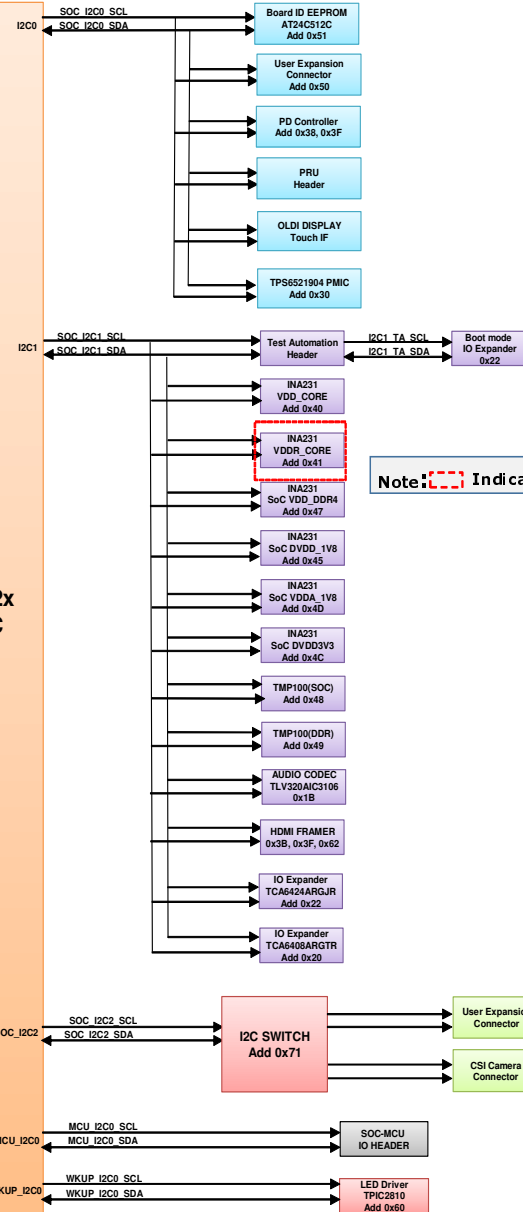
### R-Note:

Refer to the following section of the data sheet:  
Timing and Switching Characteristics - I2C - Exceptions

### R-Note:

Add -  
Indicates  
Address

AM62x  
SOC



### R-Note:

For emulated open-drain output type LVCMOS I2C interfaces (I2C0, I2C1, I2C2, I2C3), pull-up resistors are recommended when the IOs are configured for I2C interface. The IOs associated with these I2C interfaces are not compliant to the fall time requirements defined in the I2C specification. A series resistor is used to control the fall time. Location of the pull-up is not critical. The recommendation to connect the pull-ups with the shortest possible stub.

### R-Note:

For I2C interfaces with open-drain output type buffer (MCU\_I2C0 and WKUP\_I2C0), an external pull-up is recommended irrespective of peripheral usage and IO configuration. An RC to limit the slew rate (C placed near to SOC pin) is recommended. Refer to the Pin Connectivity Requirements section of the SoC data sheet.

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## GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	Functionality	GPIO USED	SOC MUXED SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE CONNECTED ON SKEWM
1	Enable for WLAN Interface	SoC_WLAN_EN_1V8	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	SoC_WLAN_IRQ_1V8	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC_3V3	ENABLE	MCU_GPIO0_1	MCU_SPI0_CS0	OUTPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_N Tn/PRU_JN Tn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
	PRU Connector Interrupt									
	PMIC_INTn									
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	SD Card IO Voltage Select	VSEL_SD	ENABLE	GPIO0_31	GPMC0_CLK	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD3V3
8	IO Expander Interrupt	MCU_GPIO0_15	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	SoC_DVDD3V3
9	TEST GPIO1 from Test Automation Connector/ User Interrupt Push Button									
10	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
<b>IO EXPANDER - 01</b>										
1	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER - P02		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER - P03		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER - P04		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
6	EXP CONN 3.3V Power Switch Enable	EXP_P5_3V3_EN	ENABLE	IO EXPANDER - P05		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
7	EXP CONN 5V Power Switch Enable	EXP_P5_5V0_EN	ENABLE	IO EXPANDER - P06		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
8	EXP CONN HAT Board Detection	RPI_HAT_DETECT	DETECTION	IO EXPANDER - P07		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	M.2 Connector Alert	WLAN_ALERT_3V3	ALERT	IO EXPANDER - P10		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	M.2 Connector WAKEUP	BT_UART_WAKE_SOC_3V3	WAKEUP	IO EXPANDER - P11		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
11	SOC UART1 Mux Select	UART1_MUX_SEL	SELECT	IO EXPANDER - P12		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
12	Enable for Wiliink Level Translators	WL_IT_EN	ENABLE	IO EXPANDER - P13		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER - P14		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	Raspberry Pi Camera CSIO GPIO1	CS1_GPIO1	INPUT/OUTPUT	IO EXPANDER - P15		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	Raspberry Pi Camera CSIO GPIO2	CS1_GPIO2	INPUT/OUTPUT	IO EXPANDER - P16		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER - P17		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER - P20		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO for communications with AM62x	IO EXPANDER - P21		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
19	MCASP2 Enable and Direction Control	AUD_BUF_EN	ENABLE	IO EXPANDER - P22		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
20		WL_BUF_EN	ENABLE	IO EXPANDER - P23		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
21		AUD_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P24		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
22		WL_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P25		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
23	OLDI Display Touch Interrupt	TS_INTn	INTERRUPT	IO EXPANDER - P26		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER - P27		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
<b>IO EXPANDER - 02</b>										
1	M.2 Connector SDIO Reset Control GPIO	WLAN_SDIO_RST_3V3	RESET	IO EXPANDER - P0		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	OLDI Display Reset control	GPIO_TS_RSTn	RESET	IO EXPANDER - P1		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	DETECTION	IO EXPANDER - P2		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	eMMC Reset control GPIO	GPIO_eMMC_RSTn	RESET	IO EXPANDER - P3		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3

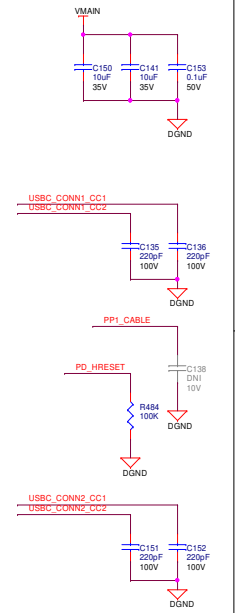
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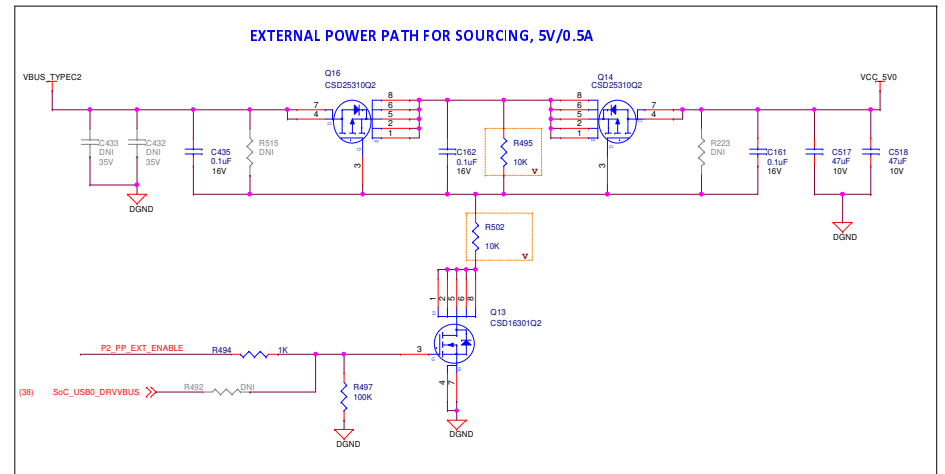
Title GPIO MAPPING TABLE

Size	Rev
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## USB TYPE-C PD CONTROLLER AND POWER SUPPLY

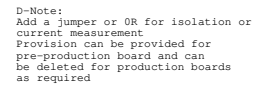


## SPI EEPROM & PROGRAMMING HEADER



Size	PROC142B(002)	Rev
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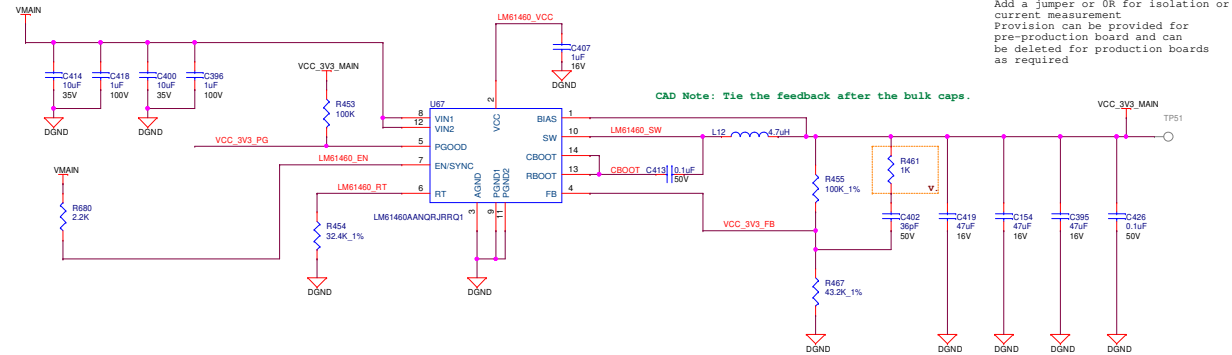
A vertical bar divided into four segments labeled A, B, C, and D from bottom to top. Segment B contains a right-pointing arrow.



## PERIPHERAL POWER SUPPLIES - 2

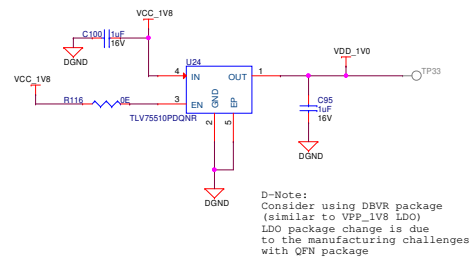
VinMin = 4.5V  
VinMax = 24V  
Vout = 3.3V @ 6A

### 3.3V, 6.0 AMPS SUPPLY

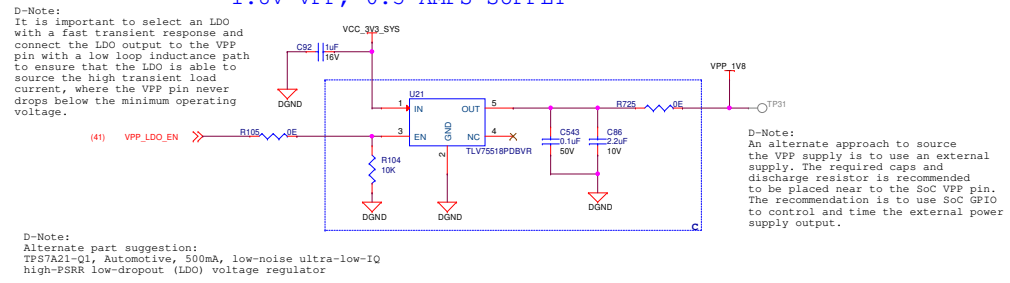


### PERIPHERAL SUPPLY - ETHERNET PHY

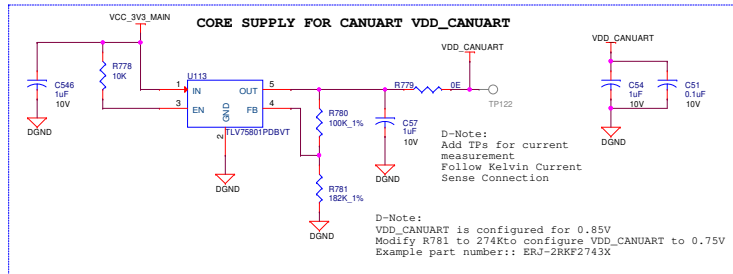
#### 1.0V, 0.5 AMPS



#### 1.8V VPP, 0.5 AMPS SUPPLY



### CORE SUPPLY FOR CANUART VDD\_CANUART



D-Note:  
Given the transient current requirement during eFuse programming, using a load switch or a FET based switch may not be a recommended approach. It is recommended to use an LDO. A load switch or FET switch is likely to have too much voltage drop that can't be compensated like when using an LDO.

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Title PERIPHERAL POWER SUPPLIES-2

Size	Rev
C	B
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# SOC POWER ARCHITECTURE - PMIC

## TPS6521904 PMIC

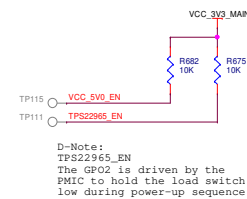
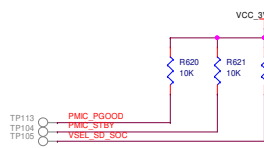
D-Note:  
Show the bulk caps connection for each of the DC/DC inputs separately. Add a 0.1 uF across the bulk caps. PVIN\_B1\_1, PVIN\_B1\_2 can share the same bulk caps.

PMIC REGULATORS	VOLTAGE RAIL	CURRENT (mA)
BUCK 1	VCC_CORE (0.85V)	2700
BUCK 2	VCC_1V8	995
BUCK 3	VDD_1V2	936
LDO 1	VDDSHV_SDIO	50
LDO 2	VDD_LDO2	150
LDO 3	VDDA1V8	200
LDO 4	VDD_2V5	300

R-Note:  
Refer PMIC data sheet and PMIC schematics review checklist for reviewing the implementation of PMIC section on the custom board

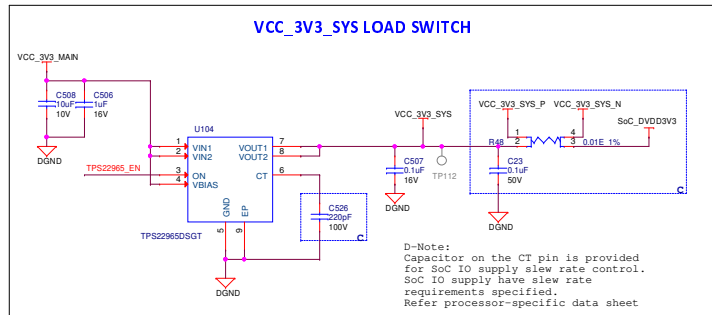
D-Note:  
Verify the PMIC data sheet or SK schematic for the recommended capacitors for the buck and LDO outputs

D-Note:  
OR resistor or jumper is added at the PMIC buck output for isolation or testing.

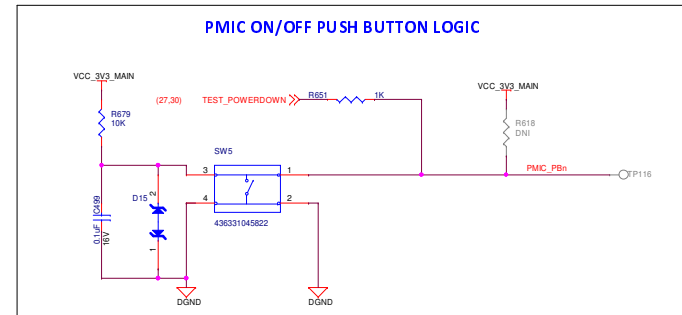


### SOC 3.3V IO SUPPLY

#### VCC\_3V3\_SYS LOAD SWITCH



#### PMIC ON/OFF PUSH BUTTON LOGIC



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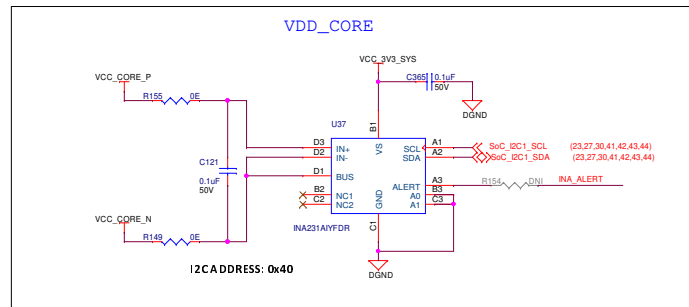


TiB SOC POWER SUPPLIES-PMIC BASED WITH SOC CURRENT MEASUREMENT SKINETS

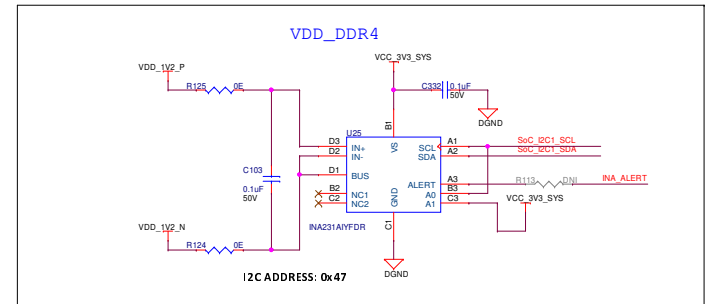
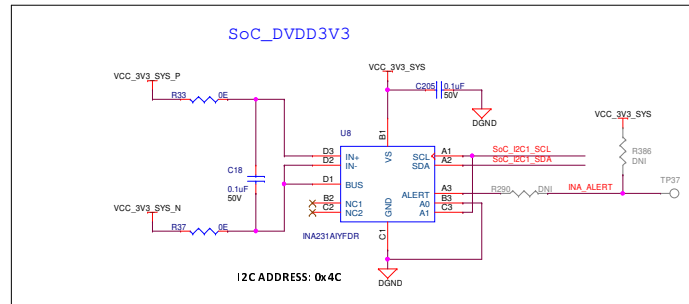
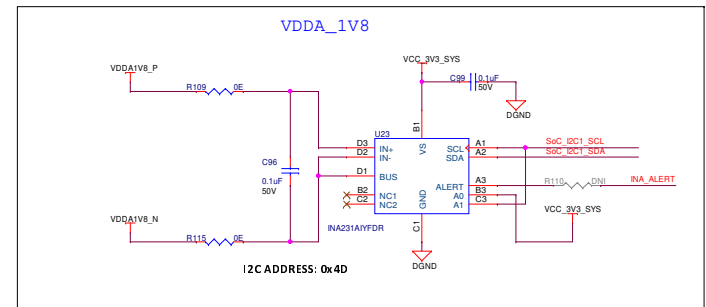
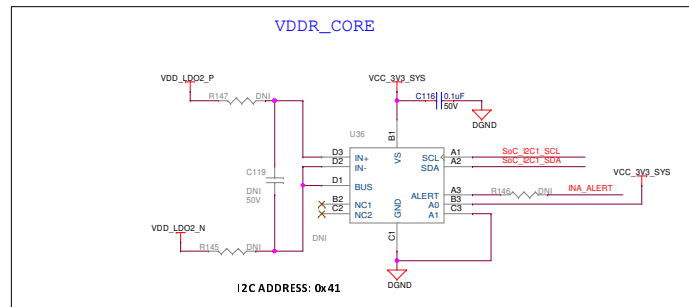
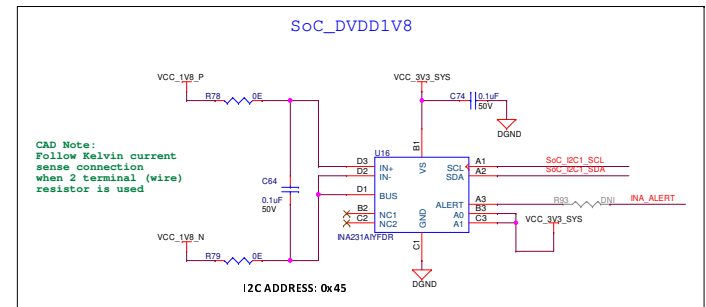
Size	Rev
C	PROC142B(002)
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# CURRENT MEASUREMENT DEVICES

D-Note:  
Note the supply rail name change across the shunt when optimizing the design (Deleting the current sense resistor).



D-Note:  
Provision for 4-wire resistor and current measurement devices have been provided for testing on the SYM board. Implementing current measurement circuit on the custom board is use case and board requirements dependent.



D-Note:  
OR resistor option to connect VDDR\_CORE to VDD\_CORE supply rail. The recommendation is to connect VDD\_CORE and VDDR\_CORE to the same supply source when VDD\_CORE is configured for 0.85V.



CORE SUPPLY	ARRAY CORE SUPPLY	Assembly
0.75 VDD_CORE	0.85 VDDR_CORE	DNI R699 and Mount R123
0.85 VDD_CORE	0.85 VDDR_CORE	DNI R123 and Mount R699

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (16 HEX)
VCC_CORE	VDD_CORE	40
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V2_DDR	VDD_DDR4	47

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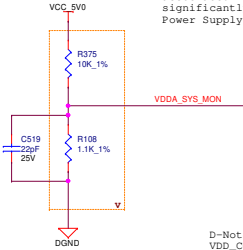


Title: SOC SUPPLY RAILS CURRENT MEASUREMENT DEVICES

Size	Rev
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## SOC POWER SUPPLIES AND SUPPLY RAILS

D-Note:  
Recommend implementing the voltage monitoring functionality using VMON\_VSYS for early detection of supply failure. It is meant to be a power-fail indicator for the main input voltage rail that enters the custom board. For example, 5, 12, or 24 volts. The error associated with this monitor would require you to set the threshold of the monitored voltage significantly lower than the nominal voltage (ROC) to avoid a false trigger. Refer to System Power Supply Monitor Design Guidelines section of the data sheet.



D-Note.  
Changing the core voltage (Dynamically) is not allowed after the SOC has been released from reset. In case the core supply is turned off, the recommendation is to turn off all power rails and ramp them down as per the power-down sequence and wait until all supply rails decay below 300mV before turning on power again.

D-Note:  
VDD\_CORE and VDDR\_CORE are recommended to be connected to the same supply source, so they ramp together when VDD\_CORE is operating at 0.85 V.

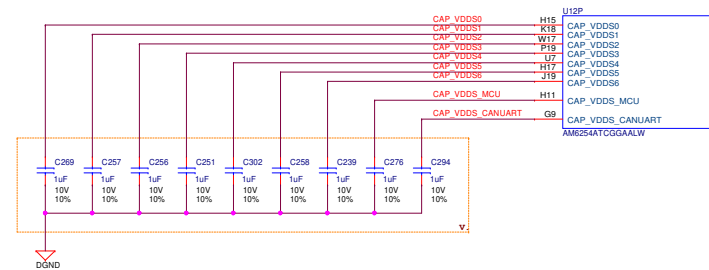
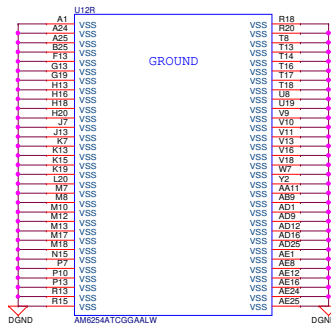
R-Note:  
Connecting a 1.8V supply source directly  
to VPP pin continuously is not  
recommended or allowed.

D-Note:  
RESERVED PINS  
Leave them unconnected

D-Note: Refer to the pin connectivity requirements section of the SoC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is not allowed to have the supplies connected and all the USB pins left unconnected, provided the USB driver is not initialized at any time and the USB calibration procedure does not happen. The recommendation is to connect (grounding) the USB supplies as per the pin connectivity requirements when not used, to optimize power when low power is a critical requirement.

D-Note:  
A trace connected to SoC is effectively an antenna that will pick up noise. A potential will be generated on the signal when noise couples into the antenna. This potential will be largest on the highest impedance end of the signal. By placing a pull-up (pullup) or pull-down (pulldown) near the SoC pin, we force the highest potential to the open-circuit end of the signal rather than the SoC end of the signal.

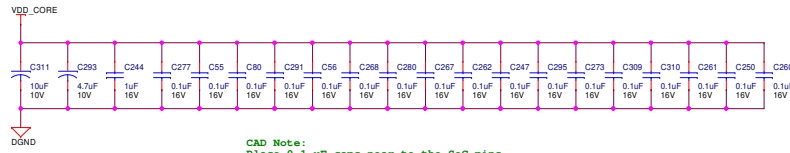
## SOC VSS



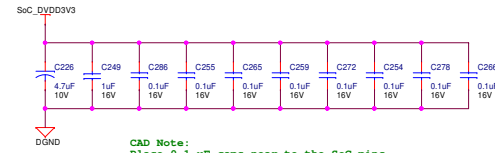
D-Note:  
Select capacitors with ESR < 1 ohm. Ensure the PCB loop inductance is < 2.5 nH. Select 0201 package or the smallest possible package.



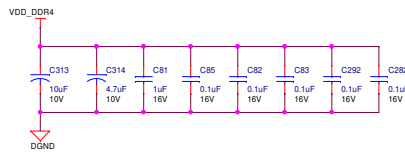
# SOC POWER SUPPLIES - DECAPS 1



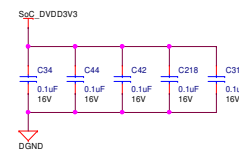
CAD Note:  
Place 0.1 uF caps near to the SoC pins.



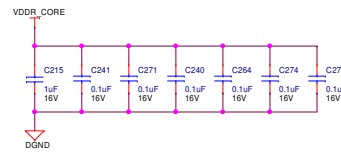
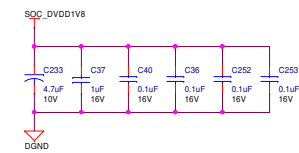
CAD Note:  
Place 0.1 uF caps near to the SoC pins.



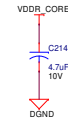
CAD Note:  
Place 0.1 uF caps near to the SoC pins.



CAD Note:  
Place 0.1 uF caps near to the SoC pins.



CAD Note:  
Place 0.1 uF caps near to the SoC pins.



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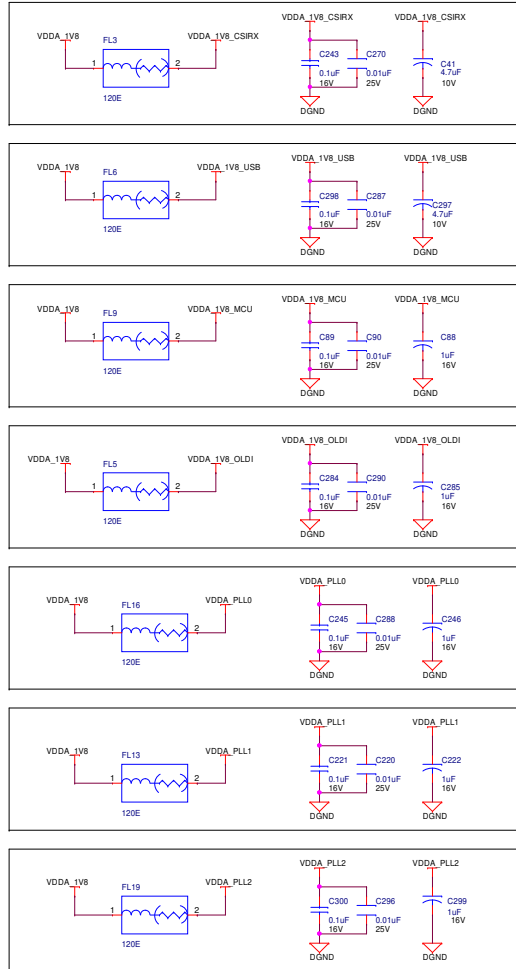


Title SOC POWER SUPPLIES - DECAPS 1

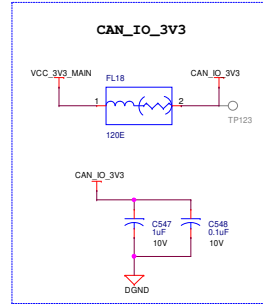
Size	Variant Name - PROC1428(002)	Rev
C		
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# SOC POWER SUPPLIES - DECAPS 2

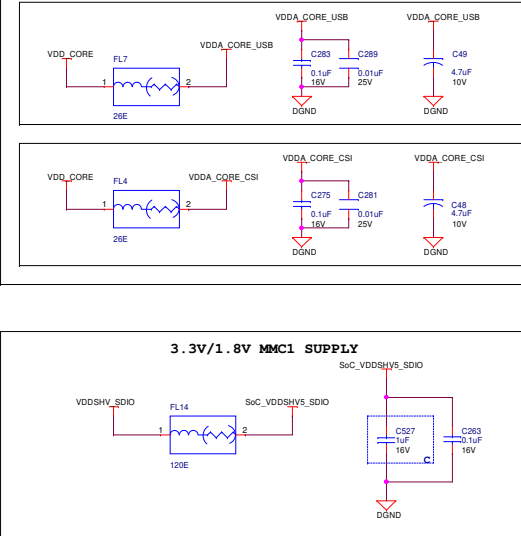
## PERIPHERALS - 1.8V ANALOG SUPPLIES



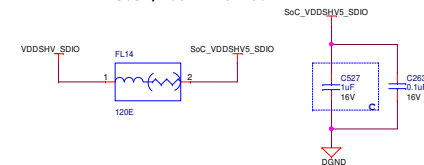
## CAN\_IO\_3V3



## PERIPHERALS - CORE SUPPLIES



## 3.3V/1.8V MMIO SUPPLY



- D-Note:
- Common SoC LVCMOS IO Interface Guidelines:
- Most of the SoC IOs are not fail-safe. No input should be applied before processor supply ramps.
  - SoC LVCMOS inputs have minimum slew rate requirements specified.
  - SoC IO buffers are off during Reset. A pull pull is required near to the attached device input being driven by the SoC IOs (input does not float).
  - Any SoC IO that has a trace connected and not being actively driven needs a parallel pull. When adding a pull is not feasible, ensure the trace is routed away from noisy signals.
  - When the IOs are unused, leave the IOs unconnected and the PADCONFIG setting in the default state.

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Title SOC POWER SUPPLIES - DECAPS 2

Size Variant Name - PROC142B(002)

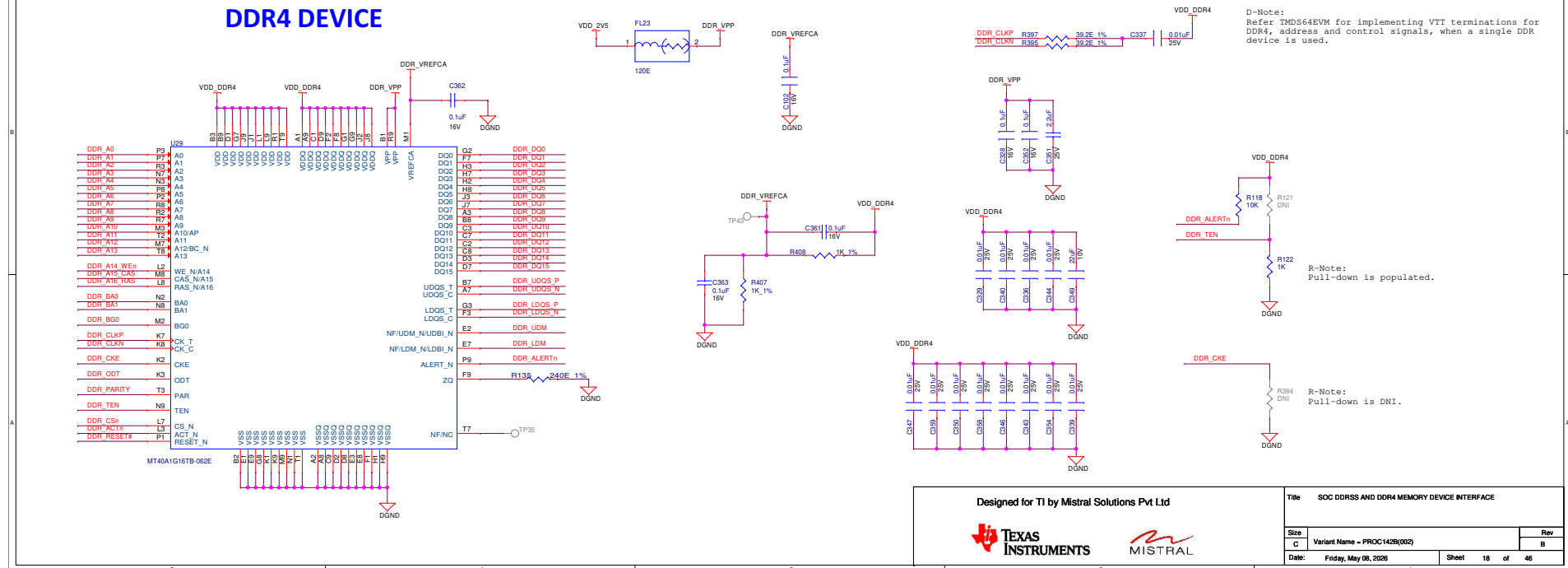
Date: Friday, May 08, 2026

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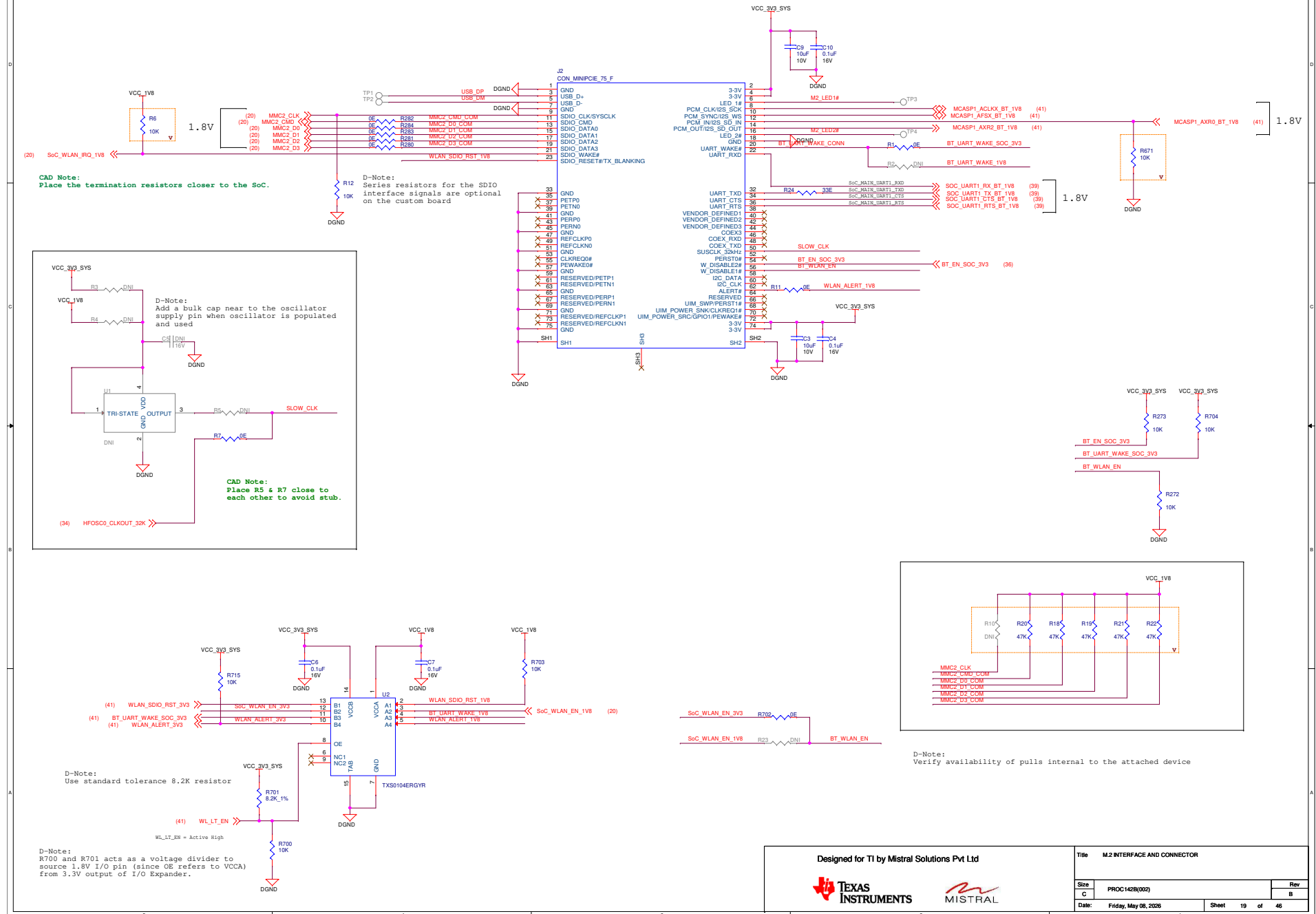
## SOC DDR4 INTERFACE



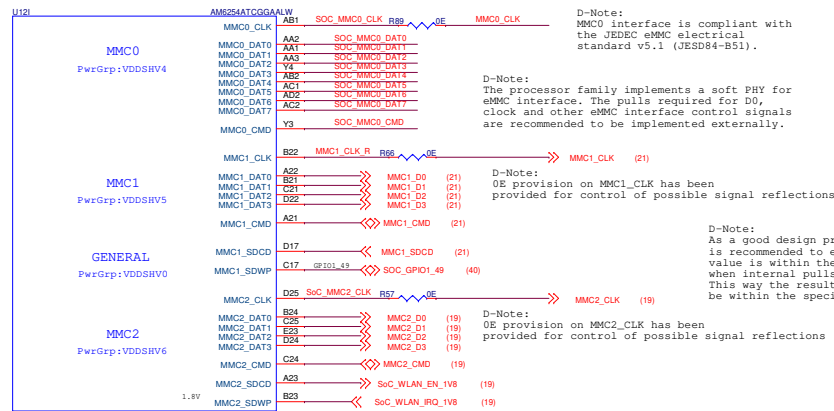
## DDR4 DEVICE



## M.2 INTERFACE



## SOC - MMC Interface



## eMMC FLASH

**D-Note:**  
Refer Custom Board Design and Simulation Guidelines for Processor High Speed Parallel Interfaces  
<https://www.ti.com/lit/pdf/sdaa087>

**D-Note:**  
The pull-up required for D7-D0, clock and other eMMC interface control signals are enabled internal to the SoC during reset and are eMMC JEDEC standard compliant. External pull-up is optional and can be deleted on the custom board. Refer to the pin connectivity requirements section for connecting the eMMC interface when not used.

**R-Note:**  
What is the reason pulldown is used for eMMC, SD card or other peripherals clock input? Because, there are cases where the clock is stopped or paused in a LOW logic state, and the pull-down option is consistent with this logic state.

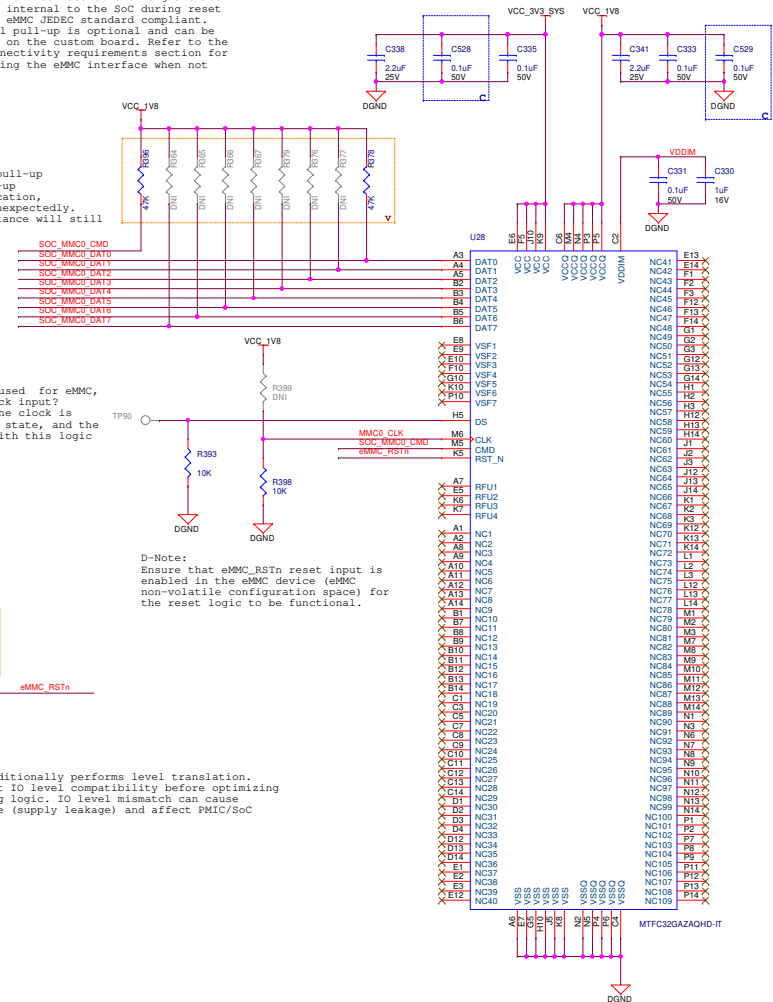
## eMMC FLASH RESET

**D-Note:**  
The GPIO reset option makes it possible for the software to reset the attached device (eMMC or OSPI or SD card or OLDI or EPHY) without resetting the entire processor, if there is a case where the peripheral becomes unresponsive.

**D-Note:**  
You could eliminate the GPIO option and only use the reset output (warm or cold), where the software forces a warm reset, if the peripheral becomes unresponsive. However, this will reset the entire device, rather than trying to recover the specific peripheral without resetting the entire device.

**D-Note:**  
In case ANDing logic is not used and the processor Main domain warm reset status output (RESETSTAT2) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTAT2 IO voltage level. A level translator is recommended to match the IO voltage level. A resistor divider can be used alternatively, provided optimum impedance value of the resistor divider is selected. In case the value is too high, the rise/fall time of the eMMC reset input can be slow and introduce too much delay. In case the value is too low, it will cause the AM62x to source too much steady-state current during normal operation.

**D-Note:**  
ANDing logic additionally performs level translation. Verify the reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch can cause residual voltage (supply leakage) and affect PMIC/SoC operation.



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Title: SOC MMC0.2 INTERFACE AND eMMC FLASH + RESET

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## SD CARD INTERFACE

D-Note:  
Refer Custom Board Design and Simulation Guidelines for Processor High Speed Parallel Interfaces  
<https://www.ti.com/lit/pdf/sdaa087>

### SD CARD LOAD SWITCH EN RESET LOGIC

**SD-Note:**  
SD Card power control power switch, along with the SD card power swtch EN reset logic and the host switched IO power supply circuit, is required to support UHS-I SD Card which begins communication using 1.8 V IO signal levels, which later switches to 1.8 V signal level when changing to a faster data transfer speed. Cycling power to the SD Card at the on and off will put the SD card back into 3.3 V mode since SD Cards do not have a reset pin. The host IO power supply must power off/on and change voltage at the same time as the SD Card. These circuits and the software driver operating the signals sourcing these circuits ensure both devices are off or on and are operating at the same IO voltage at the same time.

**LOAD SWITCH**

PMOS: V<sub>DSH</sub>, S<sub>SD</sub>      VCC, V<sub>IS</sub>, SYS

C47 10 $\mu$ F 25V      C48 1 $\mu$ F 25V      C54A 0.1 $\mu$ F 50V

DGND      DGND      DGND

R177 3.9K      R176 3.9K

D-Note:  
Series resistor is used  
for control of rise time

TPS22986H2QVCRQ1

Pin 1: VIN1  
Pin 2: VIN2  
Pin 3: GND  
Pin 4: ON1  
Pin 5: ON2  
Pin 6: VOUT1  
Pin 7: VOUT2  
Pin 8: GND

D-Note:  
Series resistor is used  
for control of rise time

D-Note:  
Dual-channel load switch is used to provide provision to reset the SD card supply, and dynamically switched Dual-voltage IO supply connected to the processor SD card IO supply for IO group VDDSHV5 and the SD card IO pullups.

D-Note:  
For UHS-I SD card support, the pull-ups are recommended to be connected to the 3.3V/1.8 V switched LDO output.

Note:  
MMC1\_CLK pull-up is a DNI.

(20) MMC1\_D0

(20) MMC1\_D1

(20) MMC1\_D2

(20,21) MMC1\_D3

(20) MMC1\_CLK

(20) MMC1\_CMD

(20) MMC1\_SDCD

D-Note:  
Add a 100R series resistor for the  
MMC1\_SDCD signal. Processor  
IO SDCD directly connects to  
ground when SD card is inserted

CAD Note:  
Place R333 near to the SD card connector

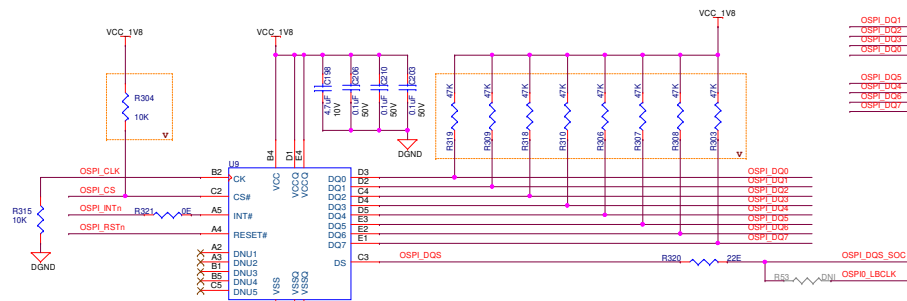
CAD Note:  
Place near the SD card connector.

D-Note:  
Refer Custom Board Design and Simulation Guidelines for  
Processor High Speed Parallel Interfaces  
<https://www.ti.com/lit/pdf/sdaa087>

R-Note:  
SoC IO buffers are off during reset and after reset.  
A pullup is recommended to hold the attached  
device IOs in a known state (does not float).  
Usage of pullups are attached device dependent.

D-Note:  
0R resistors are used for configuring QSPI0 or OSPI0 interface.  
This is optional for custom board design.

CAD Note:  
Place RA3 & RA4 closer to the attached Memory Device

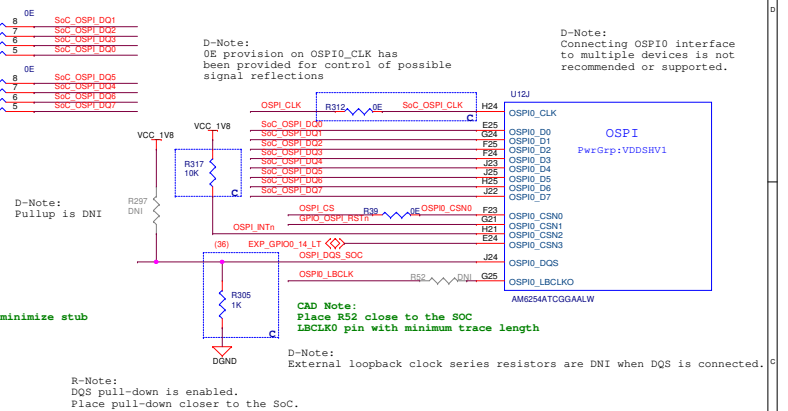


D-Note:  
Choice of QSPI memory device:  
For improved performance, it is recommended to select a QSPI memory device with an external reset input pin. The reset input pin is recommended to be **DGND** controlled using SoC reset status output or an ANDING logic as implemented in the starter kit.

D-Note:  
For QSPI configuration, remove 0E resistors from the following:  
1. OSPI\_DQ4 to OSPI\_DQ7 nets (RA4)  
2. OSPI\_INTn pullup (R317)  
OSPI NOR Flash can be replaced with a footprint compatible  
OSPI NAND Flash (Mfr Part# W35N01JWTRAG).

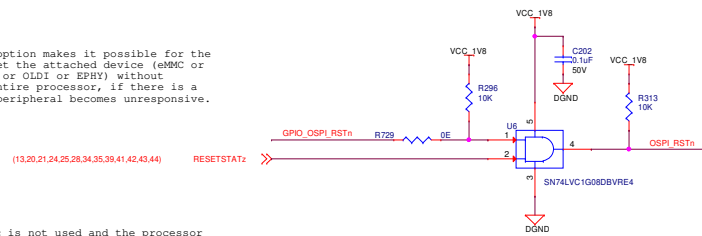
CAD Note:  
Place R53 & R320 as tripad to minimize stub

D-Note:  
Connecting OSPI0 interface  
to multiple devices is not  
recommended or supported.



D-Note:  
You could eliminate the GPIO option and only use the reset output (warm or cold), where the software forces a warm reset, if the peripheral becomes unresponsive. However, this will reset the entire device, rather than trying to recover the specific peripheral without resetting the entire device.

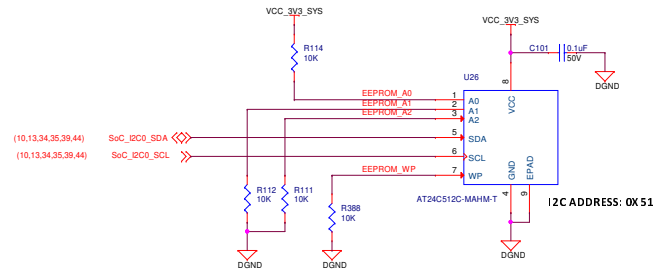
D-Note:  
The GPIO reset option makes it possible for the software to reset the attached device (eMMC or OSPI or SD card or OLDI or EPHY) without resetting the entire processor, if there is a case where the peripheral becomes unresponsive.



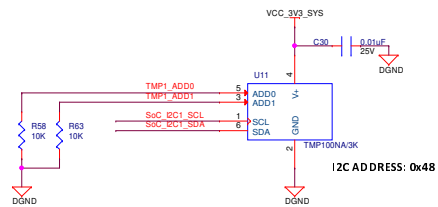
**D-Note:**  
In case ANDING logic is not used and the processor Main domain warm reset status output (RESETSTAT2) is used to reset the attached device, the IO voltage level of the attached device matches the RESETSTAT2 IO voltage level. A level translator is recommended to match the IO voltage level. A resistor divider can be used. Alternatively, provided the impedance of one value of the resistor divider is selected. In case the value is too high, the rise/fall time of the OSPI0 reset input can be slow and introduce too much delay. In case the value is too low, it will cause the current to flow too much steady-state current during normal operation.

D-Note:  
ANDing logic additionally performs level translation.  
Verify the reset IO level compatibility before optimizing  
the reset ANDing logic. IO level mismatch can cause  
residual voltage (supply leakage) and affect PMIC/SoC  
operation.

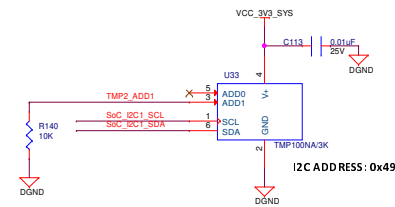
## BOARD ID EEPROM



## DIGITAL TEMPERATURE SENSORS



CAD Note:  
Place the temperature sensor closer to the SoC.



CAD Note:  
Place the temperature sensor closer to the SoC.

(14,27,30,41,42,43,44) SoC\_I2C1\_SCL TP71  
(14,27,30,41,42,43,44) SoC\_I2C1\_SDA TP72  
Silk: SOC\_I2C1

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Title BOARD ID EEPROM & DIGITAL TEMPERATURE SENSORS

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# CPSW3G RGMII 1 - ETHERNET PHY

D-Note:  
The caps and values used are as per the EPHY data sheet recommendations.

D-Note:  
OK to use 0402 package for 1uF cap to match the 10uF bulk cap package size

D-Note:  
Refer to DP83867ERG2-R-EVM when using Discrete LAN Transformer Module and RJ45 connector.

R-Note:  
Ferrite is DNI.

D-Note:  
Refer Custom Board Design and Simulation Guidelines for Processor High Speed Parallel Interfaces  
<https://www.ti.com/lit/pdf/sdass087>

D-Note:  
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration.

**RJ45 CONNECTOR WITH INTEGRATED MAGNETICS**

D-Note:  
Provide provision for series resistor based on EPHY for RDX signals near to the EPHY.

D-Note:  
Allowed amplitude for XI clock input is 1.8V irrespective of the IO supply used. Use a capacitor divider when the clock applied is 3.3V.

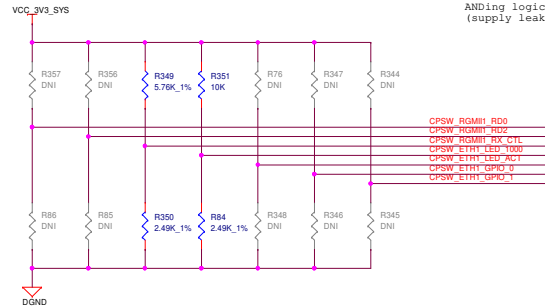
D-Note:  
Refer to the EPHY EVM for JTAG connections.

D-Note:  
RBIAS resistor value has been reduced from 11K and a parallel capacitor has been added to improve Ethernet compliance testing performance

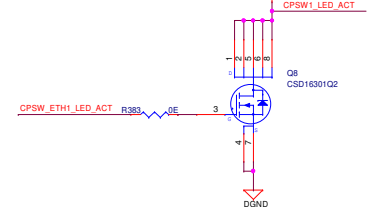
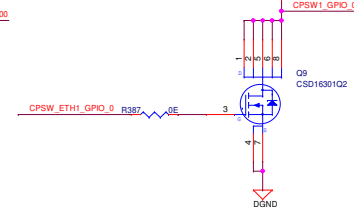
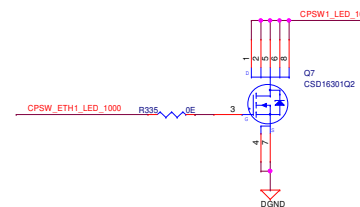
D-Note:  
ANDing logic could be optimized to a 2-input AND gate. Use RESETSTATz (or PORz\_OUT) and the SoC IO as inputs to the ANDing logic.

D-Note:  
ANDing logic additionally performs level translation. Verify the reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch can cause residual voltage (supply leakage) and affect PMIC/SoC operation.

Note:  
Pull-up is enabled for GPIO input. RESETSTATz series resistor is DNI.



PHY ADDRESS = 00000  
Auto-negotiation Enabled  
10/100/1000 advertised, Auto-MDI-X  
Tx Clock Skew = 0ns  
Rx Clock Skew = 2ns



Designed for TI by Mistral Solutions Pvt Ltd



Title CPSW3G RGMII\_1 ETHERNET PHY

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# CPSW3G RGMII 2 - ETHERNET PHY

D-Note:  
The caps and values used are as per the  
EPHY data sheet recommendations.

D-Note:  
OK to use 0402 package for 1uF cap to  
match the 10uF bulk cap package size

D-Note:  
Refer to DP83867ERGZ-R-EVM when using Discrete LAN  
Transformer Module and RJ45 connector.

R-Note:  
Ferrite is DNI.

D-Note:  
Refer Custom Board Design and Simulation Guidelines for  
Processor High Speed Parallel Interfaces  
<https://www.ti.com/lit/pdf/sdaa087>

D-Note:  
Provide provision for series resistor  
based on EPHY for RDX signals near  
to the EPHY.

D-Note:  
Refer to the EPHY EVM for JTAG connections.

D-Note:  
BIAS resistor value has  
been reduced from 11K  
and a parallel capacitor  
has been added to improve  
Ethernet compliance  
testing performance

D-Note:  
ANDing logic could be optimized to a 2-input AND gate. Use RESETSTATz (or  
PORZ\_OUT) and the SoC IO as inputs to the ANDing logic.

D-Note:  
ANDing logic additionally performs level translation. Verify  
the reset IO level compatibility before optimizing the reset  
ANDing logic. IO level mismatch can cause residual voltage  
(supply leakage) and affect PMIC/SoC operation.

RJ45 CONNECTOR WITH  
INTEGRATED MAGNETICS

Silk: CPSW PHY-2

PHY ADDRESS = 00001  
Auto-negotiation Enabled  
10/100/1000 advertised, Auto-MDI-X  
Tx Clock Skew = 0ns  
Rx Clock Skew = 2ns

Designed for TI by Mistral Solutions Pvt Ltd



Title CPSW3G RGMII 2 ETHERNET PHY

Size PROC1428(002)

C

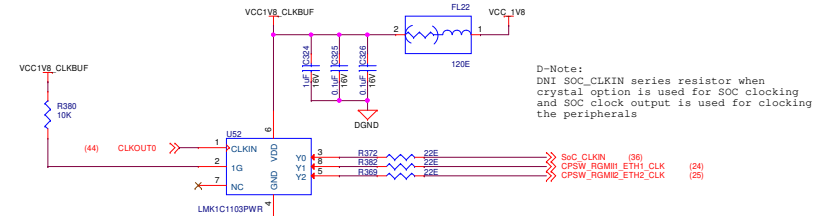
Date: Friday, May 08, 2025

Rev

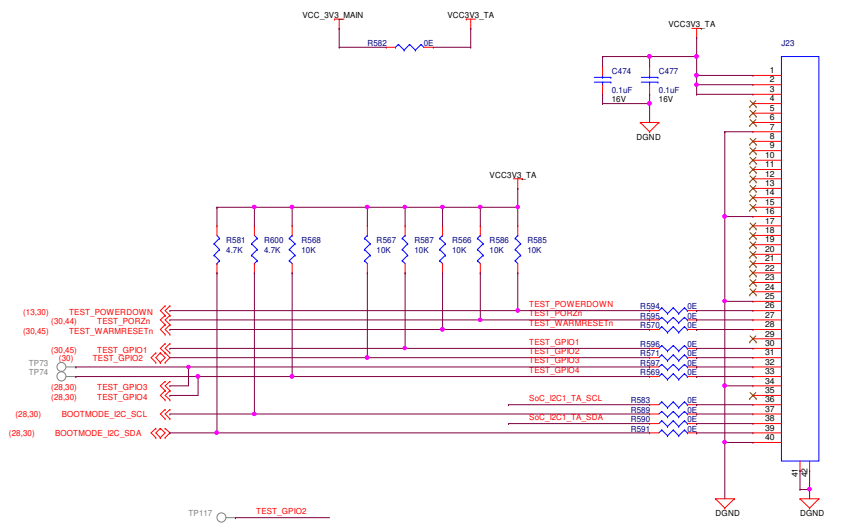
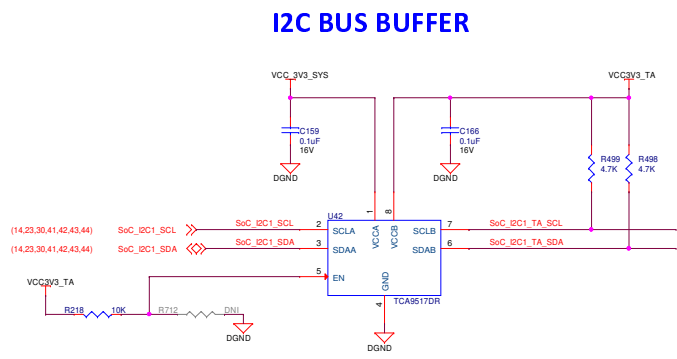
B

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D-Note:  
Series Resistor provision is provided for the TDx MAC  
interface signals near to the processor pins for control of  
possible signal reflections



40-PIN TEST AUTOMATION HEADER

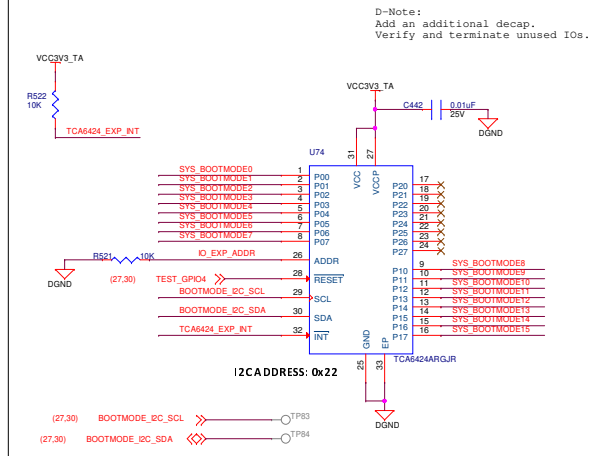


CON\_FLEX\_40X1\_FH12A-40S-0.5SH  
Silk: AUTOMATION HDR

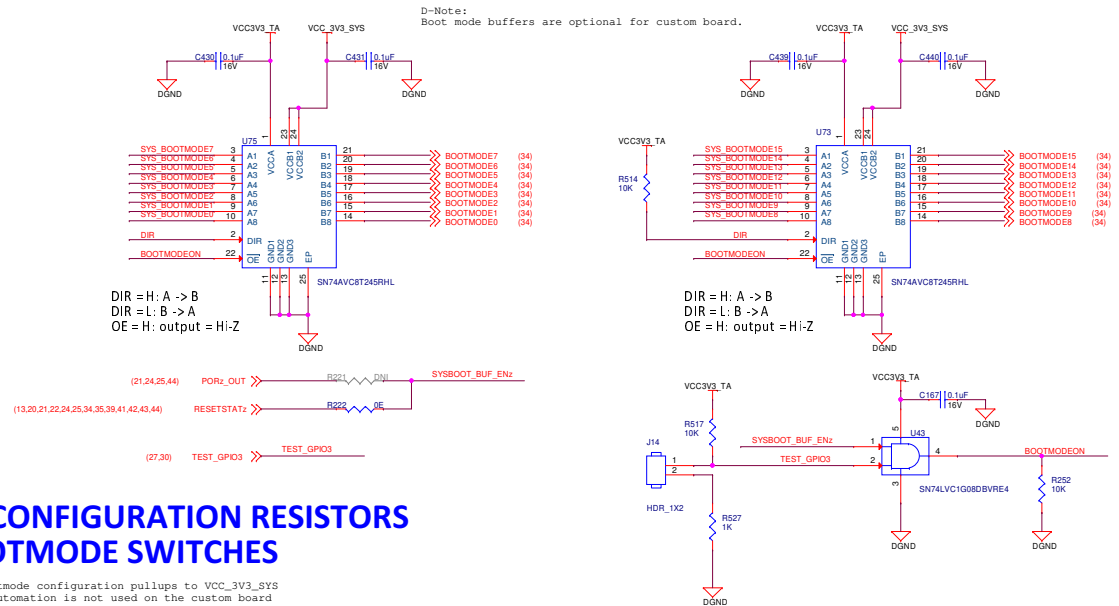
TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on MCU_GPIO0_15 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to a Testpoint	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

## BOOTMODE IO EXPANDER

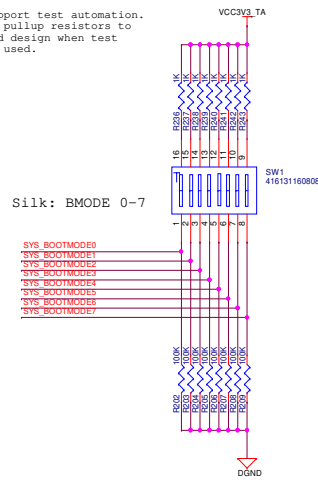


## BOOT MODE BUFFERS



## BOOTMODE CONFIGURATION RESISTORS AND BOOTMODE SWITCHES

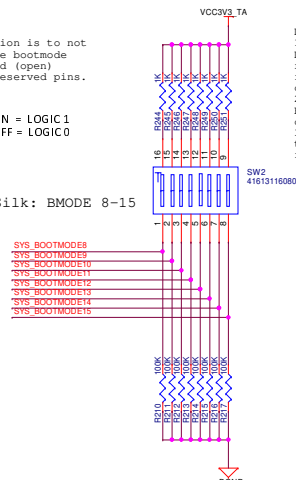
D-Note:  
VCC3V3\_TA supply is used to support test automation.  
Connect bootmode configuration pullup resistors to Soc\_DVDD3V3 on the custom board design when test automation and buffers are not used.



D-Note:  
The recommendation is to not leave any of the bootmode pins unconnected (open) including the reserved pins.

SWITCH ON = LOGIC1  
SWITCH OFF = LOGIC0

Silk: BMODE 8-15



D-Note:  
1. Dip switches are used on the SK for ease of configuration.  
DIP switches are optional on the custom board. A pull-up or pull-down resistor can be used to set the bootmode configuration. Provide provisions for pull-up and pull-down resistors for the bootmode pins that have configuration capability.  
2. When DIP switches are used on the custom board, provision for an external ESD protection may be required if the DIP switches are expected to be configured in an uncontrolled ESD environment.  
3. When DIP switches are used, reduce the resistor values used for the divider to 47k and 2K (1K) ohms to optimize the current draw in case the IOs are used for alternate functions (output).

### BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. USB0 DFU
6. BACKUP BOOT OPTION

## FAQs FOR REFERENCE TO IMPLEMENT BOOTMODE CONFIGURATION (WITH BUFFER OR WITHOUT BUFFER):

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1391522/faq-am625-am623-am644x-am243x-am62a-am62p-am62d-q1-am62l---bootmode-implementation-without-buffers>

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1414148/faq-am625-am623-am644x-am243x-am62a-am62p-am62d-q1-am62l---bootmode-implementation-with-buffers>

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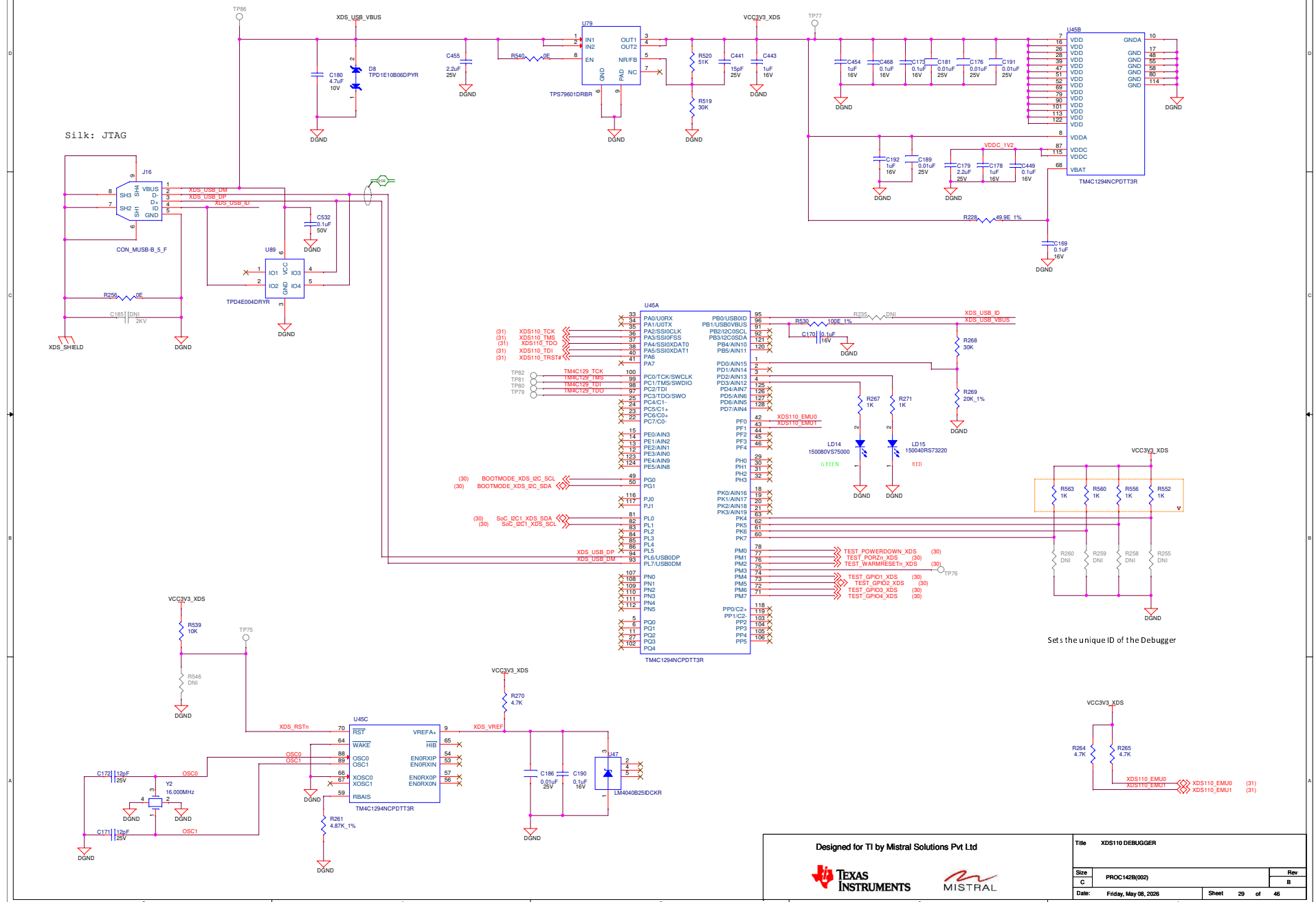
Title BOOT MODE CONFIGURATION BUFFERS & DIP SWITCHES

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## XDS110 DEBUGGER

D-Note:  
Please follow SK-AM62P-LP EVM implementations for the latest updates on XDS110.



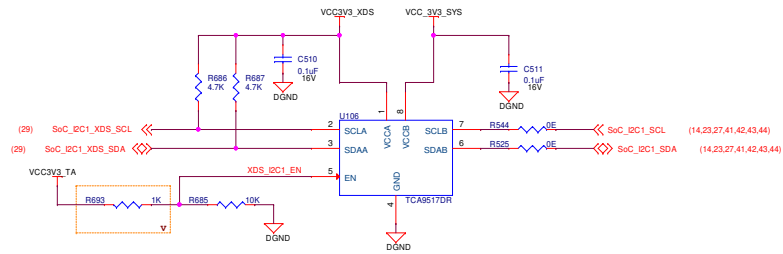
Designed for TI by Mistral Solutions Pvt Ltd



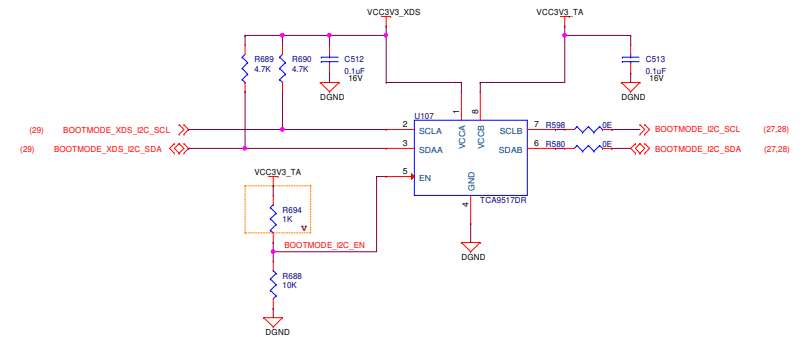
Title	XDS110 DEBUGGER
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Size	PROC142B(002)	Rev
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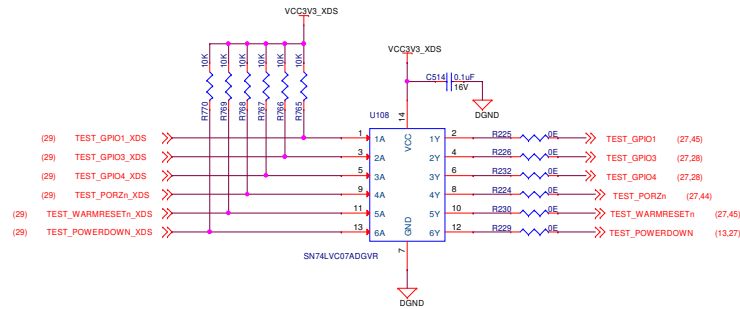
## SOC I2C BUS BUFFER



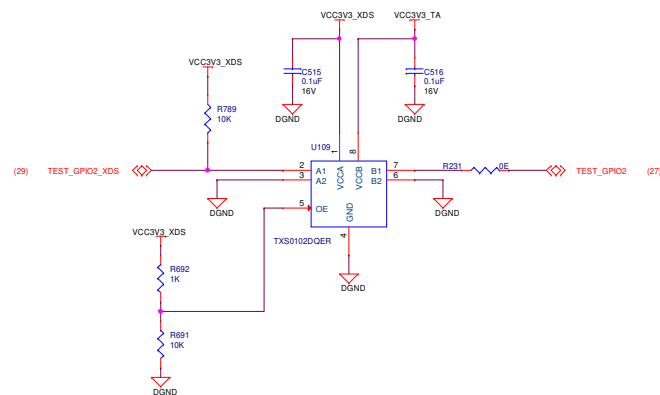
## BOOTMODE\_I2C\_TA BUFFER



## ISOLATION BUFFERS FOR TA SIGNALS



D-Note:  
Pull-up's (R587, R517, R568, R566, R565 & R567) referenced to VCC3V3\_TA are added near to the test automation header



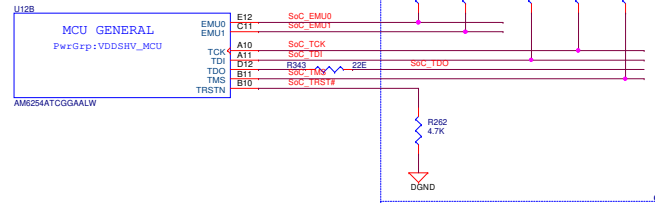
Designed for TI by Mistral Solutions Pvt Ltd



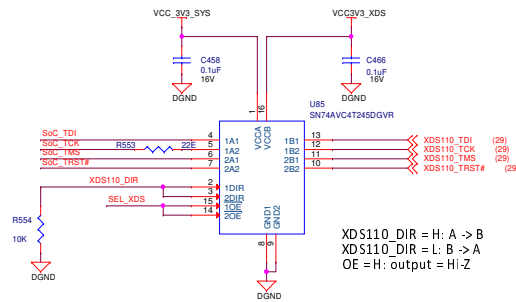
Title AUTOMATION SIGNALS BUFFER

Size	Rev
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## JTAG SOC SECTION

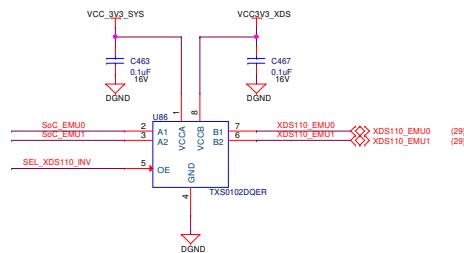
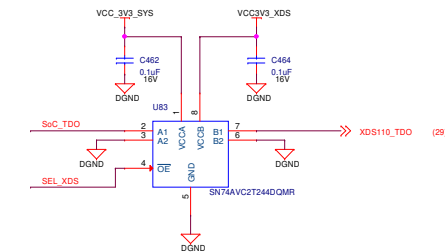


## BUFFER XDS110

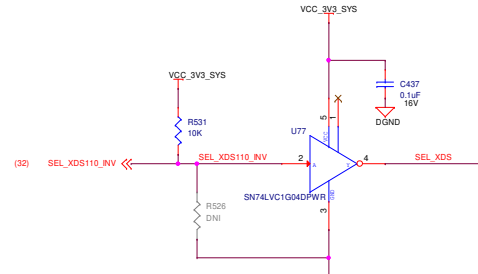


XDS110\_DIR = H: A -> B  
XDS110\_DIR = L: B -> A  
OE = H: output = Hi-Z

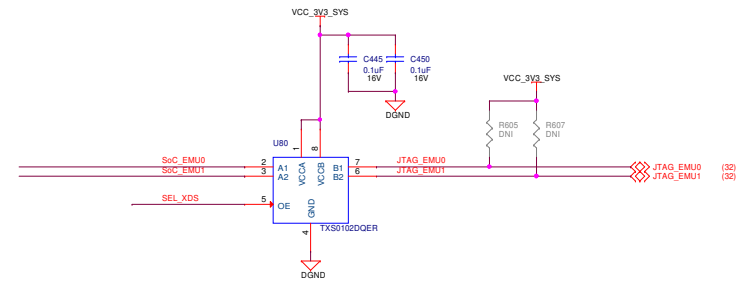
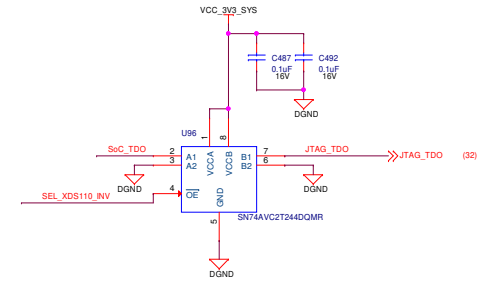
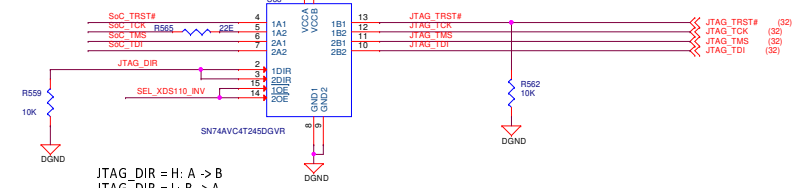
CAD Note:  
Buffers U88 and U96 need to be placed closer to the cTI - 20 pin connector J17 to reduce the stub length of the JTAG signals.



## cTI20 JTAG BUFFERS



JTAG\_DIR = H: A -> B  
JTAG\_DIR = L: B -> A  
OE = H: output = Hi-Z



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Title SOC JTAG INTERFACE AND JTAG BUFFERS

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A vertical bar divided into four segments labeled A, B, C, and D from bottom to top. Segment B contains a right-pointing arrow.

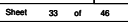


A schematic diagram of a vertical tube. The tube is divided into two sections by a horizontal line. The bottom section is labeled 'A' and the top section is labeled 'B'.



5	4	3	2	1
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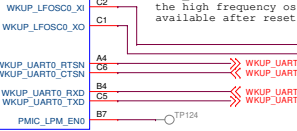
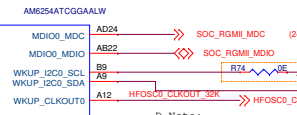
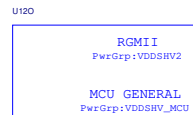
D-Note:  
Follow SK-AM62P-LP for the latest  
FT4232 implementations.



U120

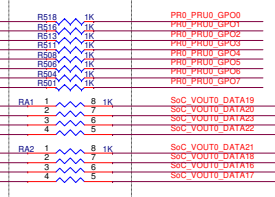
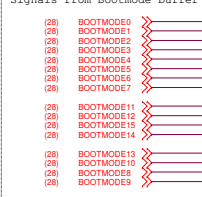
RGMI I  
PwrGrp:VDDSHV2

MCU GENERAL  
PwrGrp:VDDSHV\_MCU



D-Note:  
Delete or reduce the series resistor value to 0R when buffers are not used. The series resistors can be used to isolate the alternative function for testing the bootmode configuration.

Signals from Bootmode buffer



D-Note:  
Shorting of multiple boot mode inputs (IOs) together is not recommended or allowed since the IOs have alternative functions that could be configured after booting. Shorting the boot mode pins directly to VCC or ground is not recommended. Connect each of the boot mode pins through separate resistors. Choose the boot mode resistor value based on the use case (10K or similar).

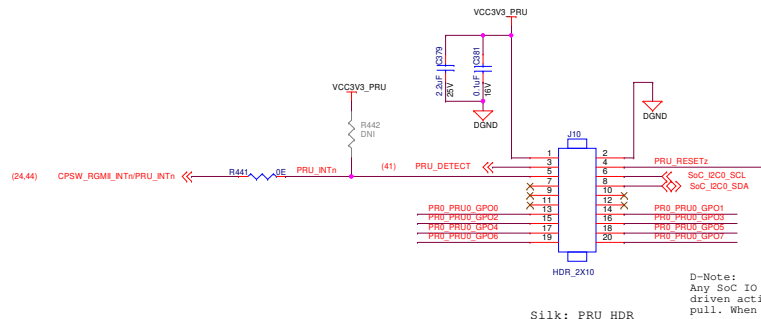
D-Note:  
LVC MOS IO buffers used to implement GPMC interface are off during reset and after reset until the host configures the interface. The recommendation is to add pulls for memory interface signals that can float. The required pulls for the GPMC interface signals are added on the GPMC interface add-on card.

**D-Note:**  
When the boot mode isolation buffers are not used, connect the boot mode configuration resistors directly to the SoC boot mode input pins. Connect the SoC bootmode signal used for alternative function to the attached device through OR for isolation or testing.

istor at the output of the buffer is recommended when the bootmode signal is used for alternate functions to limit the buffer current. When bootmode isolation buffers are not used, connect the bootmode signal resistors directly to the SoC bootmode input pins. Connect the bootmode signal used for alternate function to the attached device for isolation or testing.

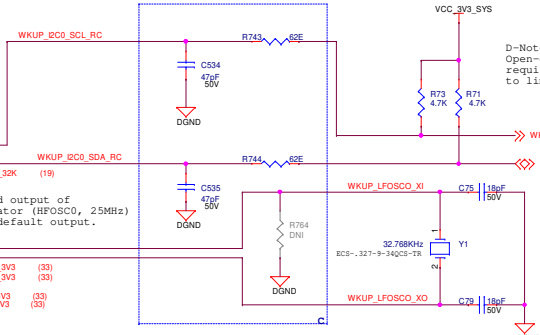
D-Note:

1. 1k resistor at the output of the buffer is recommended when the bootmode pins are used for alternate functions to limit the buffer current
2. When bootmode isolation buffers are not used, connect the bootmode configuration resistors directly to the SoC bootmode input pins. Connect the SOC bootmode signal used for alternate function to the attached device through OR for isolation or testing.



D-Note:  
Any SoC IO that has a trace connected but not being driven actively needs to be connected to an external pull. When adding pull is not feasible, ensure that the traces are routed away from noisy signals.

D-Note:  
Processor IOs connected to the PRU Header are not fail-safe.  
No external input shall be driven when the starter kit is not powered-up.

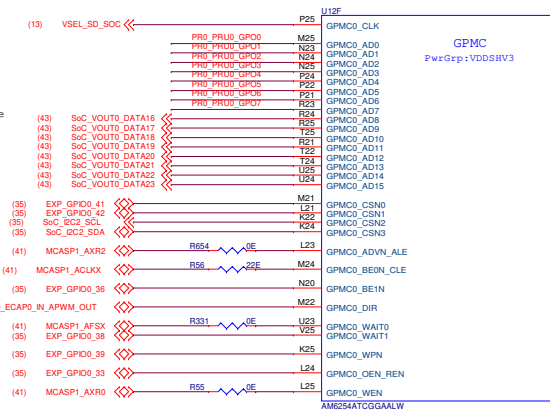


D-Note:  
Open-drain output type buffer I2C interfaces have slew rate requirement specified when pulled to 3.3 V. An RC is used to limit the slew rate

D-Note: The only LFOSC0 register bits that should be changed by the customer are BP\_C, PD\_C, and CTRLMMR\_WKUP\_LFOSC0\_TRIM[18:16], where PD\_C is reset (0) to enable the oscillator and the BP\_C bit is only set (1) to place the oscillator in bypass mode when using an LVCMOS clock source. The CTRLMMR\_WKUP\_LFOSC0\_TRIM[18:16] bits are set based on the actual capacitance load applied to the crystal, as defined by the Load Capacitance Equation. The load capacitance range of the crystal will be half of the recommended capacitor value range, since they are connected in series with the resonant circuit of the crystal.

D-Note:  
Add a series resistor 0R when used as GPMC0\_CLK.

D-Note:  
Add a series resistor 0R when used as GPMC0\_CLK.

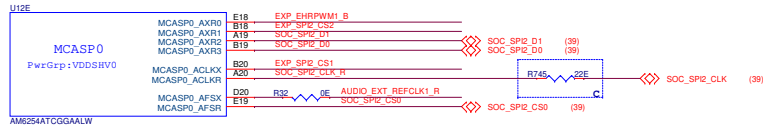


D-Note:  
LDO can source up to  
500mA current

## USER EXPANSION CONNECTOR

D-Note:  
SoC IO buffers are off during reset. A parallel pull is recommended near to the attached device input that is being driven by the SoC IO (input does not float).

R-Note:  
These supplies are off by default. The supplies are controlled by the below load switches and need to be enabled.



CAD Note:  
R32 (Series damping resistor) should be placed closer to the SoC.

D-Note:  
EXP\_CLKOUT\_SEL is high by default to maintain compatibility with the previous version EVM

VCC\_3V3\_SYS

R717

(34) EXP\_GPIO0\_42

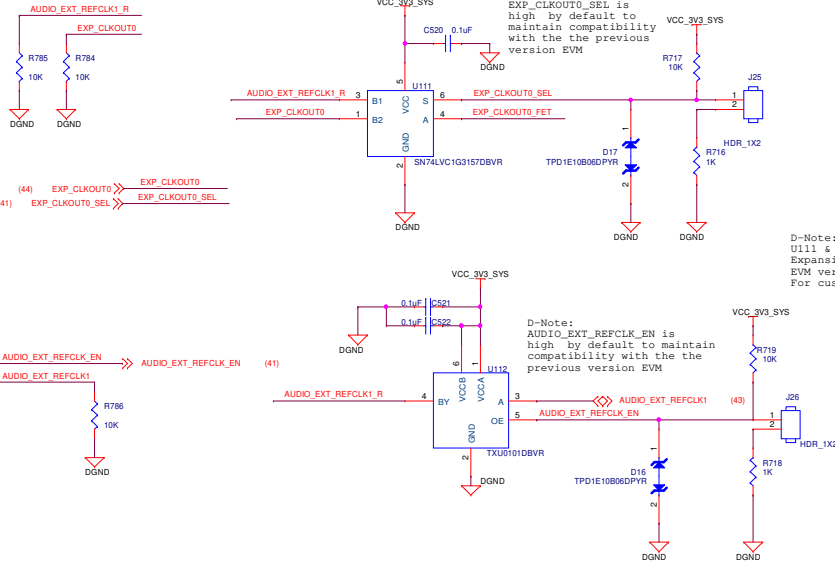
(44) EXP\_GPIO1\_22

(44) EXP\_SPD0\_D0

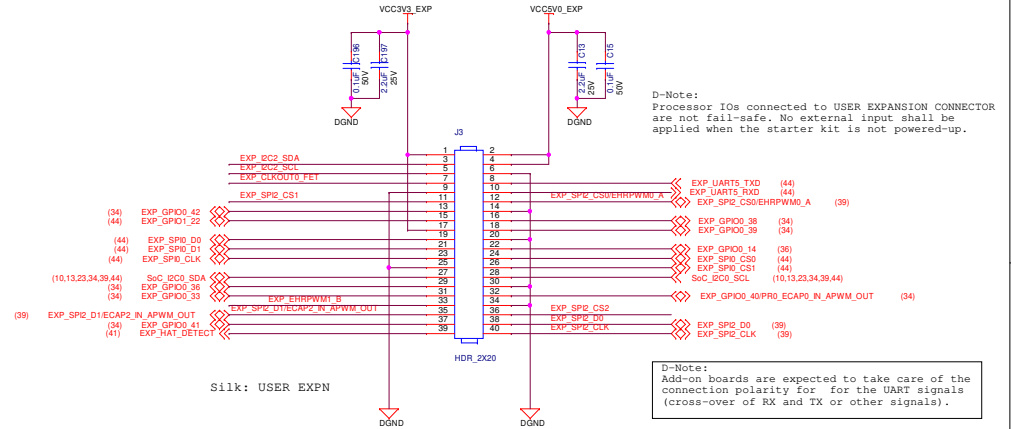
(44) EXP\_SPD0\_D1

(44) EXP\_FPGA\_0

EXP\_SP2\_CS1

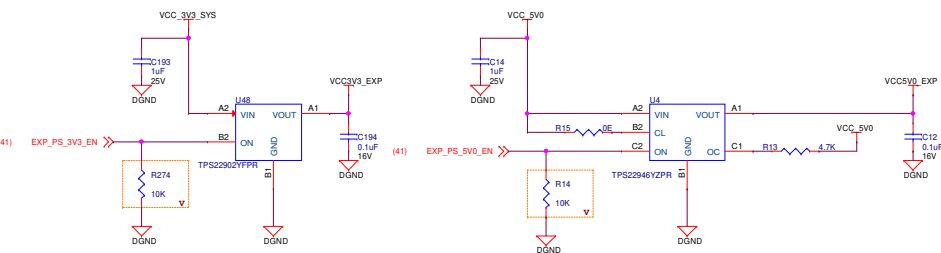


D-Note:  
U111 & U112 are added to provide support for connecting DANTE daughter card on the User Expansion Connector (without affecting the connection compatibility with the previous EVM version).  
For custom board designs, U111 & U112 can be deleted (based on the architecture).



**D-Note:**  
Add-on boards are expected to take care of the connection polarity for for the UART signals (cross-over of RX and TX or other signals).

## LOAD SWITCHES FOR USER EXPANSION CONNECTOR



**R-Note:**

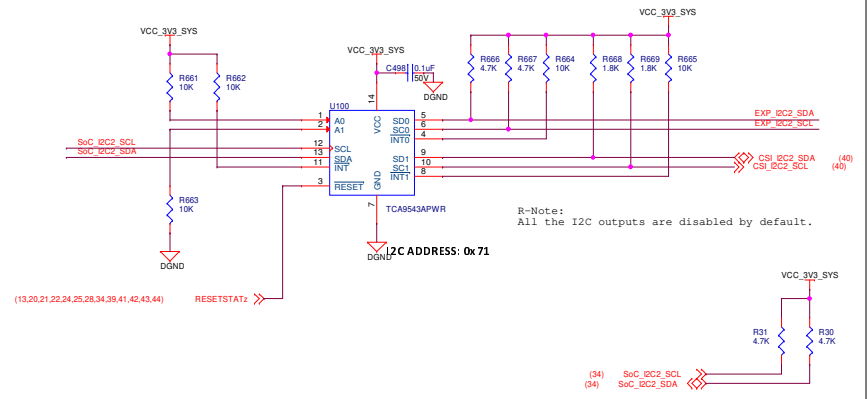
The Starter Kit shall not be powered through the 5V0 or 3V3 supply pins on the 40-pin User Expansion Connector (the pins are output supply).

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62P Starter Kit is not powered.

5V supply on User Expansion Connector can source 150mA max.

3V3 supply on User Expansion Connector can source 500mA max.

## I2C SWITCH FOR SoC\_I2C2



R-Note:  
All the I2C outputs are disabled by default.

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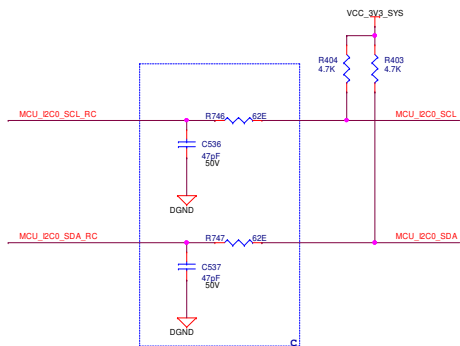
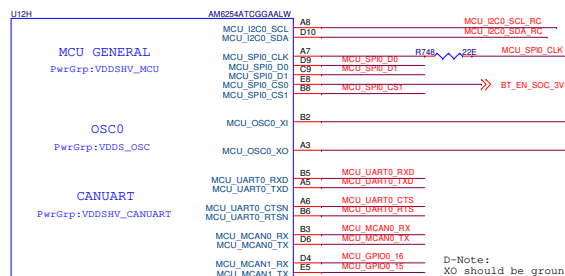


Title	USER EXPANSION CONNECTOR
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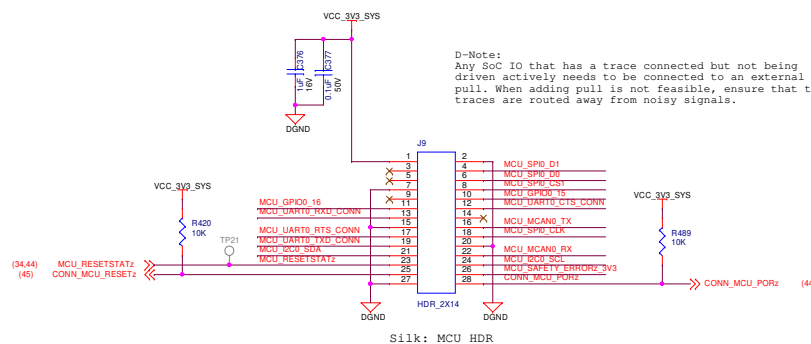
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D-Note:  
MCU\_I2C0  
A pull-up is recommended for open-drain output type I2C interfaces, irrespective of the IO usage or IO configuration. Refer to the Pin Connectivity Requirements table of the SoC datasheet.

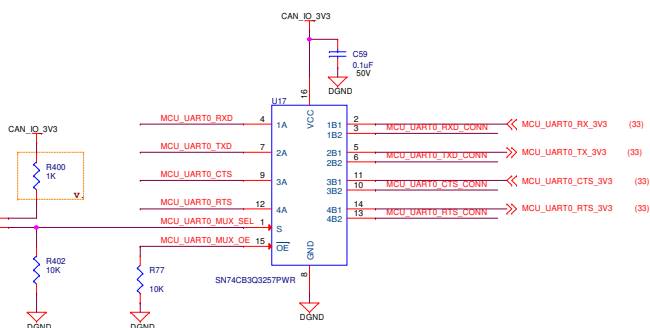
## SOC - MCU DOMAIN



## SOC-MCU HEADER



## SOC - MCU\_UART0 MUX



OEn	SEL	INPUT/OUTPUT An	
L	L (DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER

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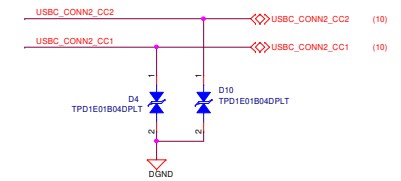


Title SOC-MCU DOMAIN IO, OSC0 and SOC-MCU IO HEADER

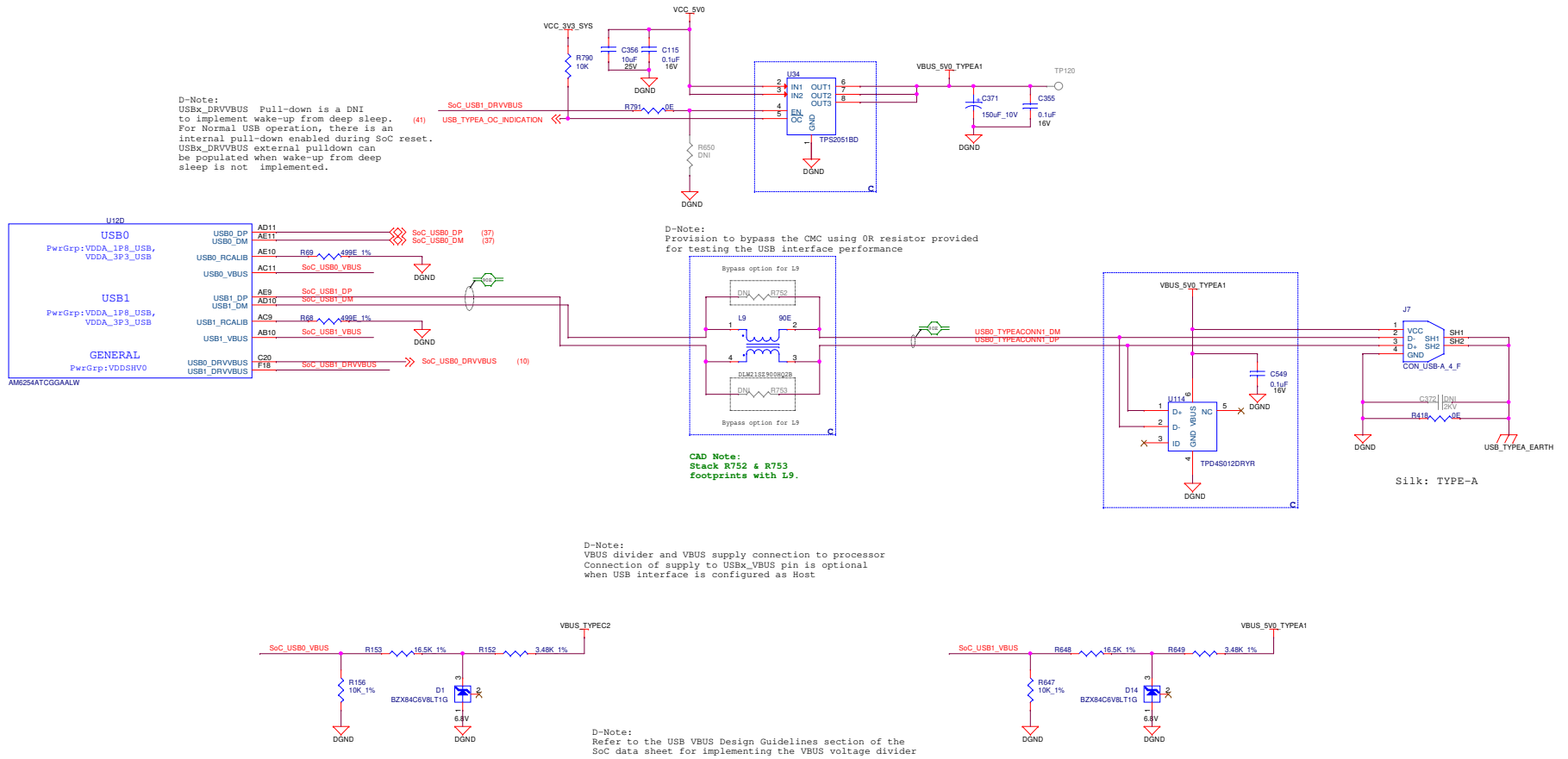
Size	Rev
C	B
Date: Friday, May 08, 2025	Sheet 36 of 46



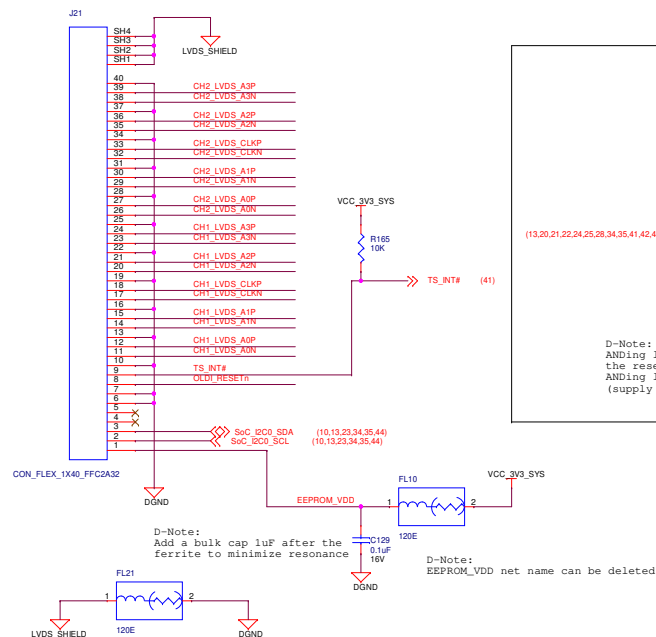
D-Note:  
Refer to the SK/EVM user's guide for the recommended power adapters.  
Using the recommended adapter is recommended for proper functioning of SK/EVM  
Reference Document:  
EVM User's Guide : <https://www.ti.com/lit/pdf/SPRUJ40>  
Reference section : Power Requirement

[illegible]

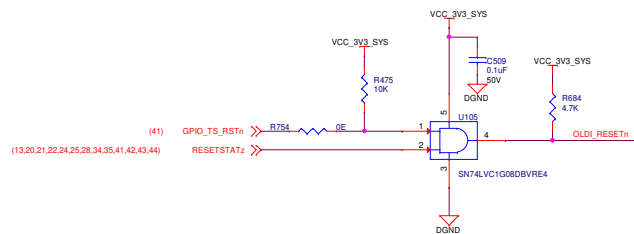
## USB1 - USB 2.0 TYPE-A



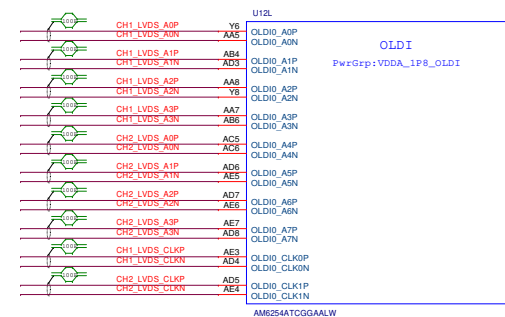
## OLDI DISPLAY INTERFACE



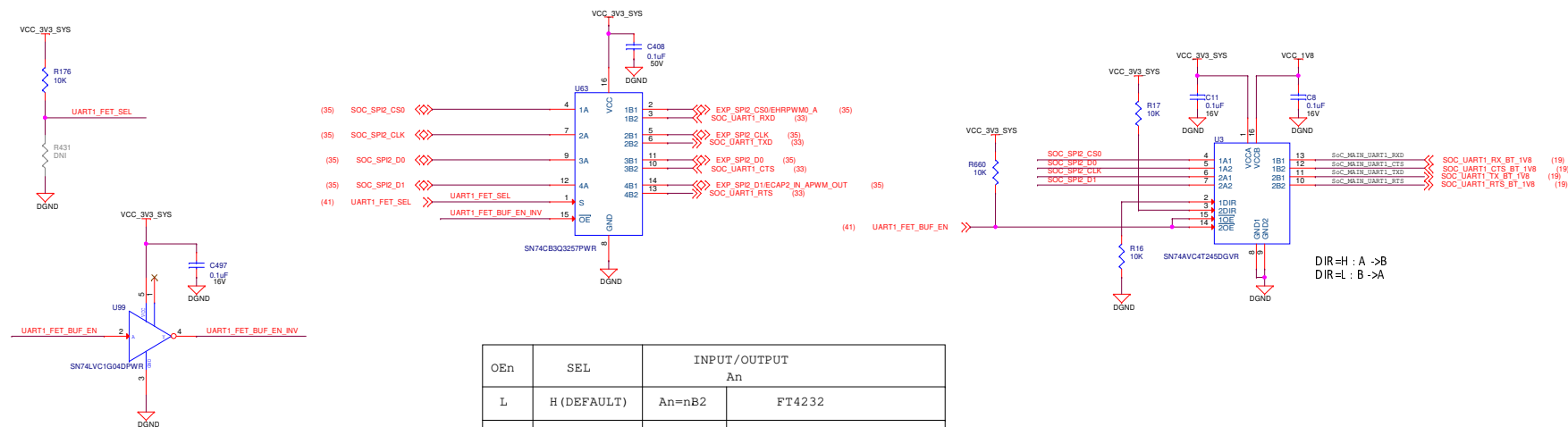
**OLDI RESET**



D-Note:  
 ANDING logic additionally performs level translation. Verify  
 the reset IO level compatibility before optimizing the reset  
 ANDING logic. IO level mismatch can cause residual voltage  
 (supply leakage) and affect PMIC/SoC operation.



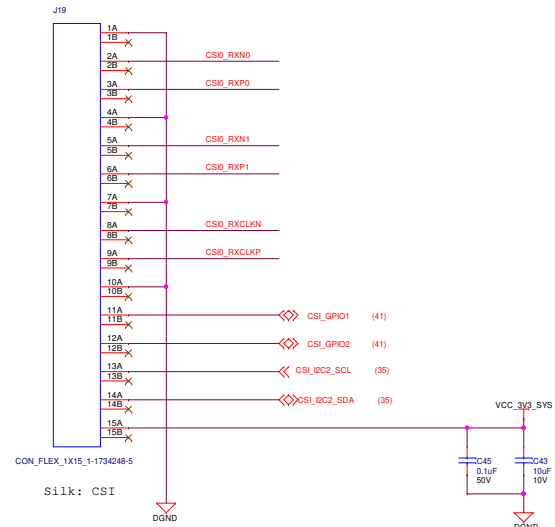
## SoC UART1 FET SWITCH & BUFFER



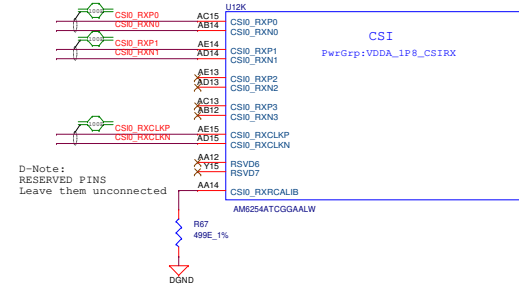
OEn	SEL	INPUT/OUTPUT An	
L	H (DEFAULT)	An=nB2	FT4232
L	L	An=nB1	USER EXPANSION CONNECTOR

# CSI INTERFACE

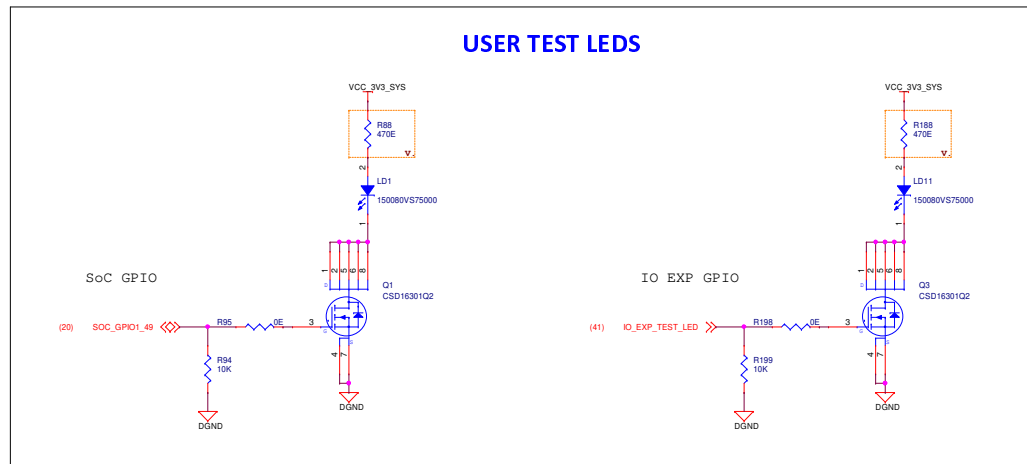
## CSI CAMERA HEADER



R-Note:  
Based on the end product requirement, interface the CSI signals to the respective attached devices.



## USER TEST LEDS



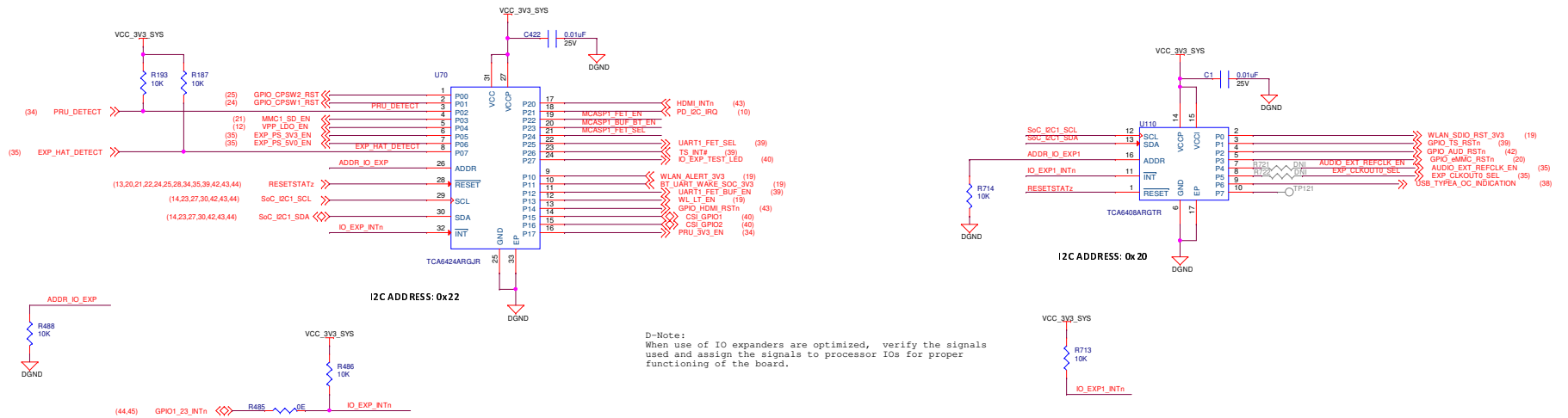
Designed for TI by Mistral Solutions Pvt Ltd



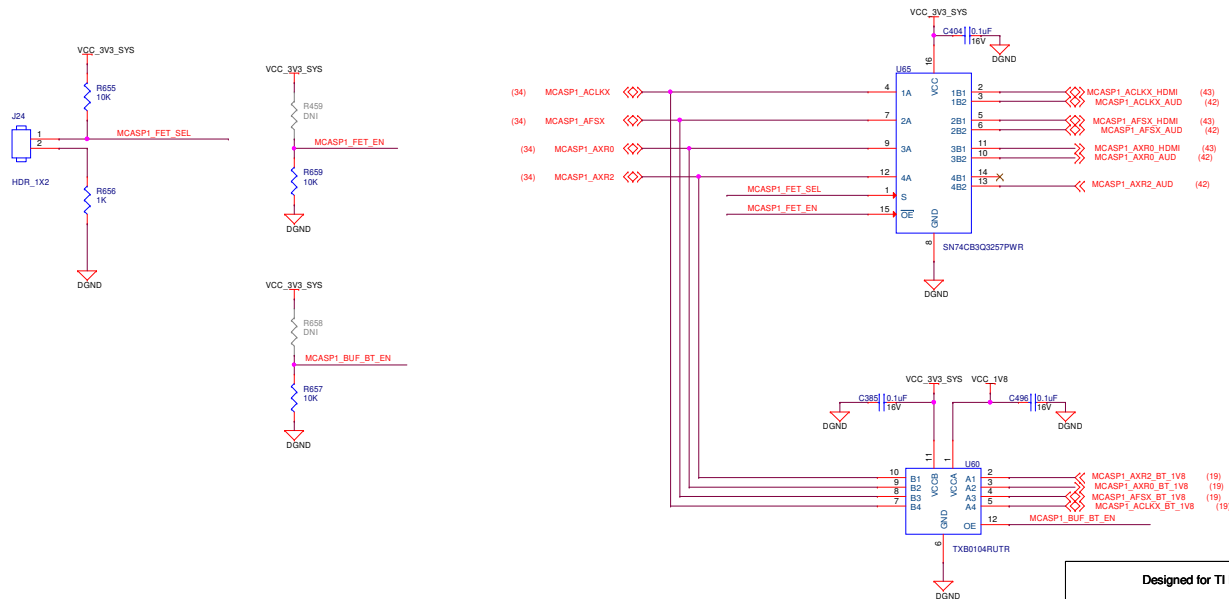
Title SOC CSI INTERFACE AND CAMERA CONNECTOR

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## IO EXPANDERS



## MCASP1 FET SWITCH & BUFFER



OEn	SEL	INPUT/OUTPUT	
		An=nB2	An
L	H (DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

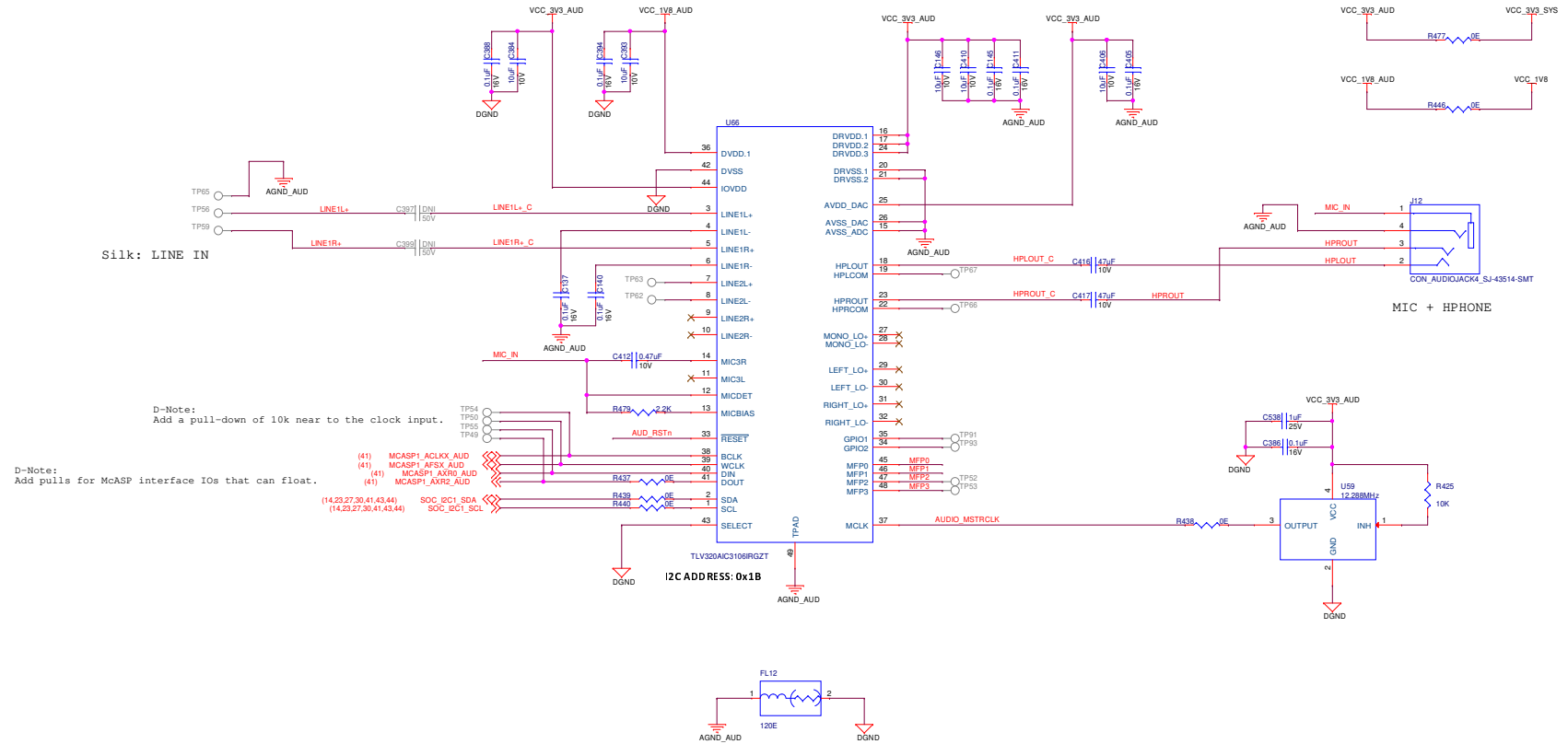
Designed for TI by Mistral Solutions Pvt Ltd



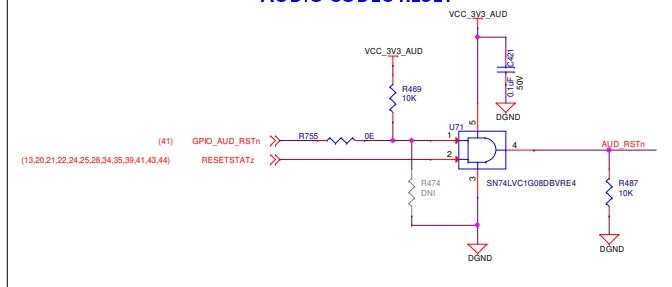
Title IO EXPANDER AND MCASP1 FET SWITCH & BUFFER

Size	Rev
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Date: Friday, May 08, 2025	Sheet 41 of 46

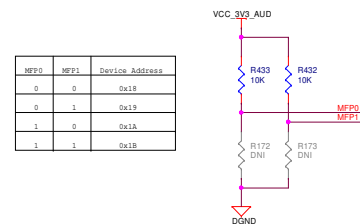
# AUDIO CODEC



## AUDIO CODEC RESET



## CODEC I2C ADDRESS SELECTION



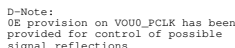
Designed for TI by Mistral Solutions Pvt Ltd



Title AUDIO CODEC

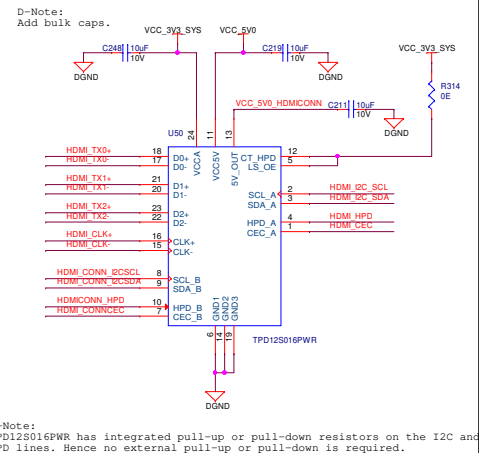
Size	Rev
C	B
Date: Friday, May 08, 2025	Sheet 42 of 46

A vertical bar divided into four segments labeled A, B, C, and D from bottom to top. Segment B contains an arrow pointing to the right.

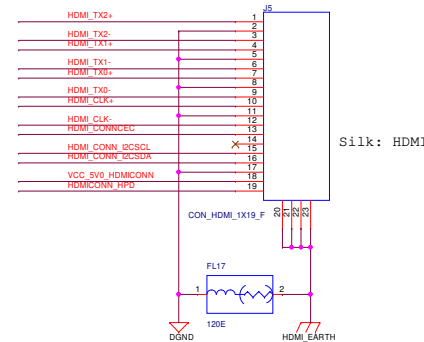


## HDMI INTERFACE

I2C ADDRESS: 0x3B, 0x3E, 0x62



D-Note:  
TPD12S016PWR has integrated pull-up or pull-down resistors on the I2C and HPD lines. Hence no external pull-up or pull-down is required.



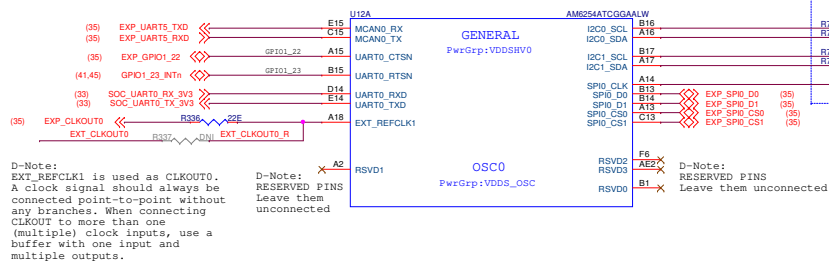
**HDMI RESET**

The diagram illustrates the HDMI RESET circuit. It features an inverter (SN74LVC1G08DBVRE4) with its input (pin 1) connected to the GPIO\_HDMI\_RSTn signal (pin 41) through a 75Ω resistor (R756). The input is also pulled up to VCC\_3V3\_SYS by resistor R389 (10K) and pulled down to DGND by resistor R390 (DN1). The output (pin 4) of the inverter is connected to the RESETSTATz signal (pins 13, 20, 21, 22, 24, 25, 28, 34, 35, 39, 41, 42, 44) through a 10K resistor (R373). The output is also pulled up to VCC\_3V3\_SYS by resistor R389 (10K) and pulled down to DGND by resistor R390 (DN1). A decoupling capacitor C323 (0.1μF) is connected between VCC\_3V3\_SYS and DGND.

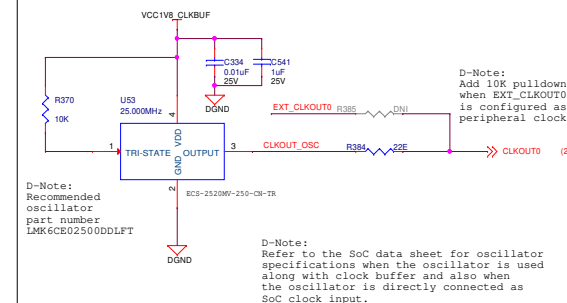

MISTRA

C	PROC142B(002)
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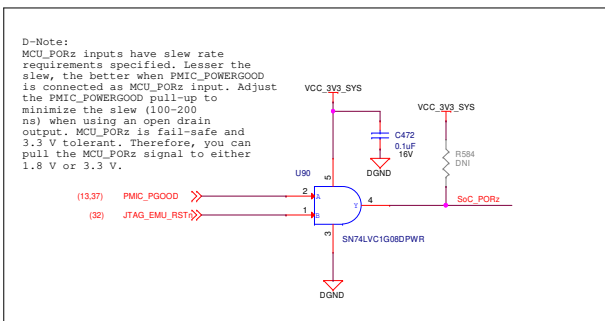
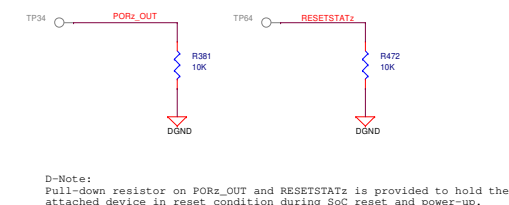
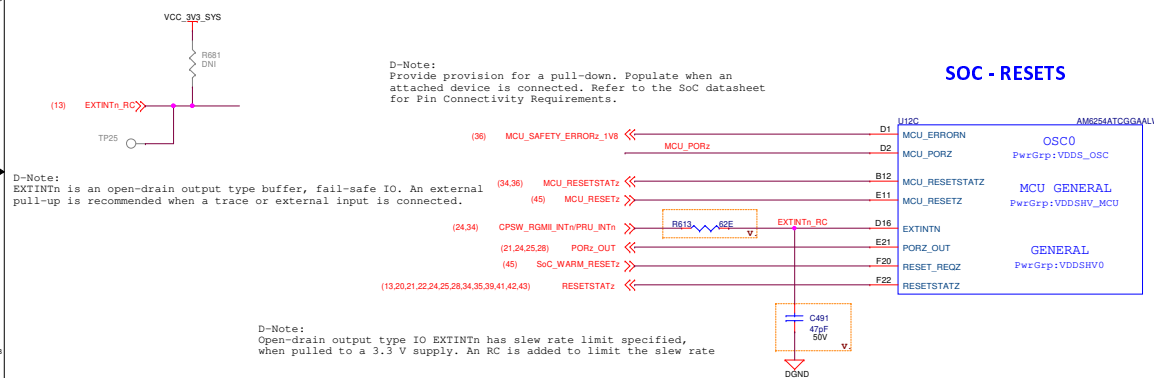
## SOC - GENERAL



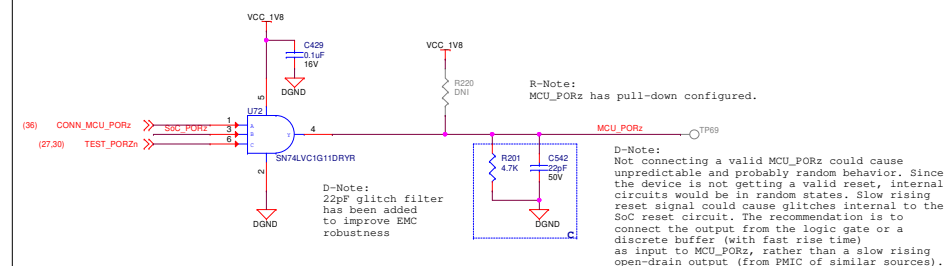
## OSCILLATOR



## SOC - RESETS



## MCU POWER ON RESET



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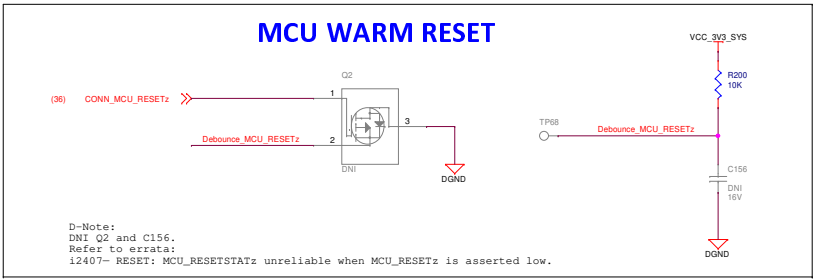
Title SOC RESETS AND IOs, AND EXTERNAL LVCMOS CLOCK (OSCILLATOR)

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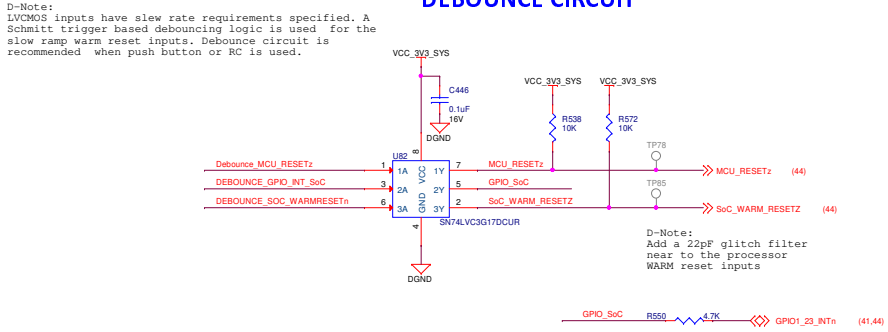


# EXTERNAL RESET INPUT AND SCHMITT TRIGGER DEBOUNCE LOGIC

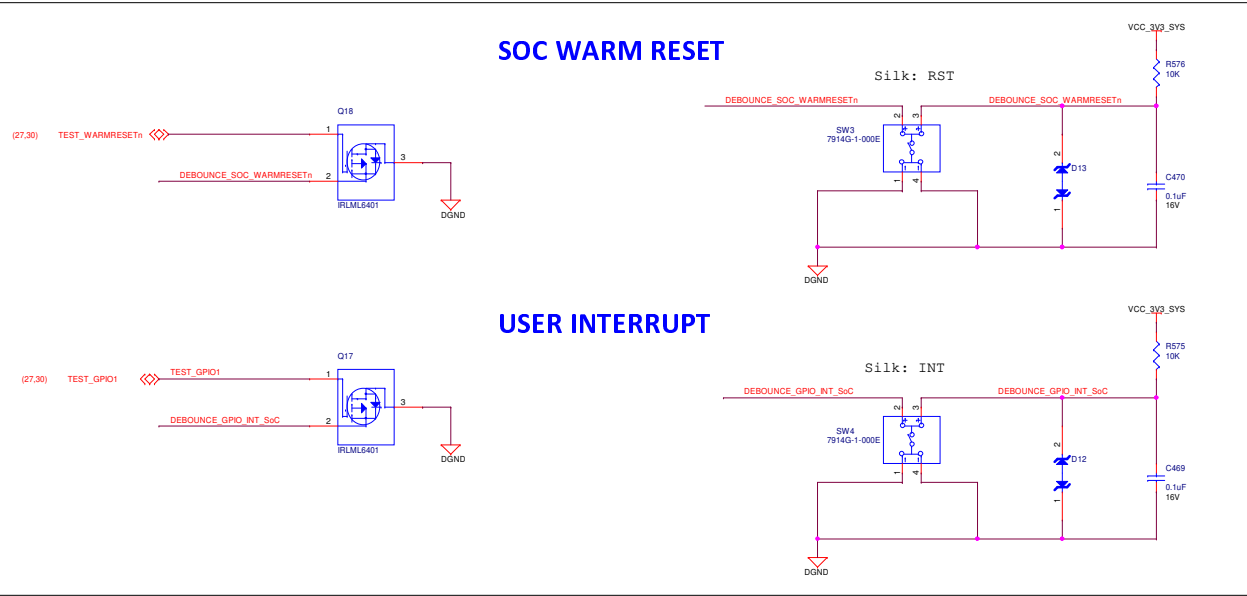
## MCU WARM RESET



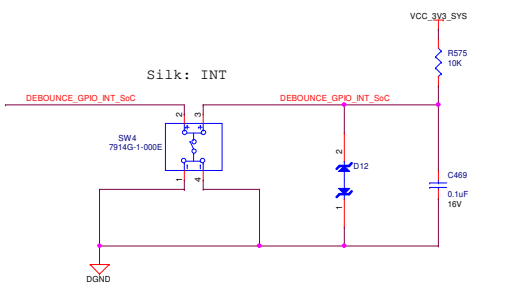
## DEBOUNCE CIRCUIT



## SOC WARM RESET



## USER INTERRUPT



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Title		SOC PUSH BUTTON RESET INPUTS, DEBOUNCE LOGIC FOR RC RESET	
Size	PROC142B(002)	Rev	B
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MOUNTING HARDWARE

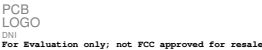
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards, IPC-A-610 Class 2, unless otherwise specified
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB



LOGOs



LABELS

Board Serial No.



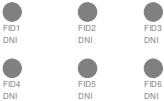
Assembly Revision



STANDOFF,SCREW & WASHER FOR PCIe M.2



FIDUCIALS



ORDERABLE PART NO



Oderable Part Number	
Variant	Label Text
001	SK-AM62-P1
002	SK-AM62B-P1

R-Note:  
Refer to STRAP CONFIGURATION OF ETHERNET PHYS  
page from SK-AM648 schematics.

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Title ASSEMBLY NOTES AND MOUNTING HARDWARE

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