

AM62A7 / AM62A3 LOW POWER STARTER KIT SK (EVM) WITH TPS65931211-Q1 PMIC

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Revision Number

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REV	A1
VER	1.2

D-Note :-

SK/EVM is a device evaluation board or platform. The SK/EVM is not a reference design. In some cases the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SOC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata, and TRM when designing their custom board. The information found in the datasheet should always take precedence over the SK/EVM implementation.

R-Note :-

- * Verify the DNI components configuration with respect to the SK schematics (Use PDF) after completion of board design before board assembly
- * A standard 5% tolerance resistor can be used for most of the series and parallel pull resistor
- * Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build. (Refer FAQs listed for additional details)

KEY LINKS TO COLLATERALS

Hardware Design Guide : https://www.ti.com/lit/an/sprad85/sprad85.pdf
Schematic Design and Review Checklist : https://www.ti.com/lit/an/sprad21d/sprad21d.pdf
PMIC Power Solutions Application Note : https://www.ti.com/lit/po/slv204/slv204.pdf
DDR Board Design and Layout Guidelines : https://www.ti.com/lit/an/sprad66a/sprad66a.pdf
SKs (Starter Kits) for reference : SK-AM62B, SK-AM62B-P1, SK-AM62-LP, SK-AM62-SIP, SK-AM62A-LP, SK-AM62P-LP

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REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	09 AUG 2023	Drafted from "PROC135E3_SCH" document.	Mistral Design Team	Nishant	Ajit MB
0.2	18 AUG 2023	Updated SoC, eMMC & PMIC Part Number	Mistral Design Team	Nishant	Ajit MB
1.0	21 AUG 2023	Baselined and Released	Mistral Design Team	Nishant	Ajit MB
1.1	11 JUNE 2024	Updated SoC Pin name (VMON_VSYS), Enabled Voltage ratings for all the capacitors and added Design Review notes Moved to DNI : C33, C36, C291, C177, R272, U56, Y1 Moved to Mount : C556, R295, R296, R297, R299, R300, R301, R302, R303, R505, R534 C290 - 1uF changed to 2.2uF; C288,C184,C181,C39 - 1uF changed to 0.1uF; C45,C42 - 9pF changed to 18pF; C182,C179 - 2.2uF changed to 1uF; C40 - 4.7uF changed to 1uF; C38 - 0.1uF changed to 4.7uF R350 - 2.2K changed to 10K; R125,R135 - 3.4K_1% changed to 3.48K_1%; R343 - 22E changed to 0E; R315,R242,R371 - 49.9K_1% changed to 10K; R368 - 10K_1% changed to Std 10K; R311 - 100K changed to Std 10K; R342,R341,R586,R584 - 22E_1% changed to 0E; R331,R344,R328 - 499E_0.1% changed to 499_1%; R451 - 10K changed to 47K; R351,R611 - 11K_1% changed to 10K_1%.	Mistral Design Team	Pandiya Rajan	Ajit MB
1.2	13 FEB 2025	Updated SoC Part Number	Mistral Design Team	Pandiya Rajan	Ajit MB

LINKS TO KEY FAQs

https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1203305/faq-am62a7-and-am62a7-q1-custom-board-hardware-design-collaterals-to-get-started
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1203441/faq-am62a3-and-am62a3-q1-custom-board-hardware-design-collaterals-to-get-started
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1306030/faq-am62p-am62p-q1-custom-board-hardware-design---faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1340905/faq-am62a7-am62a7-q1-am62a3-am62a3-q1---custom-board-hardware-design---guidelines-for-reuse-of-sk-am62a-lp-schematics
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1347063/faq-am62a7-and-am62a7-q1-am62a3-and-am62a3-q1---custom-board-hardware-design---design-and-review-notes-for-reuse-of-sk-am62a-lp-schematics
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1280753/faq-am62a7-am62a7-q1-am62a3-am62a3-q1-custom-board-hardware-design---faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit

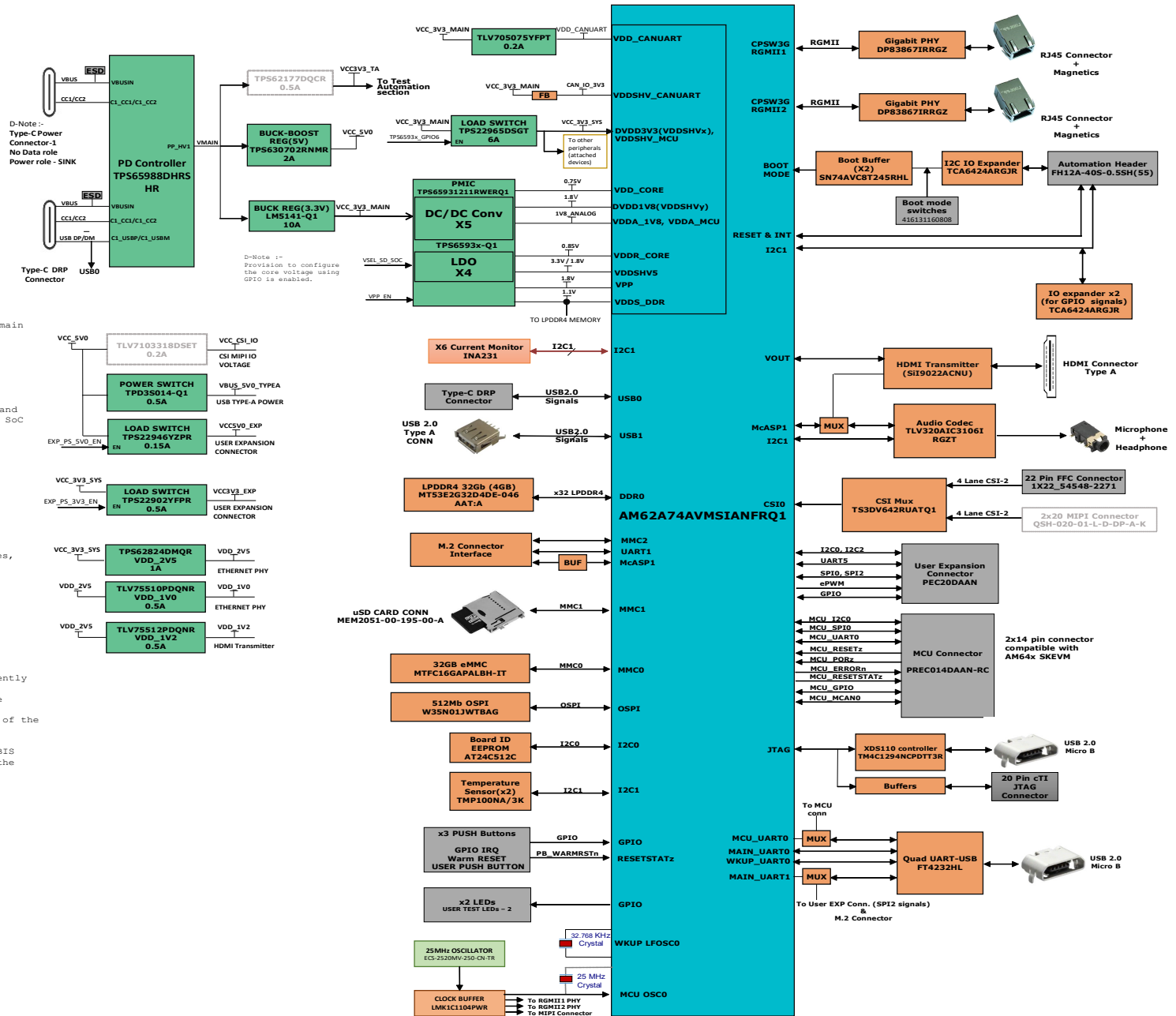
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BLOCK DIAGRAM SK-AM62A-LP



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BLOCK DIAGRAM_XDS110

D-Note :-
Please follow SK-AM62P-LP implementations
for latest updates on XDS110

The diagram illustrates the internal architecture of the XDS110, which acts as a bridge between the AM62A SoC and the TI20 pin JTAG Connector. Key components and connections include:

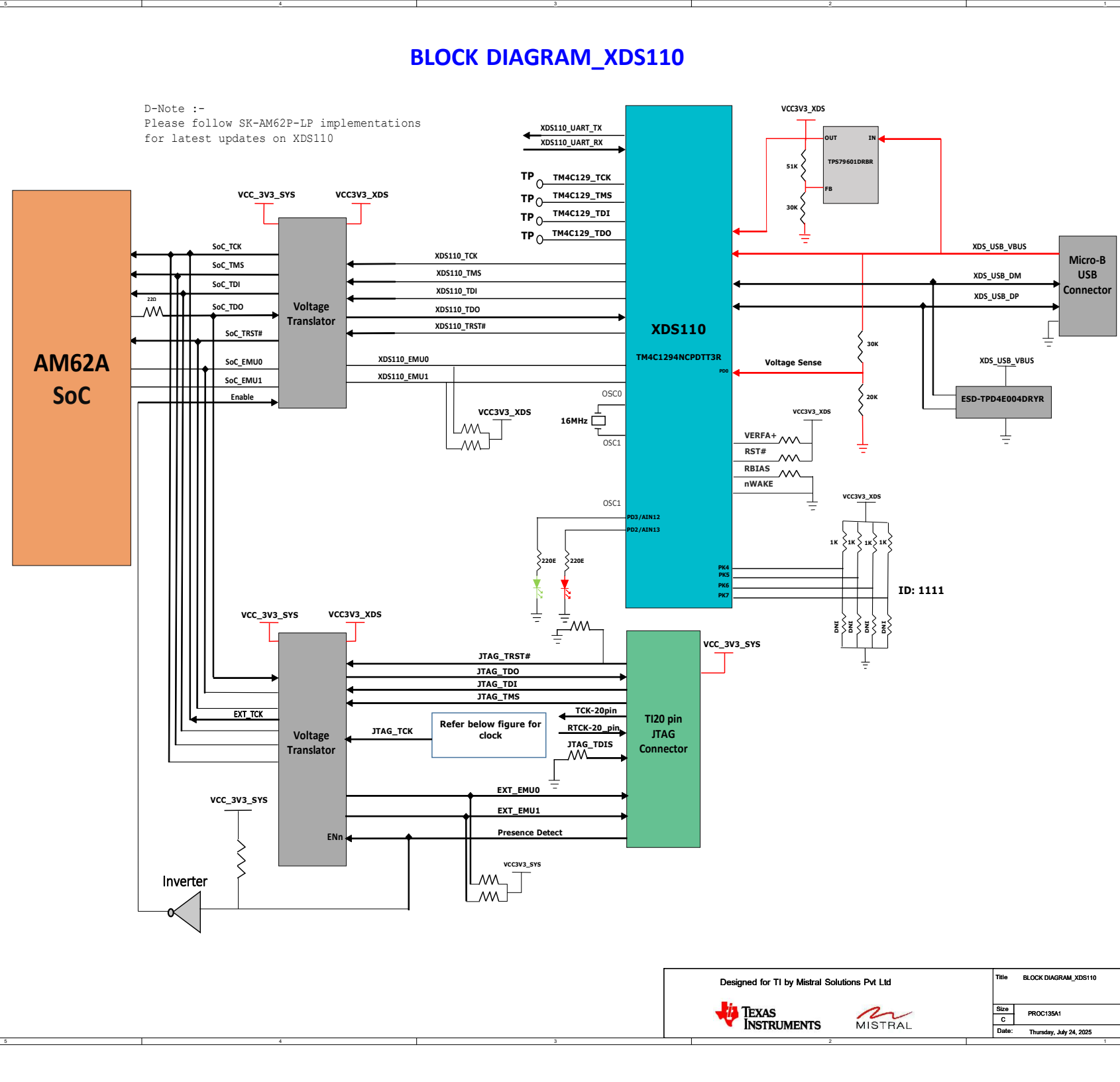
- AM62A SoC:** The target device on the left, providing various control signals to the XDS110.
- Voltage Translators:** Two translators are used to interface the SoC's logic levels with the XDS110's internal logic and the JTAG connector's signals.
- XDS110 Microcontroller:** The central component, a TM4C1294NCPDTT3R, which manages the data flow and control signals.
- UART Interface:** XDS110_UART_TX and XDS110_UART_RX lines connect the microcontroller to the SoC.
- JTAG Interface:** Signals like JTAG_TRST#, JTAG_TDO, JTAG_TDI, JTAG_TMS, and JTAG_TCK are routed through the translators to the TI20 pin JTAG Connector.
- USB Interface:** The XDS110 connects to a Micro-B USB Connector via XDS_USB_VBUS, XDS_USB_DM, and XDS_USB_DP lines. It also includes a voltage sense circuit and a USB-to-I2C bridge (ESD-TPD4E004DRYR).
- Power and Ground:** VCC3V3_SYS and VCC3V3_XDS planes are shown, along with various pull-up and pull-down resistors and capacitors for signal integrity.
- Other Components:** Includes a 16MHz oscillator, a TPS79601DRBR LDO, and an ESD-TPD4E004DRYR bridge.

BLOCK DIAGRAM_XDS110

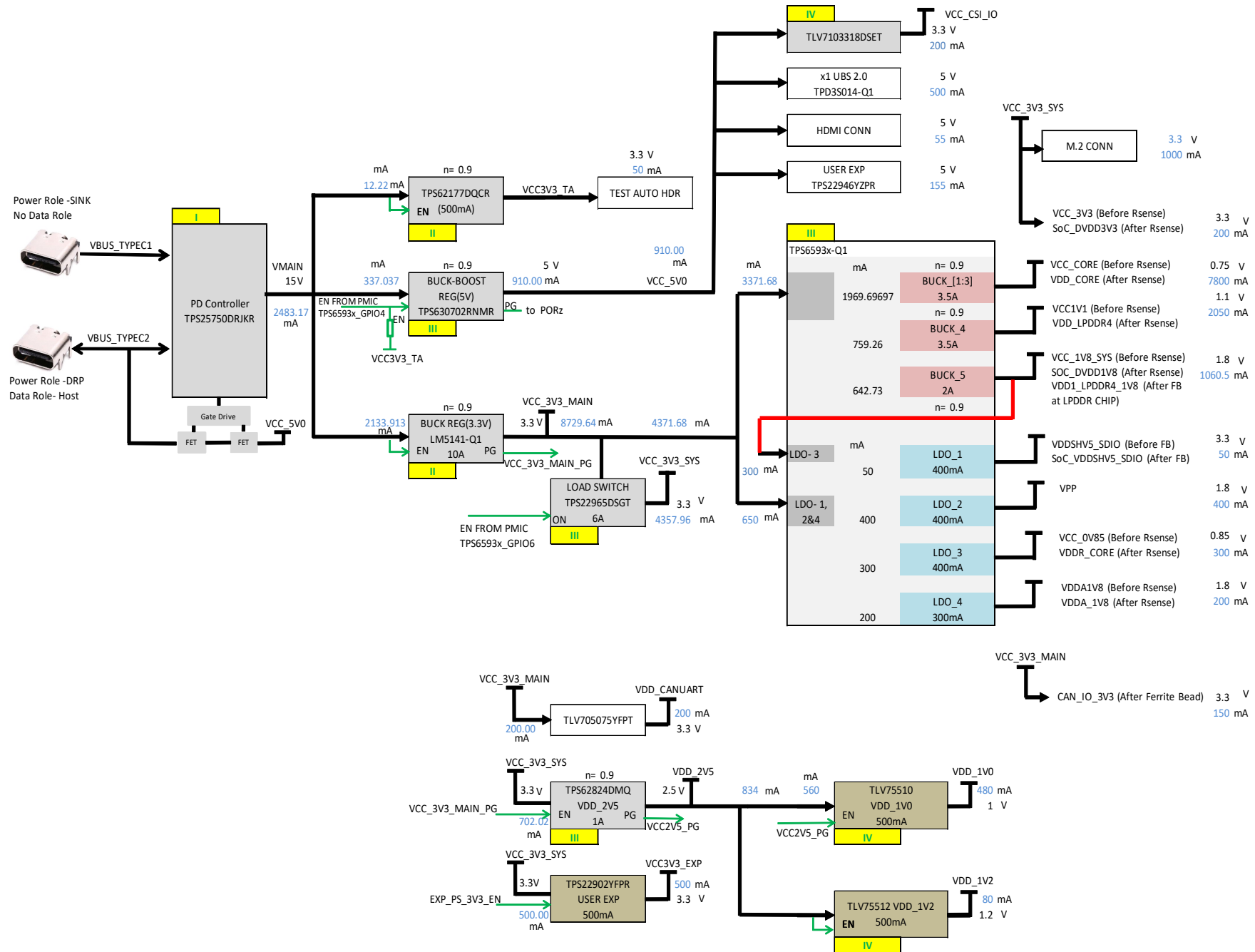
D-Note :-
Please follow SK-AM62P-LP implementations
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- USB Interface:** The microcontroller interfaces with a Micro-B USB Connector via XDS_USB_VBUS, XDS_USB_DM, and XDS_USB_DP lines.
- Power and Ground:** VCC3V3_SYS and VCC3V3_XDS planes are shown, along with various decoupling capacitors and pull-up/pull-down resistors.
- Peripheral Components:** Includes a TPS79601DRBR voltage regulator, an ESD-TPD4E004DRYR ESD protection device, and a 16MHz oscillator.



POWER BLOCK DGM



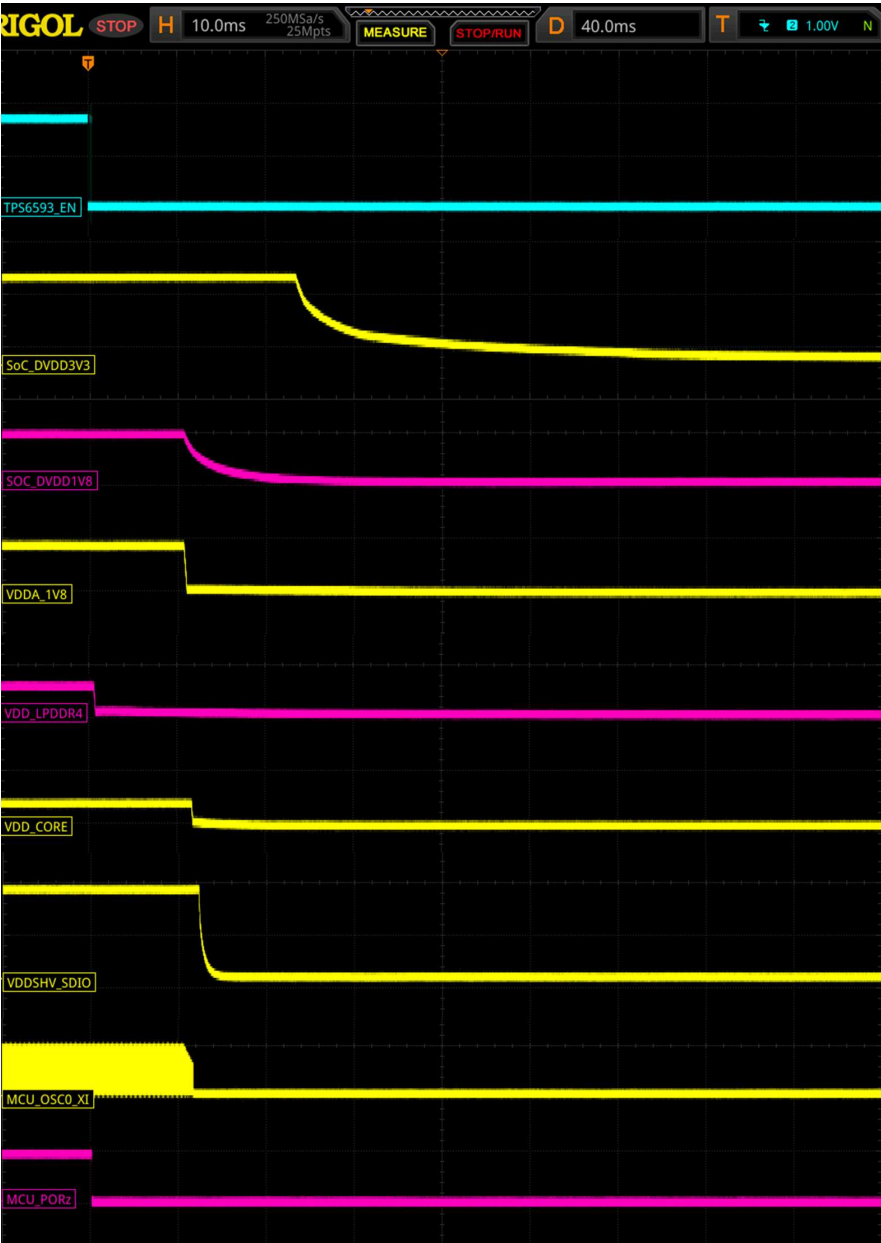
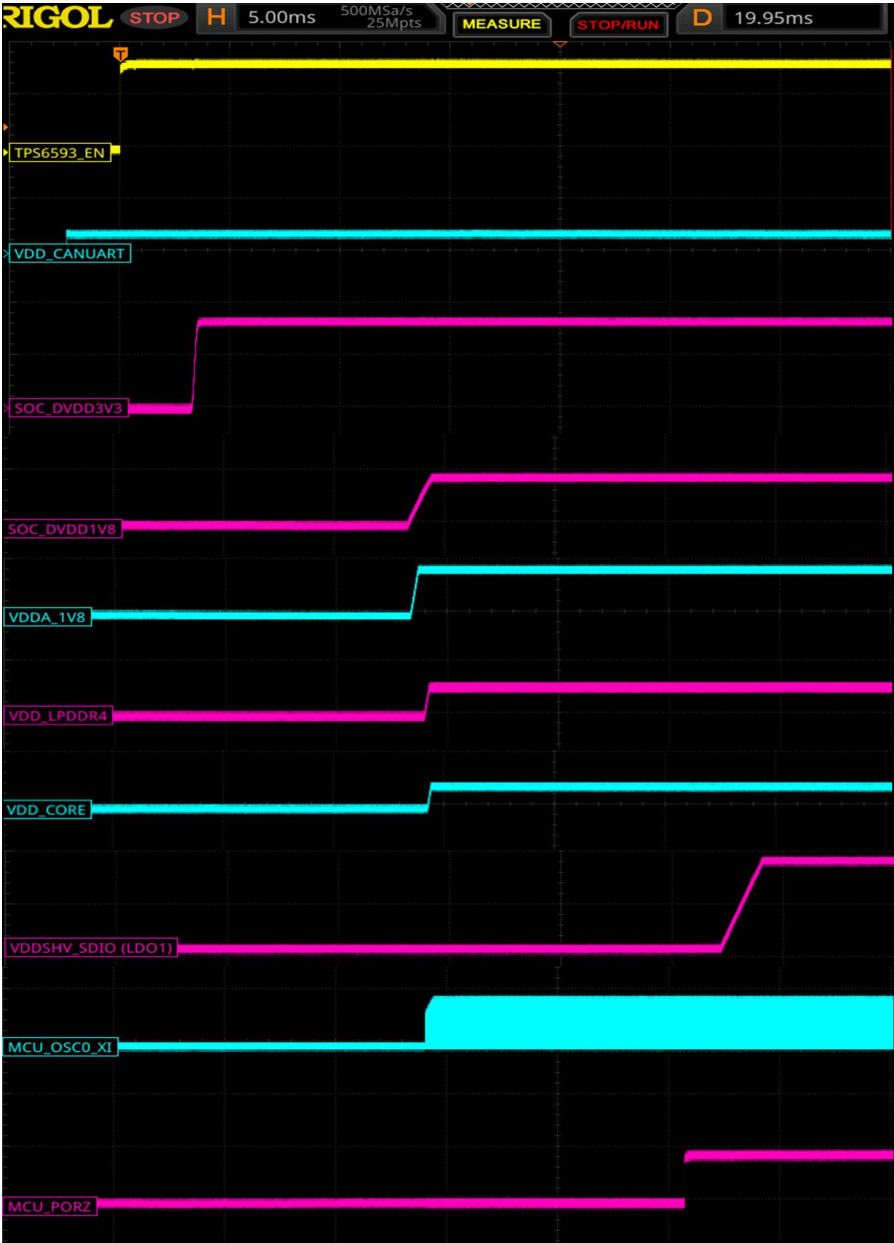
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POWER SEQUENCE



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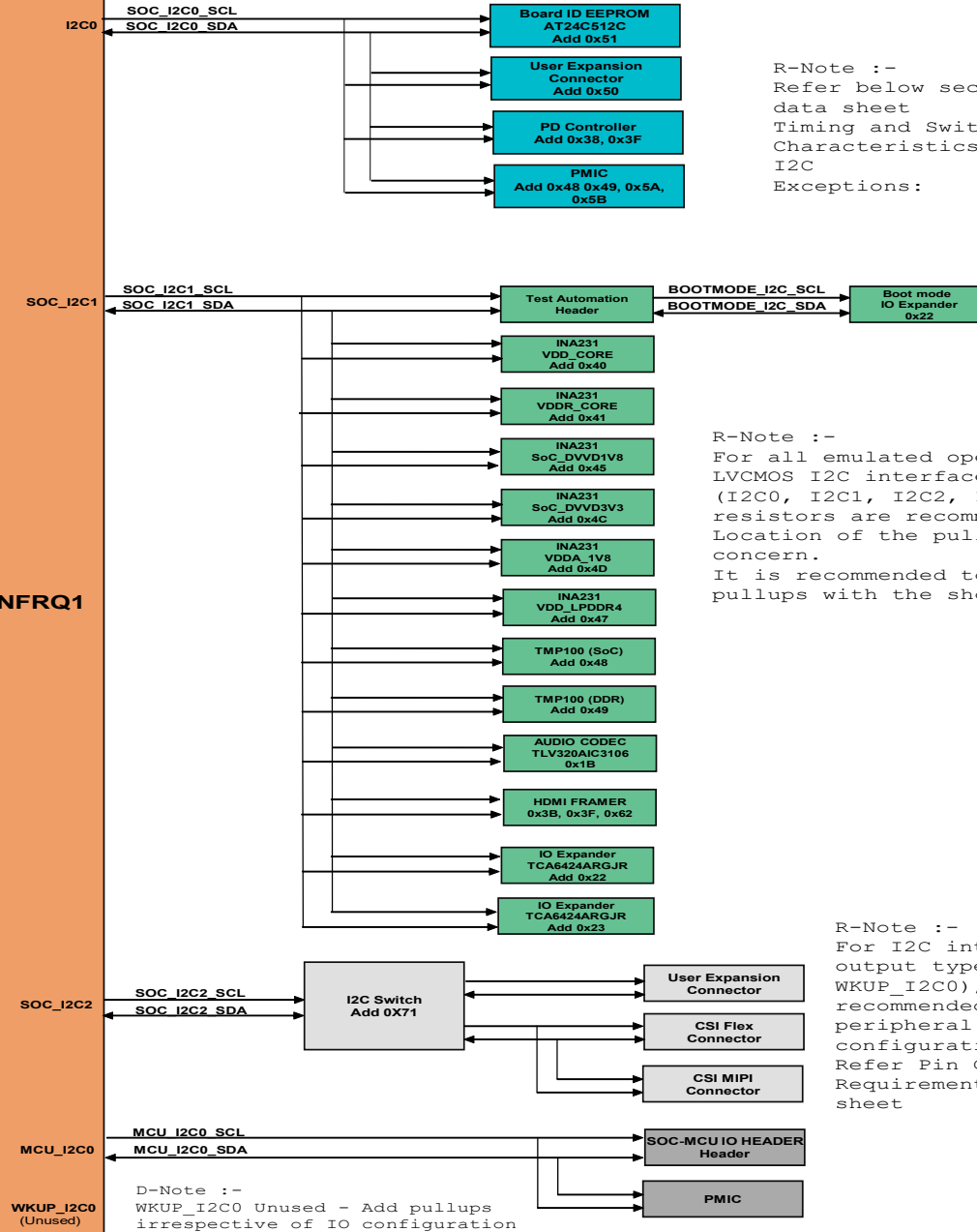


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I2C TREE

R-Note
Add - Indicates
Address

**AM62A74AVMSIANFRQ1
SoC**



R-Note :-
Refer below section of the SOC
data sheet
Timing and Switching
Characteristics
I2C
Exceptions:

R-Note :-
For all emulated open-drain output
LVCMOS I2C interfaces.
(I2C0, I2C1, I2C2, I2C3) pullup
resistors are recommended
Location of the pullup is not a
concern.
It is recommended to connect the
pullups with the shortest possible stub

R-Note :-
For I2C interfaces with open-drain
output type buffer (MCU_I2C0 and
WKUP_I2C0), an external pullup is
recommended irrespective of
peripheral usage and IO
configuration.
Refer Pin Connectivity
Requirements section of SOC data
sheet

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GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE RAIL CONNECTED ON SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SD0D	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC	ENABLE	MCU_GPIO0_0	MCU_SPIO_CS0	OUTPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	MCU Header GPIO0_16	MCU_GPIO0_16	GPIO	MCU_GPIO0_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
7	MCU Header GPIO0_15	MCU_GPIO0_15	GPIO	MCU_GPIO0_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
8	PMIC Interrupt	PMIC_INT_B	INTERRUPT	GPIO0_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV3	SoC_DVDD3V3
9	CAN-FD fast wake up signal from switch	CAN_FD_WKUP_SW_INH	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
10	CAN-FD fast wake signal from MCU header	CAN_FD_WKUP_HDR_INH								
11	Interrupt signal from Automotive Ethernet ADD-ON board	CPSW_ETH2_INH								
12	User test LED control signal	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	Watchdog trigger input signal for Watchdog Trigger mode	PMIC_WDOG_TRIGG	ENABLE	MCU_GPIO0_19	WKUP_I2C0_SCL	INPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
14	WKUP Signal from RGMII2	CPSW_ETH2_WAKE	INTERRUPT	MCU_GPIO0_20	WKUP_I2C0_SDA	INPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
15	User EXP Conn GPIO	EXP_GPIO1_22	GPIO	GPIO1_22	UART0_CTSn	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	GPIO1_23	UART0_RTSn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
17	User Interrupt									
18	User EXP Conn GPIO	EXP_GPIO0_14_LT	GPIO	GPIO0_14	OSPI0_CSn3	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
19	PMIC Standby Disable	PMIC_LPM_EN0	ENABLE	MCU_GPIO0_22	PMIC_LPM_EN0	OUTPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
20	User EXP Conn GPIO	EXP_EHRPWM1_B	GPIO	GPIO1_10	MCASP0_AXR0	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 01										
1	Ethernet Daughter Card plug in detect	RGMII2_BRD_CONN_DET	DETECTION	IO EXPANDER-P00		INPUT	HIGH	LOW		VCC_3V3_SYS
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P01		OUTPUT	HIGH	LOW		VCC_3V3_SYS
3	M.2 module Bluetooth LDO Enable	BT_EN_SOC	ENABLE	IO EXPANDER-P02		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	NA	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P06		OUTPUT	LOW	HIGH		VCC_3V3_SYS
8	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
9	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	IO EXPANDER-P10		OUTPUT	HIGH	LOW		VCC_3V3_SYS
10	eMMC Reset control GPIO	GPIO_EMMC_RSTn	RESET	IO EXPANDER-P11		OUTPUT	HIGH	LOW		VCC_3V3_SYS
11	SOC UART1 Mux Select	UART1_FET_BUF_EN	ENABLE	IO EXPANDER-P12		OUTPUT	HIGH	LOW		VCC_3V3_SYS
12	BT UART WKUP Signal	BT_UART_WAKE_SOC_3V3	INTERRUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER-P14		OUTPUT	HIGH	LOW		VCC_3V3_SYS
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO0	INPUT/OUTPUT	IO EXPANDER-P15		NA	NA	NA		VCC_3V3_SYS
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER-P16		NA	NA	NA		VCC_3V3_SYS
16	WLAN Alert Interrupt	WLAN_ALERTn	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC_3V3_SYS
19	MCASP1 Enable and Direction Control	MCASP1_FET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
20		MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
21		MCASP1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	-		VCC_3V3_SYS
22		UART1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P25		OUTPUT	HIGH	-		VCC_3V3_SYS
23		PD_I2C_IRQ	INTERRUPT	IO EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_SYS
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER - 02										
1	SoC SPI0 MUX Selection	SPIO_FET_SEL	CONTROL	IO EXPANDER-P20		OUTPUT	LOW	-		VCC_3V3_SYS
2	SoC SPI0 MUX Enable	SPIO_FET_OE	ENABLE	IO EXPANDER-P21		OUTPUT	LOW	LOW		VCC_3V3_SYS
3	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	CSI flex and mipi MUX Selection	CSI_SEL2	CONTROL	IO EXPANDER-P23		OUTPUT	HIGH	-		VCC_3V3_SYS
5	CSI MUX Enable	CSI_EN	ENABLE	IO EXPANDER-P24		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
6	Auto PHY mode config	AUTO_100M_1000M_CONFIG	CONTROL	IO EXPANDER-P25		OUTPUT	NA	NA		VCC_3V3_SYS
7	CSI I/O Voltage Select(VCC_CSI_IO)	CSI_VLDO_SEL	CONTROL	IO EXPANDER-P26		OUTPUT	LOW	-		VCC_3V3_SYS
8	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	Wilink Enable	WL_LIT_EN	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
10	CSI Reset Control GPIO	CSI_RSTz	RESET	IO EXPANDER-P11		OUTPUT	LOW	LOW		VCC_3V3_SYS

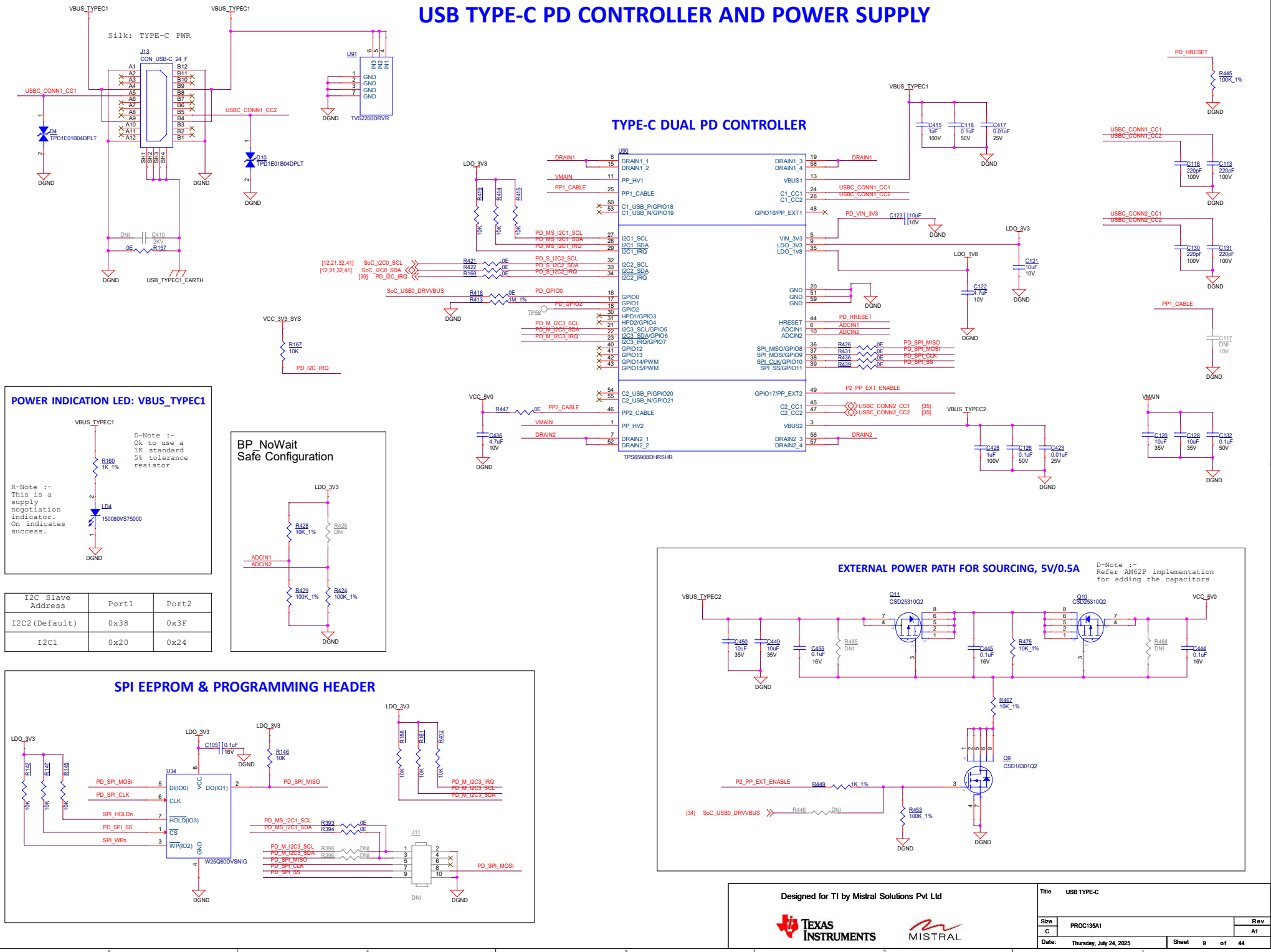
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Title GPIO MAPPING TABLE

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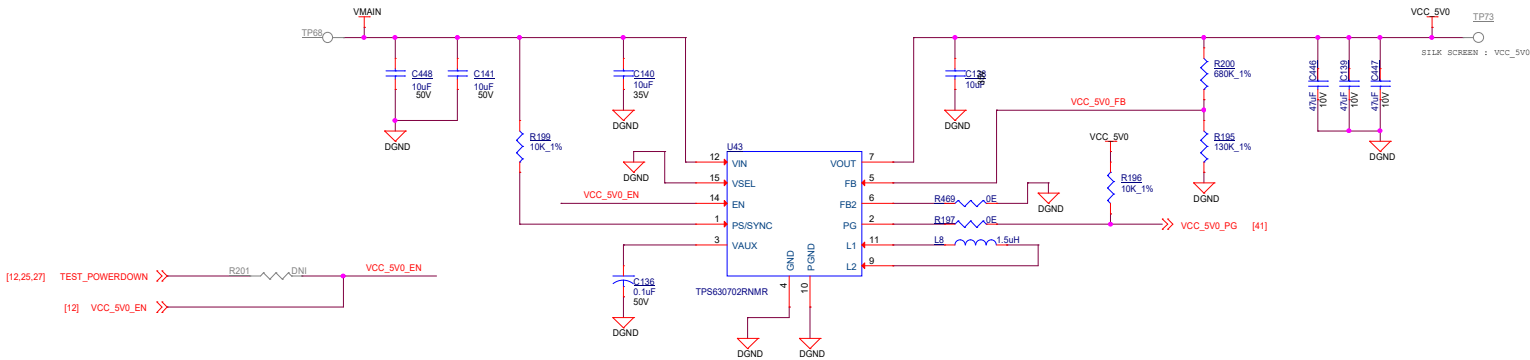
USB TYPE-C PD CONTROLLER AND POWER SUPPLY



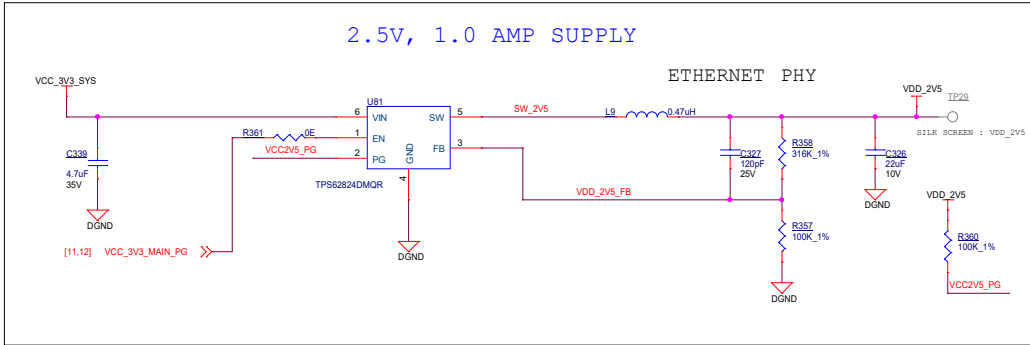
PERIPHERAL POWER SUPPLIES - 1

VinMin = 4.5V
VinMax = 15V
Vout = 5V @ 2A

D-Note :-
Add a Jumper or OR for isolation
or Current measurement for
preproduction board

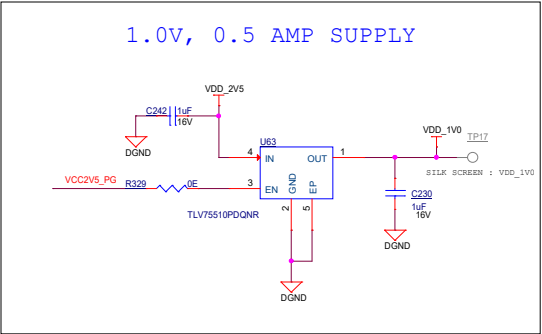


2.5V, 1.0 AMP SUPPLY

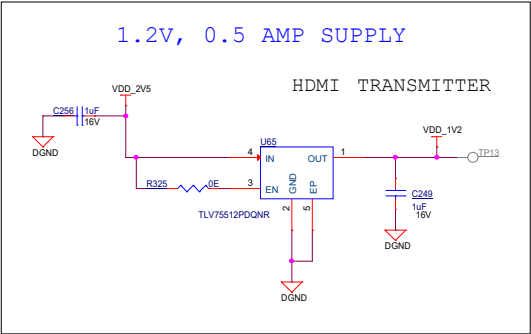


PERIPHERAL SUPPLY - ETHERNET PHY

1.0V, 0.5 AMP SUPPLY



1.2V, 0.5 AMP SUPPLY



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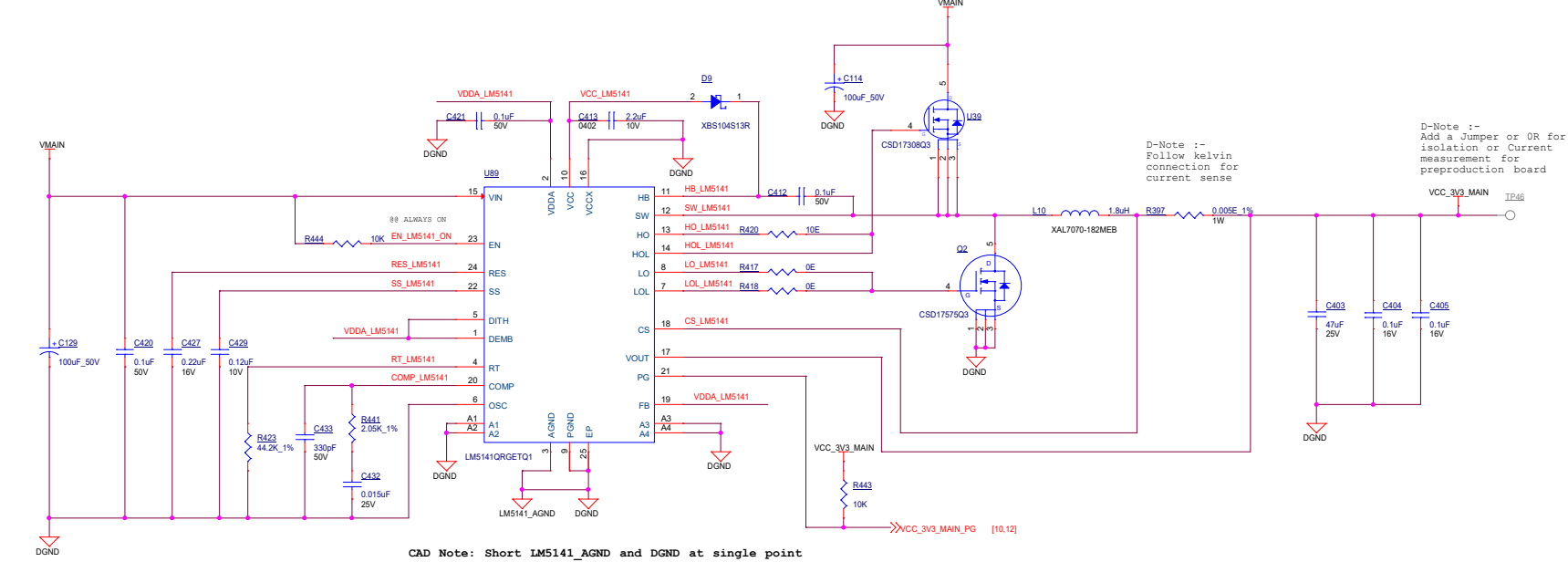


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PERIPHERAL POWER SUPPLIES - 2

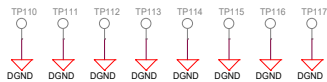
3.3V, 10.0 AMPS SUPPLY

VinMin = 4.5V
VinMax = 15V
Vout = 3.3V @ 10A



[33] ETH_CAN_INH_PREREG >> DNR R81 EN_LM5141_ON

GND TEST POINTS



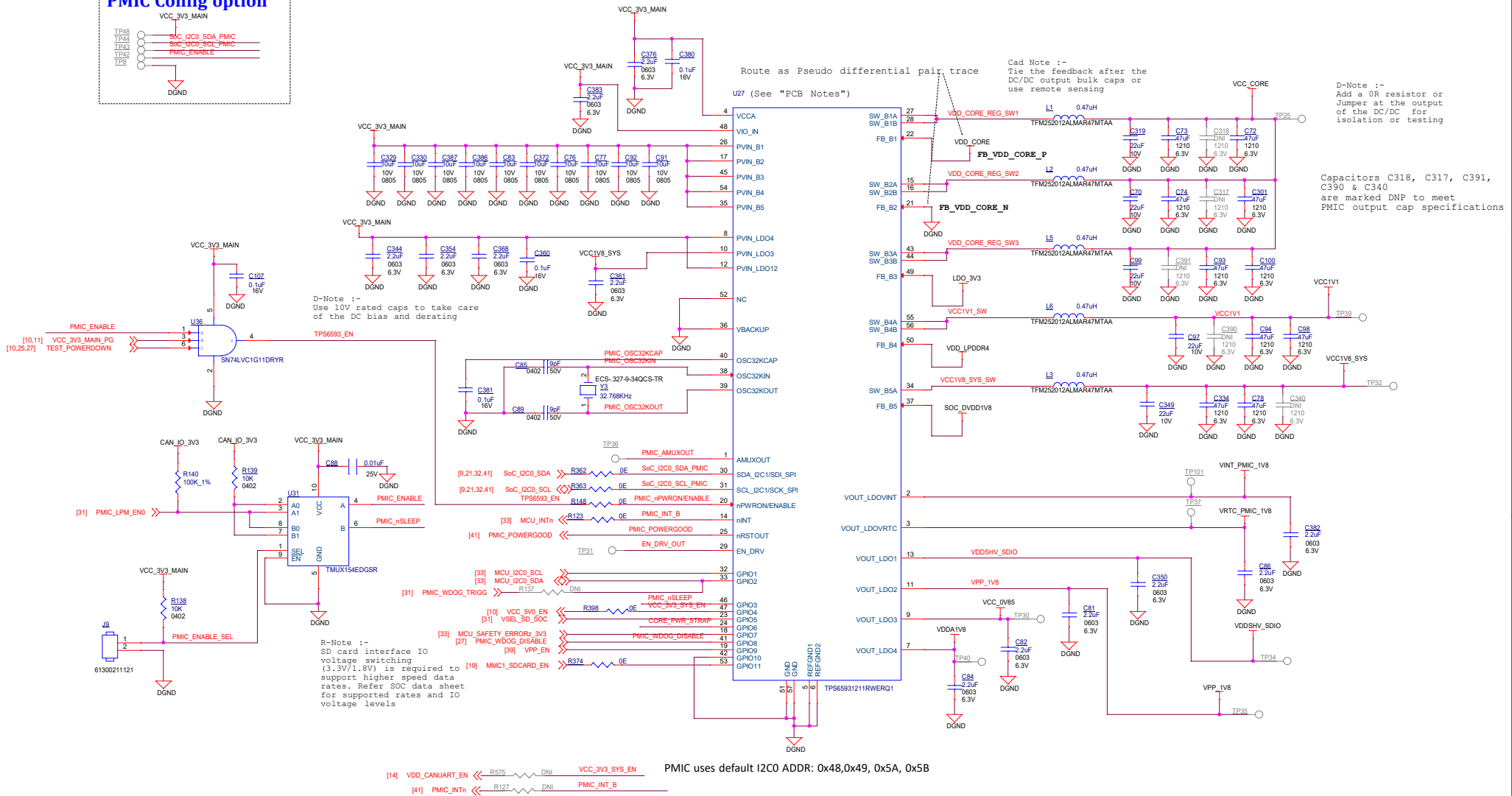
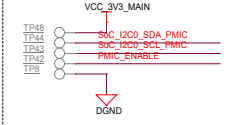
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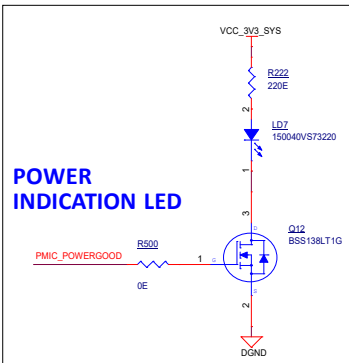
Title PERIPHERAL POWER SUPPLY-2		
Size	PROC135A1	Rev A1
C		
Date: Thursday, July 24, 2025	Sheet 11 of 44	

SOC POWER SUPPLY PMIC

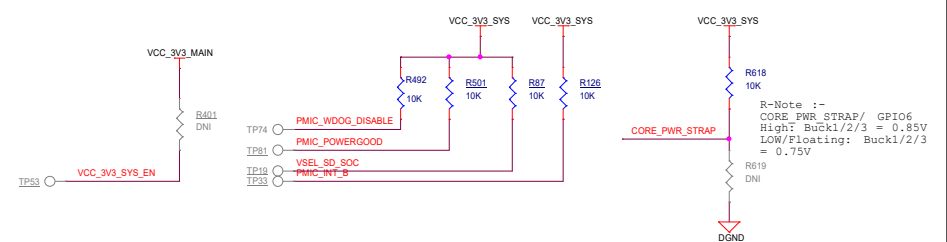
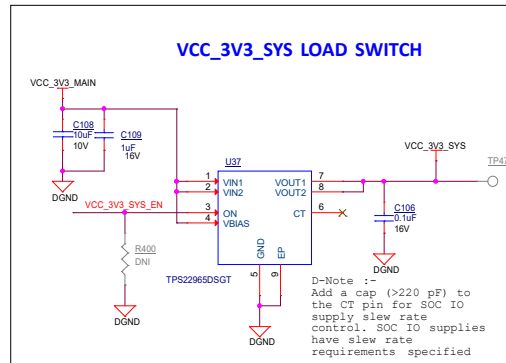
PMIC Config option



**POWER
INDICATION LED**



VCC_3V3_SYS LOAD SWITCH



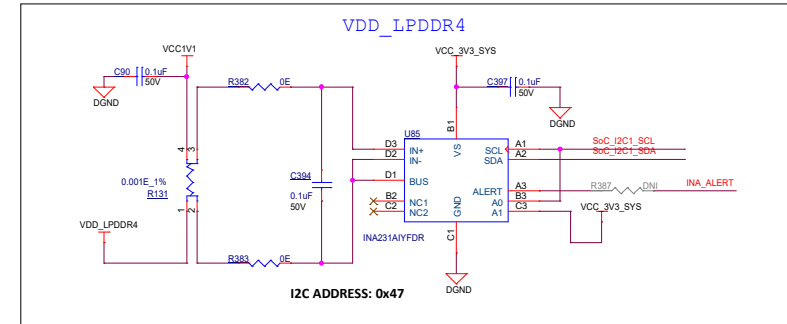
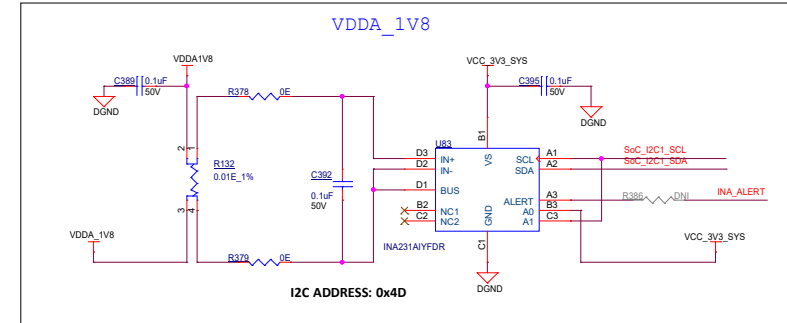
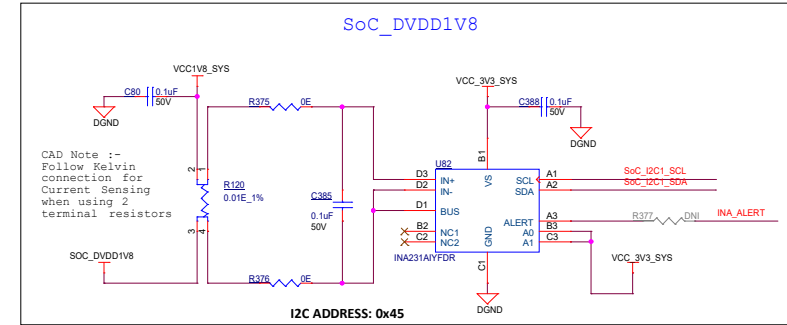
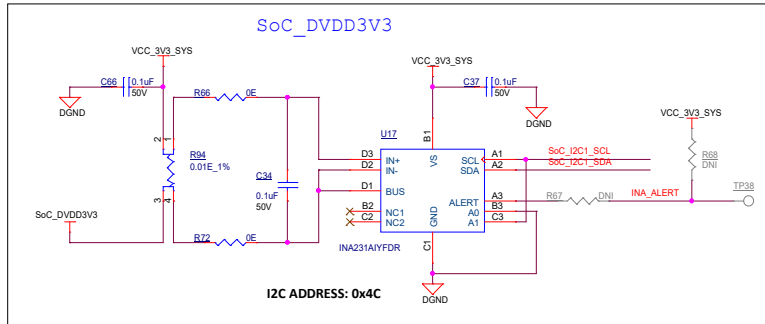
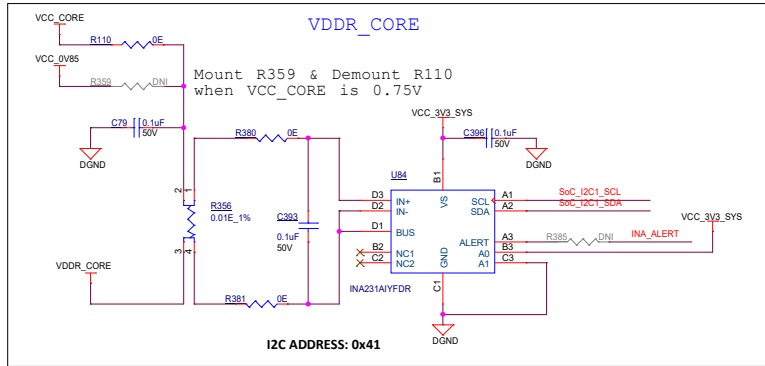
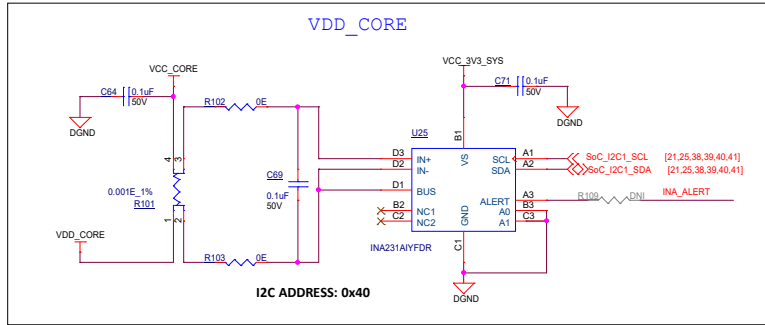
Designed for TI by Mistral Solutions Pvt Ltd



Title		SOC POWER SUPPLY PMIC	
Size	PROC135A1		Rev
C			A1
Date:	Thursday, July 24, 2025	Sheet	12 of 44

CURRENT MONITORING DEVICES

D-Note :-
Note the supply rail name change across
the shunt when optimizing the design
(Deleting the current sense resistor)



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_OV85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

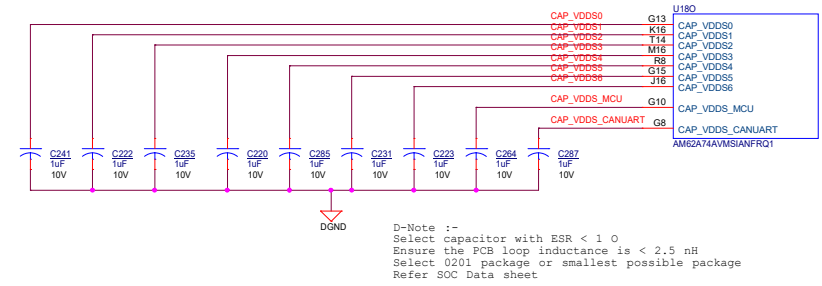
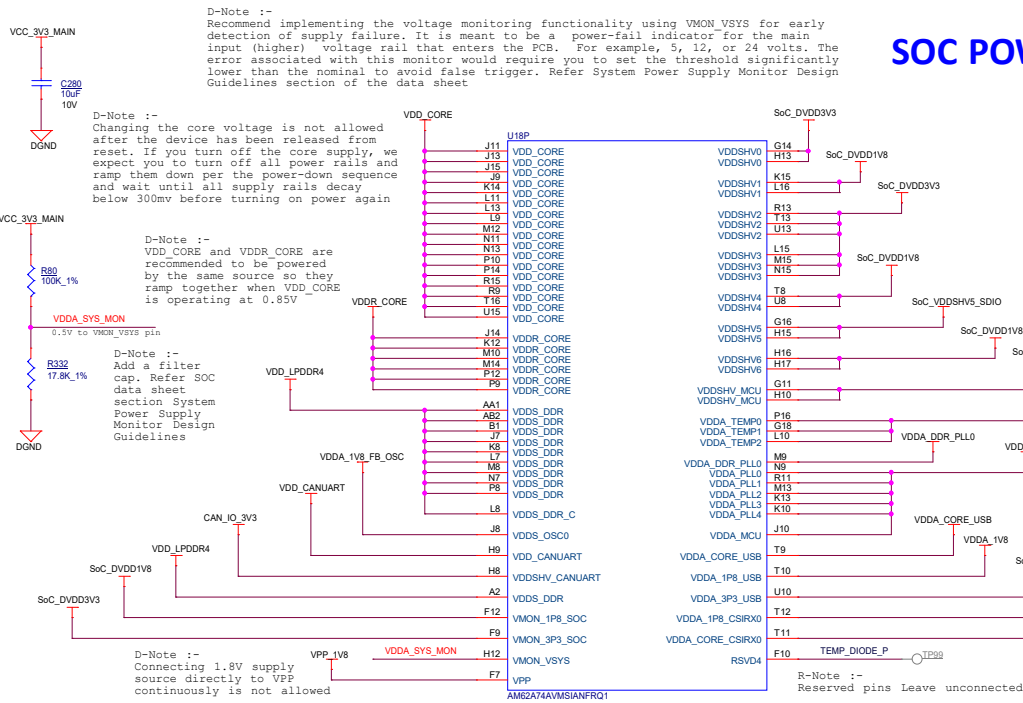
Designed for TI by Mistral Solutions Pvt Ltd



Title CURRENT MONITORING DEVICES

Size	PROC135A1	Rev
C		A1
Date:	Thursday, July 24, 2025	Sheet 13 of 44

SOC POWER



D-Note :-

Common SOC LVCMOS IO interface guidelines

1. Most of the SOC IOs are not fail-safe. No input should be applied before supply ramps.
2. SOC LVCMOS inputs have minimum slew rate requirements specified
3. SOC IO buffers are off during Reset. A pull is required near to the attached device being driven by the SOC IOs
4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull. When adding pull is not feasible, ensure the traces are routed away from noisy signals

D-Note :-
A Trace connected to SOC is effectively an antenna that will pick up noise. A potential will be generated on the signal when noise couples into the antenna. This potential will be largest on the highest impedance end of the signal. By placing a pull-up or pull-down near the SOC pin, we force the highest potential to the open-circuit end of the signal rather than the SOC end of the signal.

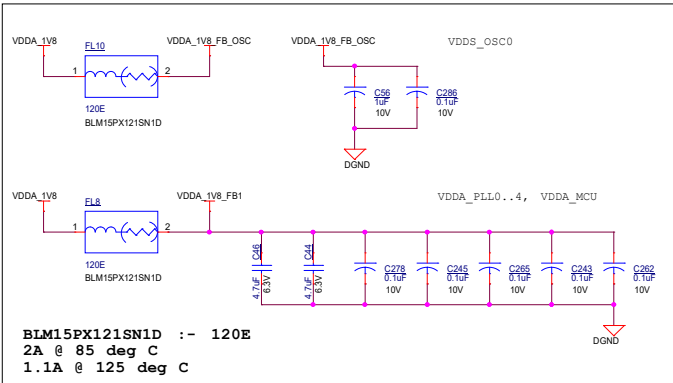
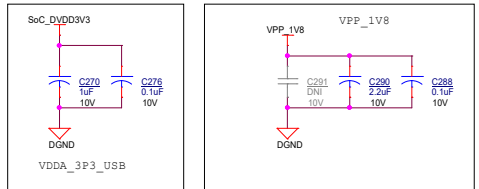
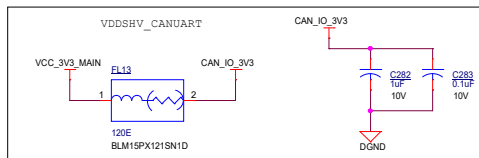
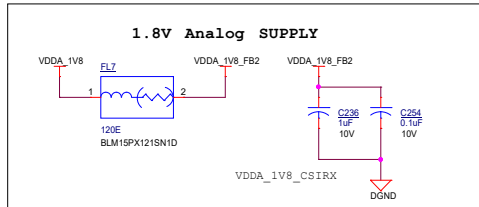
D-Note :-
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized and the USB configuration procedure does not happen. Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

R-Note :-
Reserved pins Leave unconnected

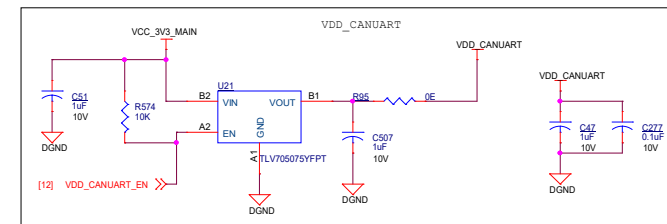
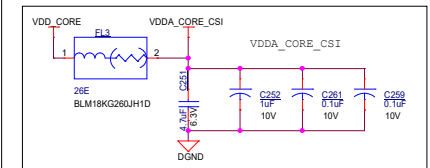
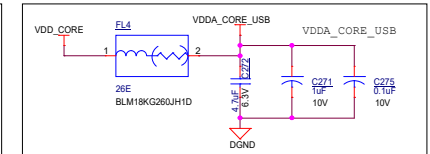
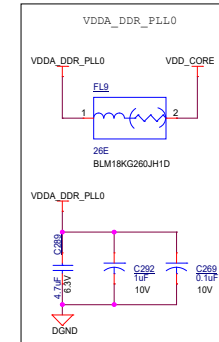
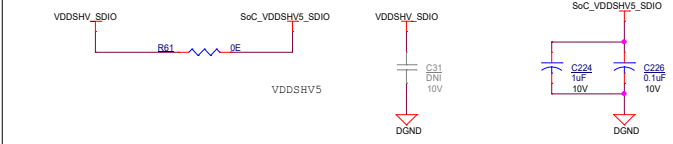
D-Note :-
Refer Pin connectivity requirements to connect the CSIO supplies (analog and core) when CSIO interface is not used
Ferrite and Bulk Caps are optional when CSIO is not used and
Boundary scan functionality is required

D-Note :-
It is very important to select an LDO with very fast transient response and connect its output to the VPP pin with a low loop inductance path to ensure it is able to source the high transient load, where the VPP pin never drops below the minimum operating voltage.

CORE SUPPLY



3.3V/1.8V MMC1 SUPPLY

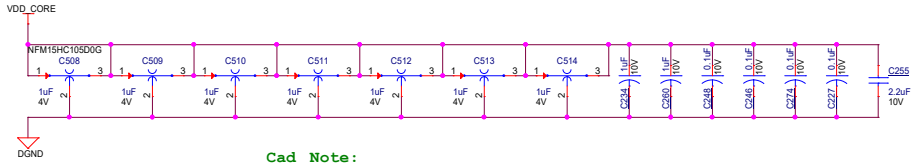


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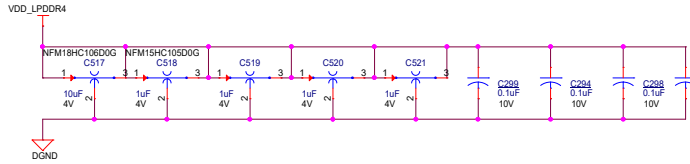


Title		SOC POWER	
Size			Rev
C	PROC135A1		A1
Date:	Thursday, July 24, 2025	Sheet	14 of 44

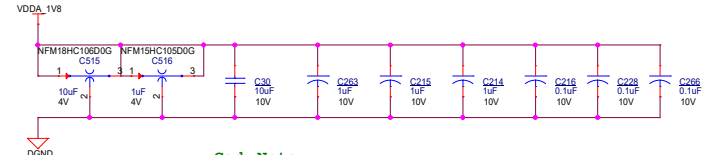
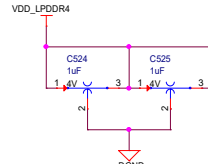
SOC POWER SUPPLIES - DECAPS



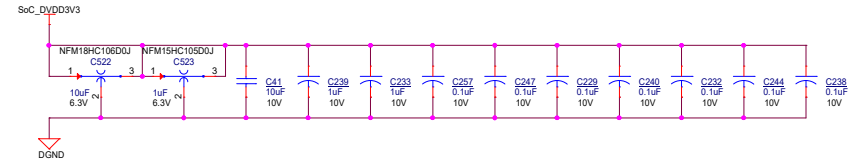
Cad Note:
Place 0.1 uF caps near to SoC pins



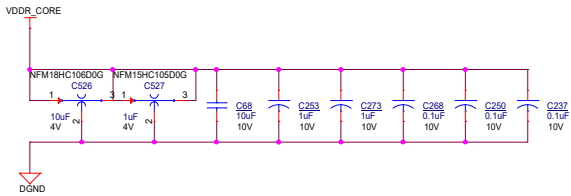
Cad Note:
Place 0.1 uF caps near to SoC pins



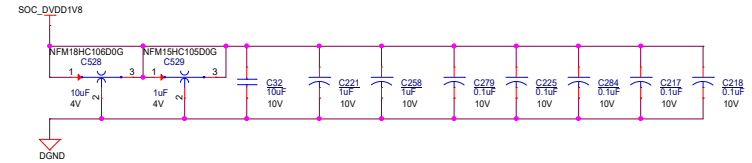
Cad Note:
Place 0.1 uF caps near to SoC pins



Cad Note:
Place 0.1 uF caps near to SoC pins

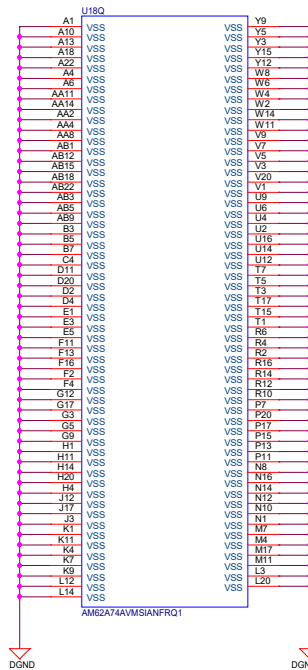


Cad Note:
Place 0.1 uF caps near to SoC pins



Cad Note:
Place 0.1 uF caps near to SoC pins

SOC VSS



R-Note :-
Use of 3 terminal caps optimizes
use of bulk caps and minimizes the
PCB inductance



U18G			
LPDDR4_CA0	J5	DOR0_DQ0	D1 LPDDR4_DQ0
LPDDR4_CA1	J6	DOR0_DQ1	D1 LPDDR4_DQ0#N
LPDDR4_CA2	J4	DOR0_A0	
LPDDR4_CA3	J4	DOR0_A1	DOR0_DQ8_N
LPDDR4_CA4	J4	DOR0_A2	
LPDDR4_CA5	K5	DOR0_A4	
	K5	DOR0_A5	DOR0_DQ0
	X J2	DOR0_A6	DQ1 DQ1
	X L6	DOR0_A7	DQ2 DQ2
	L2	DOR0_A8	DQ3 DQ3
	X K2	DOR0_A9	DQ4 DQ4
	X L5	DOR0_A10	DQ5 DQ5
	M5	DOR0_A11	DQ6 DQ6
	X M2	DOR0_A12	DQ7 DQ7
	K5	DOR0_A13	
	H3	DOR0_BA0	
	X K6	DOR0_BA1	
	P4	DOR0_BC0	
	X R7	DOR0_BC1	
	K3	DOR0_BG0	
LPDDR4_DMIO	C2	DOR0_DM0	
LPDDR4_DMIO	F3	DOR0_DM1	
LPDDR4_DMIO	UT	DOR0_DM2	
LPDDR4_DMIO	W3	DOR0_DM3	
LPDDR4_CK_P	M1	DOR0_DQ8	DOR0_DQ8
LPDDR4_CK_N	L1	DOR0_CK0	DOR0_DQ9
LPDDR4_CK0	P3	DOR0_CK1	DOR0_DQ10
LPDDR4_CK1	P5	DOR0_CK2	DOR0_DQ11
	X F6	RSVD3	DOR0_DQ12
	X G7	RSVD5	DOR0_DQ13
	X H5	DOR0_ODT0	DOR0_DQ14
	X H3	DOR0_ODT1	DOR0_DQ15
LPDDR4_CS0_A	J6	DOR0_CS0	
LPDDR4_CS1_A	N4	DOR0_CS1_N	
LPDDR4_RESET_N	P6	DOR0_RESET_N	
	X H7	DOR0_ALERT_N	
	X N2	DOR0_PAR	
IOE 1% LPDDR4_CA0	H6	DOR0_CA0	
	X N5	DOR0_ACT_N	
LPDDR4_CS0_B	M6	DOR0_RAS_N	
LPDDR4_CS1_B	M5	DOR0_CAS_N	
	X N6	DOR0_WE_N	
AM22A74AMVSIANFRQ1			

VDDQ_LPDDR4_1V1

VDDQ_LPDDR4

VDD2_LPDDR4_1V1

VDD2_LPDDR4

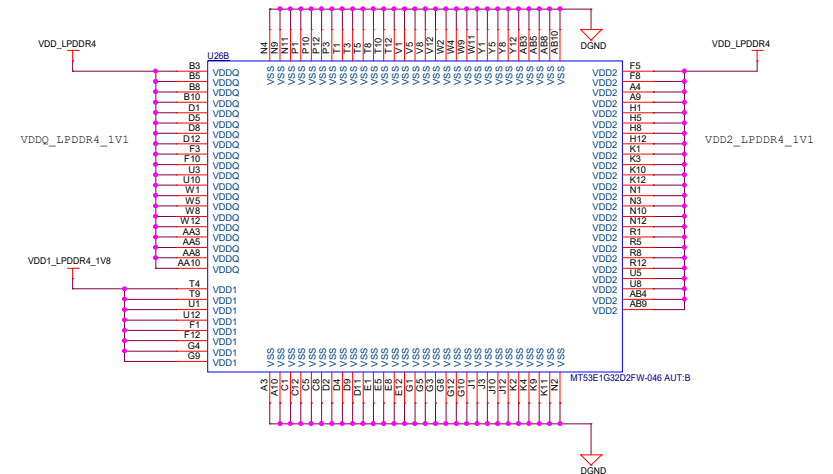
VDD1_LPDDR4_1V8

VDD1_LPDDR4

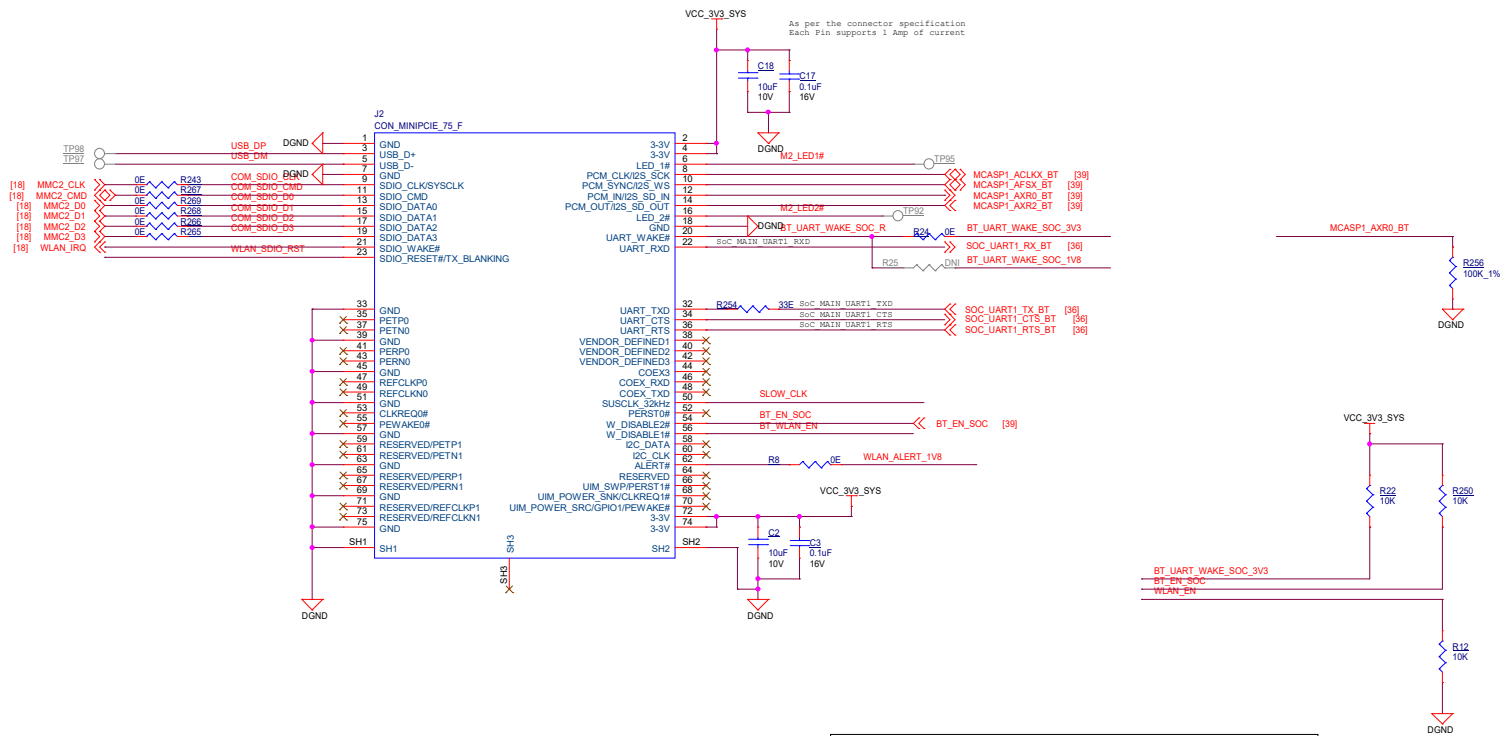
SOC_DVDD1V8

FL12

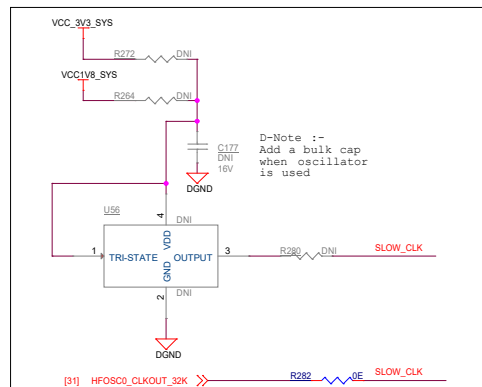
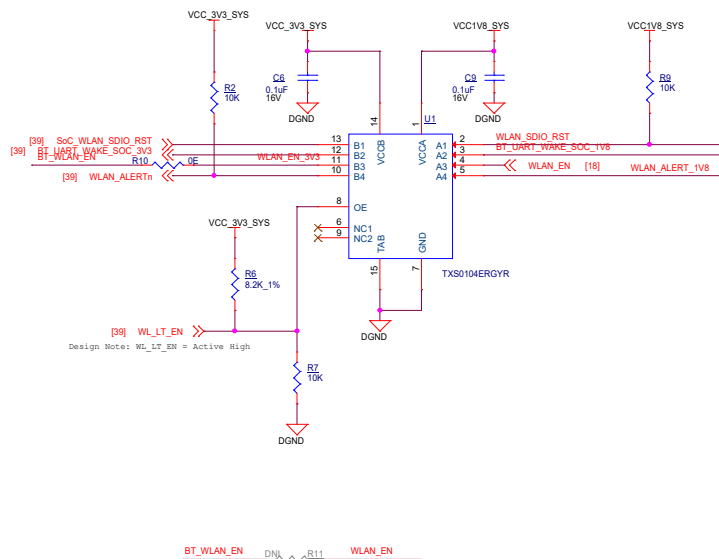
120E



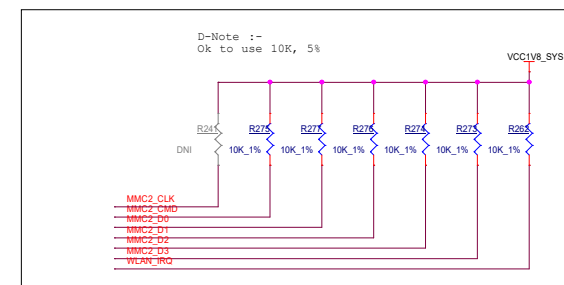
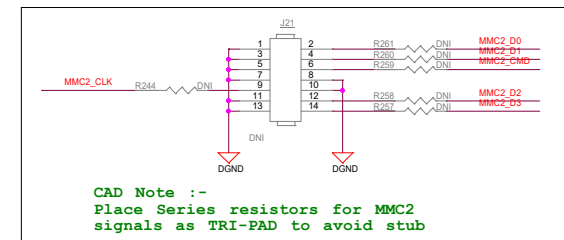
M.2 INTERFACE - SDIO



M.2 LEVEL TRANSLATOR



Cad Note :-
Place R1 & R2 close to each other to avoid stub.



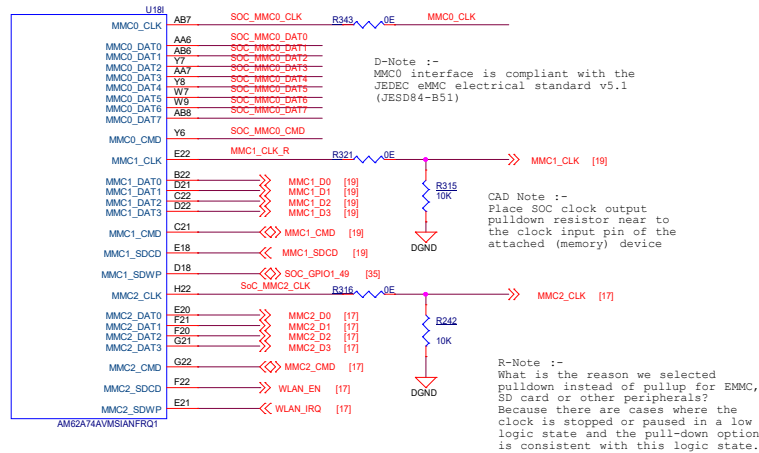
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Title		M.2 CONNECTOR I/F	
Size	PROC135A1	Rev	
C		A1	
Date:	Thursday, July 24, 2025	Sheet	17 of 44

D-Note :-
This family of processor implements a soft PHY for eMMC interface. The pulls required for D0, Clock and other eMMC interface control signals are recommended to be implemented externally.

D-Note :-
OE provision on MMC0_CLK
helps improve signal integrity



D-Note :-
The GPIO reset option makes it possible for software to reset the attached device (eMMC or OSPI or SD card or OLDIO or EPHY) without resetting the entire processor if there is a case where the peripheral becomes unresponsive.

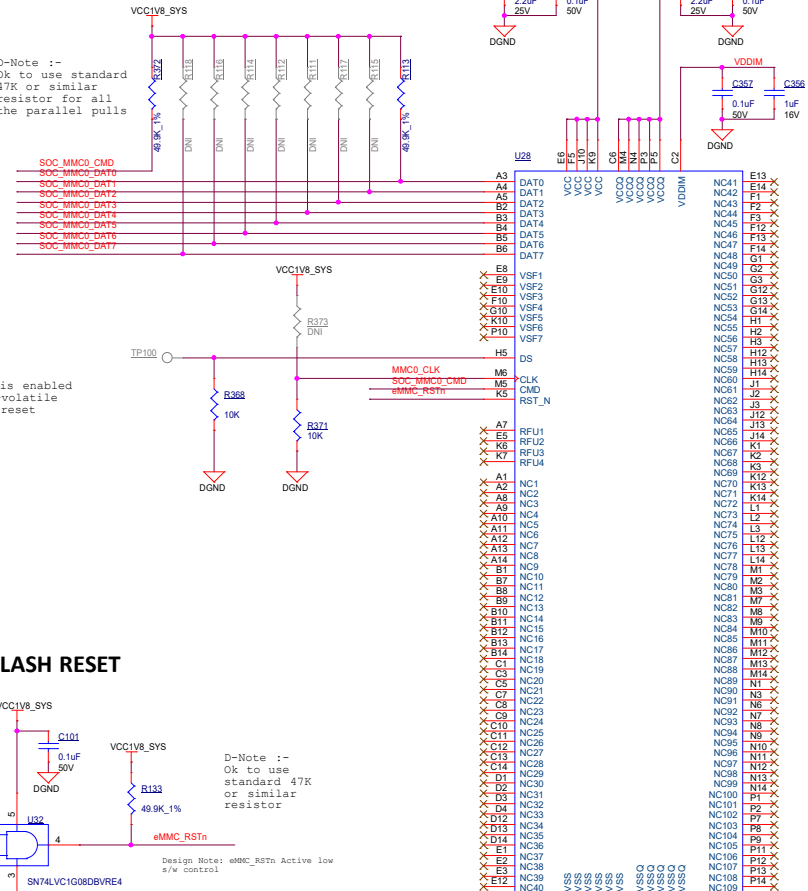
D-Note :-
Ensure eMMC_RSTn Reset input is enabled in the eMMC device (eMMC non-volatile configuration space) for the reset logic to be functional

eMMC FLASH

D-Note :-
Add additional decaps as required
Refer SK-AM62P-LP schematics

D-Note :-
For D7..D1 eMMC device is expected to have the pullups enabled by default. The eMMC host/phy disables the eMMC device pullups and enables SOC internal pullups. Provision for external pullups is optional or the pullups can be deleted

D-Note :-
Ok to use standard
47K or similar
resistor for all
the parallel pulls



D-Note :-
Ok to use
standard
or simila
resistor

```
D-Note :-
Add a ser
input for
SK-AM62P-
```

-Note :-
In case ANDING logic is not used and the processor Main Domain warm reset status output (RSETSTzTzTz) is used to reset the attached device, ensure the 10 voltage level of the attached device matches the RSETSTzTzTz 10 voltage level. A level translator is recommended to match the 10 voltage level. A resistor divider could be used alternatively, provided optimum impedance value of the resistor divider is selected. If too high the rise/fall time of the eMMC reset input could be affected. If the impedance is too low it will cause the AM65x to source too much steady-state current during normal operation.

D-Note :-
ANDing logic additionally performs level translation
Verify the Reset IO level compatibility before
optimizing the reset ANDing logic. IO level mismatch
could cause supply leakage and affect SOC operation

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Title		eMMC FLASH INTERFACE	
Size	PROC135A1		Rev
C			A1
Date:	Thursday, July 24, 2025	Sheet	18 of 44

SD CARD INTERFACE

D-Note :-
This power switch, along with the reset logic, and the host IO power supply circuit is required to support UHS-I SD Cards which begins communications using 3.3V signal levels and later change to 1.8V signal levels when changing to one of the faster data transfer speeds. Cycling power to the SD Card is the only way to put it back into 3.3V mode since SD Cards do not have a reset pin. The host IO power supply must power off/on and change voltage at the same time as the SD Card. These circuits and the software driver operating the signals sourcing these circuits ensure both devices are off, or on and operating at the same IO voltage at the same time.

LOAD SWITCH

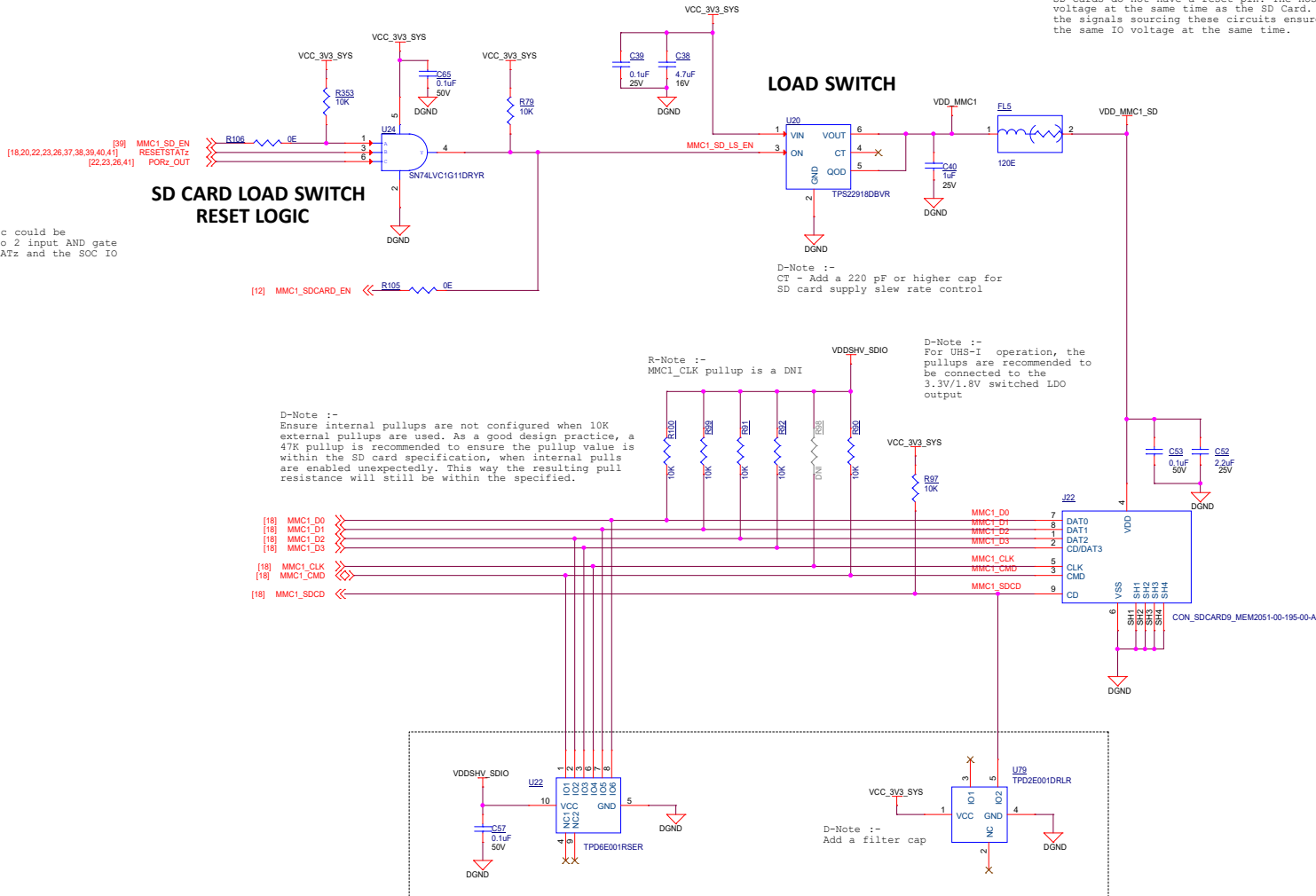
D-Note :-
CT - Add a 220 pF or higher cap for SD card supply slew rate control

R-Note :-
MMC1_CLK pullup is a DNI

D-Note :-
For UHS-I operation, the pullups are recommended to be connected to the 3.3V/1.8V switched LDO output

D-Note :-
Ensure internal pullups are not configured when 10K external pullups are used. As a good design practice, a 47K pullup is recommended to ensure the pullup value is within the SD card specification, when internal pulls are enabled unexpectedly. This way the resulting pull resistance will still be within the specified.

CAD Note :-
Place near SD Card Connector



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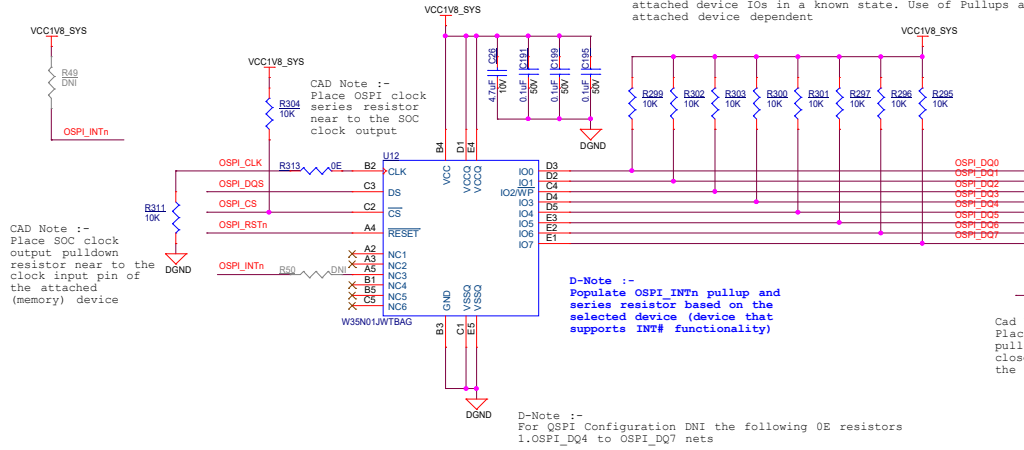
Title		SD CARD INTERFACE	
Size	PROC135A1	Rev	
C		A1	
Date:	Thursday, July 24, 2025	Sheet	19 of 44

OSPI FLASH

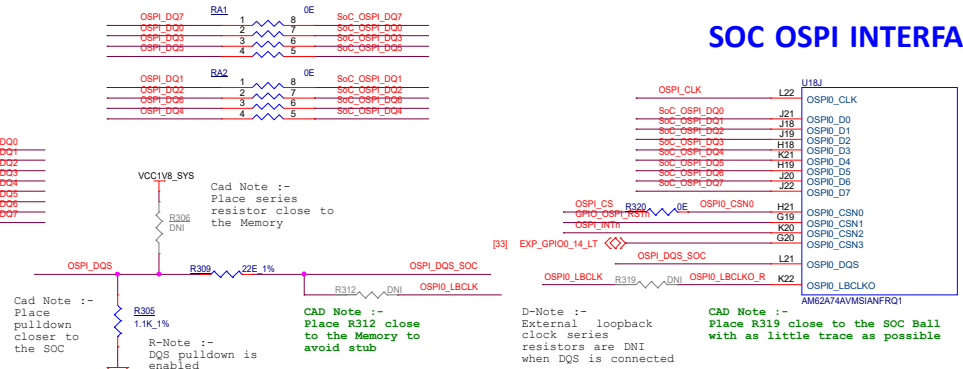
R-Note :-
SOC IO buffers are off during power-up. A pullup is recommended near to the attached device, to hold the attached device IOs in a known state. Use of Pullups are attached device dependent

R-Note :-
These 0.0 resistors are used for configuring QSPI and OSPI. This is optional during custom board design

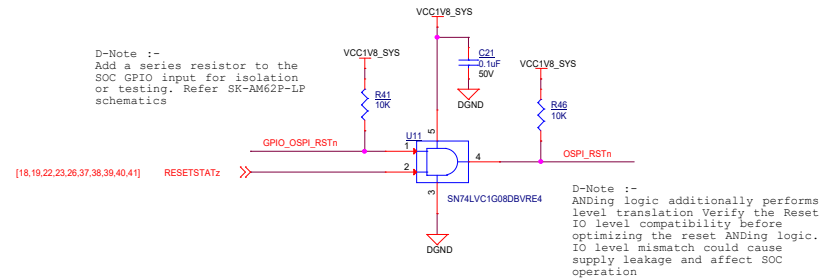
D-Note :-
Connecting OSPI interface to multiple devices is not recommended or supported



SOC OSPI INTERFACE



OSPI FLASH RESET



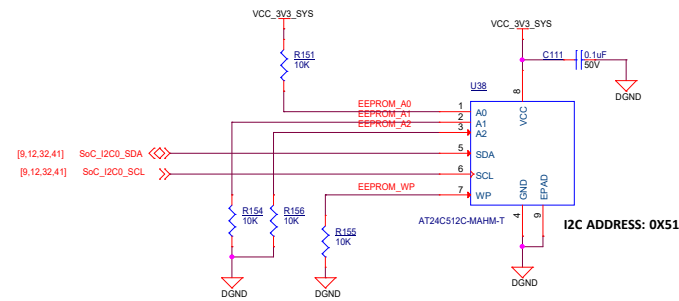
Designed for TI by Mistral Solutions Pvt Ltd



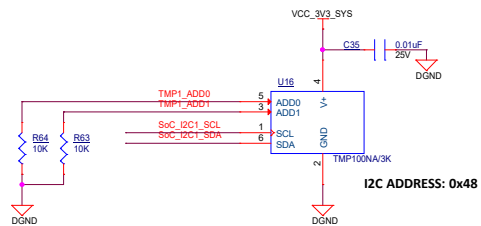
Title OSPI INTERFACE

Size	PROC135A1	Rev
C		A1
Date:	Thursday, July 24, 2025	Sheet 20 of 44

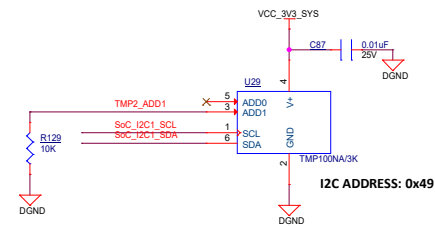
BOARD ID EEPROM



DIGITAL TEMPERATURE SENSORS



CAD NOTE: PLACE TEMP SENSOR CLOSE TO SoC



CAD NOTE: PLACE TEMP SENSOR CLOSE TO LPDDR4

[13,25,38,39,40,41] SoC_I2C1_SCL >> TP49
[13,25,38,39,40,41] SoC_I2C1_SDA >> TP50
Silk: SOC_I2C1

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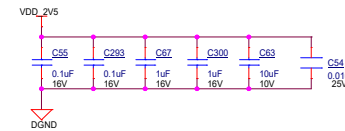
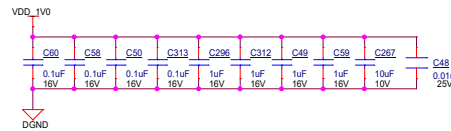
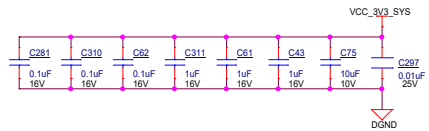
Title BOARD ID EEPROM & TEMPERATURE SENSORS

Size	PROC135A1	Rev
C		A1
Date:	Thursday, July 24, 2025	Sheet 21 of 44

D-Note :-
The caps and values used are as per
the EPHY data sheet recommendations.

CPSW3G RGMII 1 - ETHERNET PHY

D-Note :-
Refer to DP83867ERG2-R-EVM when using LAN
Discrete Transformer Module and RJ45 connector



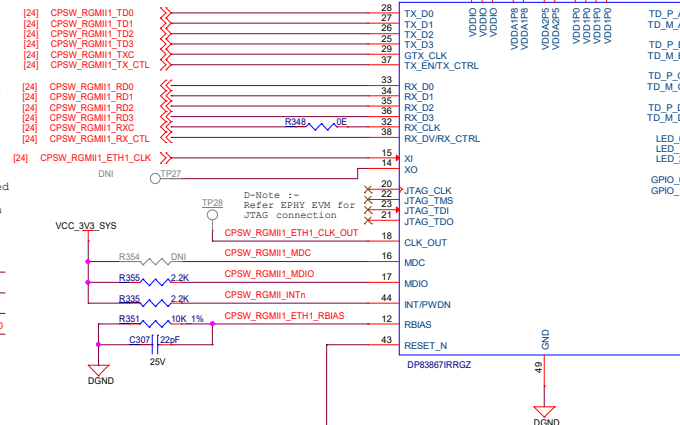
D-Note :-
Verify the power sequence
requirements for Two-Supply
Configuration and Three-Supply
Configuration

R-Note :-
Ferrite is DNI

RJ45 CONNECTOR WITH INTEGRATED MAGNETICS

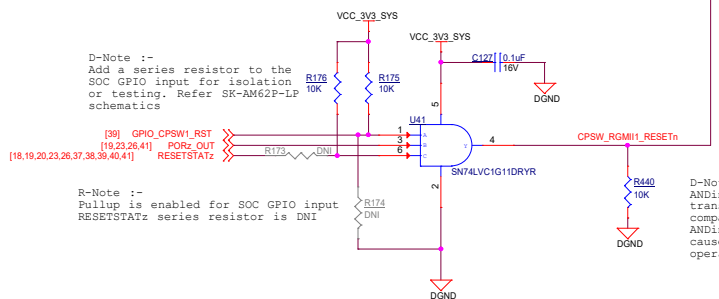
D-Note :-
Provide provision for series
resistor based on EPHY for
RX signals near to EPHY

D-Note :-
XI clock Input amplitude allowed
is 1.8V irrespective of the IO
supply. Use a CAP DIVIDER when
the clock amplified is 3.3V



D-Note :-
ANDing logic could be
optimized to 2 input AND
gate Use RESETSTATz (or
PORz OUT) and the SOC IO
as inputs

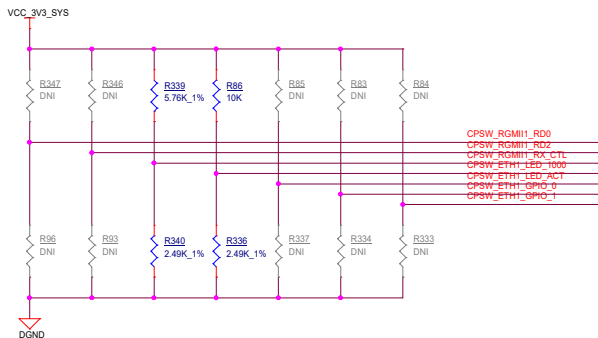
D-Note :-
Add a series resistor to the
SOC GPIO input for isolation
or testing. Refer SK-AM62P-LP
schematics



R-Note :-
Pullup is enabled for SOC GPIO input
RESETSTATz series resistor is DNI

D-Note :-
ANDing logic additionally performs level
translation Verify the Reset IO level
compatibility before optimizing the reset
ANDing logic. IO level mismatch could
cause supply leakage and affect SOC
operation

CON_RM45-14_LPJG16314MNL
Silk: RGMII-1



PHY ADDRESS = 000000
Auto-Negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

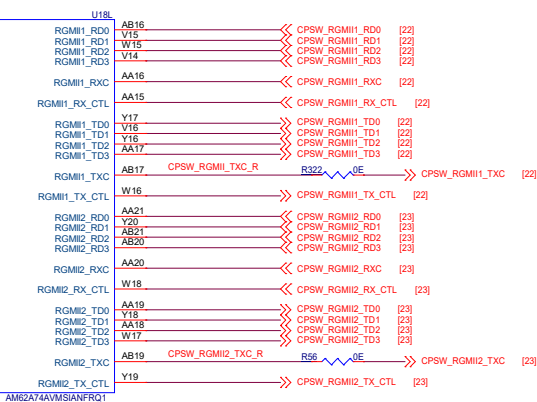
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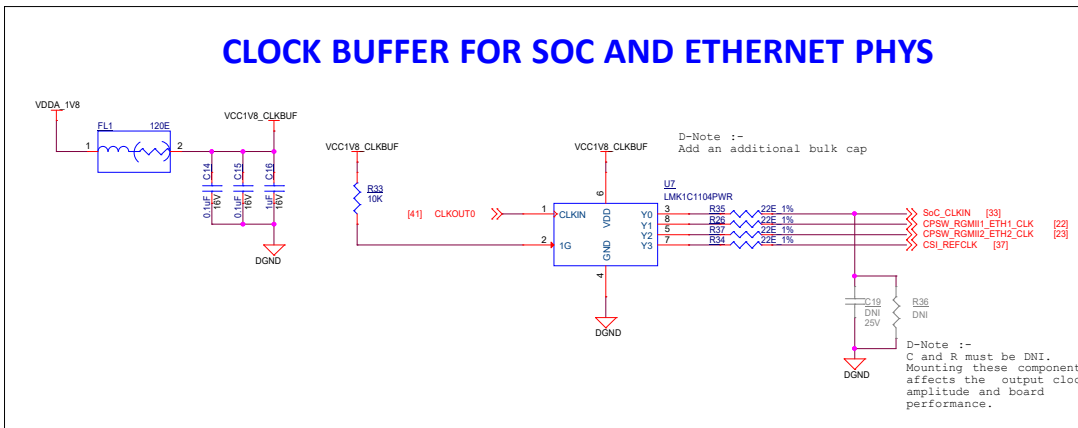
Title		CPSW RGMII 1 ETHERNET PHY	
Size	PROC135A1	Rev	A1
C		Date	Thursday, July 24, 2025
Sheet	22	of	44

Size	PROC135A1	Rev
C		A1
Date:	Thursday, July 24, 2025	Sheet 23 of 44

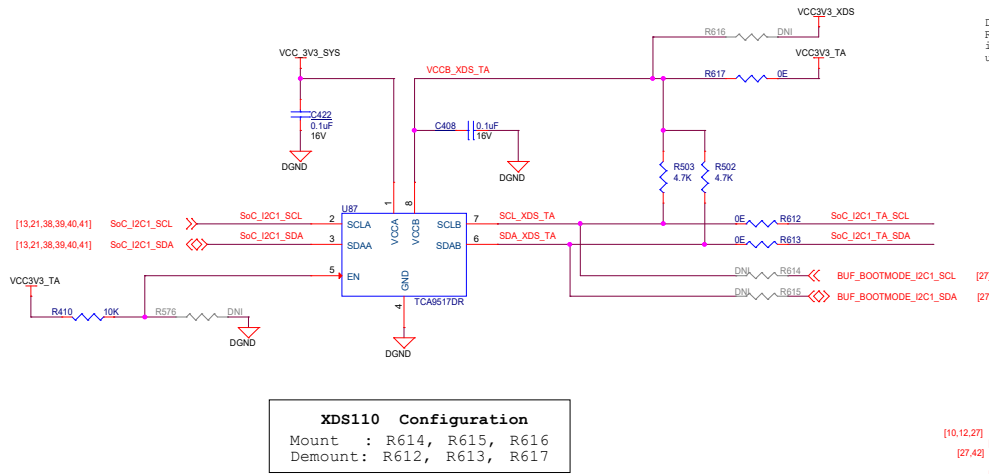
SOC MAC INTERFACE



D-Note :-
Add series resistors 22 0 on the
Ethernet interface TX (TDx)
signals near to the SOC

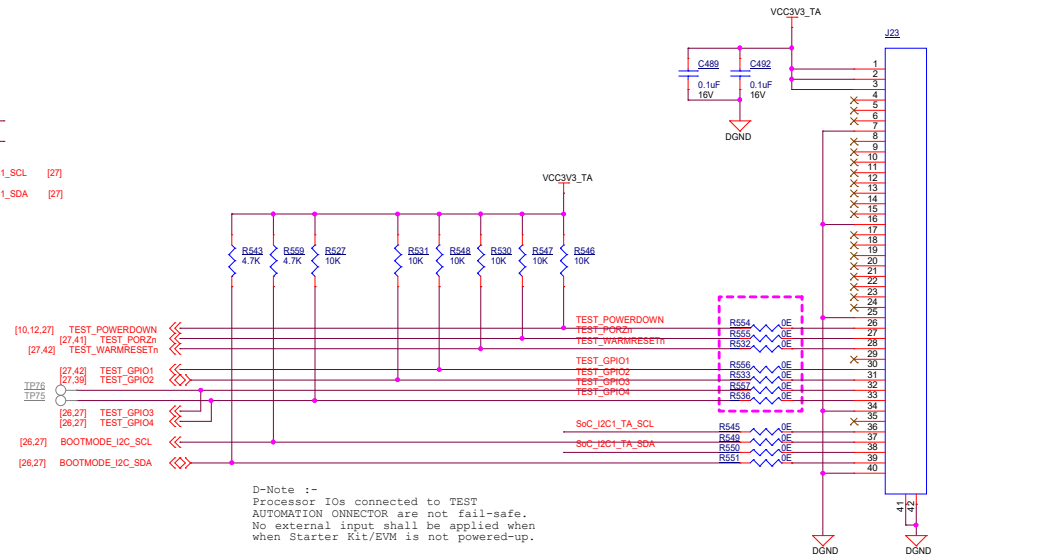


I2C BUS BUFFER



D-Note :-
Refer SK-AM62P-LP
implementation for the latest
updates

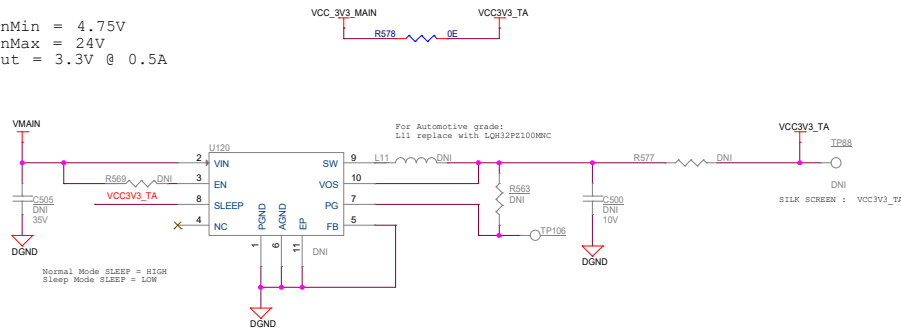
40-PIN TEST AUTOMATION HEADER



CON_FLEX_40X1_FH12A-40S-0.5SH
Silk: AUTOMATION HDR

TEST AUTOMATION BOARD POWER

VinMin = 4.75V
VinMax = 24V
Vout = 3.3V @ 0.5A



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SOC_GPIO1_23 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

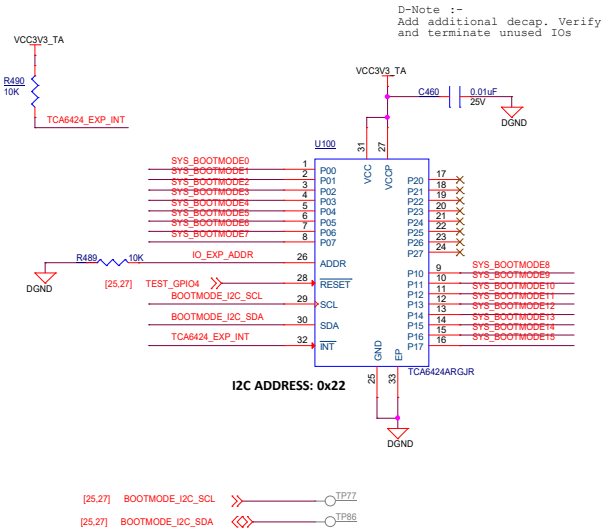
Designed for TI by Mistral Solutions Pvt Ltd



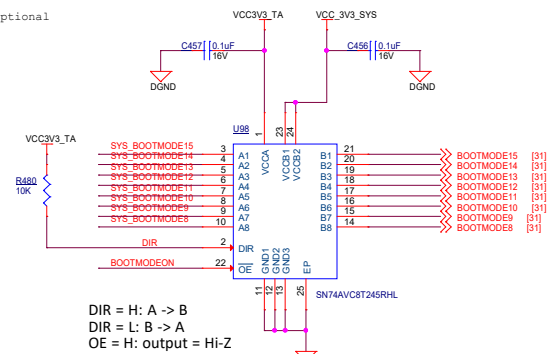
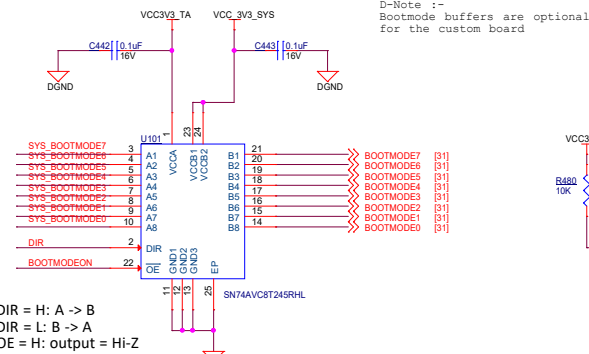
Title TEST AUTOMATION

Size	PROC135A1	Rev
C		A1
Date:	Thursday, July 24, 2025	Sheet 25 of 44

BOOTMODE IO EXPANDER

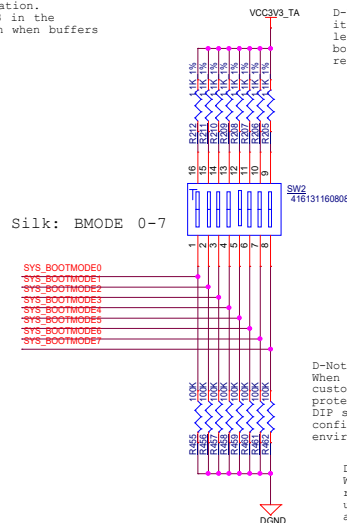


BOOT MODE BUFFERS

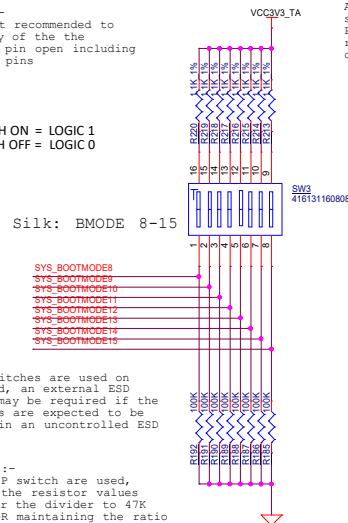


BOOTMODE CONFIGURATION RESISTORS AND BOOTMODE SWITCHES

D-Note :-
VCC3V3_XDS_Ta supply is used to support test automation.
Connect SOC DVDD3V3 in the custom board design when buffers are not used



D-Note :-
When dip switches are used on custom board, an external ESD protection may be required if the DIP switches are expected to be configured in an uncontrolled ESD environment



D-Note :-
Dip switch is optional and used on the SK for ease of configuration
A pullup or pulldown resistor can be used to set the BOOTMODE configuration
Provide provision for Pullup and Pulldown resistors for the bootmode pins that have configuration capability

BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. ETHERNET
6. USB0 Dfu
7. USB0 MS

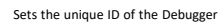
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Title BOOT MODE BUFFER & SWITCHES

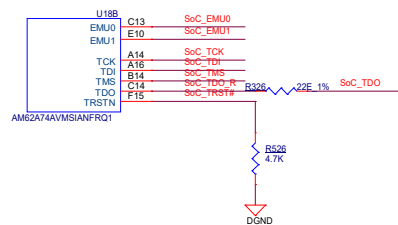
Size	PROC135A1	Rev
C		A1
Date:	Thursday, July 24, 2025	Sheet 26 of 44

D-Note :-
Please follow SK-AM62P-LP
implementations for latest
updates on XDS110

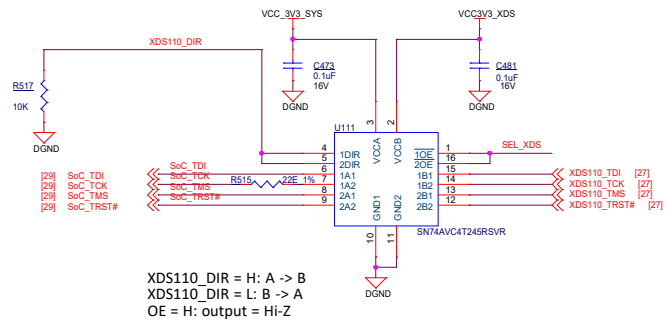
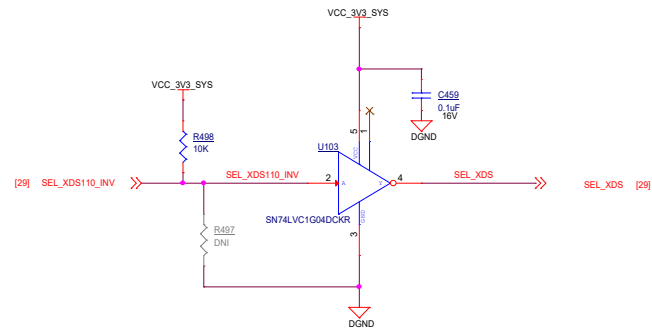


Title				XDS110 DEBUGGER			
Size		PROC135A1				Rev	
C						A1	
Date:			Thursday, July 24, 2025		Sheet 27 of 44		

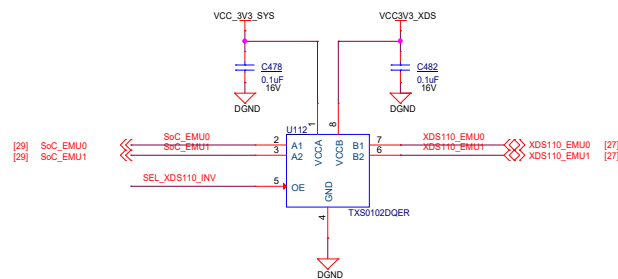
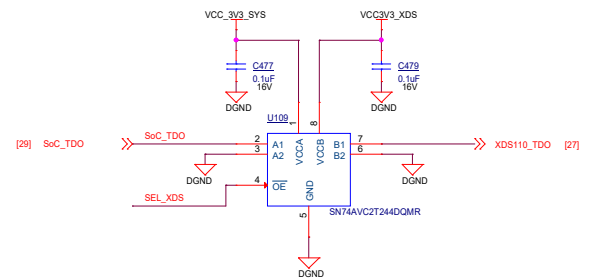
SOC JTAG INTERFACE



BUFFER XDS110



XDS110_DIR = H: A -> B
XDS110_DIR = L: B -> A
OE = H: output = Hi-Z



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Title JTAG BUFFER

Size PROC135A1

C

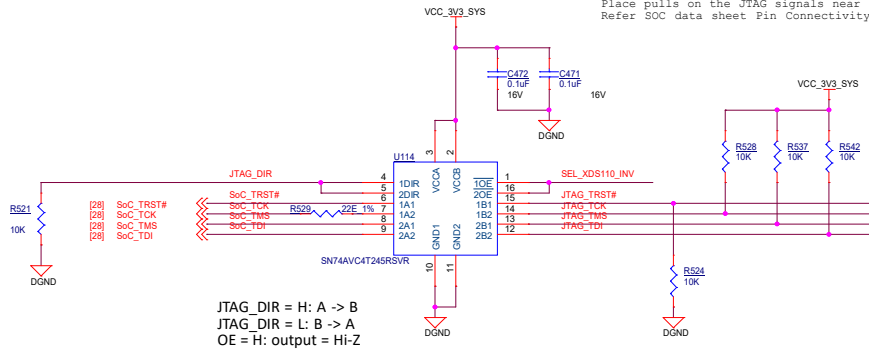
Date: Thursday, July 24, 2025

Rev A1

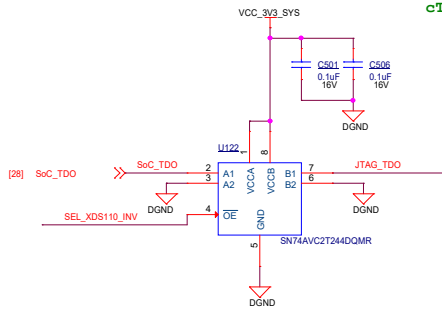
Sheet 28 of 44

cTI20 JTAG BUFFERS

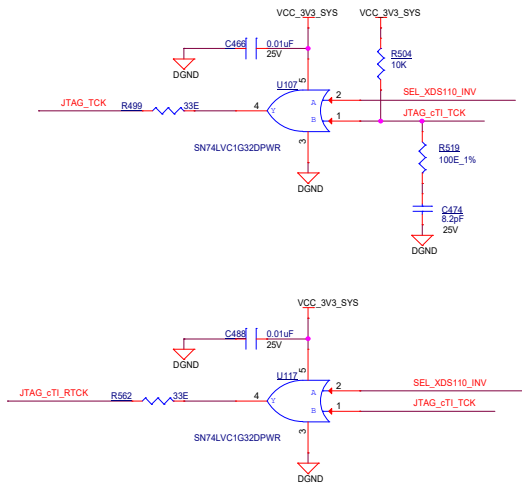
D-Note :-
Place pulls on the JTAG signals near to the SOC
Refer SOC data sheet Pin Connectivity Requirements section



CAD NOTE: Buffers U114 and U122 need to be placed closer to the cTI-20pin connector J19 to reduce Stub length of the JTAG signals.

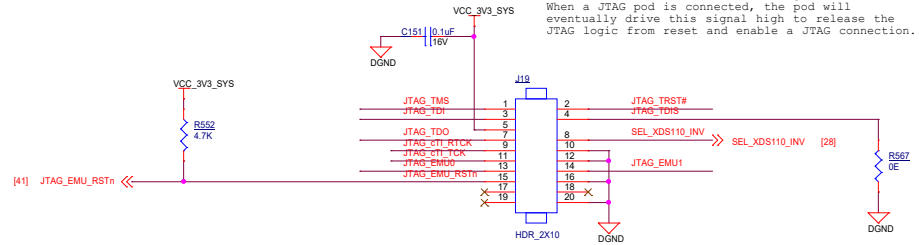


JTAG CLOCK BUFFER

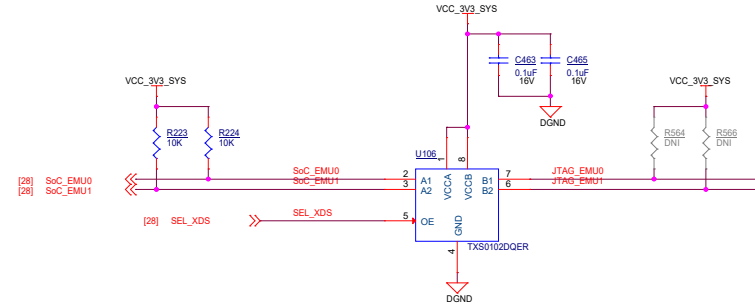


JTAG 20 PIN cTI CONNECTOR

D-Note :-
TRSTn is the reset to the JTAG logic. For normal operation, this is pulled low, and thus the JTAG remains in reset as it is not being used. When a JTAG pod is connected, the pod will eventually drive this signal high to release the JTAG logic from reset and enable a JTAG connection.



Silk: cTI



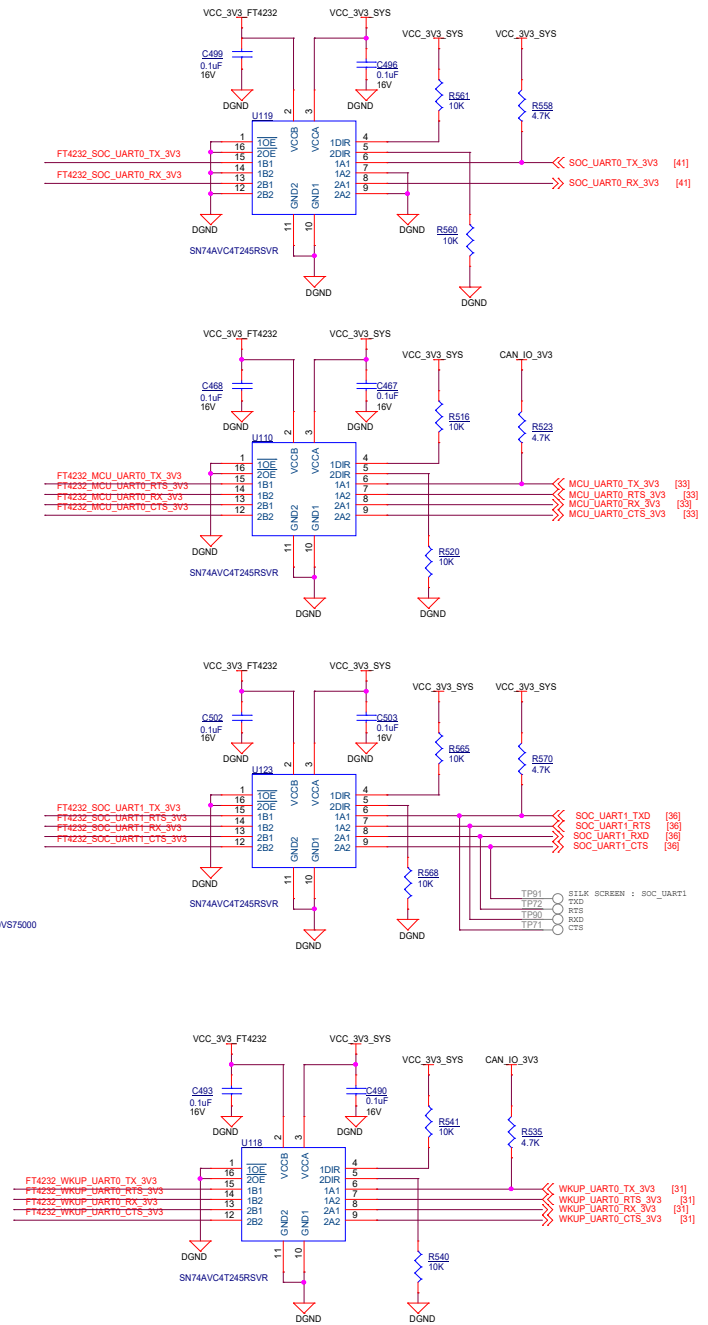
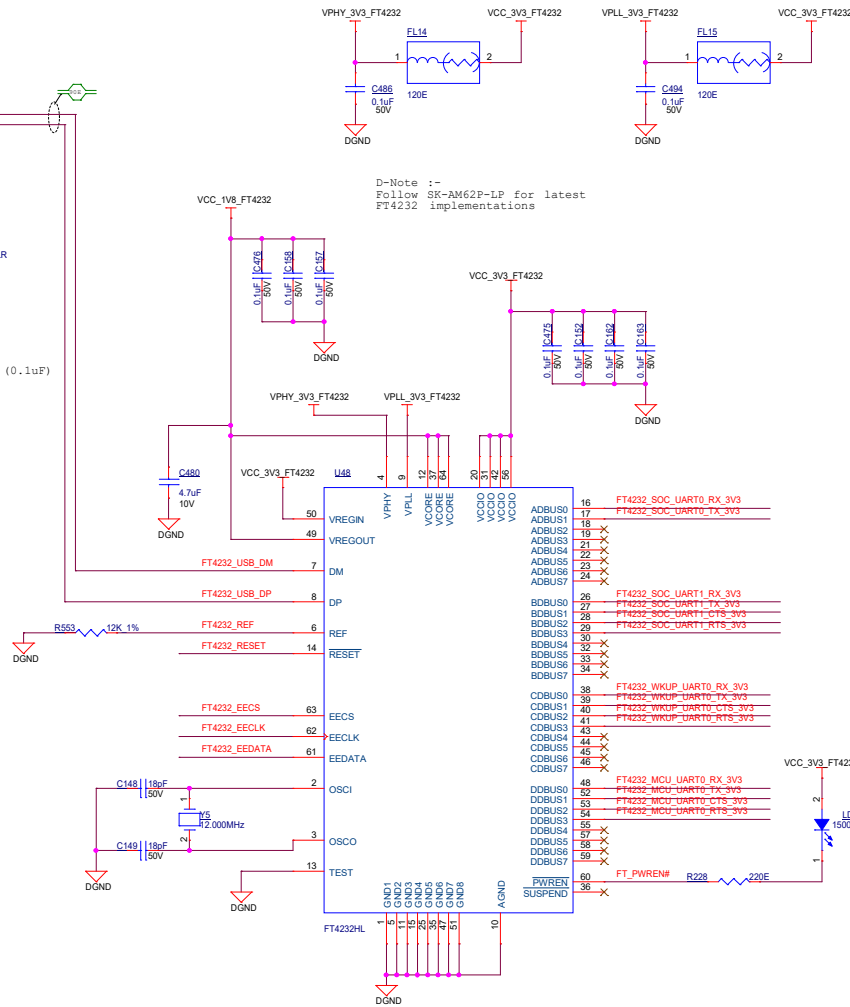
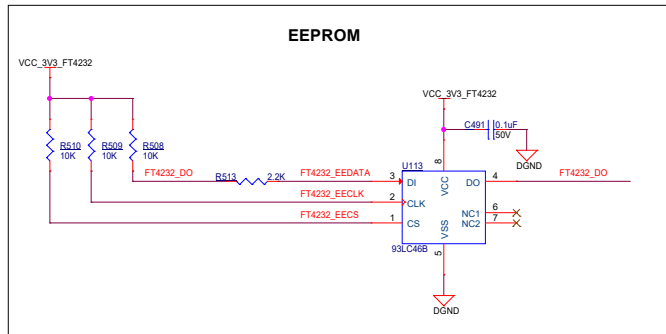
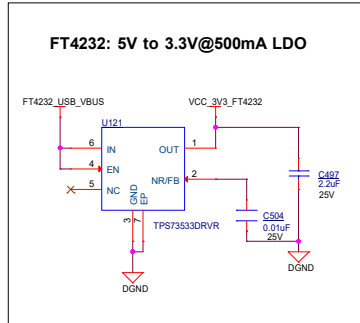
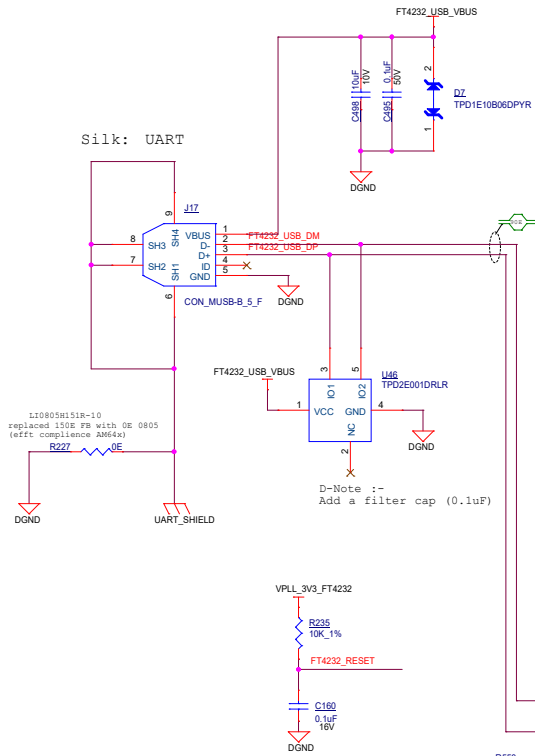
Designed for TI by Mistral Solutions Pvt Ltd



Title JTAG 20 PIN cTI CONNECTOR

Size	PROC135A1	Rev
C		A1
Date:	Thursday, July 24, 2025	Sheet 29 of 44

FT4232 UART TO USB BRIDGE



R-Note :-
Verify the implementation with
the device manufacturer

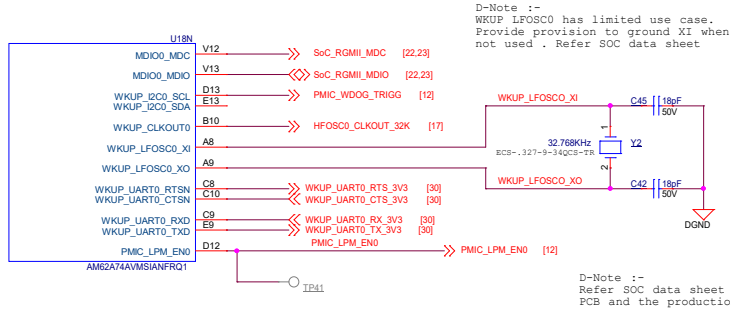
Designed for TI by Mistral Solutions Pvt Ltd



Title				FT4232 UART to USB BRIDGE			
Size	PROC135A1						Rev
C							A1
Date:	Thursday, July 24, 2025			Sheet	30	of	44

D-Note :-
Open-drain output type buffer I2C interfaces A pullup is recommended for Open-drain output type I2C interfaces irrespective of the IO configuration Refer pin connectivity table of SOC data sheet

SOC WKUP DOMAIN

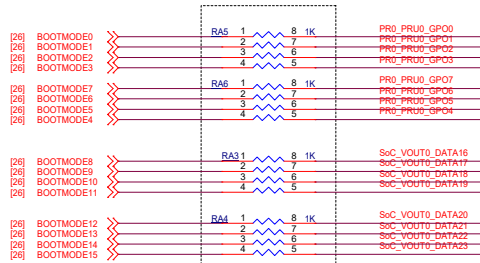


D-Note :-
Shorting of bootmode inputs (IOs) is not recommended or allowed since the IOs have alternate functions that could be configured after boot. Shorting the bootmode pins directly to VCC or ground directly is not recommended. Connect each of the bootmode pins through separate resistor. Choose the bootmode resistor value based on the use case (10K or similar)

D-Note :-
Refer SOC data sheet for the recommended circuit configuration during preproduction PCB and the production PCB

D-Note :-
Reduce the series resistor value when buffer is not used to OR
This resistor is used to isolate the alternate function during testing

BOOTMODE PINS



D-Note :-
1K Resistors are used to isolate the BOOTMODE control logic after the value is latched

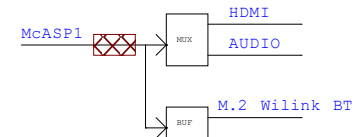
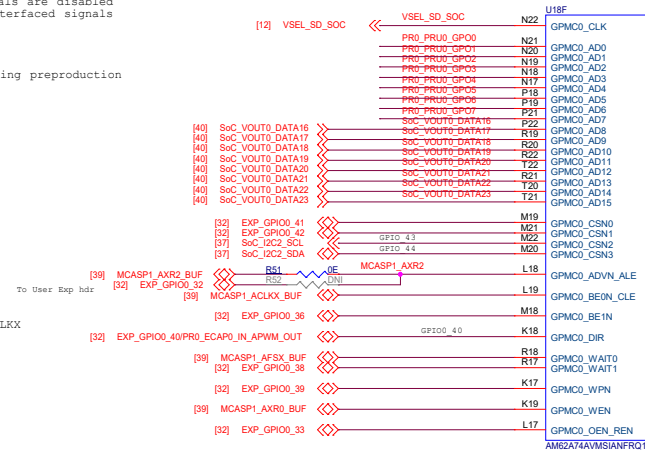
D-Note :-
The only LFOSC0 register bits that should be changed by the customer are BP_C, PD_C, and CTRLMMR_WKUP_LFXOSC_TRIM[18:16], where PD_C is reset (0) to enable the oscillator and the BP_C bit is only set (1) to place the oscillator in bypass mode when using an LVCMOS clock source. The CTRLMMR_WKUP_LFXOSC_TRIM[18:16] bits are set based on the actual capacitance load applied to the crystal, as defined by the Load Capacitance Equation. The load capacitance range of the crystal will be half of the recommended capacitor value range, since there are connected in series with the crystals resonate circuit.

D-Note :-
Open-drain output type buffer I2C interfaces have slew rate requirement when pulled to 3.3 V. An RC is recommended for slew rate control. Refer SK-AM62P-LP schematics

D-Note :-
SOC IO buffers used for GPMC interface signals are disabled during reset. The required pulls for the interfaced signals are provided on the GPMC interface card

D-Note :-
Add a series resistor OR when used as GPMC_Clk

SOC GPMC INTERFACE



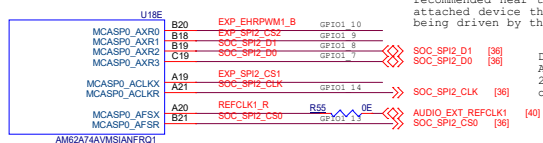
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Title SOC WKUP & GPMC

Size	PROC135A1	Rev	A1
C			
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USER EXPANSION CONNECTOR

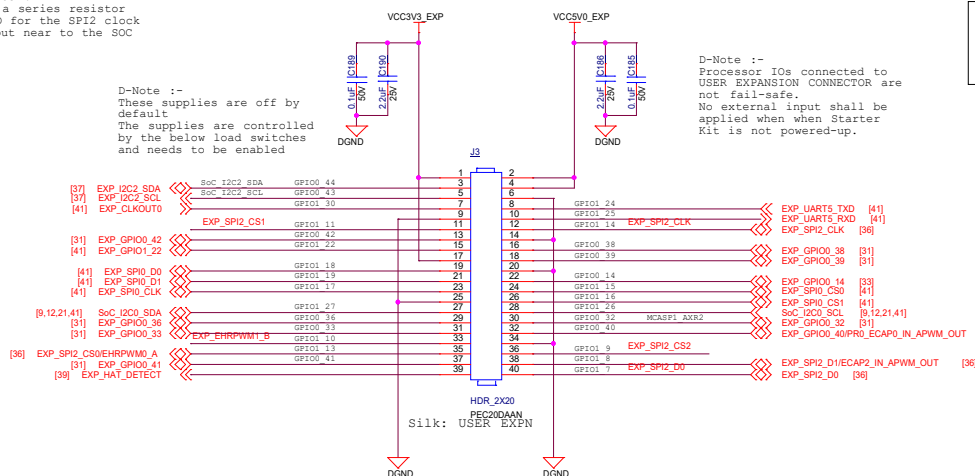


D-Note :-
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO

D-Note :-
Add a series resistor
22 0 for the SPI2 clock
output near to the SOC

CAD Note :-
R55 (Series damping resistor) should be placed close to SOC

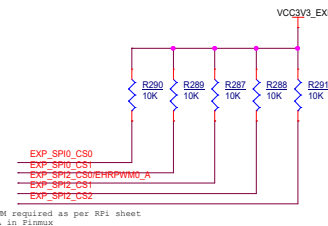
D-Note :-
These supplies are off by default
The supplies are controlled by the below load switches and needs to be enabled



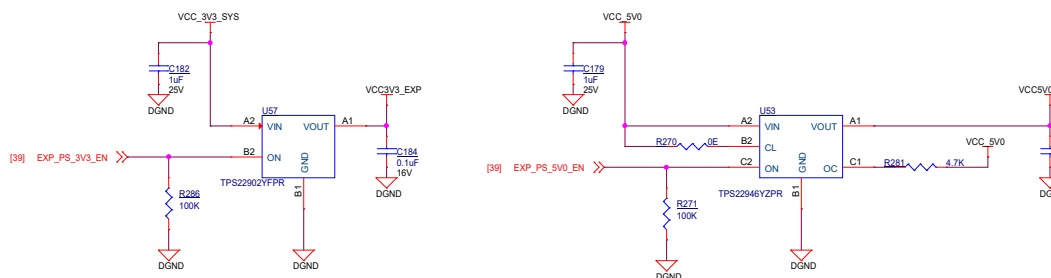
D-Note :-
Any SOC IO that has a trace connected but not being driven actively needs to be connected to an external pull

D-Note :-
Processor IOs connected to
USER EXPANSION CONNECTOR are
not fail-safe.
No external input shall be
applied when when Starter
Kit is not powered-up.

D-Note :-
Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)



LOAD SWITCHES FOR USER EXPANSION CONNECTOR



R-Note :-

AM62A Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62A Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

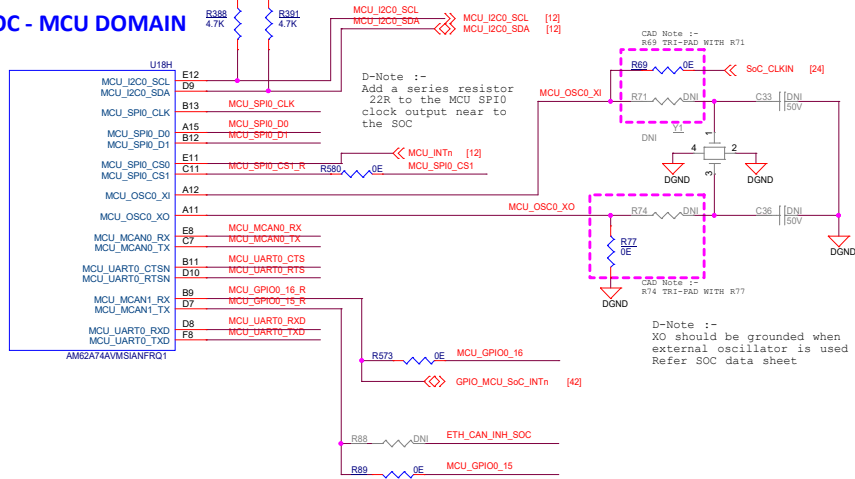


D-Note :-
A pullup is recommended for Open-drain output type I2C interfaces irrespective of the IO configuration Refer pin connectivity table of SOC data sheet

D-Note :-
Open-drain output type buffer I2C interfaces have slew rate requirement when pulled to 3.3 V An RC is recommended for slew rate control. Refer SR-AM62P-LP schematics

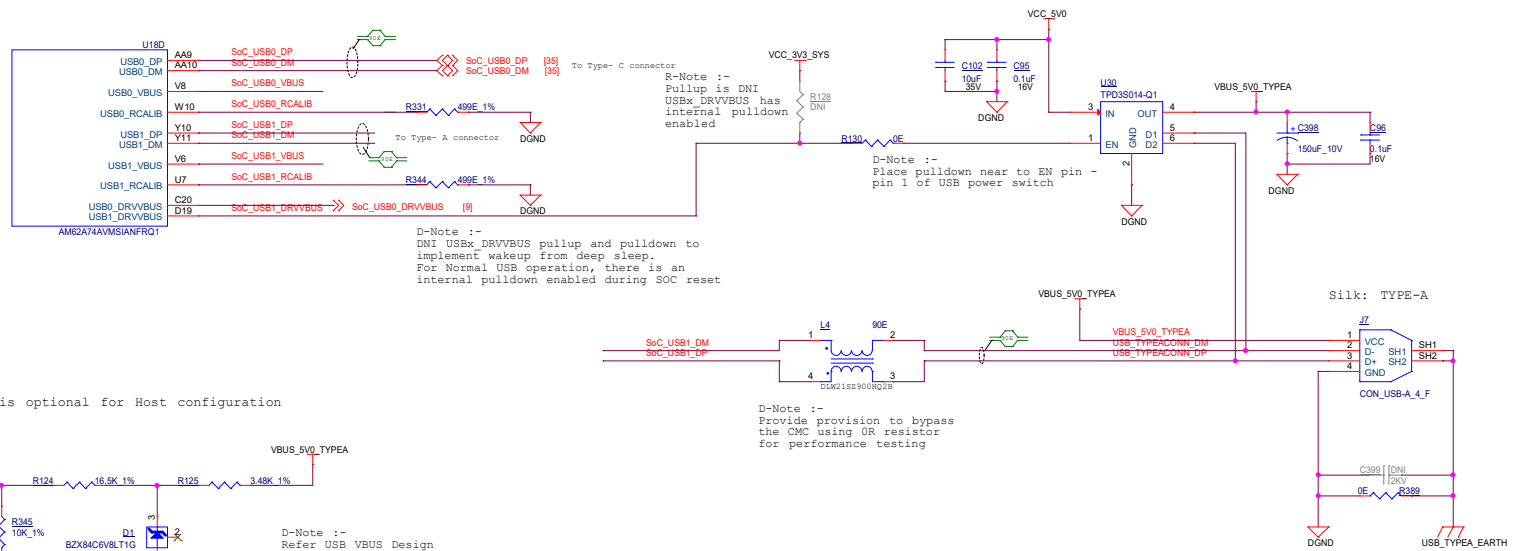
D-Note :-
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO

SOC - MCU DOMAIN

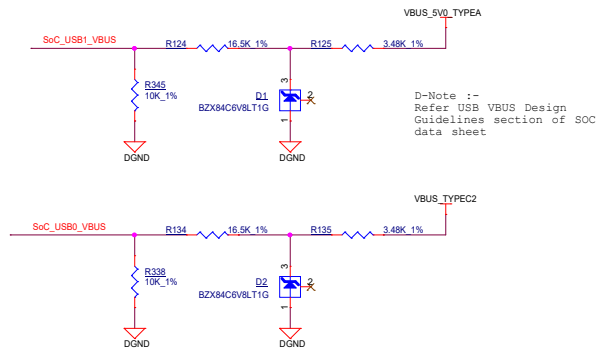


USB1 - USB 2.0 TYPE-A

D-Note :-
Use power switch with OC indication
Example TPS2051
Connect to a SOC IO for OC detection
Refer SK-AM62P-LP schematics



D-Note :-
VBUS connection is optional for Host configuration

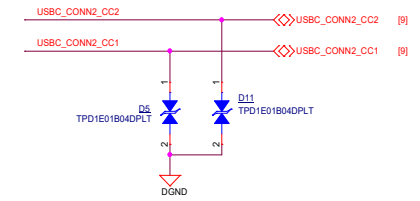
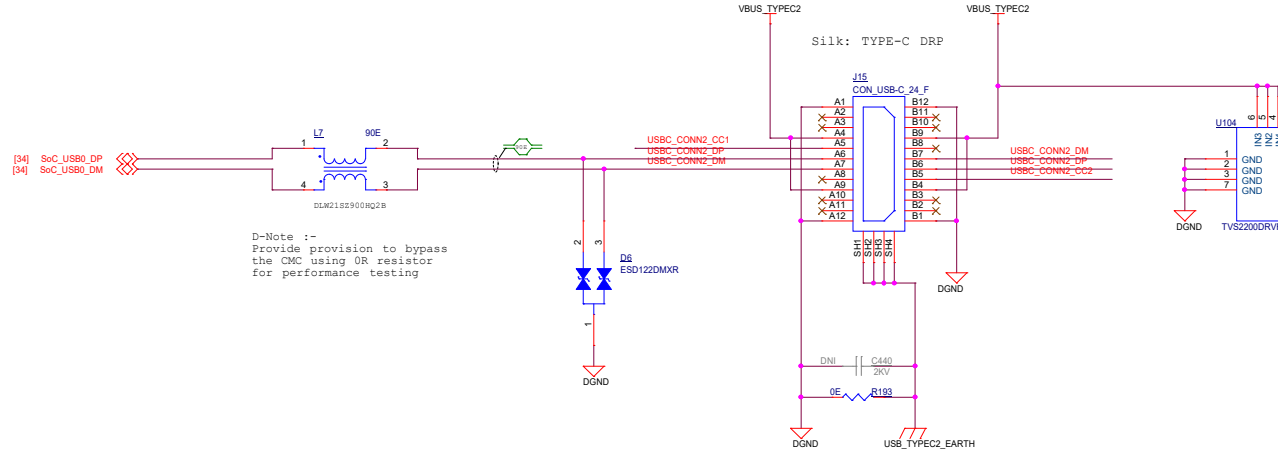


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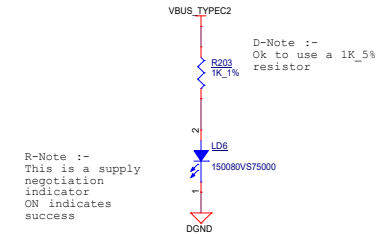


Title USB1 TYPE-A			
Size	PROC135A1		Rev
C			A1
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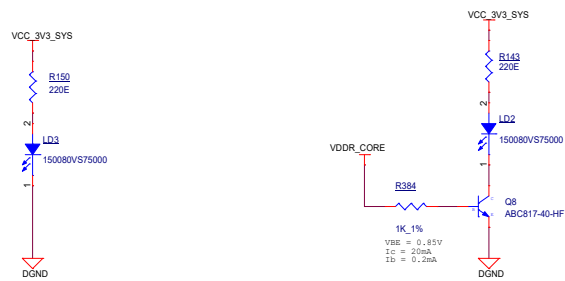
USB0 TYPE-C DRP



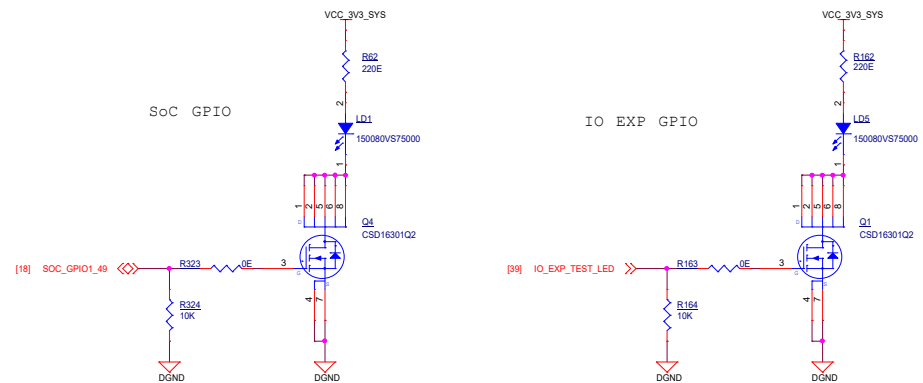
POWER INDICATION LED: VBUS_TYPEC2



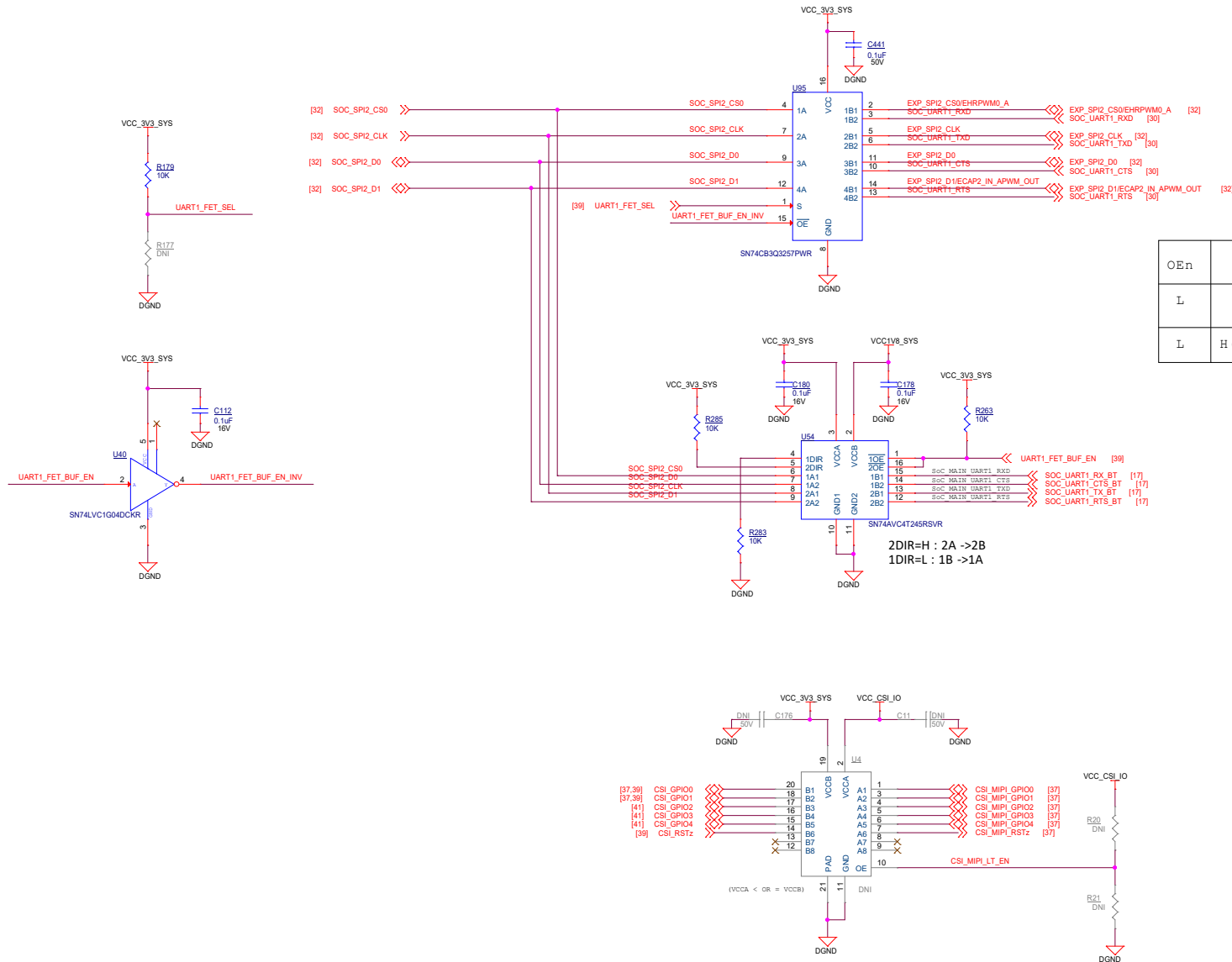
POWER RAIL LEDS



USER TEST LEDS



SoC UART1 FET SWITCH & BUFFER



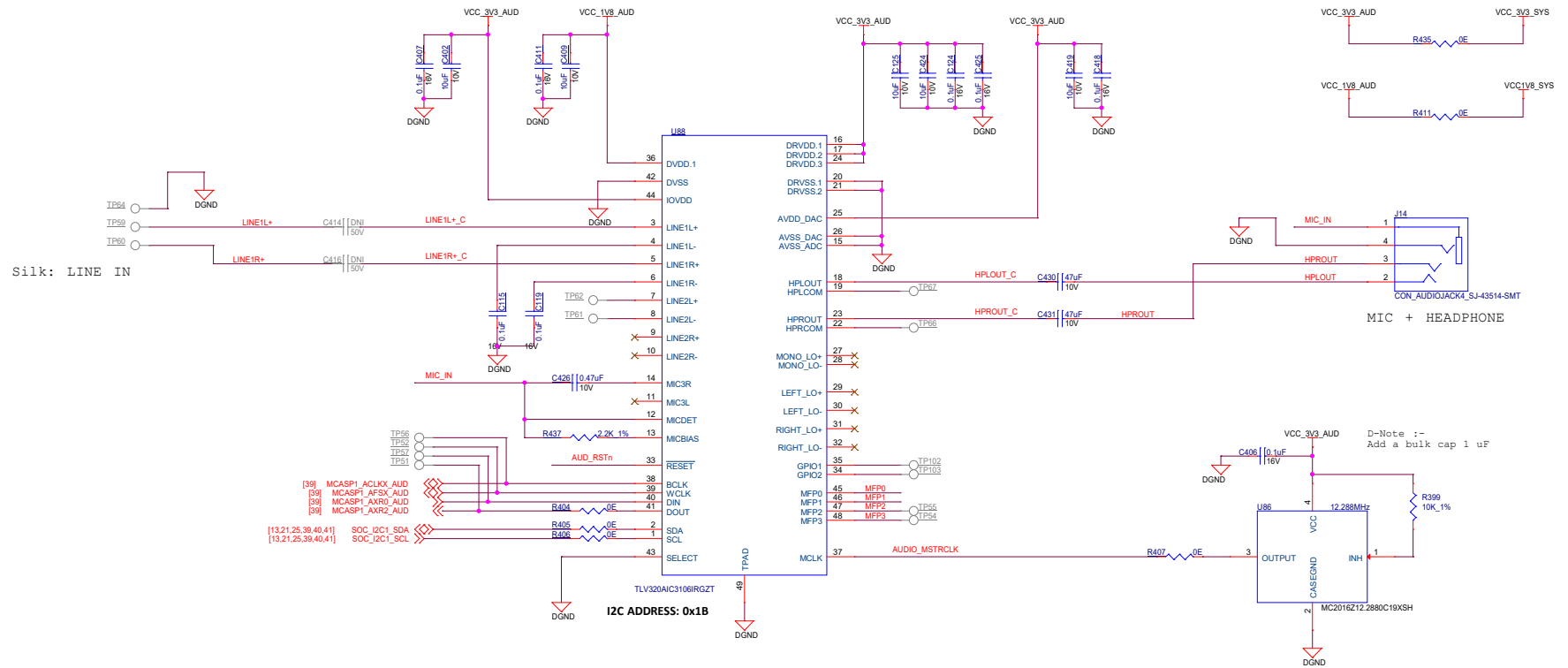
Designed for TI by Mistral Solutions Pvt Ltd



Title SoC UART1 FET SWITCH & BUFFER

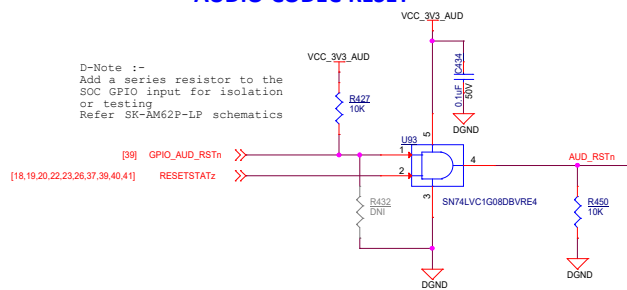
Size	PROC135A1	Rev	A1
C			
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AUDIO CODEC



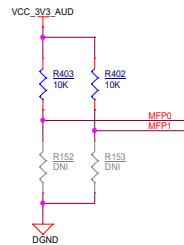
AUDIO CODEC RESET

D-Note :-
Add a series resistor to the SOC GPIO input for isolation or testing
Refer SK-AM62P-LP schematics



CODEC I2C ADDRESS SELECTION

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B



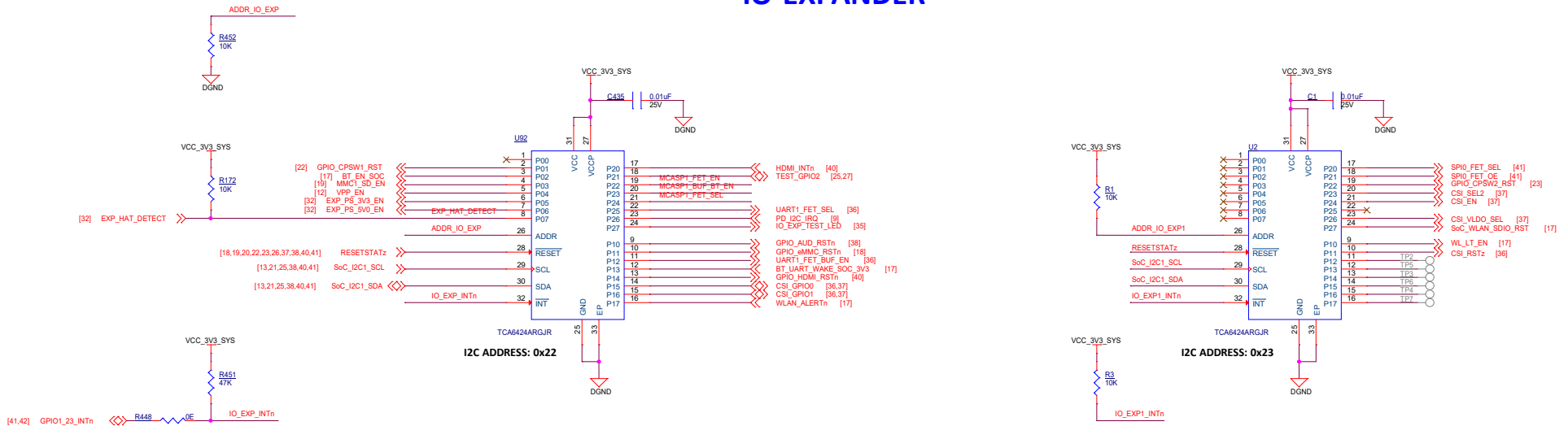
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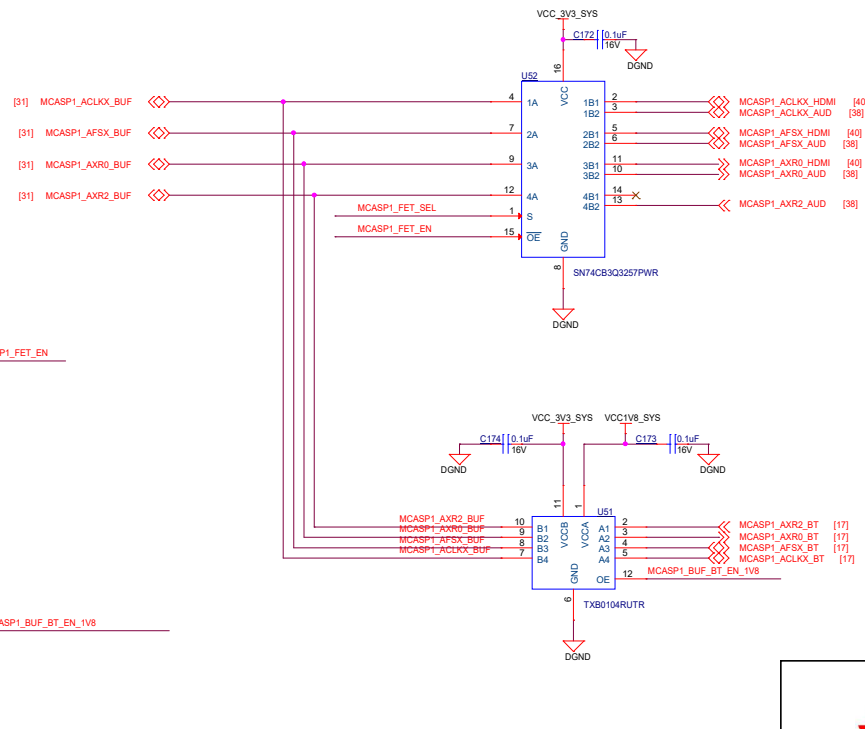
Title AUDIO CODEC

Size	PROC135A1	Rev
C		A1
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IO EXPANDER



McASP1 FET SWITCH & BUFFER



OEn	SEL	INPUT/OUTPUT	
		An	
L	H (DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

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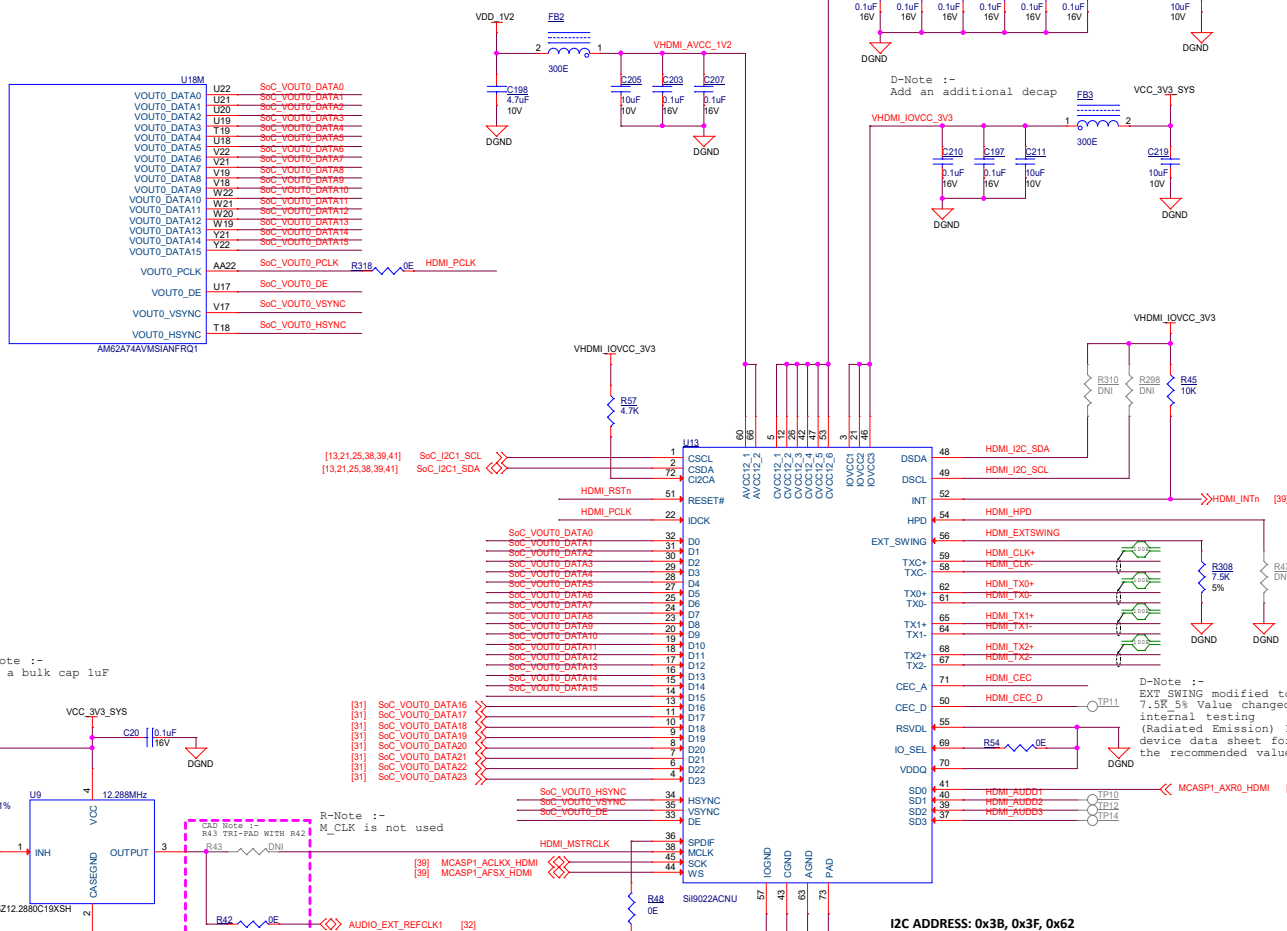


Title IO EXPANDER

Size	PROC135A1	Rev
C		A1
Date:	Thursday, July 24, 2025	Sheet 39 of 44

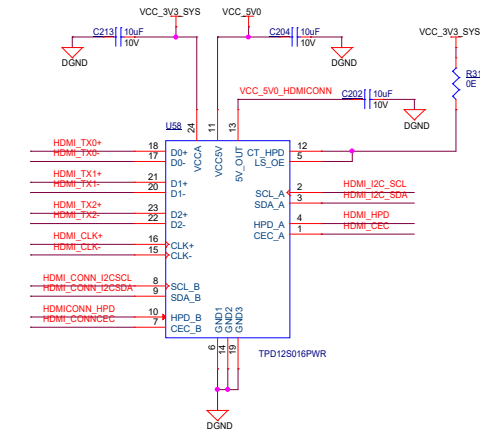
HDMI INTERFACE

R-Note :-
Verify the implementation with
the device manufacturer



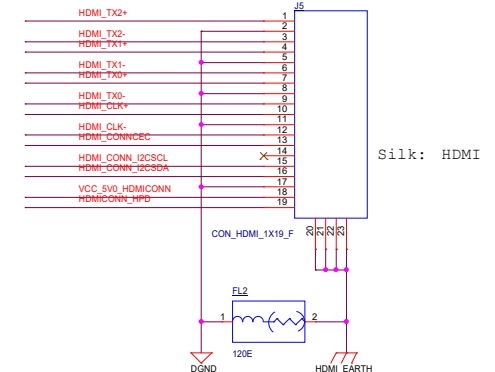
D-Note :-
Add a bulk caps

HDMI ESD DEVICE



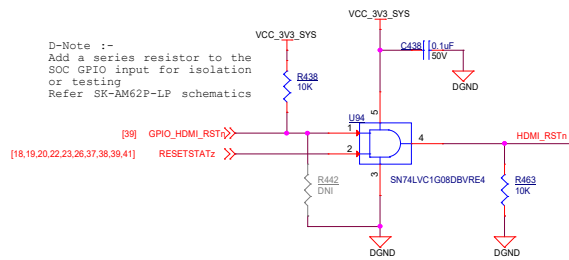
R-Note :-
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.

HDMI CONNECTOR



HDMI RESET

D-Note :-
Add a series resistor to the
SOC GPIO input for isolation
or testing
Refer SK-AM62P-LP schematics



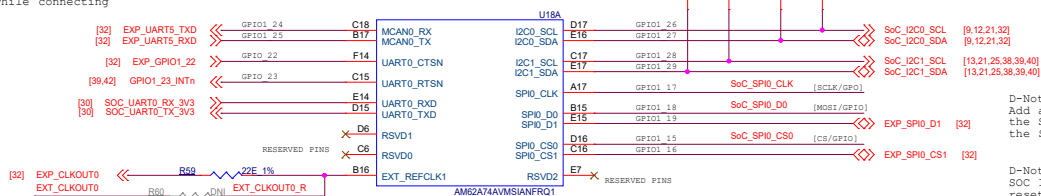
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Title		HDMI INTERFACE	
Size	PROC135A1		Rev
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D-Note :-
The TXD and RXD net names for UART are reverse with respect to MCAN(Refer pin attributes section of the data sheet)
Take note while connecting

SOC - GENERAL

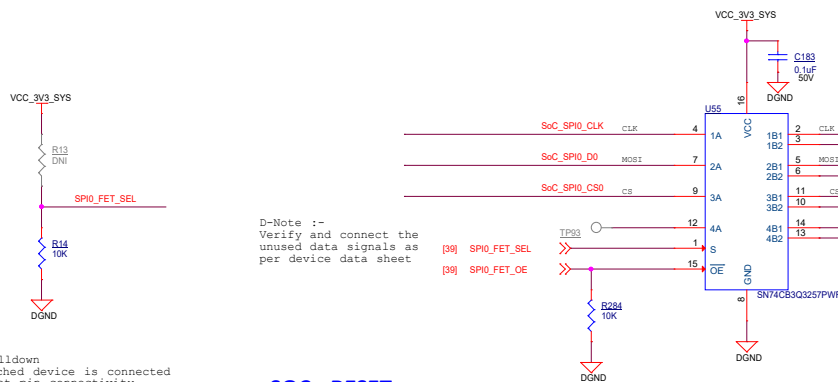


D-Note :-
Ext Refclk1 used as Clkout0
A clock signal should always be connected point to point without any branches. When connecting Clkout0 to more than one (multiple) clock inputs, use a buffer with one input and multiple outputs.

D-Note :-
Add a series resistor 22R for the SPI0 clock output near to the SOC

D-Note :-
SOC IO buffers are off during reset. A pull is recommended near to the attached device that is being driven by the SOC IO

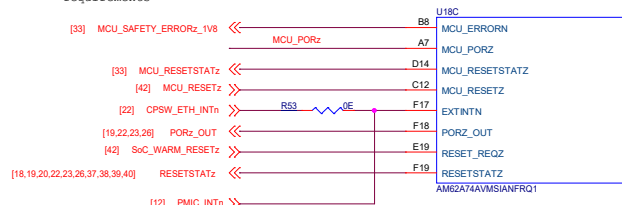
Soc SPI0 FET SWITCH



D-Note :-
Verify and connect the unused data signals as per device data sheet

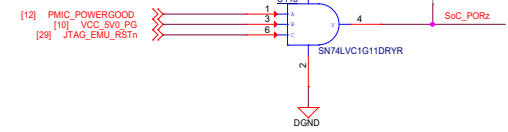
D-Note :-
Provision for a pulldown
Populate when attached device is connected
Refer SOC data sheet pin connectivity requirements

SOC - RESET



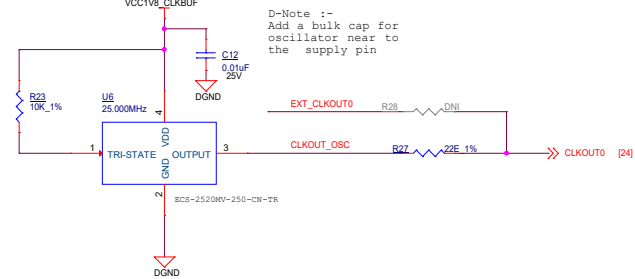
D-Note :-
Open drain output type IO EXTINTn has slew rate limit specified when pulled to 3.3V supply. Add an RC at the input. Refer TMDS64EVM.

D-Note :-
MCU PORz input have a maximum rise/fall time requirements when PMIC_POWERGOOD is connected to the MCU PORz. Adjust the pullup to minimize the rise time (100..200 ns) when using open drain output. MCU PORz is fail-safe and 3.3v tolerant. Therefore, you can pull the MCU_PORz signal to 1.8V or 3.3V.

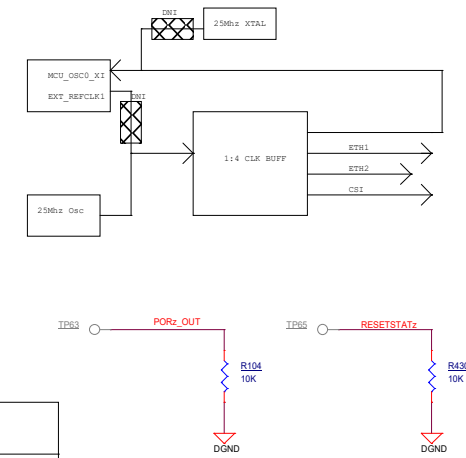


OSCILLATOR

D-Note :-
Refer SOC data sheet for oscillator specs

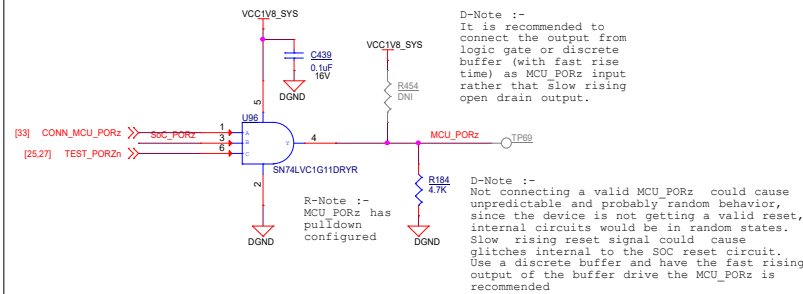


D-Note :-
Add a bulk cap for oscillator near to the supply pin



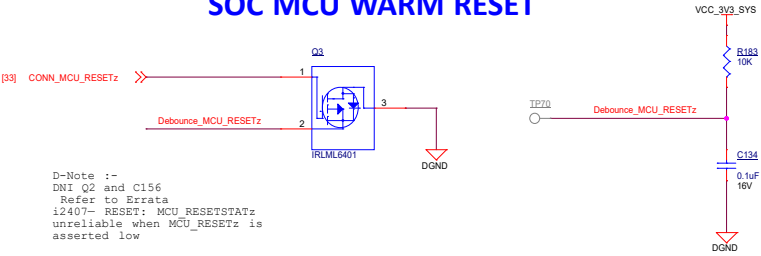
D-Note :-
Pull-down resistor on PORz_OUT and RESESTATz is provided to hold the attached device in reset condition during SOC reset and power-up

MCU POWER ON RESET



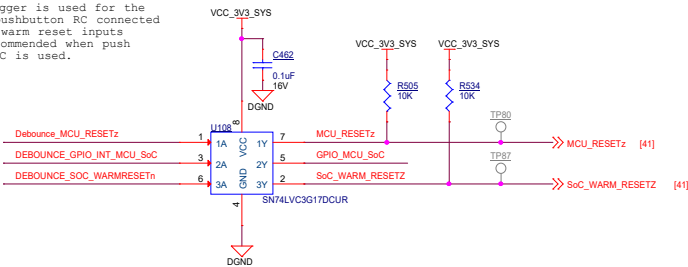
EXTERNAL RESET INPUT AND SCHMITT TRIGGER DEBOUNCE LOGIC

SOC MCU WARM RESET



D-Note :-
DNI Q2 and C156
Refer to Errata
i2407- RESET: MCU RESETSTATz
unreliable when MCU_RESETz is
asserted low

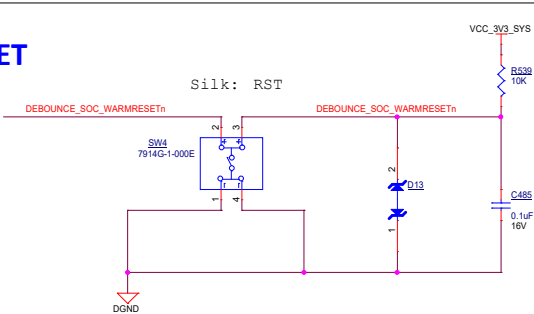
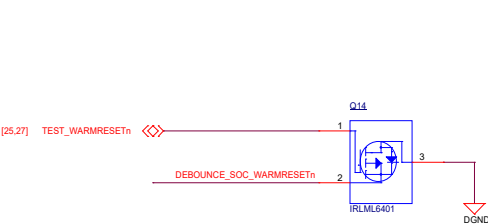
DEBOUNCE CIRCUIT



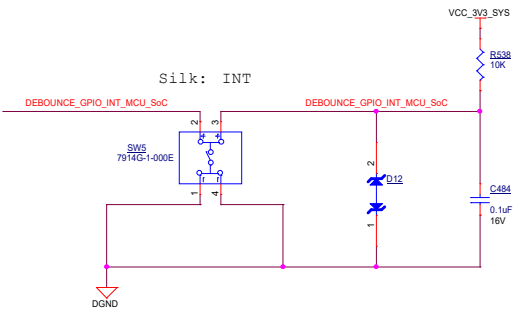
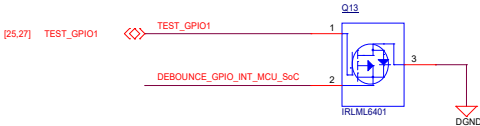
GPIO_MCU_SoC R512 4.7K GPIO1_23_INTn [38,41]

GPIO_MCU_SoC R572 DNI GPIO_MCU_SoC_INTn [33]

SOC WARM RESET



USER INTERRUPT

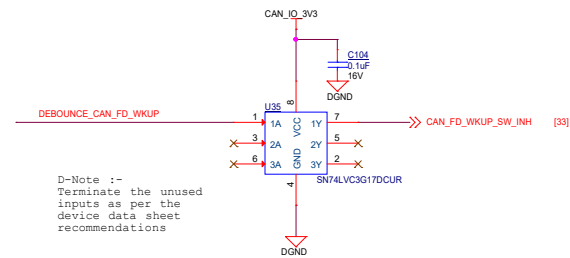
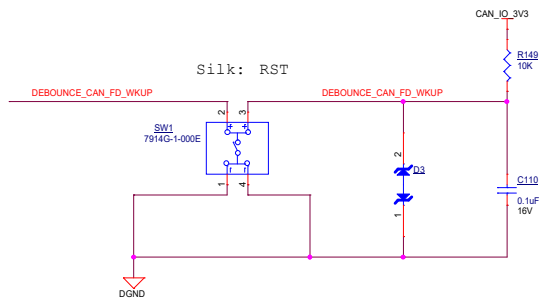


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Title		RESET
Size	PROC135A1	Rev
C		A1
Date:	Thursday, July 24, 2025	Sheet 42 of 44

CAN-FD FAST WAKE UP SW



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Title CAN FD WKUP SW

Size PROC135A1

C

Date: Thursday, July 24, 2025

Rev A1

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MOUNTING HARDWARE

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

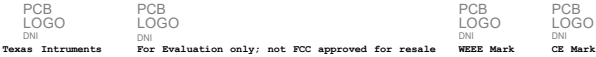
BARE PCB



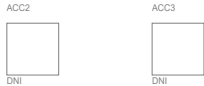
AM62A SOCKET



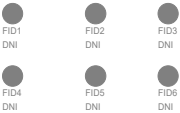
LOGOs



JUMPERS



FIDUCIALS



LABELS



SCREW & WASHER FOR PCIe M.2



D-Note :-
Refer STRAP CONFIGURATION OF
ETHERNET PHYS page from
SR-AM64B schematics

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Title		HARDWARE SCHEMATICS	
Size	PROC135A1	Rev	A1
C			
Date:	Thursday, July 24, 2025	Sheet	44 of 44