

AM62A7 / AM62A3 LOW POWER STARTER KIT SK (EVM) WITH TPS65931211-Q1 PMIC

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Revision Number

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REV	B
VER	0.3

D-Note :-

SK/EVM is a device evaluation board or platform. The SK/EVM is not a reference design. In some cases the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SOC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata, and TRM when designing their custom board. The information found in the datasheet should always take precedence over the SK/EVM implementation.

R-Note :-

- * Verify the DNI components configuration with respect to the SK schematics (Use PDF) after completion of board design before board assembly
- * A standard 5% tolerance resistor can be used for most of the series and parallel pull resistor
- * Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build. (Refer FAQs listed for additional details)



Indicates circuit level change



Indicates that the value of the component has been updated.

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REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	03 JUNE 2026	Drafted from "PROC135EA_SCH" document.	Mistral Design Team	Pandiyarajan	Ajit MB
0.2	08 JUNE 2026	Below components have been updated based on TI review comments checklist: - U30 part number has been changed to TPS2051BD and the corresponding circuit has been updated - U129 and the corresponding circuit have been added for ESD protection of USB data lines - Replaced U20 with a dual-channel load switch of Part number TPS22996HQDYCRQ1 - Added RC filter of value 62E and 47pF to WKUP_I2C0_SCL, WKUP_I2C0_SDA, MCU_I2C0_SCL, MCU_I2C0_SDA and EXTINTn signals - Added a series resistor of value 22E R782, R746 and R761 to the nets SOC_SPI2_CLK, MCU_SPI0_CLK and SoC_SPI0_CLK respectively - Added a series resistor of value 47E R757, R758 and R759, R760 to SoC_I2C0_SCL, SoC_I2C0_SDA, SoC_I2C1_SCL and SoC_I2C1_SDA respectively - Tolerance value of R160, R475, R467 has been changed from 1% to 5% - Tolerance value of C241, C222, C235, C220, C285, C231, C223, C264, C287 from 20% to 10% - Pull-ups of OSPI, MMC0, MMC1 and MMC2 have been changed from 10k to 47k - Added four 0.01uF capacitors each to VBUS_TYPEC1 and VBUS_TYPEC2 respectively. - Changed VMON_VSYS monitoring voltage from VCC_3V3_MAIN to VCC_5V0 - Shifted all the current sense resistors to the PMIC page - Added 0E series resistor to all of the GPIO Reset signals that are connected to eMMC, OSPI, SD Card, HDMI, Audio CODEC, RGMII interfaces - Added and updated D-Notes	Mistral Design Team	Pandiyarajan	Ajit MB
0.3	25 JUNE 2026	- Added R792 series 0E Resistor to the SoC Pin PMIC_LPM_EN0 - Updated D-Notes	Mistral Design Team	Pandiyarajan	Ajit MB

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LINKS TO KEY COLLATERALS

Hardware Design Guide : https://www.ti.com/lit/an/sprad85/sprad85.pdf
Schematic Design guidelines combined for Sitara processor families : https://www.ti.com/lit/an/sprad21d/sprad21d.pdf
PMIC Power Solutions Application Note : https://www.ti.com/lit/po/sltv204/sltv204.pdf
DDR Board Design and Layout Guidelines : https://www.ti.com/lit/an/sprad66a/sprad66a.pdf
SKs (Starter Kits) for reference : SK-AM62B, SK-AM62B-P1, SK-AM62-LP, SK-AM62-SIP, SK-AM62A-LP, SK-AM62P-LP

LINKS TO KEY FAQs

https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1203305/faq-am62a7-and-am62a7-q1-custom-board-hardware-design-collaterals-to-get-started
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1203441/faq-am62a3-and-am62a3-q1-custom-board-hardware-design-collaterals-to-get-started
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1306030/faq-am62p-am62p-q1-custom-board-hardware-design--faq-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1340905/faq-am62a7-am62a7-q1-am62a3-am62a3-q1---custom-board-hardware-design---guidelines-for-reuse-of-sk-am62a-lp-schematics
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1347063/faq-am62a7-and-am62a7-q1-am62a3-and-am62a3-q1---custom-board-hardware-design---design-and-review-notes-for-reuse-of-sk-am62a-lp-schematics
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1280753/faq-am62a7-am62a7-q1-am62a3-am62a3-q1-custom-board-hardware-design---faq-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit

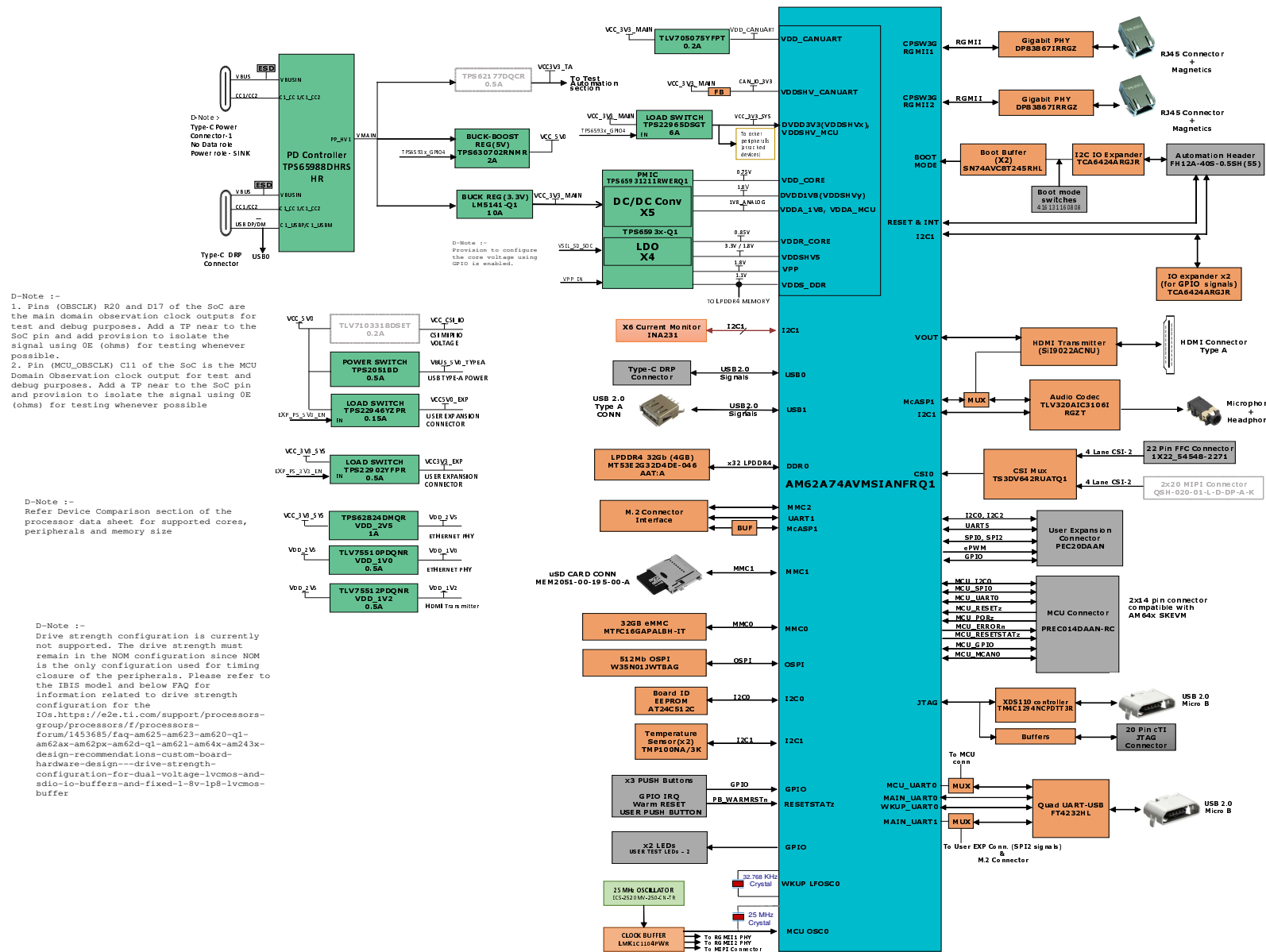
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Title LINKS TO KEY COLLATERALS AND FAQs

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BLOCK DIAGRAM SK-AM62A-LP



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Title	BLOCK DIAGRAM AM62A_SKEVM
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Size	2000-10000
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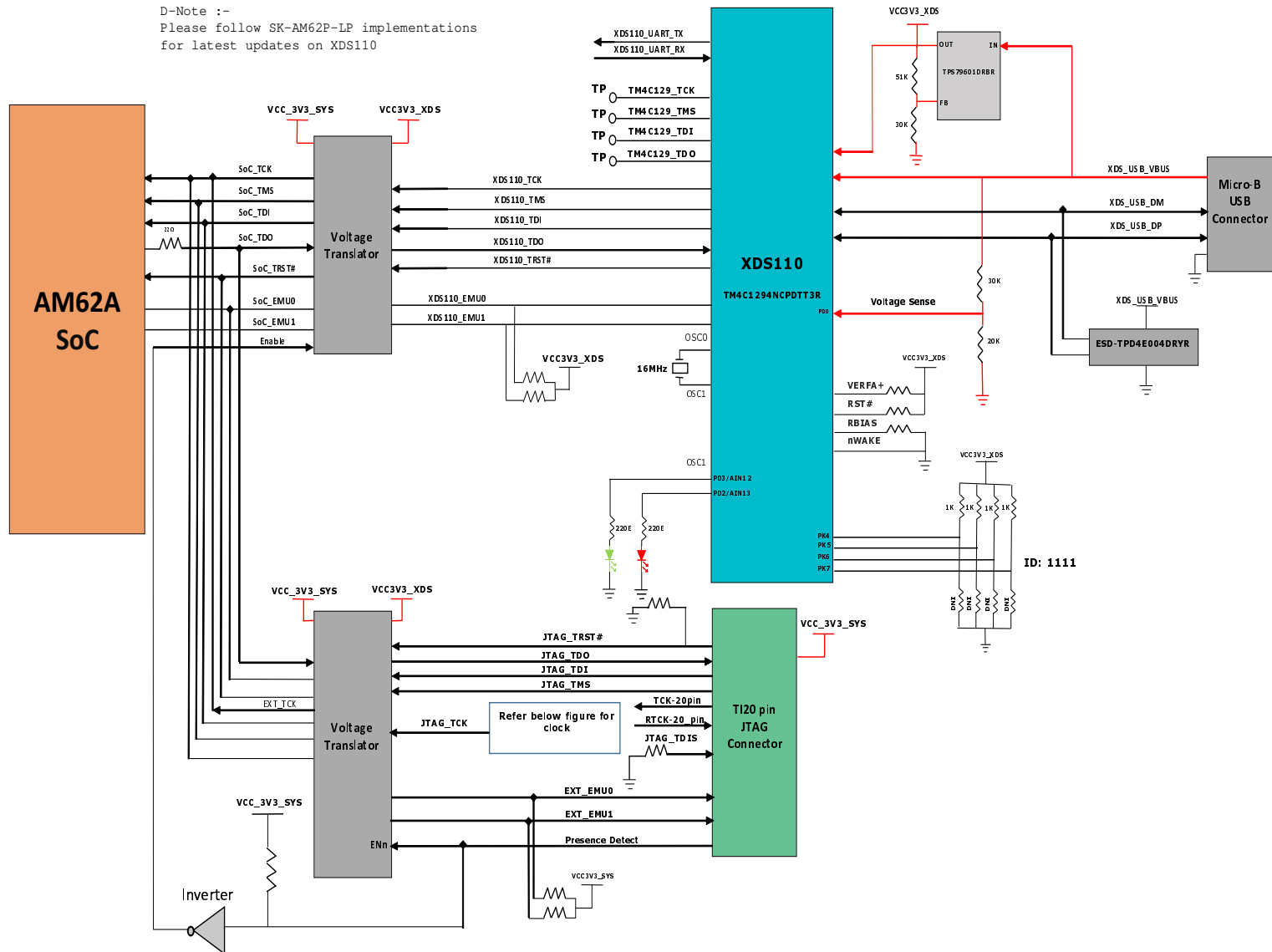
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BLOCK DIAGRAM_XDS110

D-Note :-
Please follow SK-AM62P-LP implementations
for latest updates on XDS110



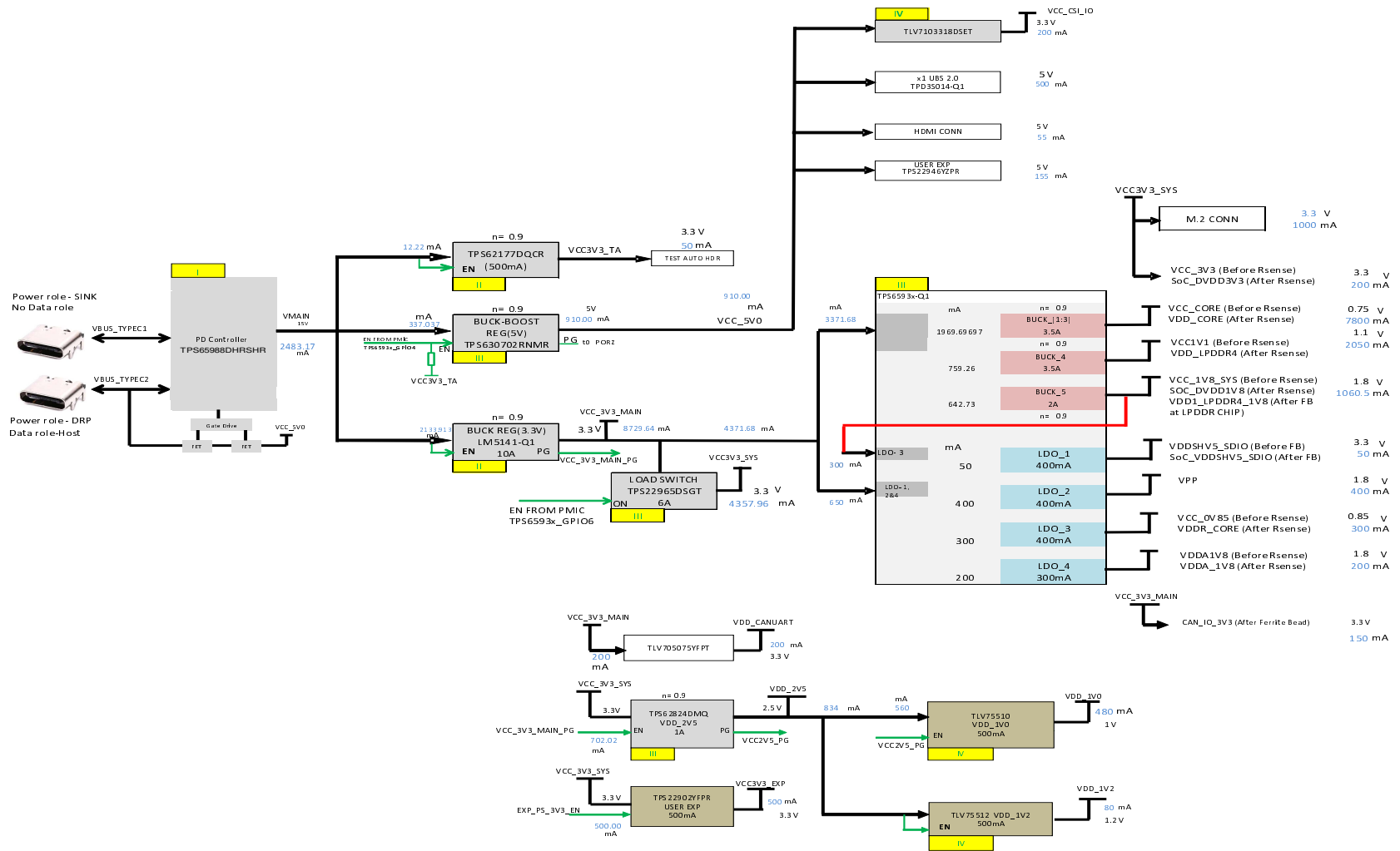
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Title BLOCK DIAGRAM XDS110 DEBUGGER

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POWER BLOCK DGM



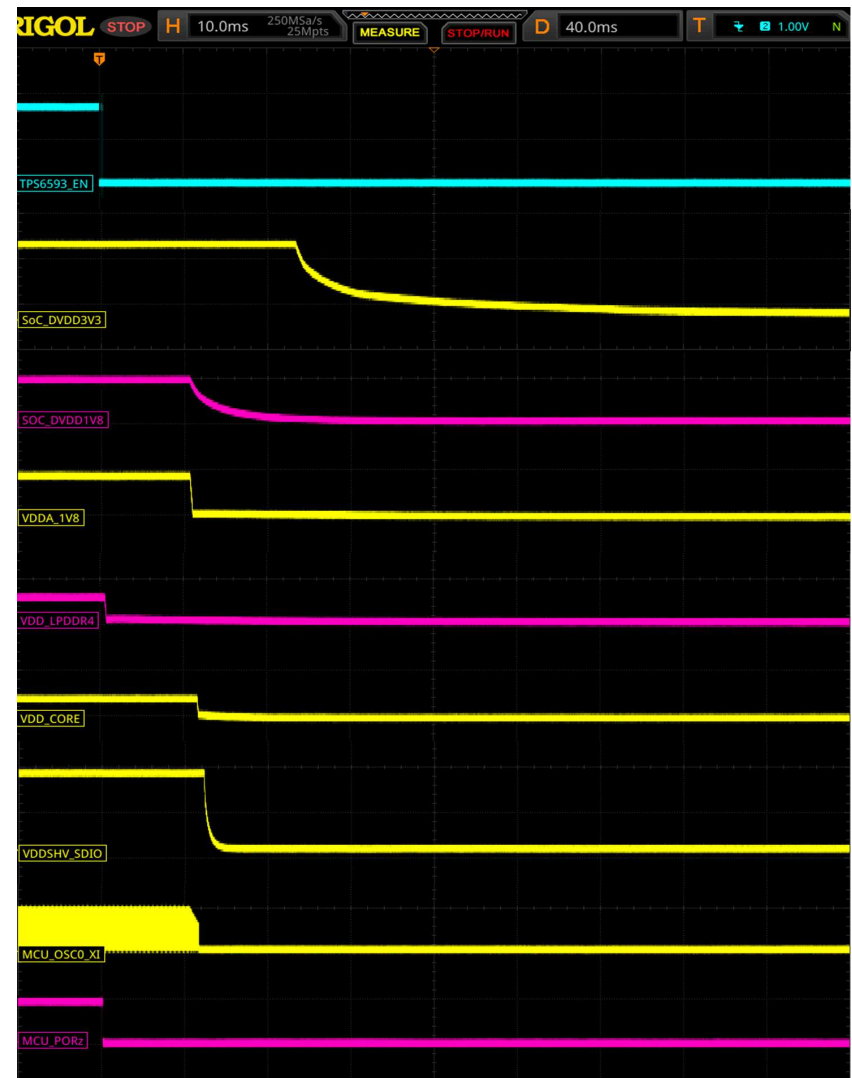
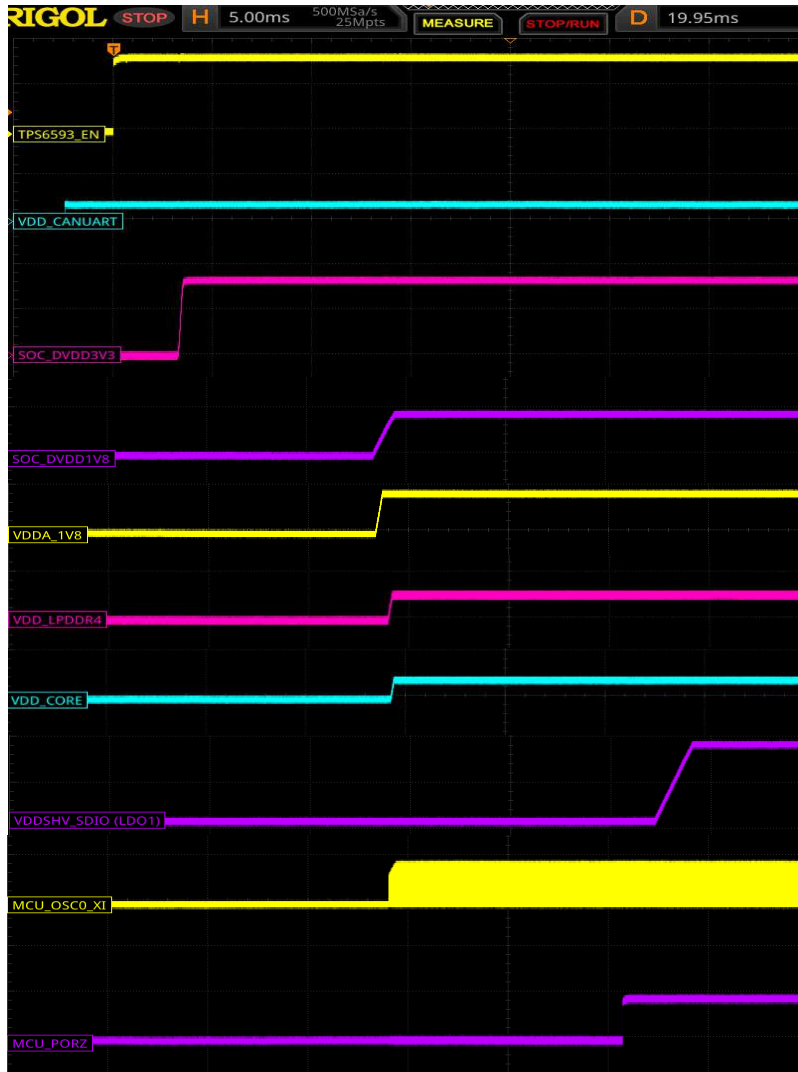
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Title POWER ARCHITECTURE BLOCK DIAGRAM

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POWER SEQUENCE



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Title POWER-UP AND POWER-DOWN SEQUENCE

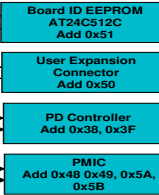
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I2C TREE

R-Note :-
Add - Indicates
Address

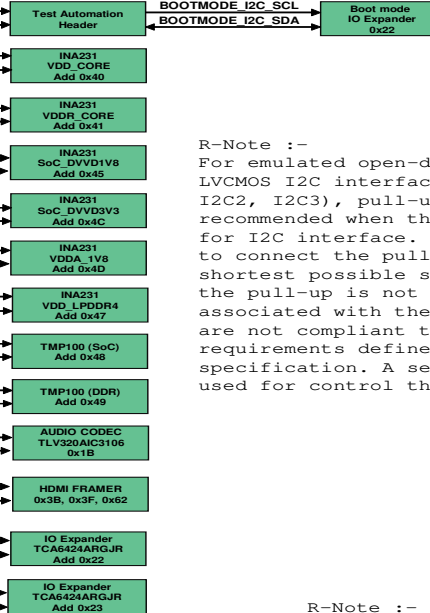
**AM62A74AVMSIANFRQ1
SoC**

I2C0
SOC_I2C0_SCL
SOC_I2C0_SDA



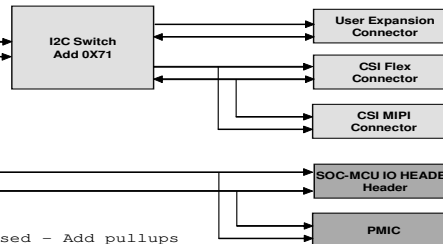
R-Note :-
Refer to the following section
of the processor-specific data
sheet:
Timing and Switching
Characteristics I2C Exceptions

SOC_I2C1
SOC_I2C1_SCL
SOC_I2C1_SDA



R-Note :-
For emulated open-drain output type
LVCMOS I2C interfaces (I2C0, I2C1,
I2C2, I2C3), pull-up resistors are
recommended when the IOs are configured
for I2C interface. The recommendation
to connect the pull-ups with the
shortest possible stub. Location of
the pull-up is not critical. The IOs
associated with these I2C interfaces
are not compliant to the fall time
requirements defined in the I2C
specification. A series resistor47E is
used for control the fall time.

SOC_I2C2
SOC_I2C2_SCL
SOC_I2C2_SDA



R-Note :-
For I2C interfaces with open-drain
output type buffer (MCU_I2C0 and
WKUP_I2C0), an external pull-up is
recommended irrespective of
peripheral usage and IO
configuration.
An RC to limit the slew rate (C
placed near to SOC pin) is
recommended. Refer to the Pin
Connectivity Requirements section
of the processor-specific data
sheet

MCU_I2C0
MCU_I2C0_SCL
MCU_I2C0_SDA

WKUP_I2C0
(Unused)

D-Note :-
WKUP_I2C0 Unused - Add pullups
irrespective of IO configuration

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GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE RAIL CONNECTED ON SKEWM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	Soc_DVDD1VB
2	WLAN Interrupt	WLAN_IRQ	INTERUPT	GPIO_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	Soc_DVDD1VB
3	Enable for BT Interface	BT_EN_SDC	ENABLE	MCU_GPIO_0	MCU_SPB_CS0	OUTPUT	LOW	HIGH	VDDSHV_MCU	Soc_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_N7n	INTERUPT	GPIO_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	Soc_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_CS_P1_RSTn	RESET	GPIO_12	OSPI_CS_n1	OUTPUT	HIGH	LOW	VDDSHV3	Soc_DVDD1VB
6	MCU Header GPIO_16	MCU_GPIO_16	GPIO	MCU_GPIO_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
7	MCU Header GPIO_15	MCU_GPIO_15	GPIO	MCU_GPIO_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
8	PMIC Interrupt	PMIC_INT_8	INTERUPT	GPIO_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV3	Soc_DVDD3V3
9	CAN-FD fast wake up signal from switch	CAN_FD_WKUP_SW_INH	INTERUPT	MCU_GPIO_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
10	CAN-FD fast wake up signal from MCU header	CAN_FD_WKUP_HDB_INH								
11	Interrupt signal from Automotive Ethernet ADD-ON board	CPSW_ETH2_INH								
12	User test LED control signal	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	Soc_DVDD3V3
13	Watchdog trigger input signal for Watchdog trigger mode	PMIC_WDOG_TRIGGER	ENABLE	MCU_GPIO_19	WKUP_DCO_SCL	INPUT	LOW	HIGH	VDDSHV_MCU	Soc_DVDD3V3
14	Wakeup signal from RGMII	CPSW_ETH2_WAKE	INTERUPT	MCU_GPIO_10	WKUP_DCO_SDA	INPUT	LOW	HIGH	VDDSHV_MCU	Soc_DVDD3V3
15	User EXP Conn GPIO	EXP_GPIO1_22	GPIO	GPIO1_22	UART0_CTSn	NA	NA	NA	VDDSHV0	Soc_DVDD3V3
16	IO Expander Interrupt	GPIO1_23_INTn	INTERUPT	GPIO1_23	UART0_CTSn	INPUT	HIGH	LOW	VDDSHV0	Soc_DVDD3V3
17	User Interrupt									
18	User EXP Conn GPIO	EXP_GPIO1_14_1T	GPIO	GPIO_14	OSPI_CS_n3	NA	NA	NA	VDDSHV1	Soc_DVDD1VB
19	PMIC Standby Disable	PMIC_P_M_END	ENABLE	MCU_GPIO_22	PMIC_P_M_END	OUTPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
20	User EXP Conn GPIO	EXP_EXPWM1_8	GPIO	GPIO1_10	MCASP0_AXI0	NA	NA	NA	VDDSHV0	Soc_DVDD3V3
IO EXPANDER - 01										
1	Ethernet Daughter Card plug in detect	RGMII_RH_DCON_DET	DETECTION	IO EXPANDER-P00		INPUT	HIGH	LOW		VCC_3V3_SYS
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P01		OUTPUT	HIGH	LOW		VCC_3V3_SYS
3	M.2 module Bluetooth LDO Enable	BT_EN_SDC	ENABLE	IO EXPANDER-P02		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
5	SOC eFuse Voltage (VPP=1.8V) Regulator Enable	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	NA	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P06		OUTPUT	LOW	HIGH		VCC_3V3_SYS
8	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
9	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	IO EXPANDER-P08		OUTPUT	HIGH	LOW		VCC_3V3_SYS
10	eMMC Reset control GPIO	GPIO_EMMC_RSTn	RESET	IO EXPANDER-P11		OUTPUT	HIGH	LOW		VCC_3V3_SYS
11	SOC UART1 Mux Select	UART1_TET_BUF_EN	ENABLE	IO EXPANDER-P12		OUTPUT	HIGH	LOW		VCC_3V3_SYS
12	BT UART WAKEUP signal	BT_UART_WAKE_SDC_3V3	INTERUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER-P14		OUTPUT	HIGH	LOW		VCC_3V3_SYS
14	Raspberry Pi Camera CSI0 GPIO1	CSI0_GPIO0	INPUT/OUTPUT	IO EXPANDER-P15		NA	NA	NA		VCC_3V3_SYS
15	Raspberry Pi Camera CSI0 GPIO2	CSI0_GPIO1	INPUT/OUTPUT	IO EXPANDER-P16		NA	NA	NA		VCC_3V3_SYS
16	WLAN Alert Interrupt	WLAN_ALERTn	INTERUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	HDMI Interrupt	HDMI_INTn	INTERUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC_3V3_SYS
19	MCASP1 Enable and Direction Control	MCASP1_TET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
20		MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
21		MCASP1_TET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	-		VCC_3V3_SYS
22		UART1_TET_SEL	DIRECTION CONTROL	IO EXPANDER-P25		OUTPUT	HIGH	-		VCC_3V3_SYS
23	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	INTERUPT	IO EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_SYS
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER - 02										
1	Soc SPD MUX Selection	SPD_TET_SEL	CONTROL	IO EXPANDER-P30		OUTPUT	LOW	-		VCC_3V3_SYS
2	Soc SPD MUX Enable	SPD_TET_OE	ENABLE	IO EXPANDER-P31		OUTPUT	LOW	LOW		VCC_3V3_SYS
3	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P32		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	CSI Hex and mipi MUX Selection	CSI_SEL2	CONTROL	IO EXPANDER-P33		OUTPUT	HIGH	-		VCC_3V3_SYS
5	CSI MUX Enable	CSI_EN	ENABLE	IO EXPANDER-P34		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
6	Auto PHY mode config	AUTO_100M_1000M_CONFIG	CONTROL	IO EXPANDER-P35		OUTPUT	NA	NA		VCC_3V3_SYS
7	CSI I/O Voltage Select (VCC_CSI_I/O)	CSI_VIDD_SEL	CONTROL	IO EXPANDER-P36		OUTPUT	LOW	-		VCC_3V3_SYS
8	WLAN Reset control GPIO	SOC_WLAN_SDB_RST	RESET	IO EXPANDER-P37		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	Wlink Enable	WL_1T_EN	ENABLE	IO EXPANDER-P30		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
10	CSI Reset Control GPIO	CSI_RSTz	RESET	IO EXPANDER-P31		OUTPUT	LOW	LOW		VCC_3V3_SYS

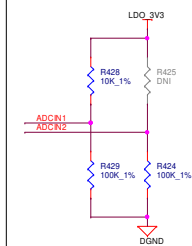
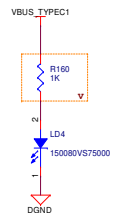
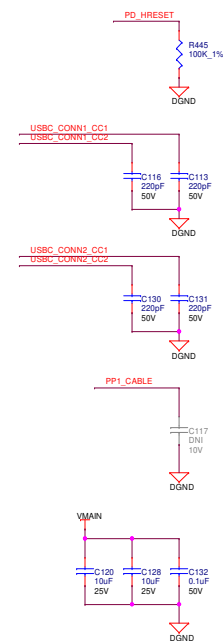
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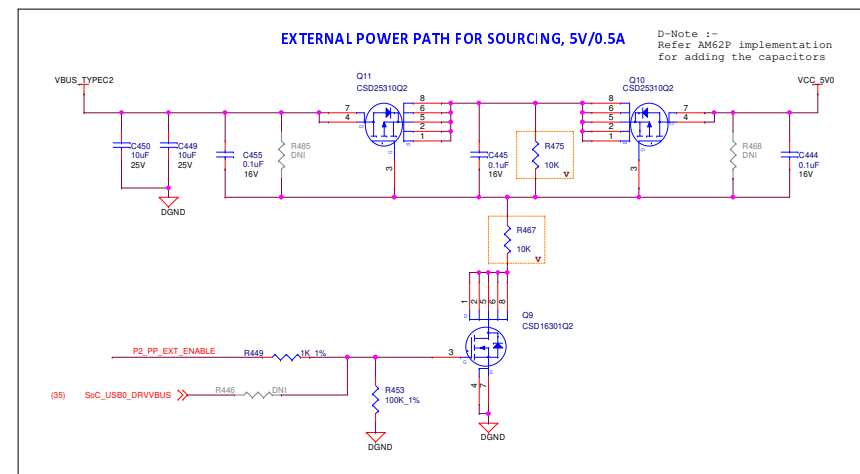
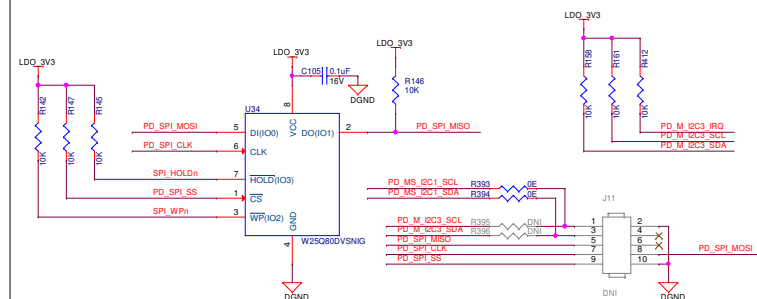
Title GPIO MAPPING TABLE

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USB TYPE-C PD CONTROLLER AND POWER SUPPLY



SPI EEPROM & PROGRAMMING HEADER



Title	USB TYPE-C PD CONTROLLER AND POWER SUPPLY
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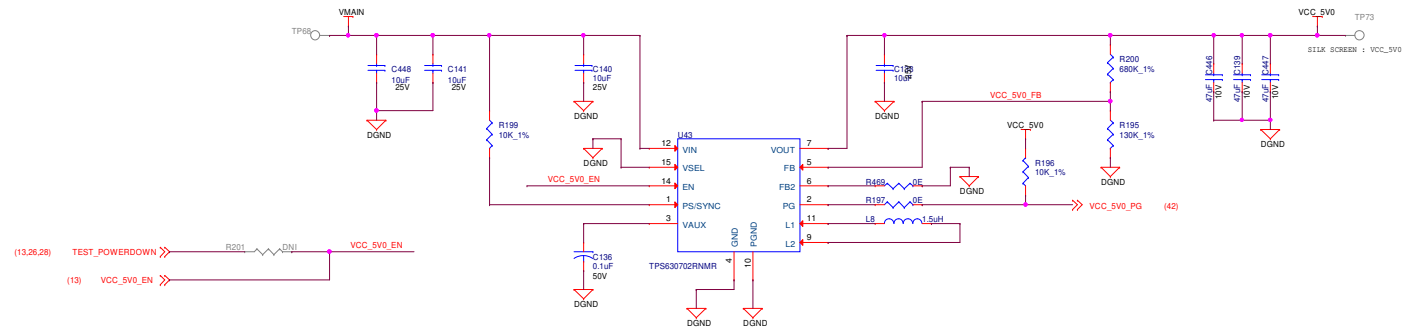


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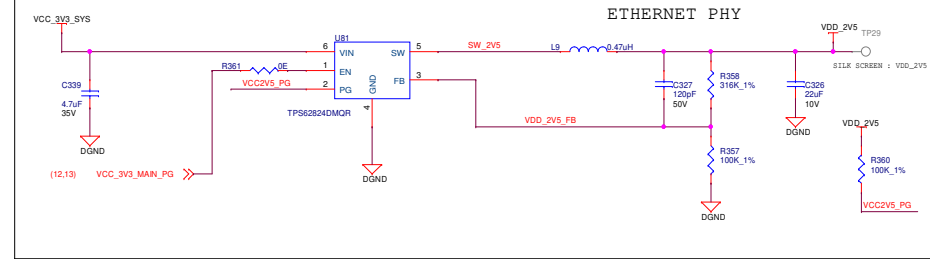
PERIPHERAL POWER SUPPLIES - 1

VinMin = 4.5V
VinMax = 15V
Vout = 5V @ 2A

D-Note :
Add a jumper or 0E (ohm) for isolation or current measurement
Provision can be provided for pre-production board and
can be deleted for production boards as required

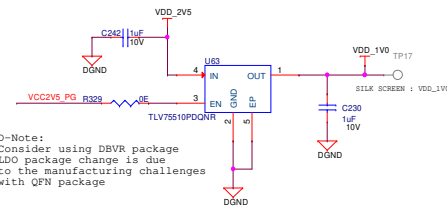


2.5V, 1.0 AMP SUPPLY

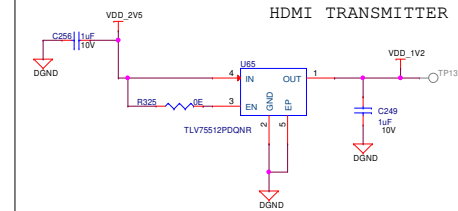


PERIPHERAL SUPPLY - ETHERNET PHY

1.0V, 0.5 AMP SUPPLY



1.2V, 0.5 AMP SUPPLY



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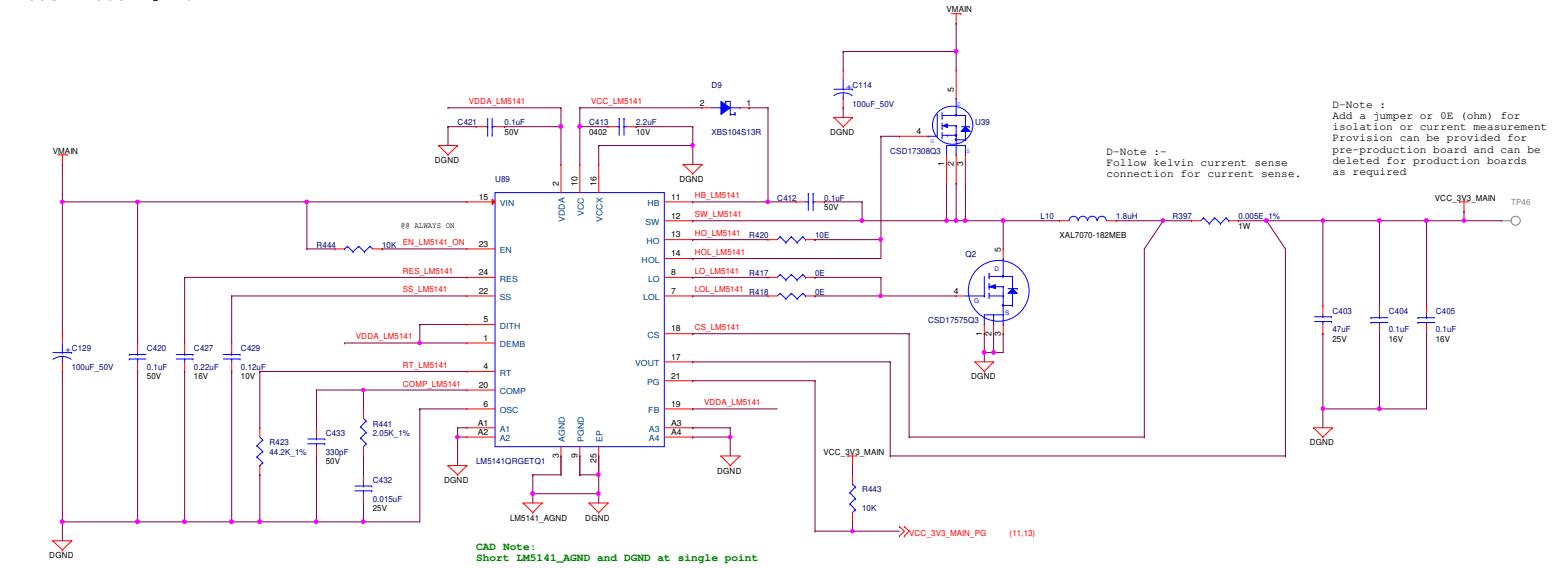
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PERIPHERAL POWER SUPPLIES - 2

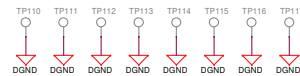
3.3V, 10.0 AMPS SUPPLY

VinMin = 4.5V
VinMax = 15V
Vout = 3.3V @ 10A



(34) ETH_CAN_NH_PREREG >> EN LM5141 ON

GND TEST POINTS



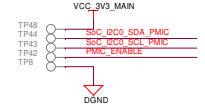
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Title PERIPHERAL POWER SUPPLIES - 2

Size	Rev
C	B
Date: Thursday, June 25, 2026	Sheet 12 of 45

D-Note: Verify the PMIC data sheet or SK schematic for the recommended capacitors for the buck and LDO outputs	D-Note: 0E (ohms) resistor or jumper is added at the PMIC buck output for isolation or testing.
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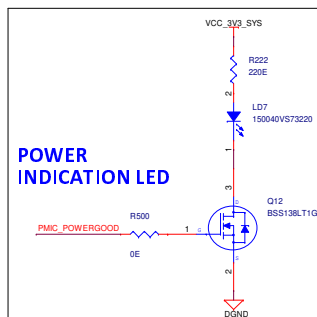
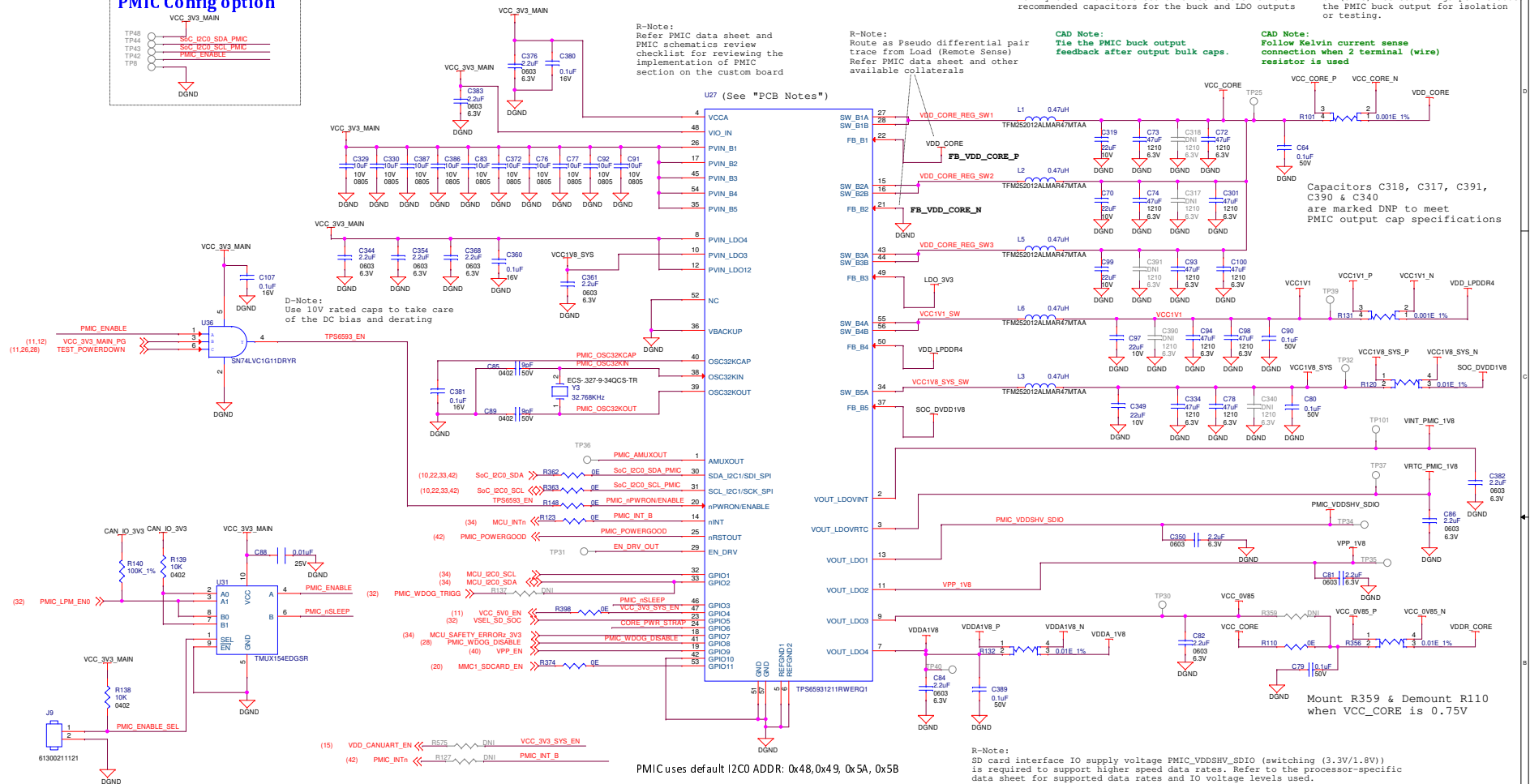


R-Note:
Refer PMIC data sheet and
PMIC schematics review
checklist for reviewing the
implementation of PMIC
section on the custom board

R-Note:
Route as Pseudo differential pair
trace from Load (Remote Sense)
Refer PMIC data sheet and other
available collaterals

CAD Note:
Tie the PMIC buck output
feedback after output bulk caps.

CAD Note:
Follow Kelvin current sense
connection when 2 terminal (wire)
resistor is used



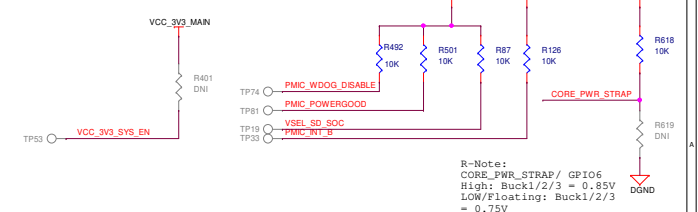
D-Note:
VCC_3V3_SYS_EN
The GPO4 is driven
by the PMIC to hold
the load switch
low during power-up
sequence

D-Note:
VCC_3V3_SYS_EN
The GPO4 is driven
by the PMIC to hold
the load switch
low during power-up
sequence

D-Note:
The Pulldown di

The Pull-down at the Load switch DVDD3V3 supply

D-Note:
Capacitor on the CT pin
is provided for SoC IO supply
slew rate control.
SoC IO supply have slew rate
requirements specified. Refer
processor-specific data sheet



R-Note:
CORE_PWR_STRAP/ GPIO6
High: Buck1/2/3 = 0.85V
LOW/Floating: Buck1/2/3
= 0.75V

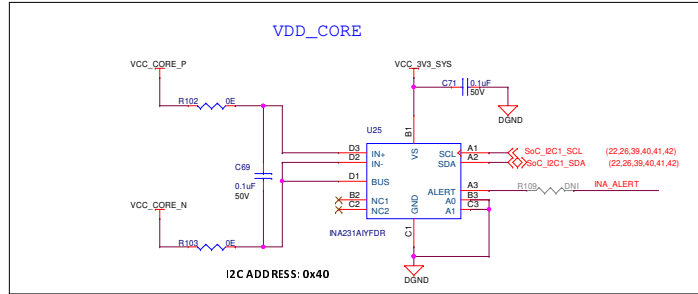
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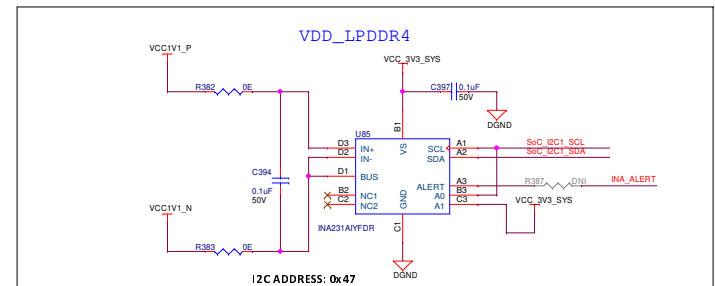
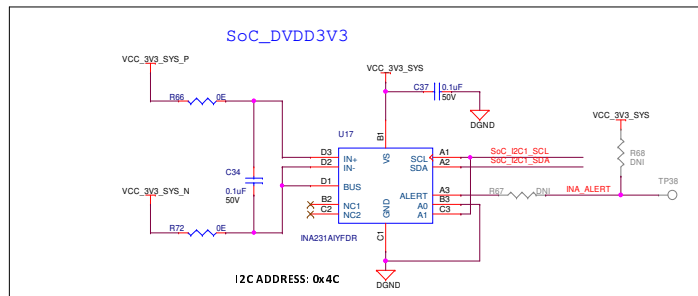
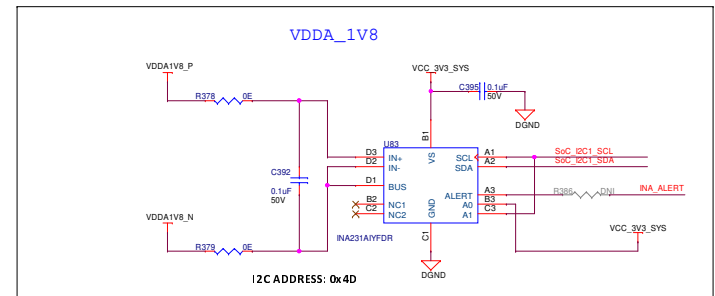
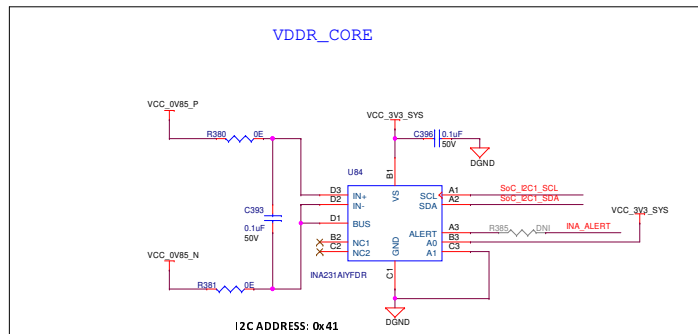
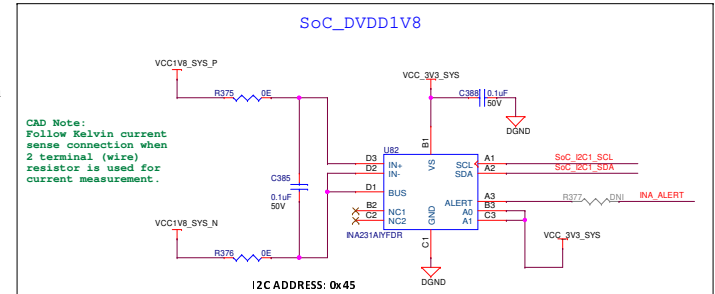
Title SOC POWER SUPPLIES - PMIC BASED WITH SOC CURRENT MEASUREMENT SHUNTS		
Size	PROC135B	Rev
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CURRENT MONITORING DEVICES

D-Note:
Note the supply rail name change across the shunt when optimizing the design (Deleting the current sense resistor).



D-Note:
Provision for 4-wire resistor and current measurement devices have been provided for testing on the EVM board. Implementing current measurement circuit on the custom board is use case and board requirements dependent.



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IIR_HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

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Title CURRENT MONITORING DEVICES

Size	Rev
C	B
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SOC POWER

D-Note:
Recommend implementing the voltage monitoring functionality using VMON_VSYS for early detection of supply failure. It is meant to be a power-fail indicator for the main input (higher) voltage rail that enters the custom board. For example, 5, 12, or 24 volts. The error associated with this monitor would require you to set the threshold of the monitored voltage significantly lower than the nominal voltage (ROC) to avoid a false trigger. Refer to System Power Supply Monitor Design Guidelines section of the processor-specific data sheet.

D-Note:
Changing the core voltage (Dynamically) is not allowed after the SOC has been released from reset. In case the core supply is turned off, the recommendation is to turn off all power rails and ramp them down as per the power-down sequence and wait until all supply rails decay below 300mV before turning on power again.

D-Note:
VDD_CORE and VDDR_CORE are recommended to be connected to the same supply source, so they ramp together when VDD_CORE is operating at 0.85 V.

VCC_3V3_MAIN

C280
10uF
10V

DGND

VDD_CORE

VDDR_CORE

VDD_LPDDR4

VDDA_SYS_MON

VDDA_1V8_FB_OSC

VDD_CANUART

CAN_IO_3V3

VDD_LPDDR4

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

VDD_CORE

VDDR_CORE

VDD_LPDDR4

VDDA_SYS_MON

VDDA_1V8_FB_OSC

VDD_CANUART

CAN_IO_3V3

VDD_LPDDR4

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

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SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

VDD_CORE

VDDR_CORE

VDD_LPDDR4

VDDA_SYS_MON

VDDA_1V8_FB_OSC

VDD_CANUART

CAN_IO_3V3

VDD_LPDDR4

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

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SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

VDD_CORE

VDDR_CORE

VDD_LPDDR4

VDDA_SYS_MON

VDDA_1V8_FB_OSC

VDD_CANUART

CAN_IO_3V3

VDD_LPDDR4

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

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SoC_DVDD3V3

SoC_DVDD1V8

SoC_DVDD3V3

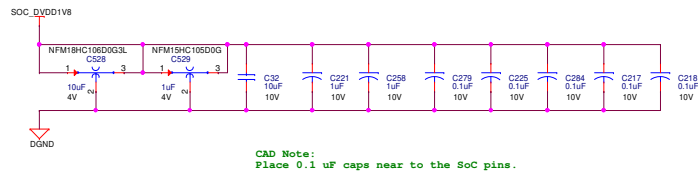
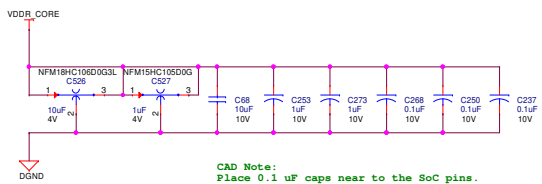
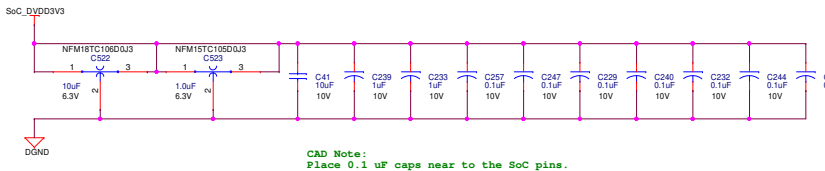
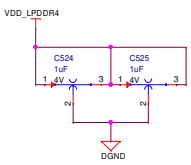
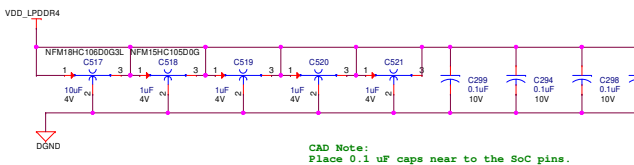
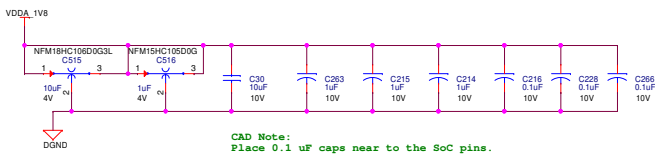
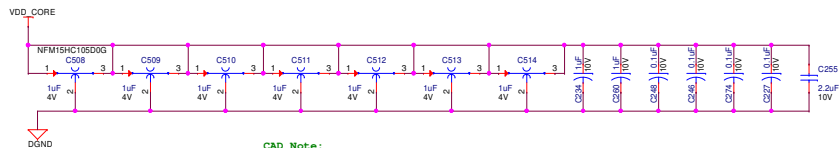
SoC_DVDD1V8

SoC_DVDD3V3

SoC_DVDD1V8

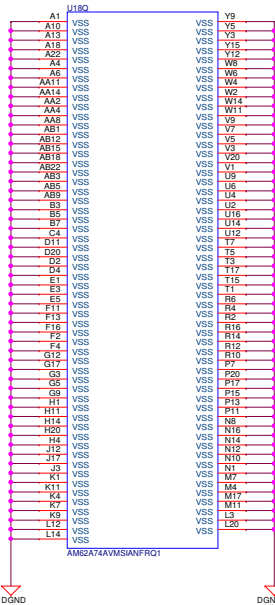
SoC_DVDD3V3

SOC POWER SUPPLIES - DECAPS



SOC VSS

R-Note :
Use of 3 terminal caps optimizes
use of bulk caps and minimizes the
PCB inductance



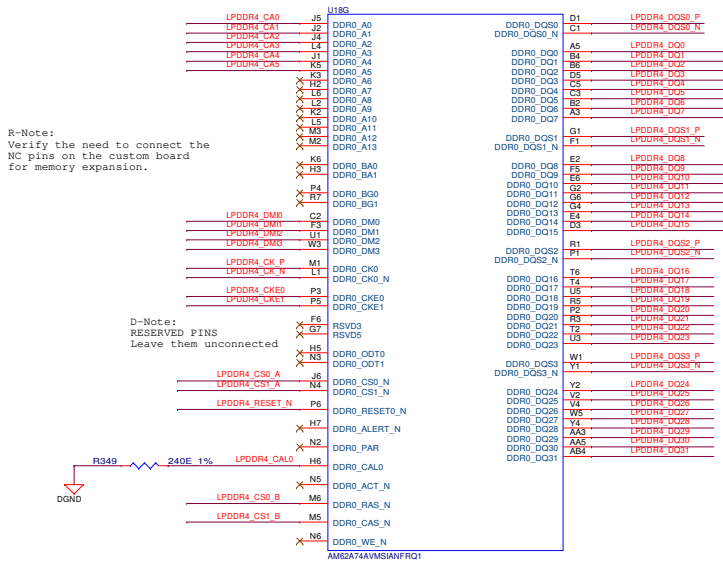
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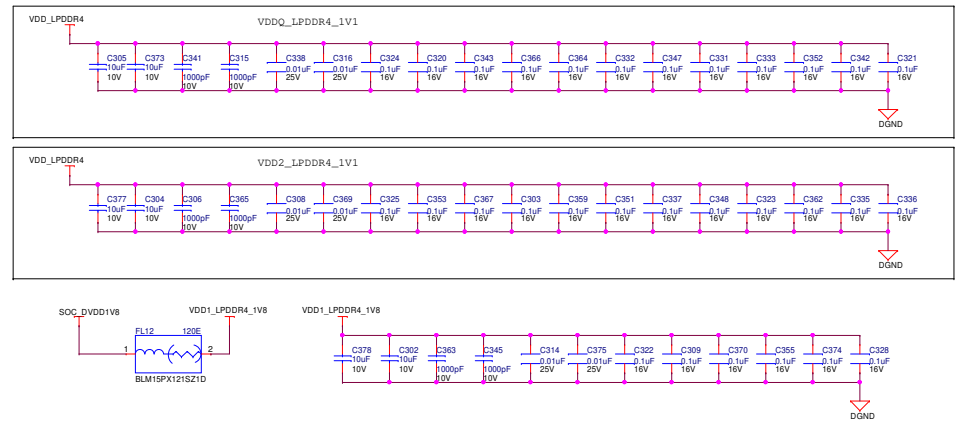
Title SOC POWER SUPPLIES - DECAPS & SOC GROUND VSS

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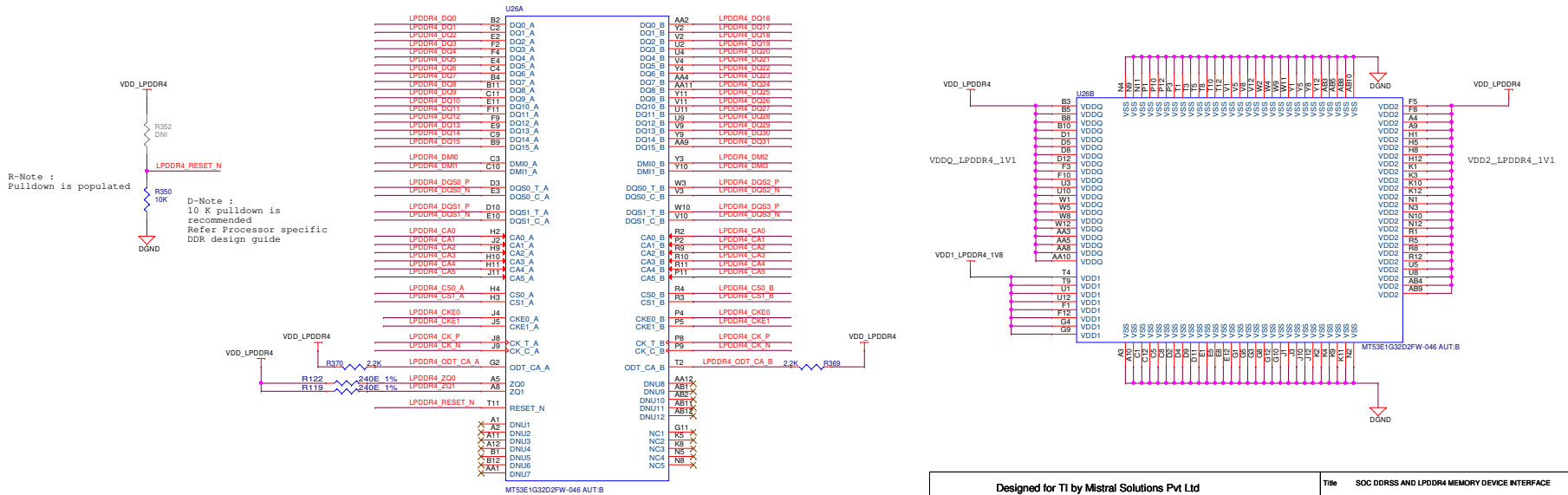
SOC LPDDR4 INTERFACE



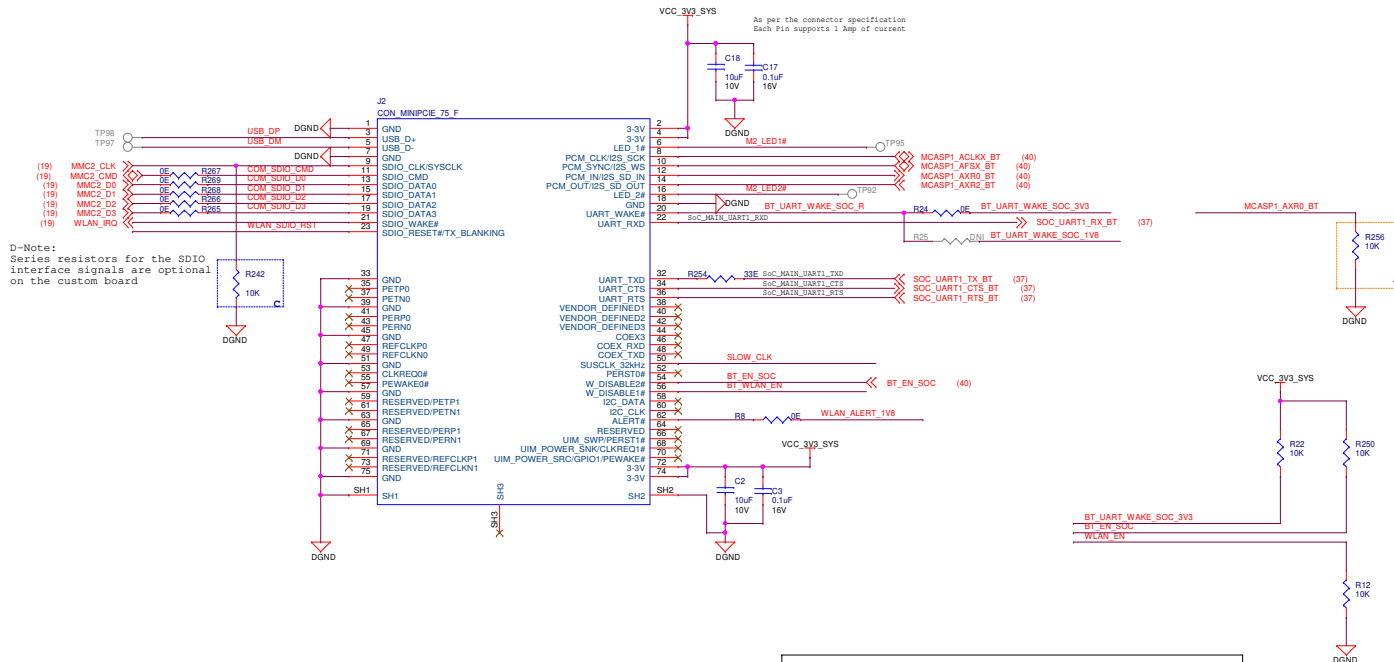
LPDDR4 POWER DECAPS



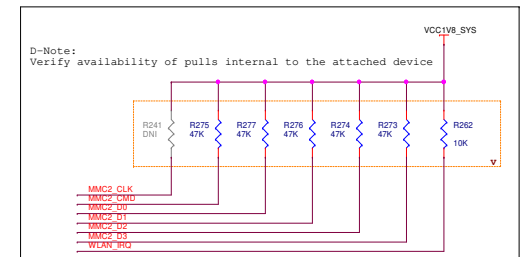
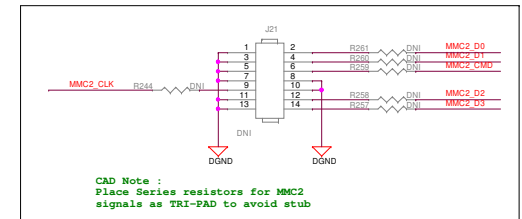
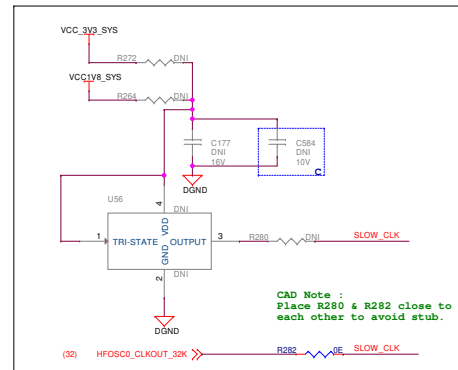
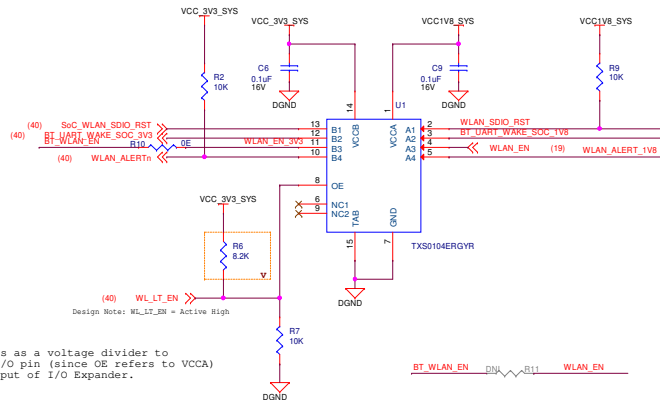
LPDDR4 DEVICE



M.2 INTERFACE - SDIO



M.2 LEVEL TRANSLATOR



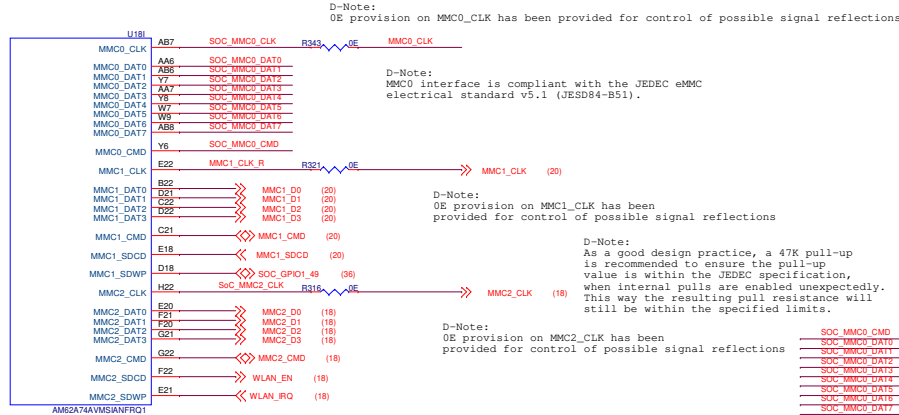
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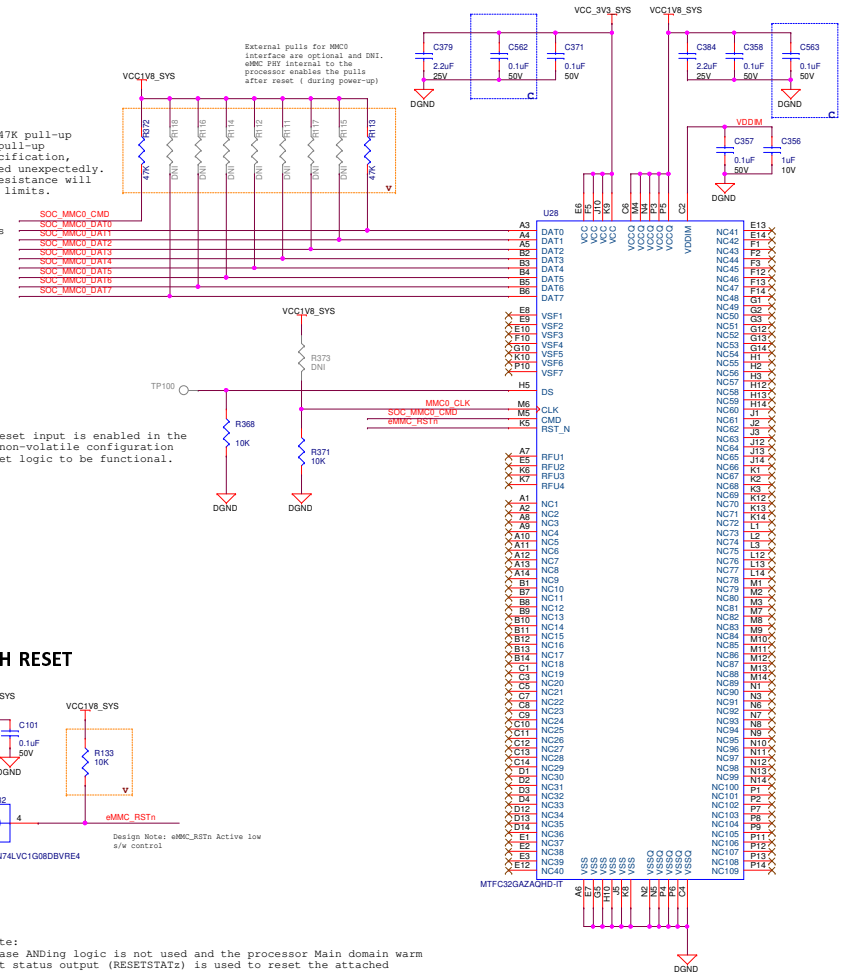
Title M.2 INTERFACE AND CONNECTOR

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SOC - MMC Interface



eMMC FLASH



eMMC FLASH RESET

- D-Note:
- You could eliminate the GPIO option and only use the reset output (warm or cold), where the software forces a warm reset, if the peripheral becomes unresponsive. However, this will reset the entire device rather than trying to recover the specific peripheral without resetting the entire device.
 - The GPIO reset option makes it possible for the software to reset the attached device (eMMC or OSPI or SD card or EPHY) without resetting the entire processor, if there is a case where the peripheral becomes unresponsive.

D-Note:
The GPIO reset option makes it possible for the software to reset the attached device (eMMC or OSPI or SD card or EPHY) without resetting the entire processor, if there is a case where the peripheral becomes unresponsive.

D-Note:
ANDing logic additionally performs level translation. Verify the reset IO level compatibility before optimizing the reset ANDing logic. IO level mismatch can cause residual voltage (supply leakage) and affect PMIC/Soc operation.

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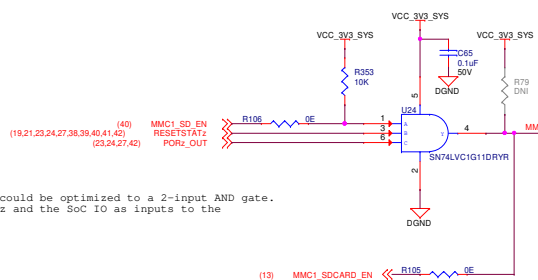


Title SOC MMC0.2 INTERFACE, eMMC FLASH AND eMMC FLASH RESET

Size	PROC136B	Rev
C		B
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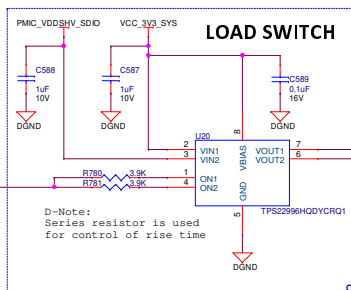
D-Note:
Refer Custom Board Design and Simulation Guidelines for
Processor High Speed Parallel Interfaces
<https://www.ti.com/lit/pdf/sdaa087>

SD CARD LOAD SWITCH EN RESET LOGIC



D-Note:
ANDing logic could be optimized to a 2-input AND gate.
Use RESETSTATz and the SoC IO as inputs to the
ANDing logic.

SD CARD INTERFACE



D-Note:
Series resistor is used
for control of rise time

D-Note:
SD card power control power switch, along with the SD card power switch EN reset logic and the host
switched IO power supply circuit, is required to support UHS-I SD Card which begins communication
using 3.3 V IO signal level which later switches to 1.8 V signal level when changing to a faster
data transfer speed. Cycling power to the SD Card is the only way to put the SD card back into
3.3 V mode since SD Cards do not have a reset pin. The host IO power supply must power off/on and
change voltage at the same time as the SD Card. These circuits and the software driver operating
the signals sourcing these circuits ensure both devices are off or on and are operating at the
same IO voltage at the same time.

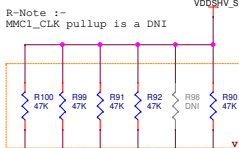
D-Note:
Dual-channel load switch is used
to provide provision to reset the
SD card supply, and dynamically
switched Dual-voltage IO supply
connected to the processor
SD card IO supply for IO group
VDDSRVS and the SD card IO pullups.

D-Note:
For UHS-I SD card support, the
pull-ups are recommended to be
connected to the 3.3V/1.8 V
switched LDO output.

D-Note:
As a good design practice, a 47K pull-up is
recommended to ensure the pull-up value is within
the SD card specification, when internal pulls are
enabled unexpectedly. This way the resulting pull
resistance will still be within the specified limits.

(19) MMC1_D0
(19) MMC1_D1
(19) MMC1_D2
(19) MMC1_D3
(19) MMC1_CLK
(19) MMC1_CMD
(19) MMC1_SDCD

D-Note:
Add a 100R series resistor for the
MMC1_SDCD signal. Processor
IO SDCD directly connects to
ground when SD card is inserted



R-Note :-
MMC1_CLK pullup is a DNI

V

V

V

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CAD Note:
ESD diode Place near the SD card connector.

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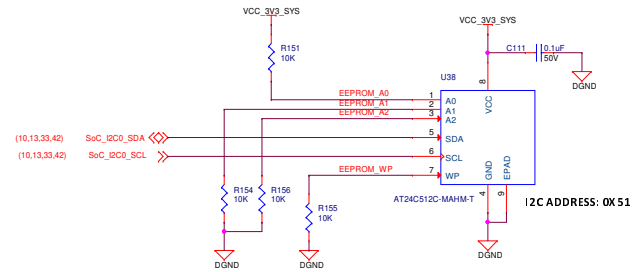


TiSD CARD - LOAD SWITCH, LOAD SWITCH RESET LOGIC AND DATA INTERFACE

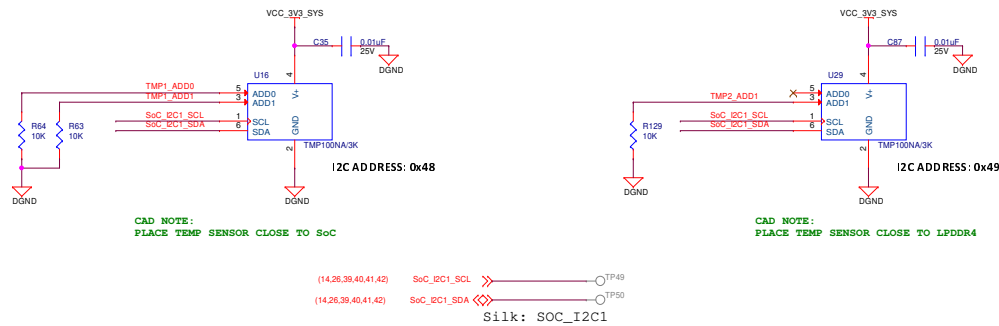
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BOARD ID EEPROM



DIGITAL TEMPERATURE SENSORS



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Title BOARD ID EEPROM & DIGITAL TEMPERATURE SENSORS

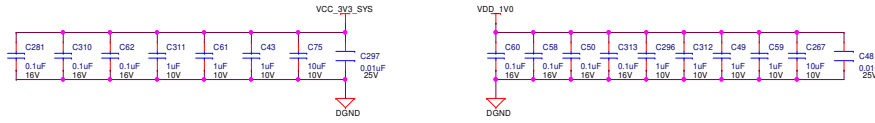
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C	B
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CPSW3G RGMII 1 - ETHERNET PHY

D-Note :-
The caps and values used are as per the EPHY data sheet recommendations.

D-Note:
OK to use 0402 package for 1uF cap to match the 10uF bulk cap package size

D-Note:
Refer to DP83867ERGZ-R-EVM when using Discrete LAN Transformer Module and RJ45 connector.



D-Note:
Refer Custom Board Design and Simulation Guidelines for Processor High Speed Parallel Interfaces
<https://www.ti.com/lit/pdf/sdaa087>

D-Note :-
Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

R-Note :-
Ferrite is DNI

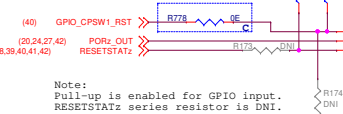
RJ45 CONNECTOR WITH INTEGRATED MAGNETICS

D-Note:
Provide provision for series resistor based on EPHY internal impedance control support for RDX signals near to the EPHY RDX pins.

D-Note:
Allowed amplitude for XI clock input is 1.8V irrespective of the IO supply used. Use a capacitor divider when the clock applied is 3.3V.

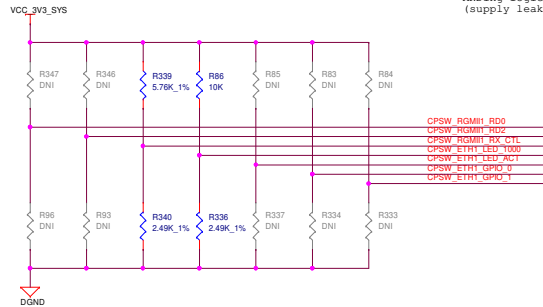


D-Note:
ANDING logic could be optimized to a 2-input AND gate. Use RESETSTATz (or PORz_OUT) and the SoC IO as inputs to the ANDING logic.

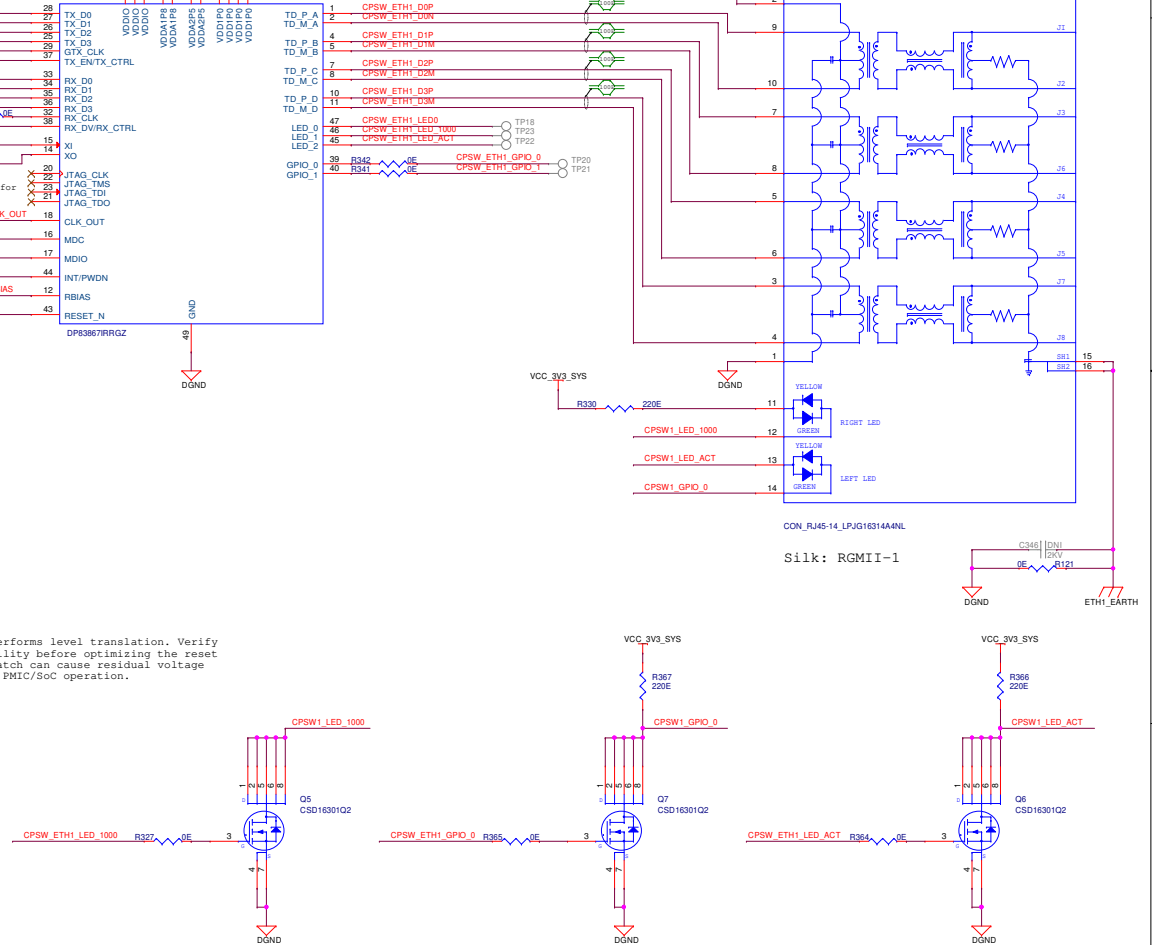


Note:
Pull-up is enabled for GPIO input. RESETSTATz series resistor is DNI.

D-Note:
ANDING logic additionally performs level translation. Verify the reset IO level compatibility before optimizing the reset ANDING logic. IO level mismatch can cause residual voltage (supply leakage) and affect PMIC/SoC operation.



PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns



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Title CPSW3G RGMII_1 ETHERNET PHY

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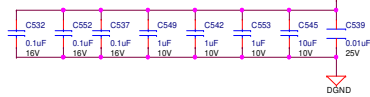
CPSW3G RGMII 2 - ETHERNET PHY

D-Note :-

The caps and values used are as per the EPHY data sheet recommendations.

D-Note:

OK to use 0402 package for 1uF cap to match the 10uF bulk cap package size



D-Note:

Refer Custom Board Design and Simulation Guidelines for Processor High Speed Parallel Interfaces
<https://www.ti.com/lit/pdf/sdaa087>

D-Note:

Provide provision for series resistor based on EPHY internal impedance control support for Rdx signals near to the EPHY Rdx pins.

D-Note:

Allowed amplitude for XI clock input is 1.8V irrespective of the IO supply used. Use a capacitor divider when the clock applied is 3.3V.

(23.32) SoC_RGMII_MDC

(23.32) SoC_RGMII_MDIO

D-Note:

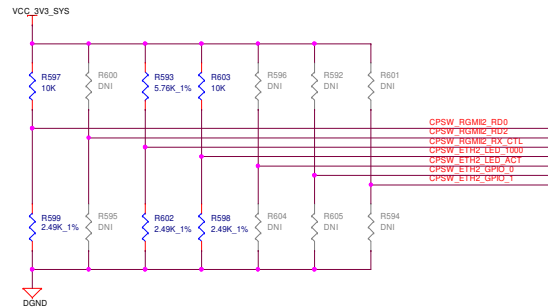
ANDING logic could be optimized to a 2-input AND gate. Use RESETSTATz (or PORz_OUT) and the SoC IO as inputs to the ANDING logic.

Note:

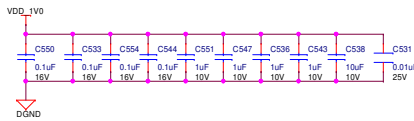
Pull-up is enabled for GPIO input. RESETSTATz series resistor is DNI.

D-Note:

ANDING logic additionally performs level translation. Verify the reset IO level compatibility before optimizing the reset ANDING logic. IO level mismatch can cause residual voltage (supply leakage) and affect PMIC/SoC operation.



PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns



D-Note:

Refer to DP83867ERG2-R-EVM when using Discrete LAN Transformer Module and RJ45 connector.

R-Note:-
Ferrite is DNI

RJ45 CONNECTOR WITH INTEGRATED MAGNETICS

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

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Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

D-Note :-

Verify the power sequence requirements for Two-Supply Configuration and Three-Supply Configuration

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TEXAS
INSTRUMENTS

MISTRAL

Title CPSW3G RGMII 2 ETHERNET PHY

Size PROC135B

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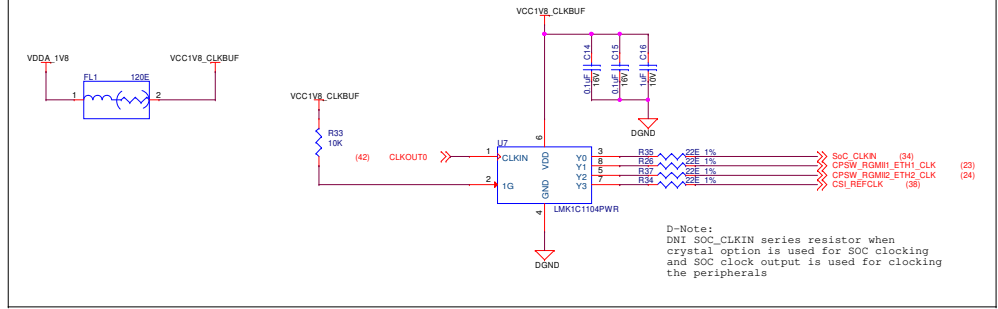
B

SOC MAC INTERFACE

D-Note:
Series Resistor provision is provided for the TDx MAC
interface signals near to the processor pins for control of
possible signal reflections



CLOCK BUFFER FOR SOC AND ETHERNET PHYS

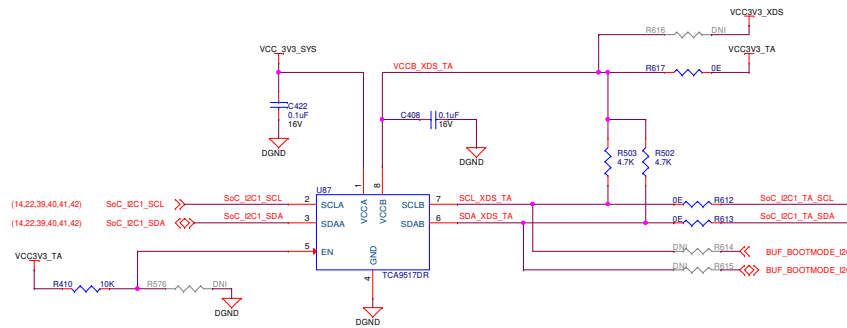


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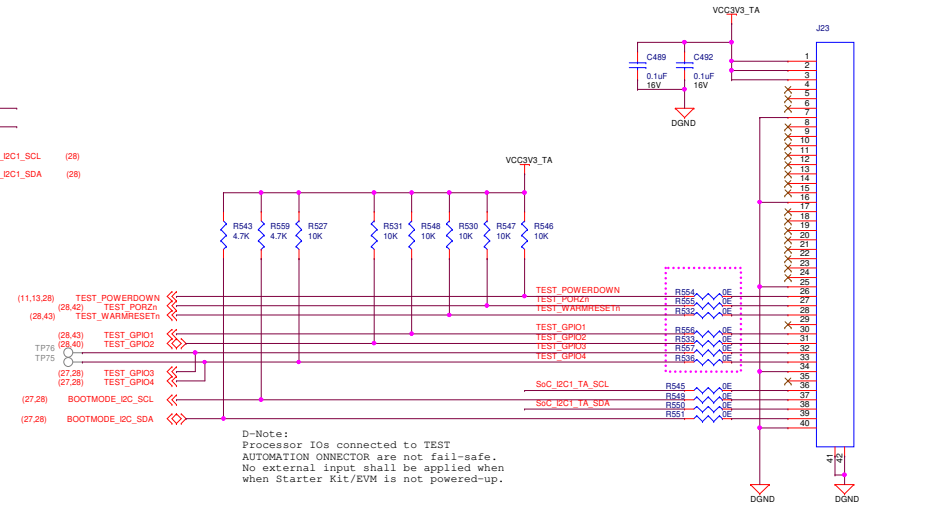
Title		SOC MAC INTERFACE, CLOCK BUFFER FOR SOC AND ETHERNET PHYS	
Size	PROC136B	Rev	B
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I2C BUS BUFFER



XDS110 Configuration
Mount : R614, R615, R616
Demount: R612, R613, R617

40-PIN TEST AUTOMATION HEADER

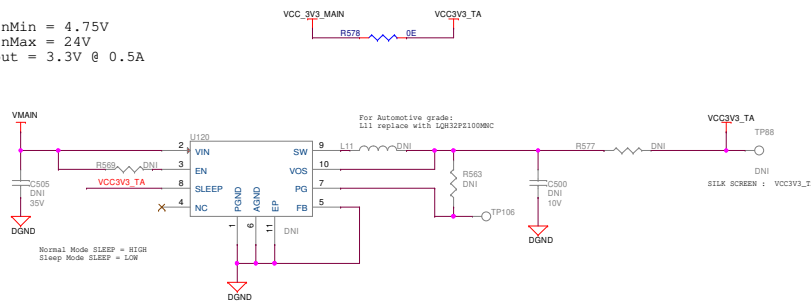


D-Note:
Processor I/Os connected to TEST
AUTOMATION CONNECTOR are not fail-safe.
No external input shall be applied when
when Starter Kit/EVM is not powered-up.

CON_FLEX_40X1_FH12A-40S-0.5SH
Silk: AUTOMATION HDR

TEST AUTOMATION BOARD POWER

VinMin = 4.75V
VinMax = 24V
Vout = 3.3V @ 0.5A



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SOC_GPIO1_23 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

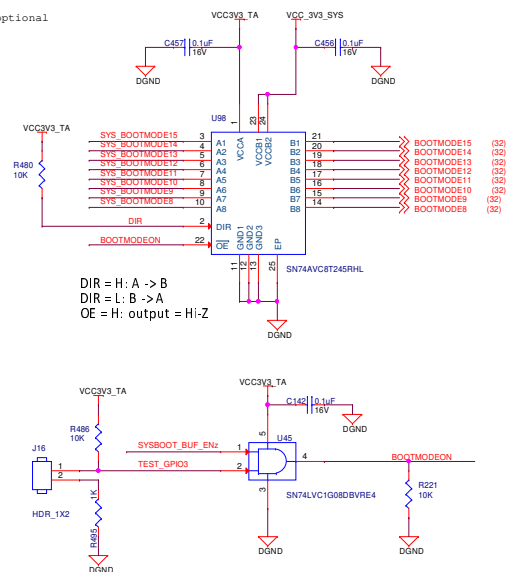
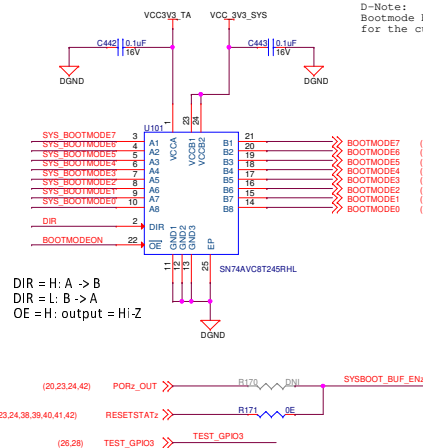
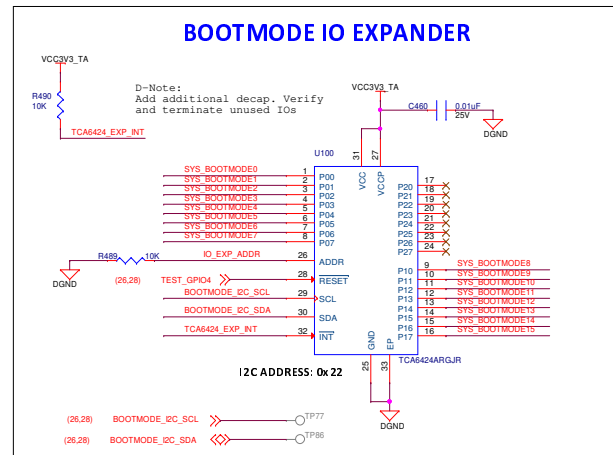
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Title TEST AUTOMATION

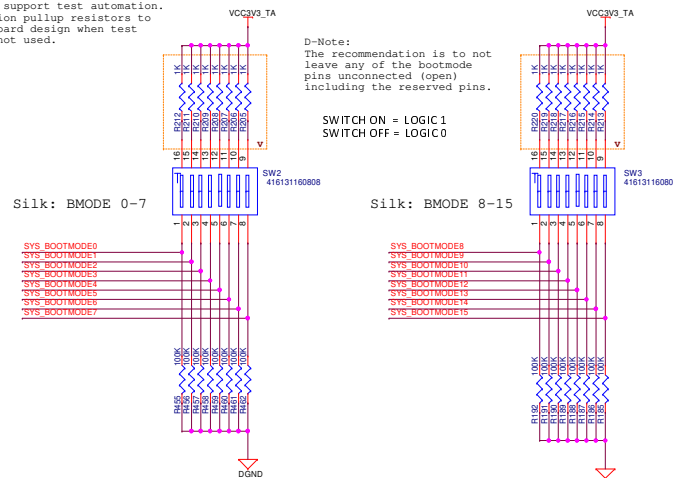
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BOOT MODE BUFFERS



BOOTMODE CONFIGURATION RESISTORS AND BOOTMODE SWITCHES

D-Note:
VCC3V3_TA supply is used to support test automation. Connect bootmode configuration pullup resistors to SoC_DVDD3V3 on the custom board design when test automation and buffers are not used.



D-Note:
1. Dip switches are used on the SK for ease of configuration. DIP switches are optional on the custom board. A pull-up or pull-down resistor can be used to set the bootmode configuration. Provide provisions for pull-up and pull-down resistors for the bootmode pins that have configuration capability.
2. When DIP switches are used on the custom board, provision for an external ESD protection may be required if the DIP switches are expected to be configured in an uncontrolled ESD environment.
3. When DIP switches are used, reduce the resistor values used for the divider to 47k and 2K (1K) ohms to optimize the current draw in case the I/Os are used for alternate functions (output).

BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. ETHERNET
6. USB0 DFU
7. USB0 MS

FAQs FOR REFERENCE TO IMPLEMENT BOOTMODE CONFIGURATION (WITH BUFFER OR WITHOUT BUFFER):

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1391522/faq-am625-am623-am644x-am243x-am62a-am62p-am62d-q1-am62l---bootmode-implementation-without-buffers>

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1414148/faq-am625-am623-am644x-am243x-am62a-am62p-am62d-q1-am62l---bootmode-implementation-with-buffers>

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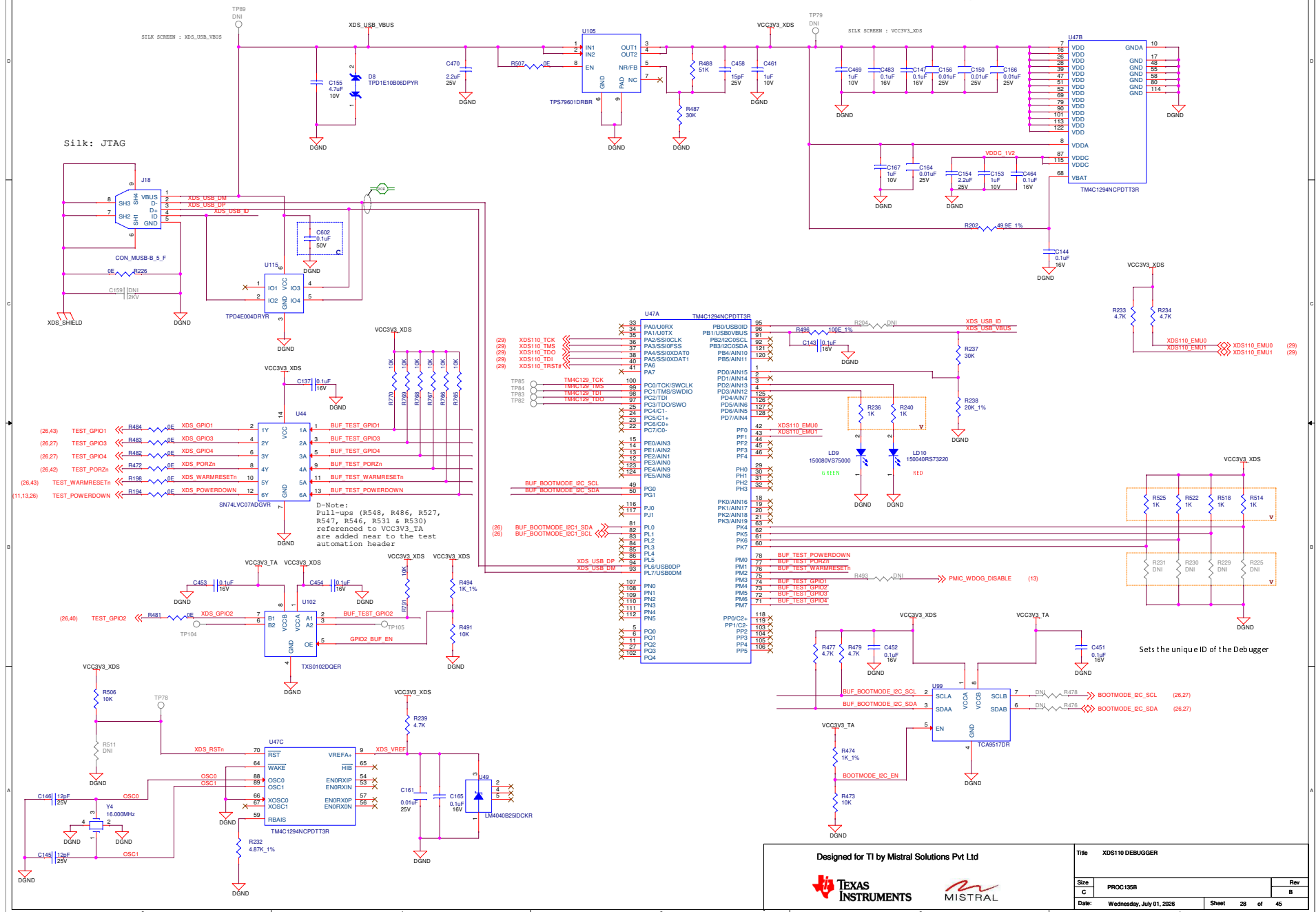


The BOOTMODE CONFIGURATION BUFFERS, RESISTOR DIVIDERS AND SWITCHES

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XDS110 DEBUGGER

D-Note:
Please follow SK-AM62P-LP
implementations for latest
updates on XDS110



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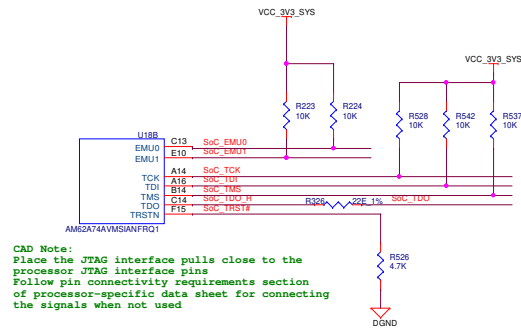
Title	XDS110 DEBUGGER
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Size	2200-1500
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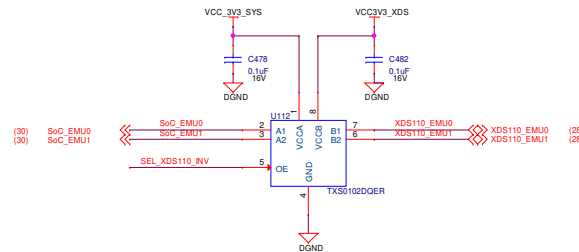
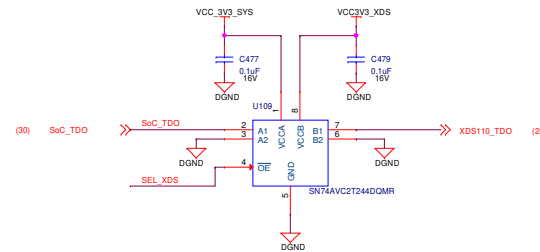
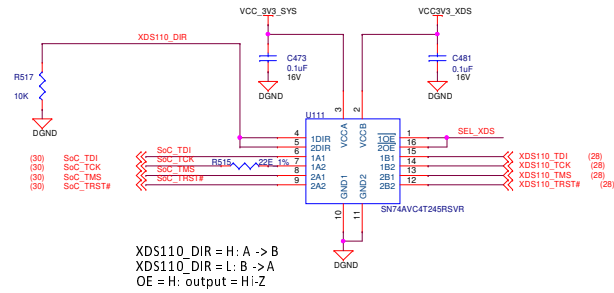
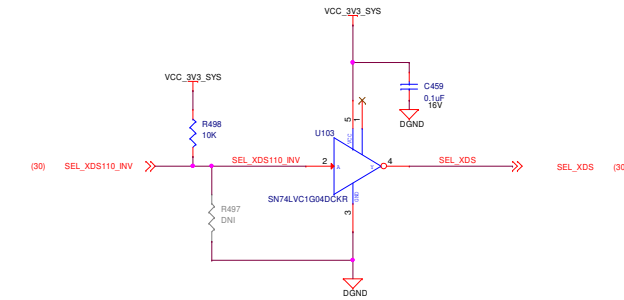
Date: Wednesday, July 01, 2026

Rev

SOC JTAG INTERFACE



BUFFER XDS110



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Title SOC JTAG INTERFACE & JTAG BUFFERS

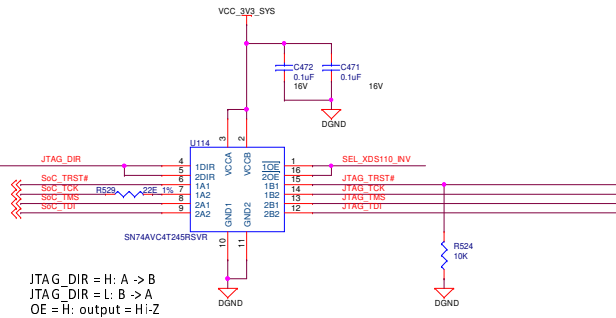
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CTI20 JTAG BUFFERS

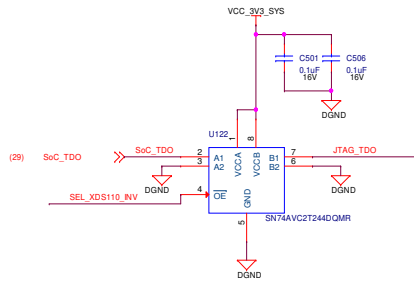
D-Note:
Add provision for external ESD protection to provide system level ESD protection,
when an external connector is used for debugging. Follow the Pin Connectivity
Requirements table for connecting the required pulls for the SoC JTAG interface.
Add test points and external ESD protection, when JTAG connector is not used.

JTAG 20 PIN cTI CONNECTOR

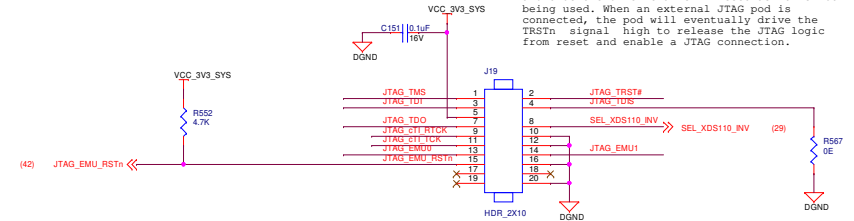
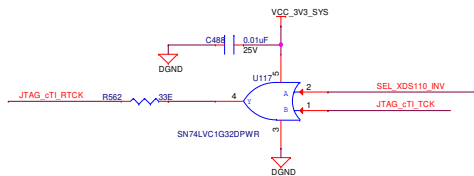
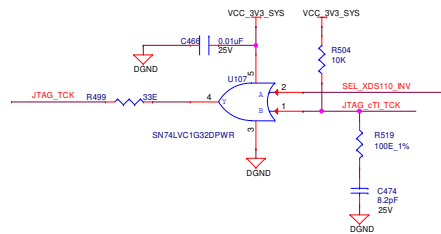
D-Note:
TRSTn is the reset to the processor JTAG logic.
For normal processor operation, this is pulled low,
and thus the JTAG remains in reset as it is not
being used. When an external JTAG pod is
connected, the pod will eventually drive the
TRSTn signal high to release the JTAG logic
from reset and enable a JTAG connection.



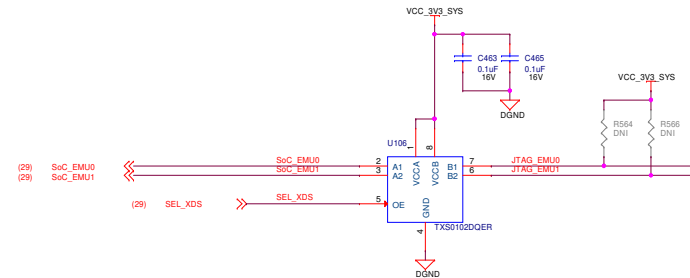
CAD Note:
Buffers U114 and U122 need to be placed closer to the cTI - 20 pin connector J19
to reduce the stub length of the JTAG signals.



JTAG CLOCK BUFFER



Silk: cTI



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Title JTAG 20 PIN cTI CONNECTOR AND BUFFERS

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D-Note :-
Follow SK-AM62P-LP for latest
FT4232 implementations



D-Note:
Connect PMIC_LPM_EN0 signal from SOC to PMIC EN through a pullup placed near the PMIC input pin through a 0E (ohm) series resistor for isolation. DNI the series resistor when partialIO functionality is not implemented. If the application will not use any of the AM62 low power modes, then the PMIC_LPM_EN0 does not have to be connected to the PMIC.

BOOTMODE PINS

Signals from Bootmode buffer

Pin	Signal	Function
RA5_1	BOOTMODE0	PR0 PRU0 GP00
RA5_2	BOOTMODE1	PR0 PRU0 GP01
RA5_3	BOOTMODE2	PR0 PRU0 GP02
RA5_4	BOOTMODE3	PR0 PRU0 GP03
RA6_1	BOOTMODE7	PR0 PRU0 GP07
RA6_2	BOOTMODE6	PR0 PRU0 GP06
RA6_3	BOOTMODE5	PR0 PRU0 GP05
RA6_4	BOOTMODE4	PR0 PRU0 GP04
RA3_1	BOOTMODE8	SiC_VOUT0 DATA16
RA3_2	BOOTMODE9	SiC_VOUT0 DATA17
RA3_3	BOOTMODE10	SiC_VOUT0 DATA18
RA3_4	BOOTMODE11	SiC_VOUT0 DATA19
RA4_1	BOOTMODE12	SiC_VOUT0 DATA20
RA4_2	BOOTMODE13	SiC_VOUT0 DATA21
RA4_3	BOOTMODE14	SiC_VOUT0 DATA22
RA4_4	BOOTMODE15	SiC_VOUT0 DATA23

D-Note

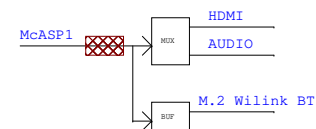
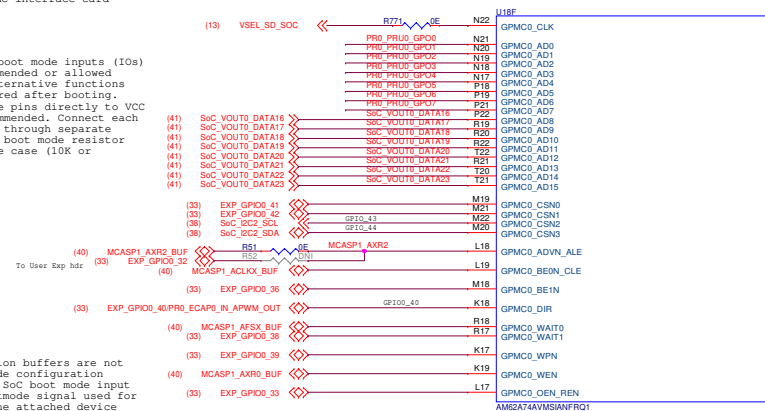
R-Note:
Series resistors are used to isolate the SoC BOOTMODE input control logic after the BOOTMODE inputs value is latched.

D-Note:
WKUP_LFOSCO has limited
use case. Populate OE (ohms) to
ground XI when LFOSCO is
not used. Refer to the
SoC datasheet.

D-Note:
Shorting of multiple boot mode inputs (IOs) together is not recommended or allowed since the IOs have alternative functions that could be configured after booting. Shorting the boot mode pins directly to VCC or ground is not recommended. Connect each of the boot mode pins through separate resistors. Choose the boot mode resistor value based on the use case (10K or similar).

D-Note:
When the boot mode isolation buffers are not used, connect the boot mode configuration resistors directly to the SoC boot mode input pins. Connect the SoC bootmode signal used for alternative function to the attached device through 0E (ohms) for isolation or testing.

SOC GPMC INTERFACE



D-Note:
SoC IO buffers are off during reset. A parallel pull is recommended near
to the attached device input that is being driven by the SoC IO (input does not float).



D-Note:
Any SoC IO that has a trace connected but not being driven actively needs to be connected to an external pull. When adding pull is not feasible, ensure that the traces are routed away from noisy signals.

D-Note:
Processor I/Os connected to USER EXPANSION CONNECTOR
are not fail-safe. No external input shall be applied
when the starter kit is not powered-up.

D-Note:
Add-on boards are expected to take care of the connection polarity for for the UART signals (cross-over of RX and TX or other signals).



The Starter Kit shall not be powered through the 5V0 or 3V3 supply pins on the 40-pin User Expansion Connector (the pins are output supply).

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62P Starter Kit is not powered.

5V supply on User Expansion Connector can source 150mA max.

3V3 supply on User Expansion Connector can source 500mA max.



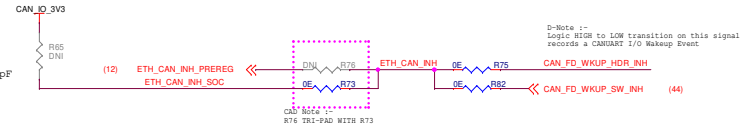
Title										USER EXPANSION CONNECTOR									
Size		PROC135B																Rev	
C																		B	
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D-Note:
MCU_I2C0
A pull-up is recommended for open-drain output type I2C interfaces, irrespective of the IO usage or IO configuration. Refer to the Pin Connectivity Requirements table of the SoC datasheet.

D-Note:
Open-drain output type buffer I2C interfaces have slew rate requirement specified when pulled to 3.3 V. An RC is used to limit the slew rate

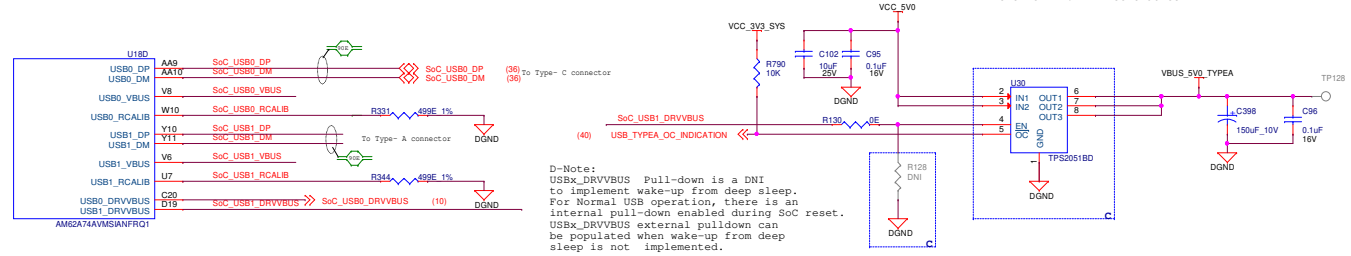
D-Note:
SoC IO buffers are off during reset.
A parallel pull is recommended near to the attached device input that is being driven by the SoC IO (input does not float).

D-Note:
Y1 recommended crystal part number:
Change the part number of Y1 to ABM11W-25.0000MHz-S-D1X-T3
Update DNI caps C305 and C303 to 12 pF

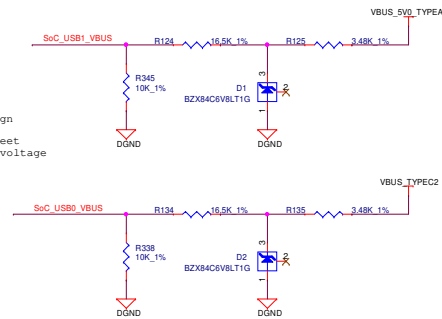


USB1 - USB 2.0 TYPE-A

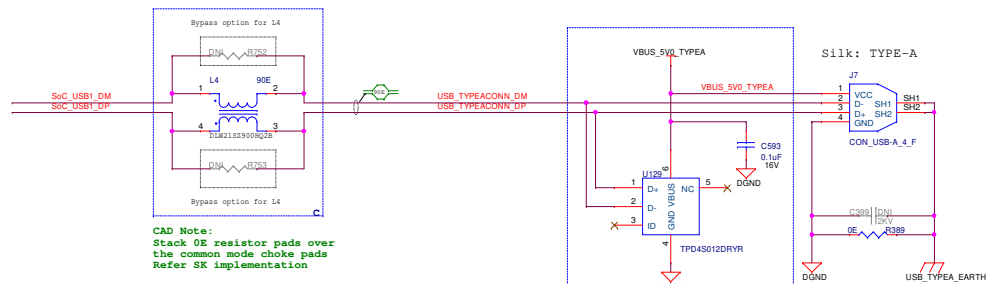
D-Note :-
Use power switch with OC indication
Example TPS2051
Connect to a SOC IO for OC detection
Refer SK-AM62P-LP schematics



D-Note:
VBUS divider and VBUS supply connection to processor USB0:1 interface:
Connection of supply to USBx_VBUS pin is optional when USB interface
is configured as Host



D-Note:
Refer to the USB VBUS Design
Guidelines section of the
processor-specific data sheet
for implementing the VBUS voltage

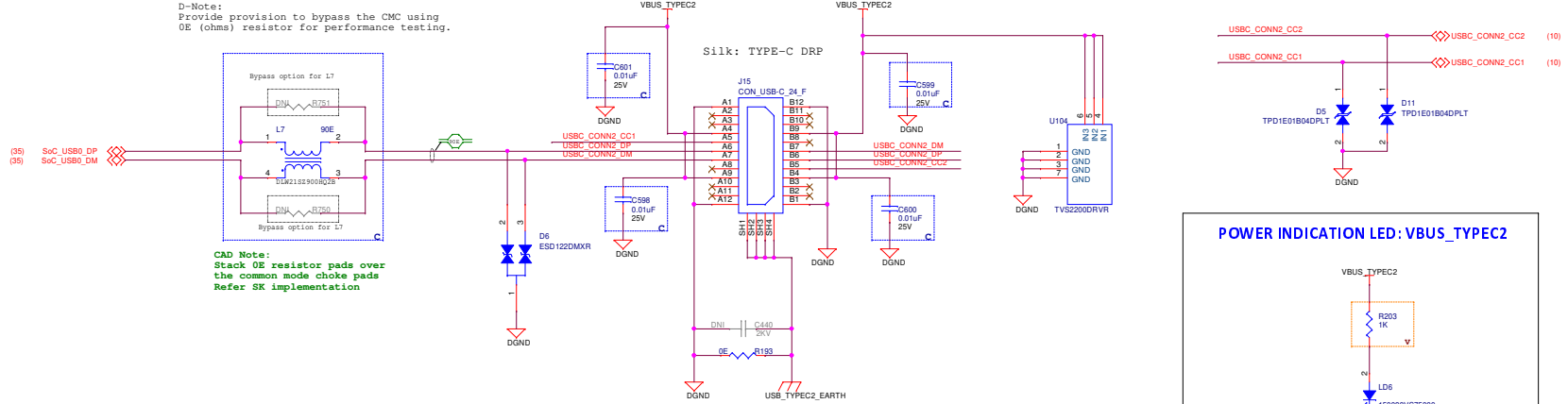


D-Note:
Provision to bypass the CMC using 0E (ohms) resistor provided
for testing the USB interface performance

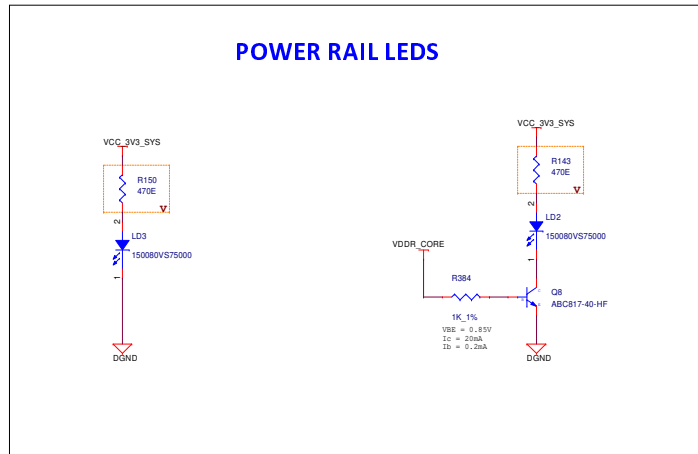
USB0 TYPE-C DRP

D-Note:
Refer to the SK/EVM user's guide for the recommended power adapters.
Using the recommended adapter is recommended for proper functioning of SK/EVM
Reference Document:
EVM User's Guide : <https://www.ti.com/lit/pdf/SPRUJ40>
Reference section : Power Requirement

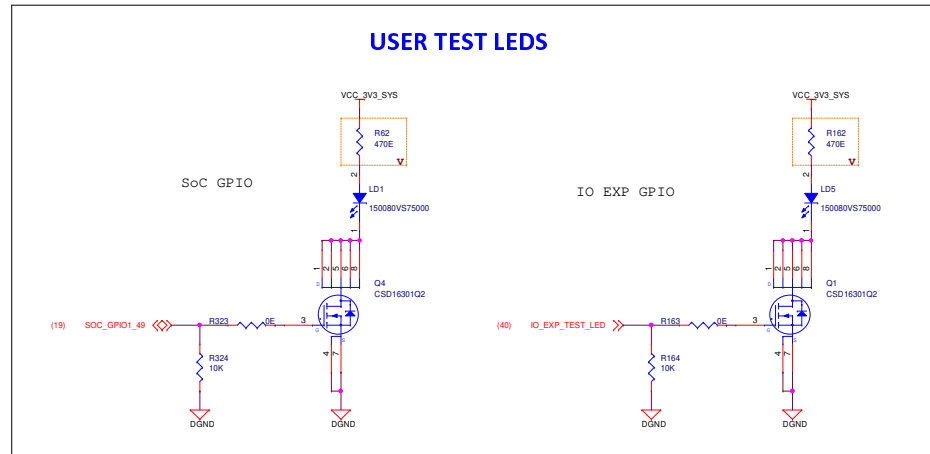
D-Note:
Provide provision to bypass the CMC using
0E (ohms) resistor for performance testing.



POWER RAIL LEDS



USER TEST LEDS



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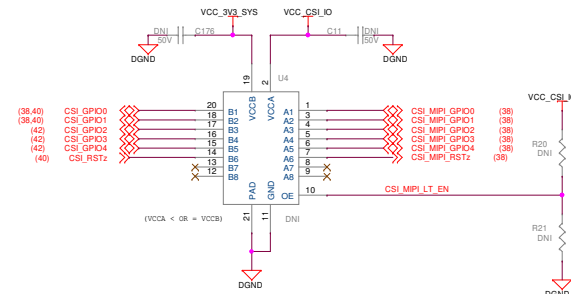
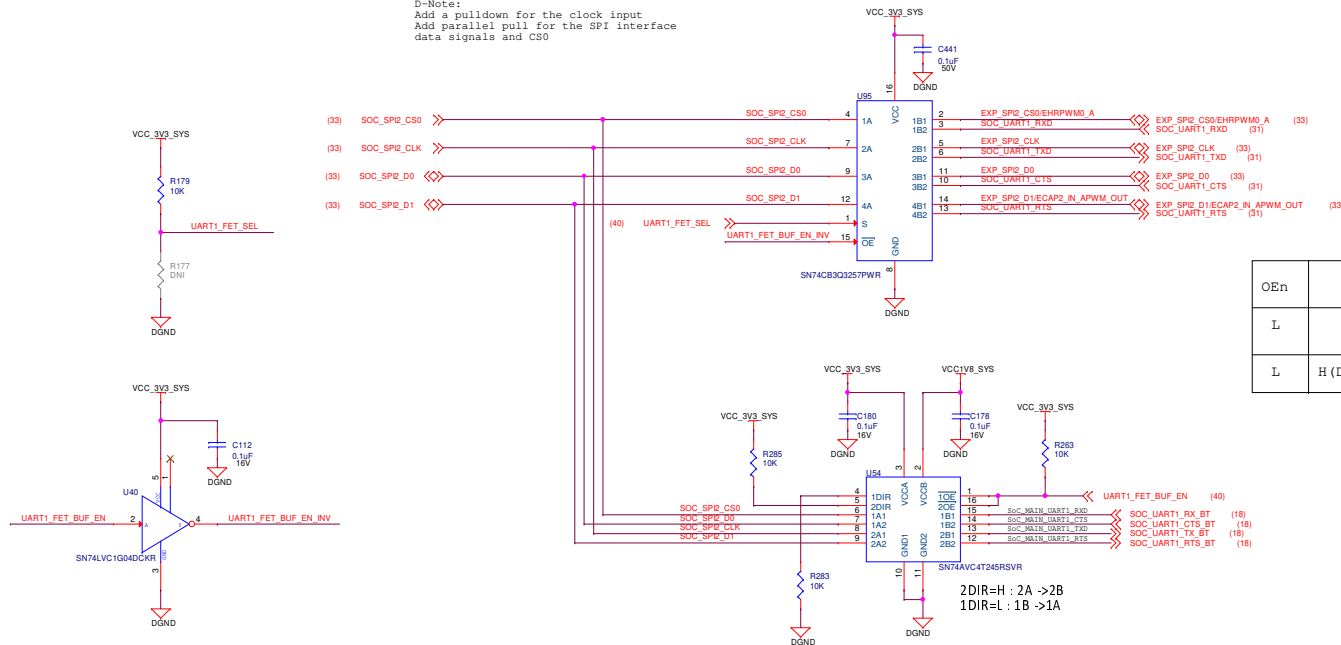


Title USB0 TYPE-C DRP & USER TEST LEDS

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SoC UART1 FET SWITCH & BUFFER

D-Note:
Add a pulldown for the clock input
Add parallel pull for the SPI interface
data signals and CS0



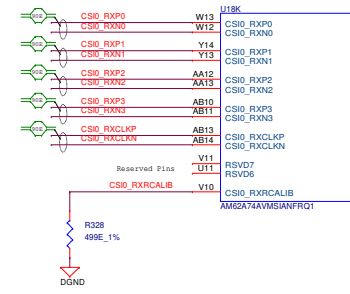
Designed for TI by Mistral Solutions Pvt Ltd



Title SoC UART1 FET SWITCH & BUFFER

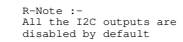
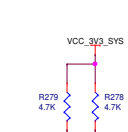
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SOC CSI INTERFACE



MUX_SEL_2	FUNCTION
LOW	INPUT<--A port [CSI-2 Connector - J1]
HIGH	INPUT<--B port [Flex Camera Connector - J20] (default)

(40)



Title	SOC CSI INTERFACE, BIDIRECTIONAL PASSIVE SWITCH AND CAMERA CONNECTOR
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Size		Rev	
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AUDIO CODEC

Silk: LINE IN

D-Note:
Add a pull-down of 10k near to the clock input.

D-Note:
Add pulls for McASP interface IOs that can float.

(40) MCASP1_ACLKX_AUD
(40) MCASP1_AFSX_AUD
(40) MCASP1_AXRQ_AUD
(40) MCASP1_AXRZ_AUD
(14,22,26,40,41,42) SOC_BC1_SDA
(14,22,26,40,41,42) SOC_BC1_SCL

TLV320AIC3106RGZT
I2C ADDRESS: 0x1B

AUDIO CODEC RESET

(40) GPIO_AUD_RSTn
(19,20,21,23,24,27,38,40,41,42) RESETSTATz

SN74LVC1G08DBVR4

CODEC I2C ADDRESS SELECTION

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B

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TEXAS INSTRUMENTS

MISTRAL

Title: AUDIO CODEC

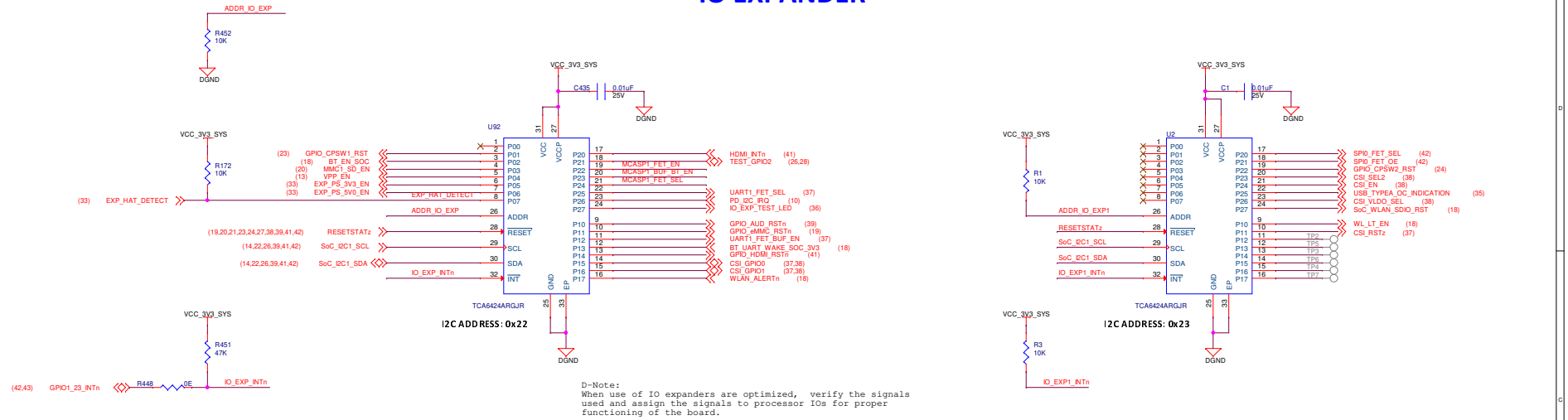
Size: C
Proc: 135B

Date: Wednesday, July 01, 2026

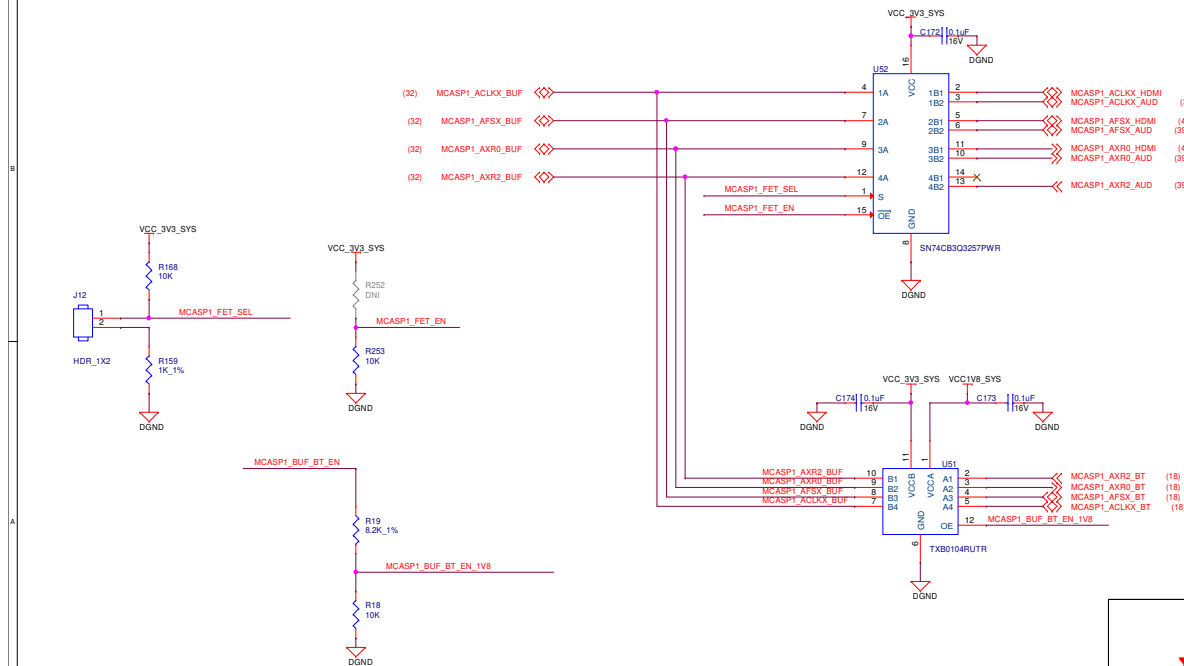
Sheet: 39 of 45

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IO EXPANDER



McASP1 FET SWITCH & BUFFER



OEn	SEL	INPUT/OUTPUT An	
L	H (DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

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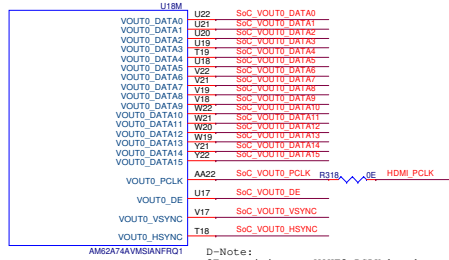
Title IO EXPANDER AND MCASP1 FET SWITCH AND BUFFER

Size	PROC136B	Rev	B
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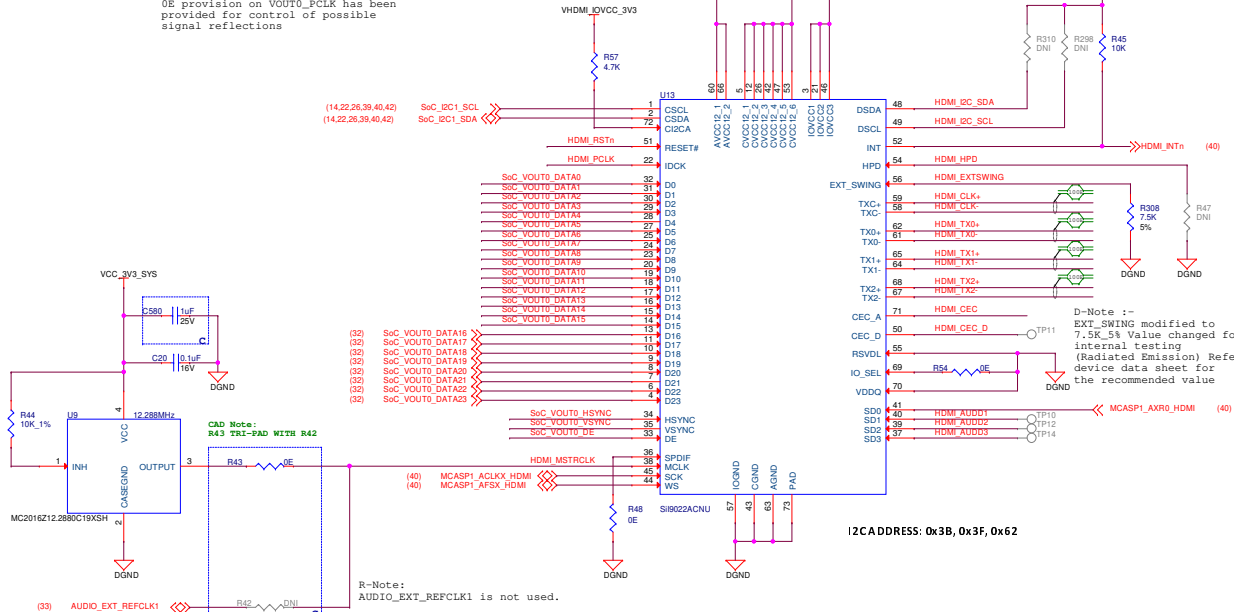
HDMI INTERFACE

R-Note :-
Verify the implementation with
the device manufacturer

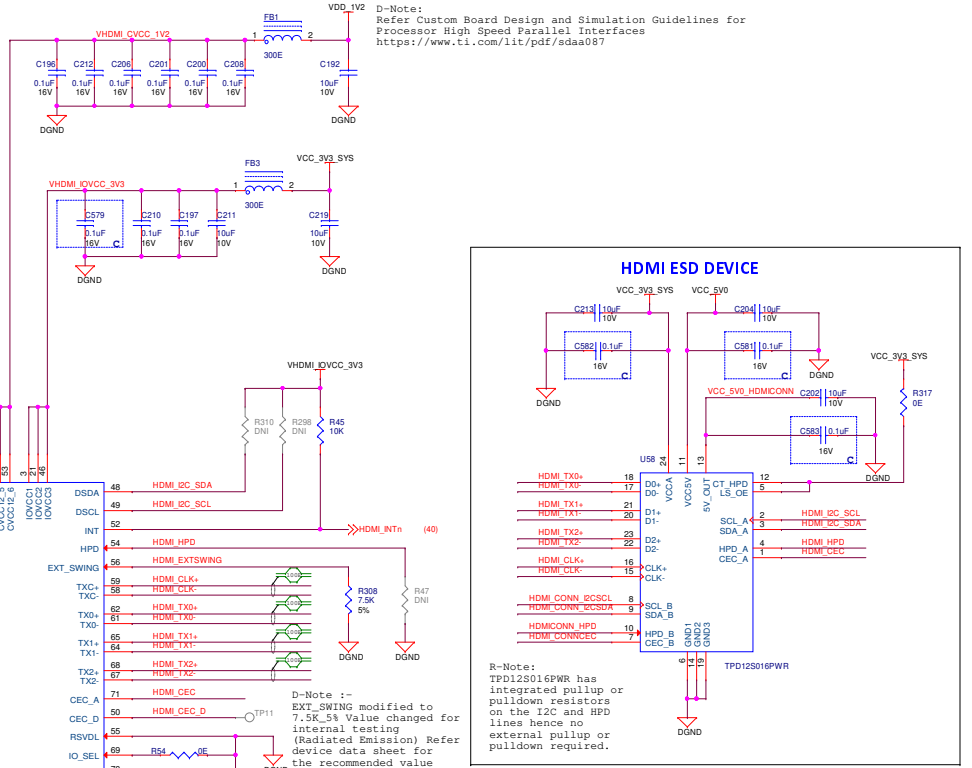
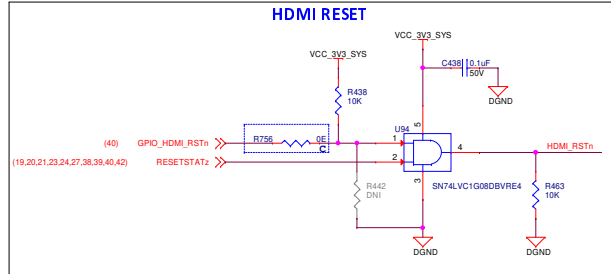
SOC - VIDEO OUTPUT INTERFACE



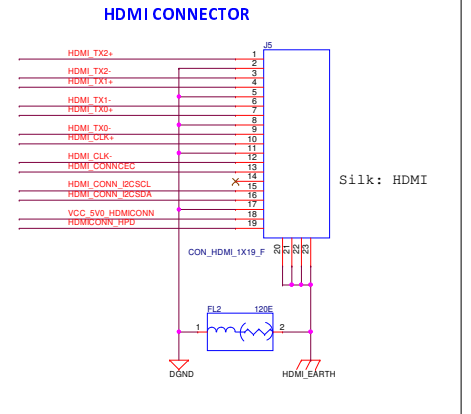
D-Note:
OE provision on VOUT0_PCLK has been
provided for control of possible
signal reflections



HDMI RESET



HDMI CONNECTOR



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Title	SOC DPI INTERFACE, DPI TO HDMI TRANSMITTER INTERFACE
-------	--

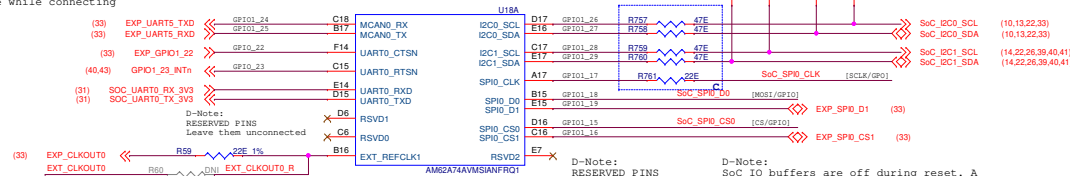
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D-Note :-
The TXD and RXD net names for UART are reverse with respect to MCAN (Refer pin attributes section of the data sheet)
Take note while connecting

D-Note:
Open-drain output type buffer I2C interfaces have slow rate requirement specified when pulled to 3.3 V. An RC can be used to limit the slew rate

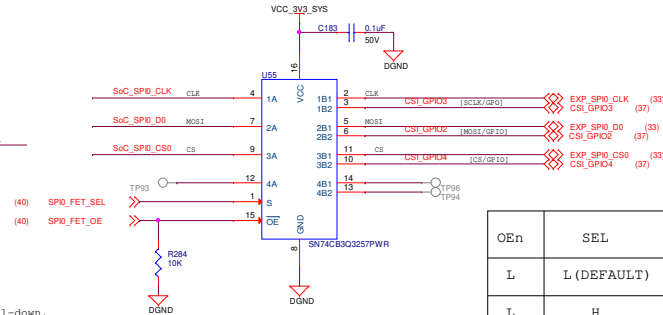
D-Note:
I2C0, I2C1 Emulated Open Drain output type I2C interface. A 47k series resistor is added to control the fall time
Note the exceptions related to emulated open drain output type I2C interface in the processor-specific data sheet

SOC - GENERAL



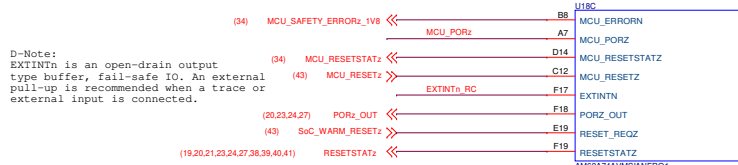
D-Note:
EXT_REPCLK1 configured as CLKOUT0:
A clock signal should always be connected point-to-point. When connecting CLKOUT to more than one (multiple) attached devices clock input, consider using a clock fanout buffer such as LMK1C110n (n = 2:4 or more, buffer with one input and multiple outputs)

SoC SPI0 FET SWITCH



D-Note:
Provide provision for a pull-down. Populate when an attached device is connected. Refer to the SoC datasheet for Pin Connectivity Requirements.

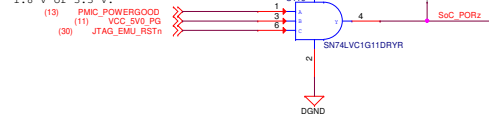
SOC - RESETS - COLD AND WARM



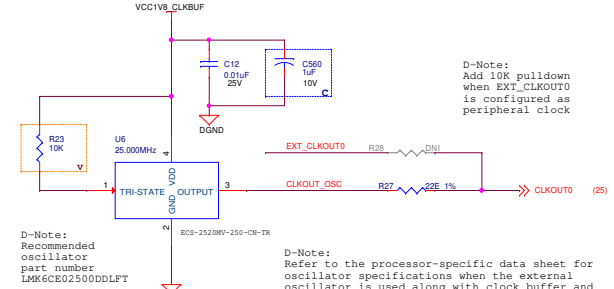
D-Note:
EXTINTn is an open-drain output type buffer, fail-safe IO. An external pull-up is recommended when a trace or external input is connected.

D-Note:
Open-drain output type IO EXTINTn has slow rate limit specified, when pulled to a 3.3 V supply. An RC is added to limit the slew rate

D-Note:
MCU_PORZ input has slow rate requirements specified. Lesser the slew, the better when PMIC_POWERGOOD is connected as MCU_PORZ input. Adjust the PMIC_POWERGOOD pull-up to minimize the slew (100-200 ns) when using an open drain output. MCU_PORZ is fail-safe and 3.3 V tolerant. Therefore, you can pull the MCU_PORZ signal to either 1.8 V or 3.3 V.



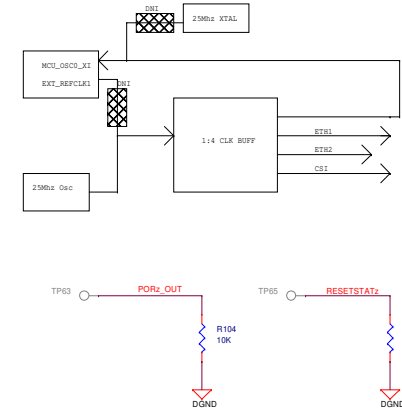
OSCILLATOR



D-Note:
Add 10K pulldown when EXT_CLKOUT0 is configured as peripheral clock

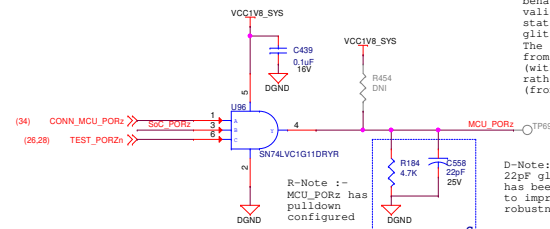
D-Note:
Recommended oscillator part number LMK6CE02500DDLFT

D-Note:
Refer to the processor-specific data sheet for oscillator specifications when the external oscillator is used along with clock buffer and also when the oscillator is directly connected as processor clock input.



D-Note:
Pull-down resistor on PORZ_OUT and RESETSTATZ is provided to hold the attached device in reset condition during SoC reset and power-up.

MCU POWER ON RESET



D-Note:
Not connecting a valid MCU_PORZ input could cause unpredictable and probably random behavior. Since the processor is not getting a valid reset, internal circuits would be in random states. Slow rising reset signal could cause glitches internal to the processor reset circuit. The recommendation is to connect the output from the logic gate or a discrete buffer (with fast rise time) as input to MCU_PORZ, rather than a slow rising open-drain output (from PMIC of similar sources).

D-Note:
22pF glitch filter has been added to improve EMC robustness

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Title SOC RESETS AND IOs, AND EXTERNAL LVCMOS CLOCK (OSCILLATOR)

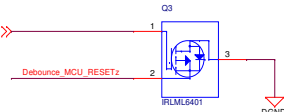
Size PROC135B Rev B

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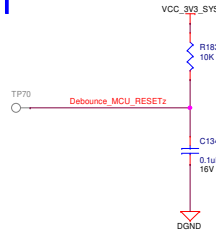
SOC RESETS - COLD AND WARM

SOC MCU WARM RESET

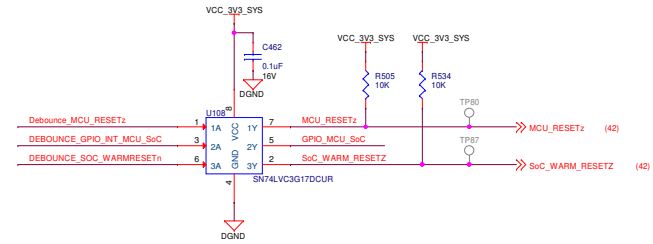
(34) CONN_MCU_RESETz



D-Note :-
DNI Q3 and C134
Refer to Errata
12407- RESET: MCU_RESETSTATz
unreliable when MCU_RESETz is
asserted low



DEBOUNCE CIRCUIT



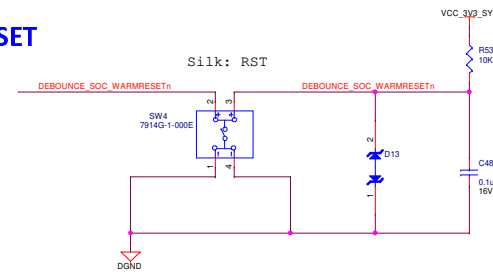
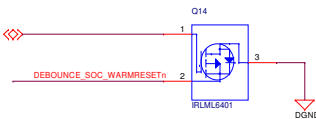
D-Note:
1VCMOS inputs have slew rate requirements specified. A
Schmitt trigger based debouncing logic is used for the slow
ramp warm reset inputs. Debounce circuit is recommended when
push button or RC is used.

GPIO_MCU_SoC R512 4.7K GPIO1_23_INTn (40,42)

GPIO_MCU_SoC R572 DNI GPIO_MCU_SoC_INTn (34)

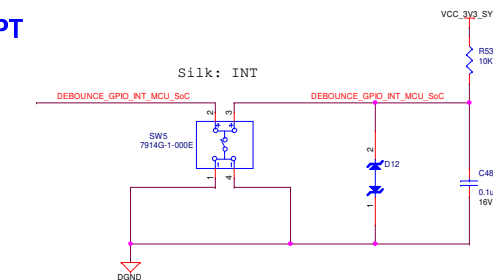
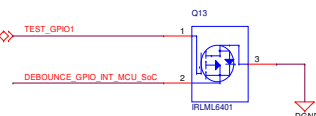
SOC WARM RESET

(26,28) TEST_WARMRESETn



USER INTERRUPT

(26,28) TEST_GPIO1



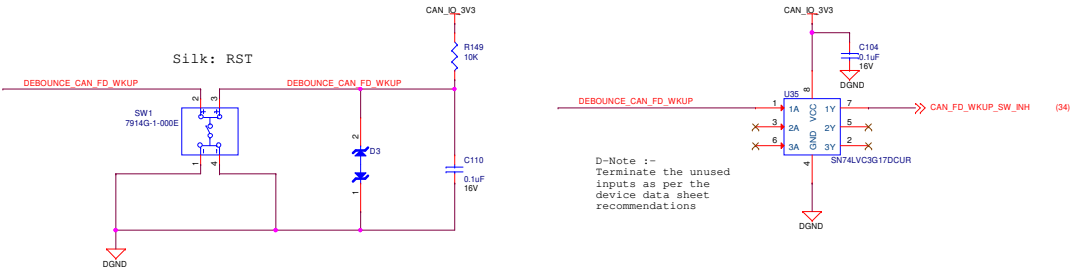
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Title SOC RESETS - COLD AND WARM

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CAN-FD FAST WAKE UP SW



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Title EXTERNAL SWITCH FOR CAN FD WKUP

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MOUNTING HARDWARE

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

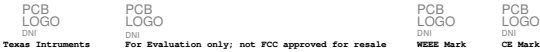
BARE PCB



AM62A SOCKET



LOGOs



JUMPERS



FIDUCIALS



LABELS



SCREW & WASHER FOR PCIe M.2



D-Note :-
Refer STRAP CONFIGURATION OF
ETHERNET PHYS page from
SK-AM64B schematics

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Title ASSEMBLY NOTES AND MOUNTING HARDWARE

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