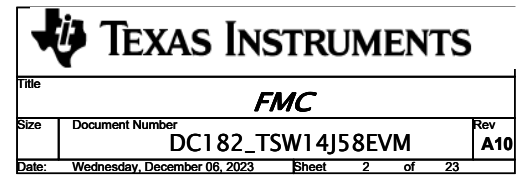
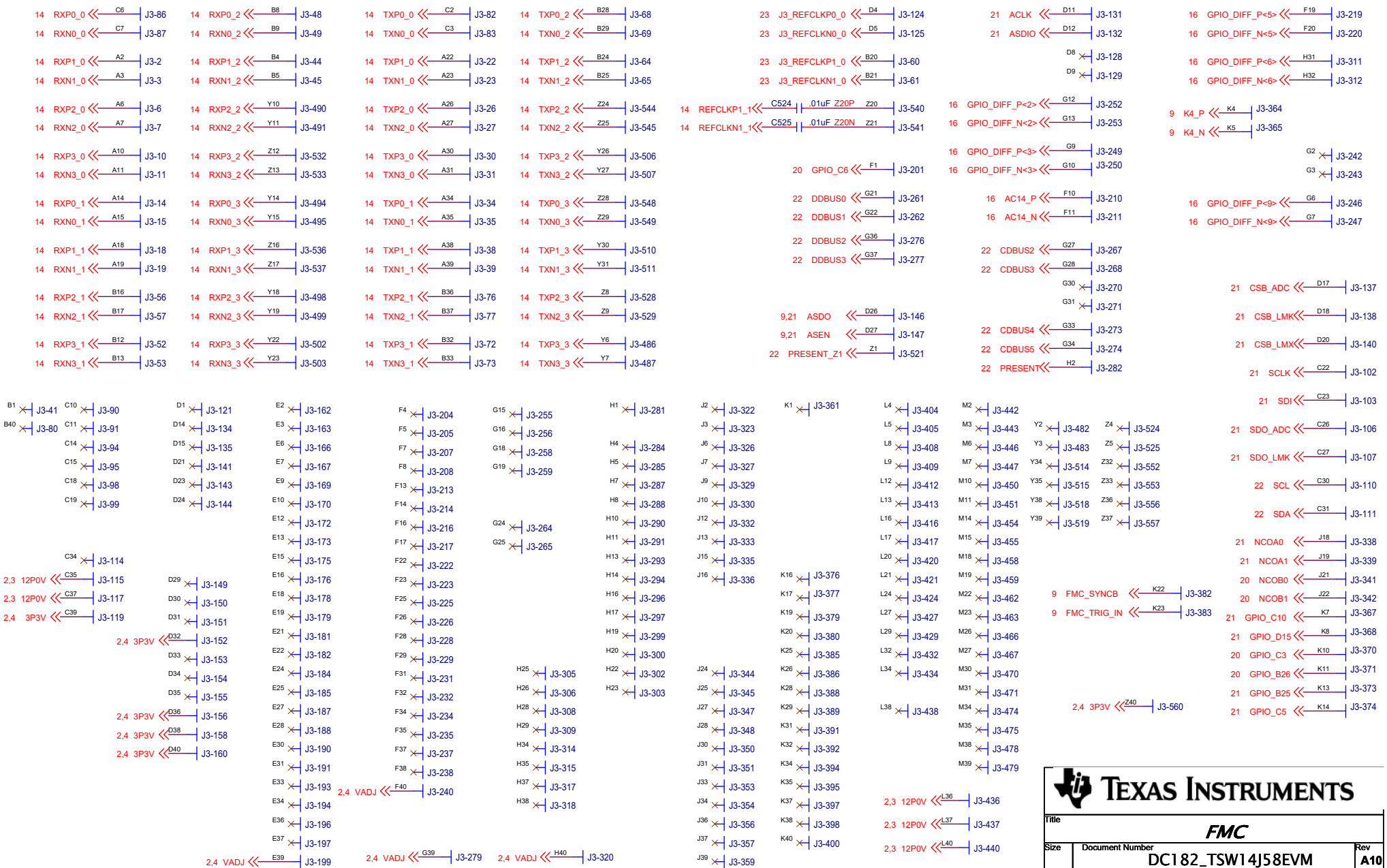
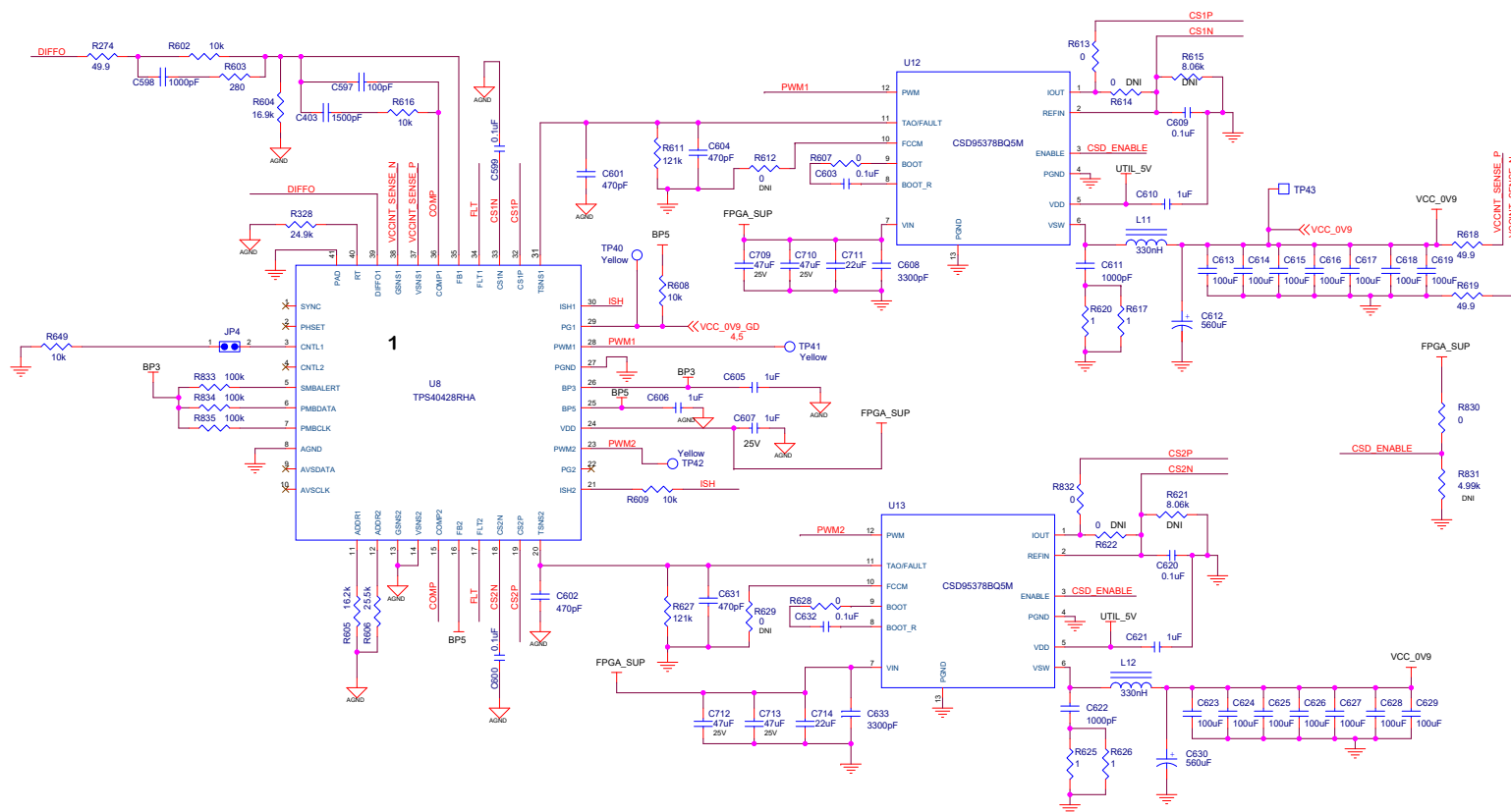
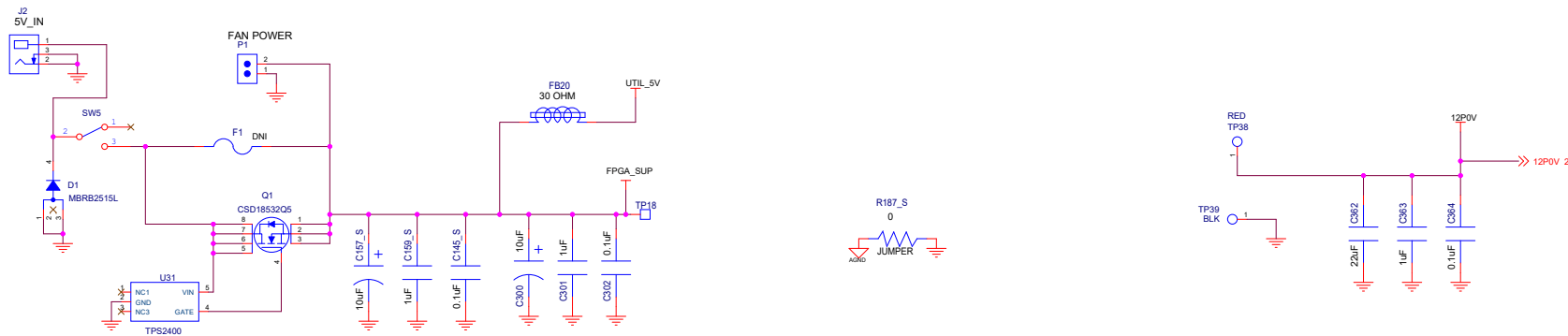
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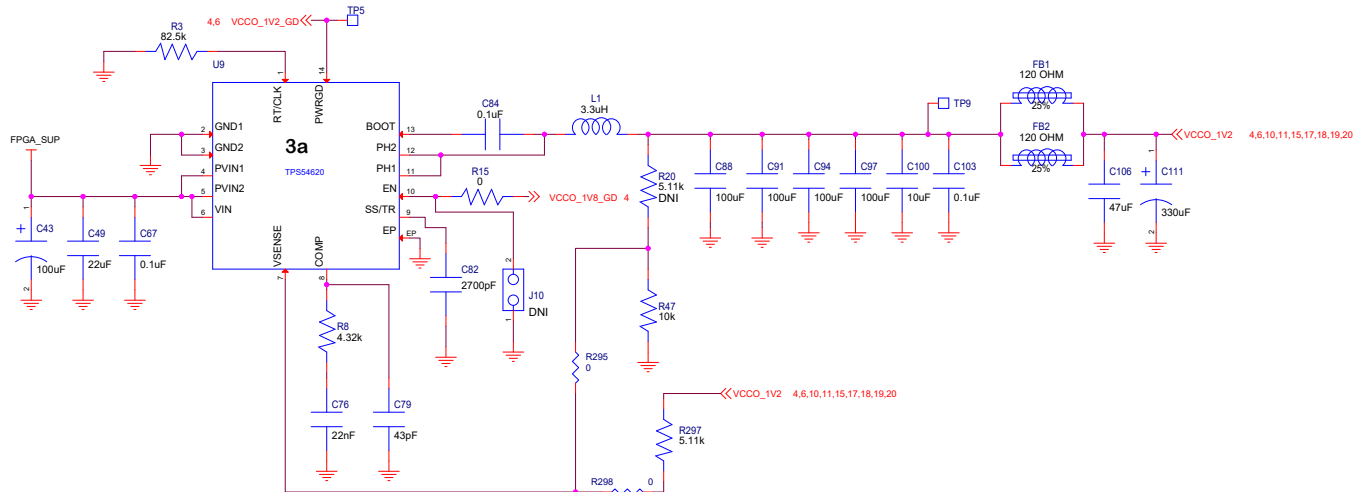
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FMC CONNECTOR		
Size	Document Number	Rev
	DC182_TSW14J58EVM	A10
Date:	Thursday, December 07, 2023	Sheet 1 of 23

Drawn:	L. Nguyen 12/2023
Eng:	B. Uhing

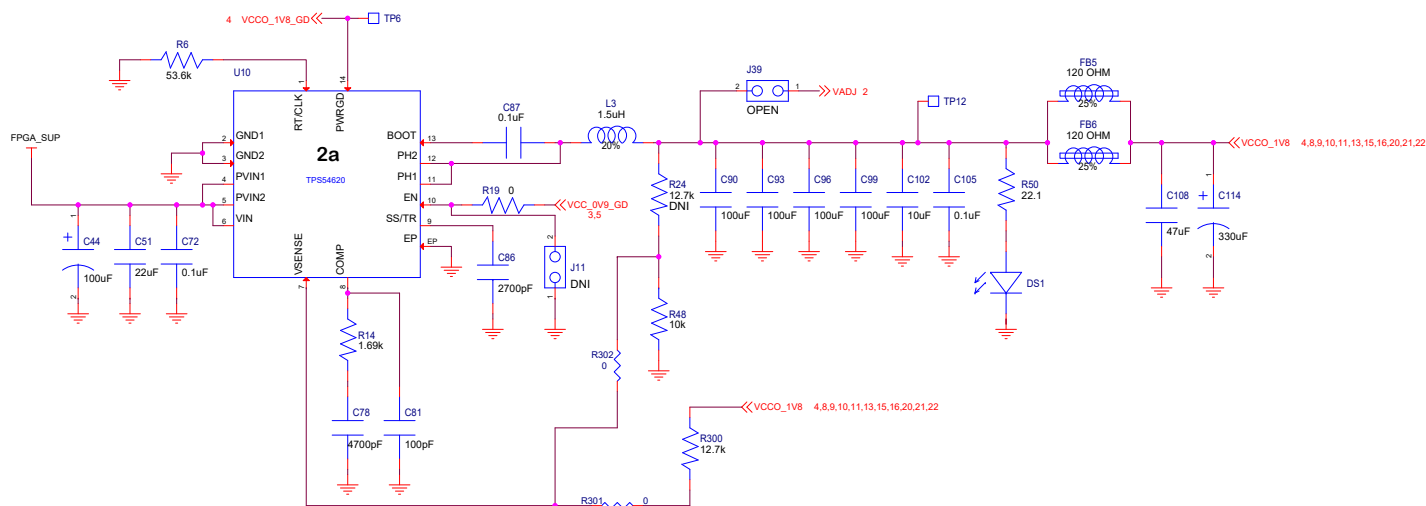




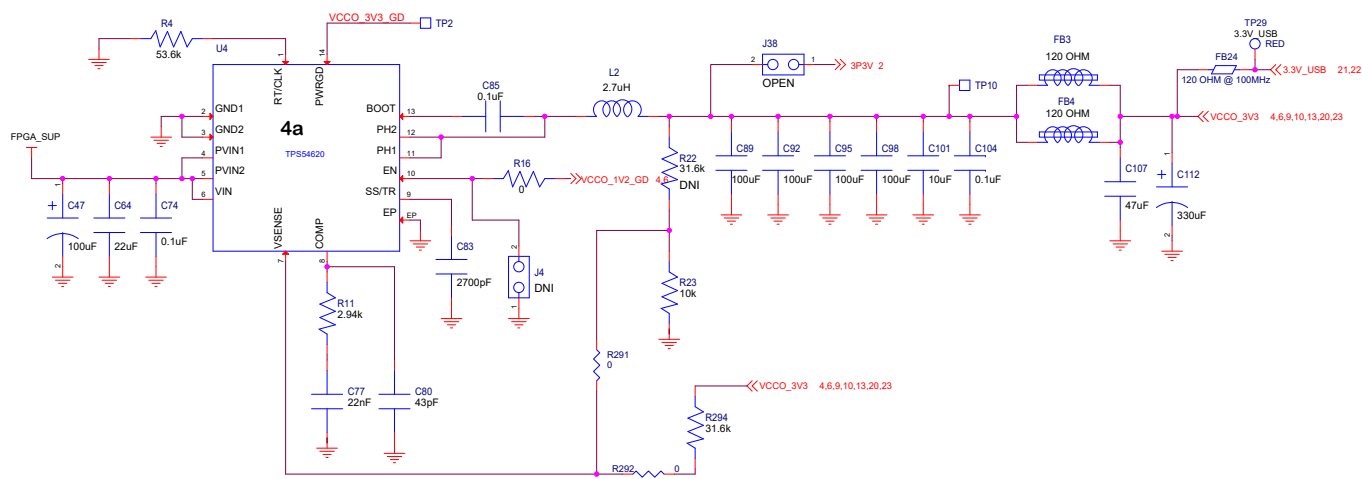
VCC_0V9
To be used for FPGA Internal Voltage 6A



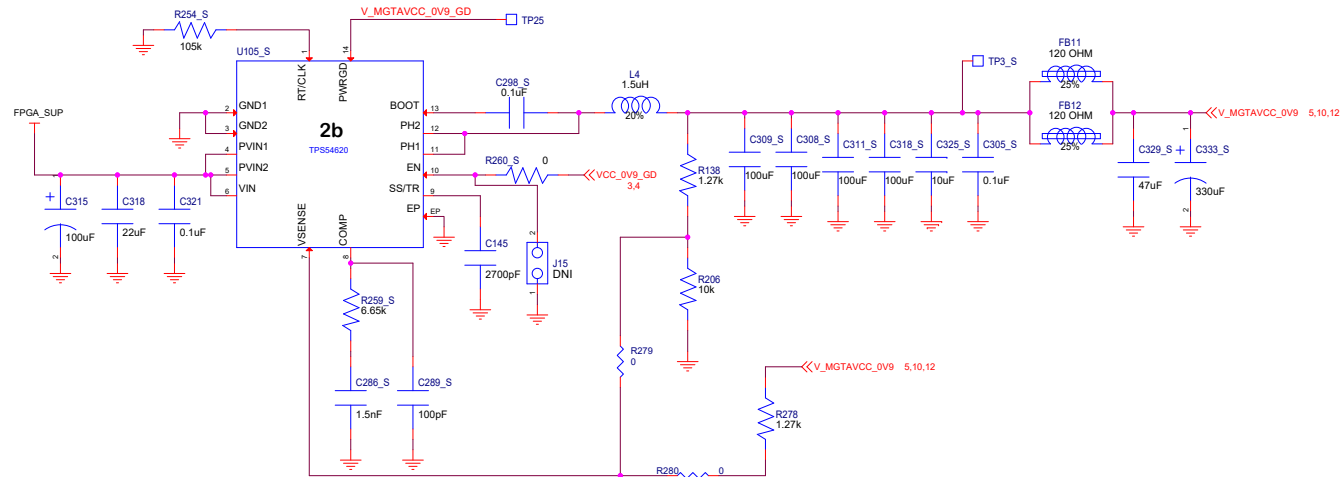
VCCO_1V2
To be used for 1.2V DDR HP IO 6A



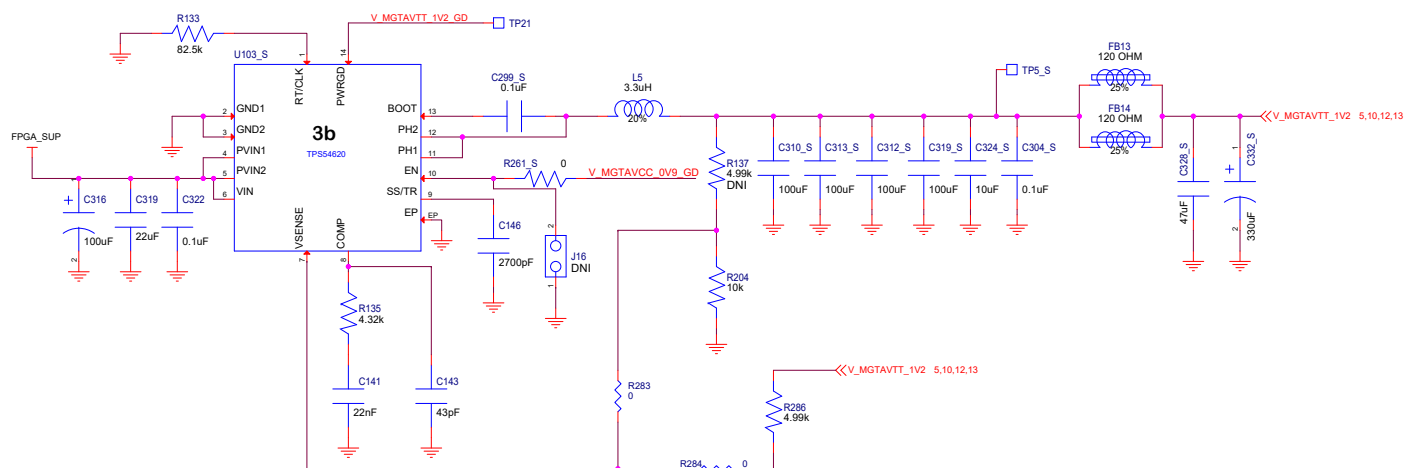
VCCO_1V8
To be used for 1.8V General IO



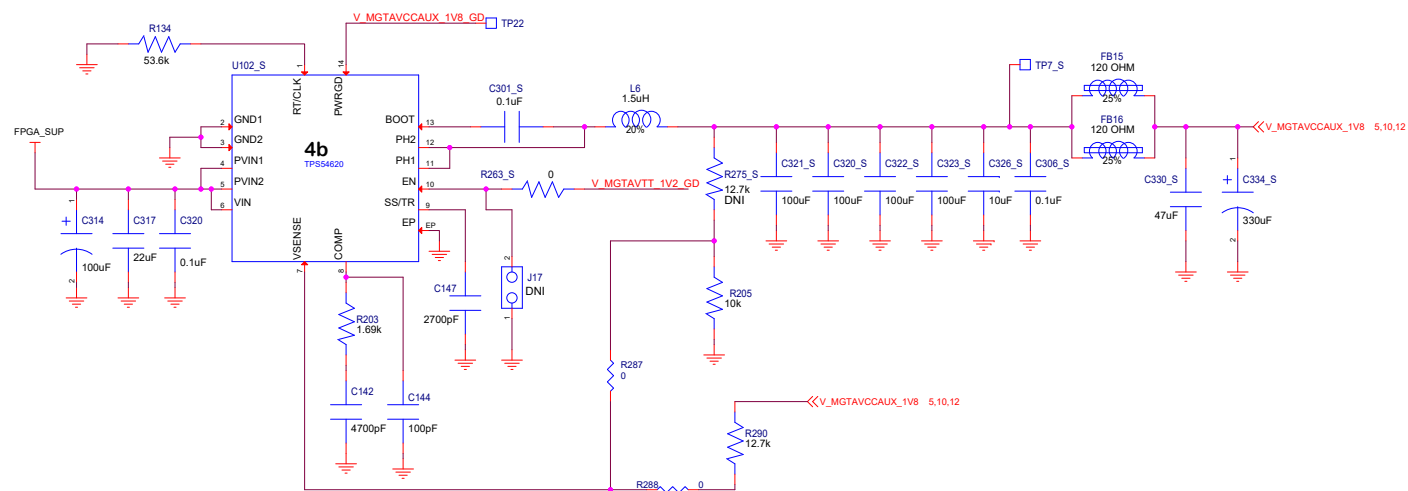
VCCO_3V3
To be used for 3.3V IO and USB interface 6A



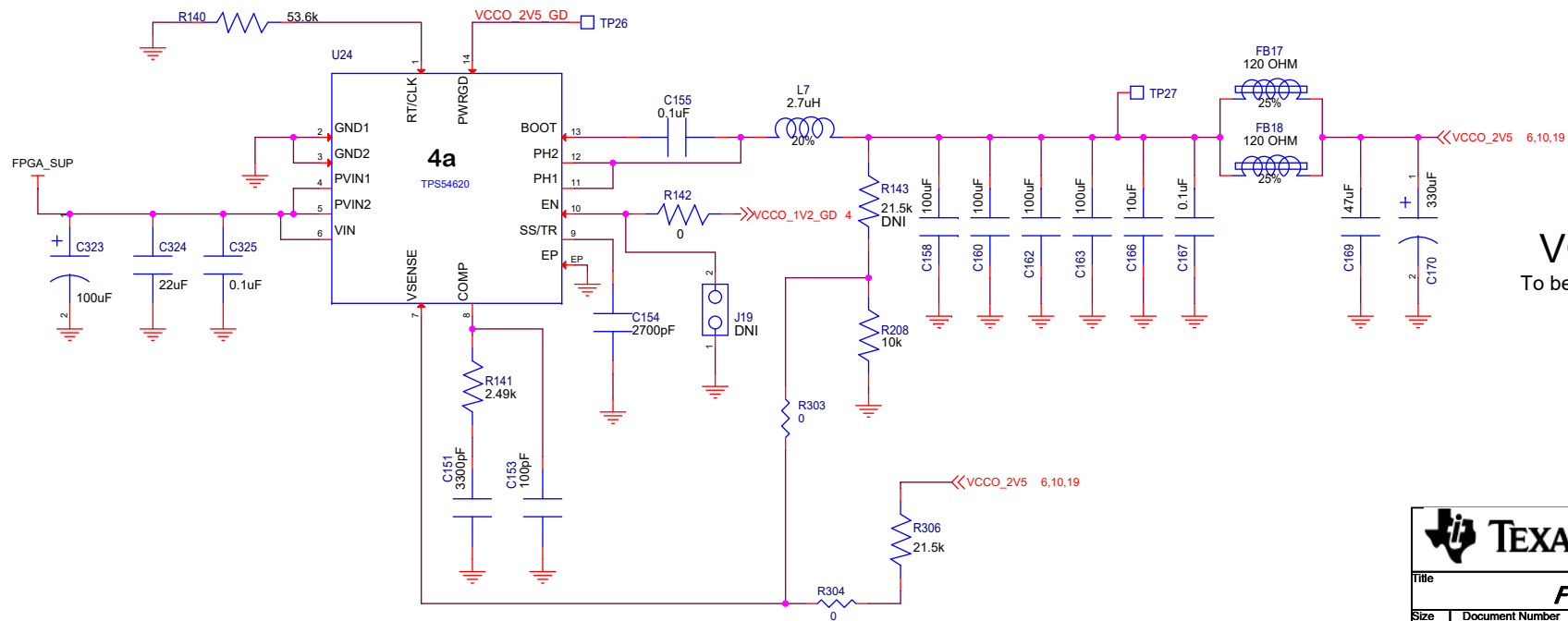
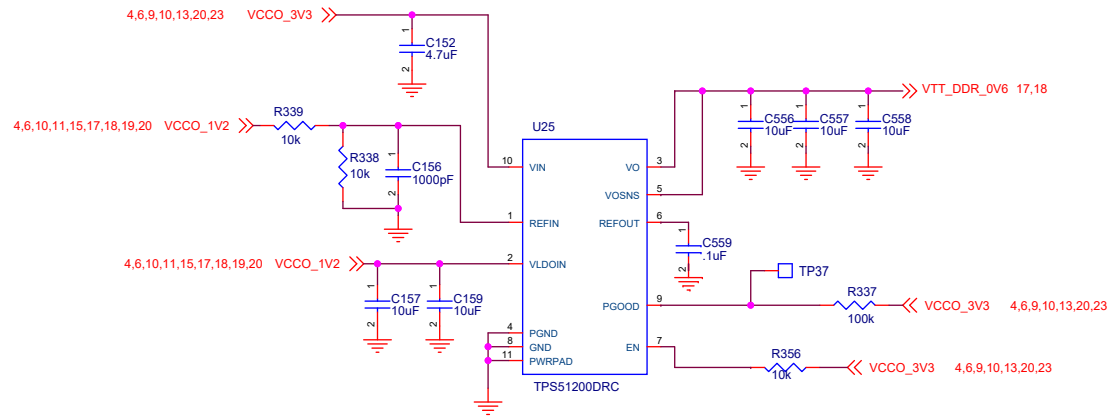
MGTAVCC_0V9
To be used for FPGA Transceiver



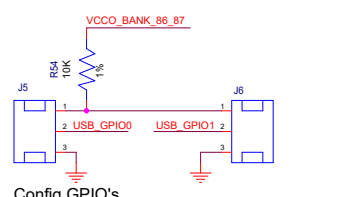
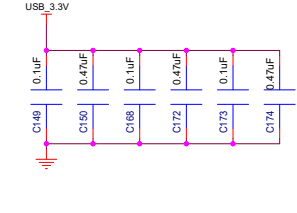
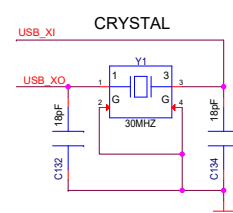
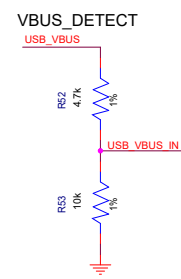
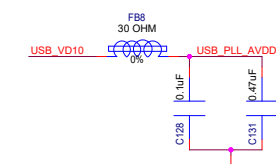
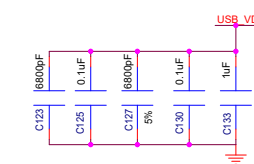
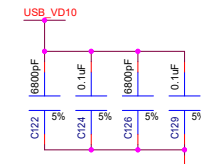
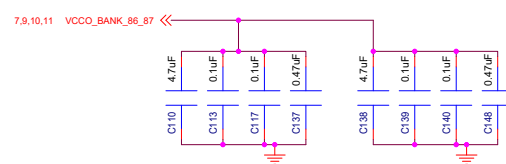
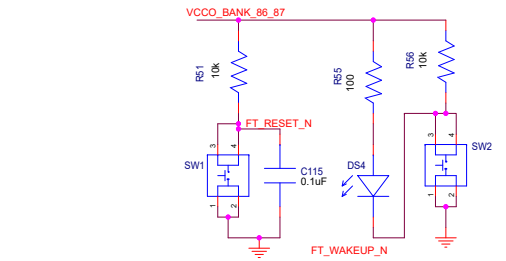
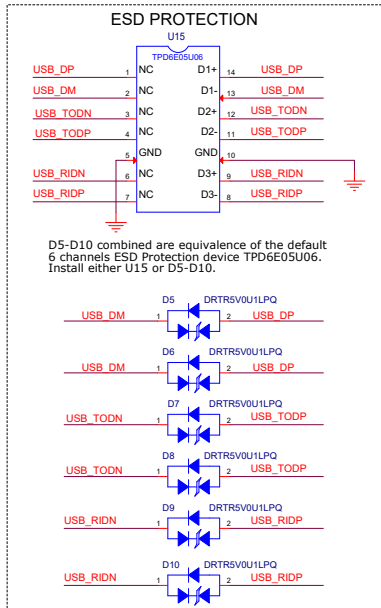
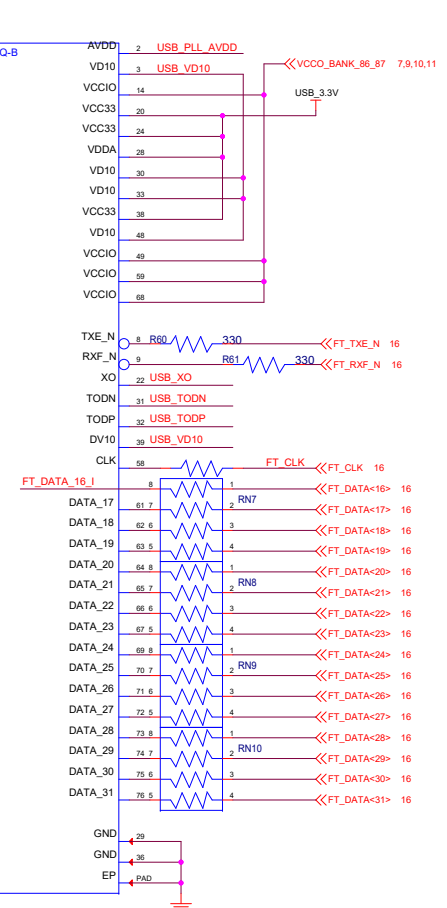
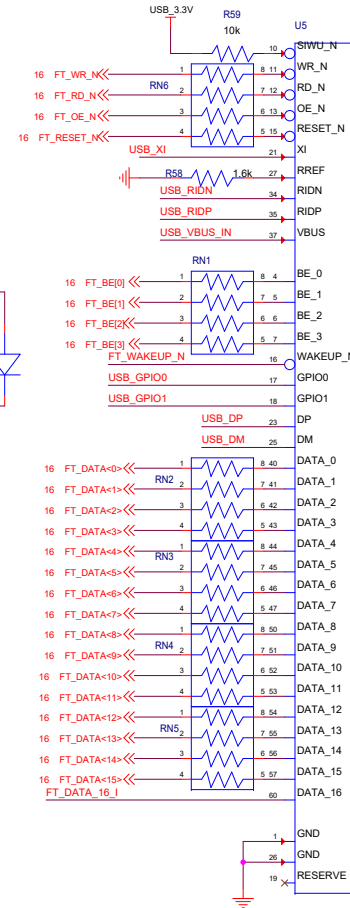
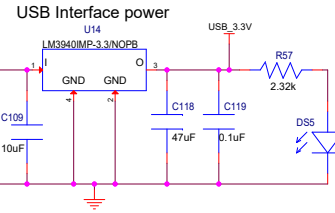
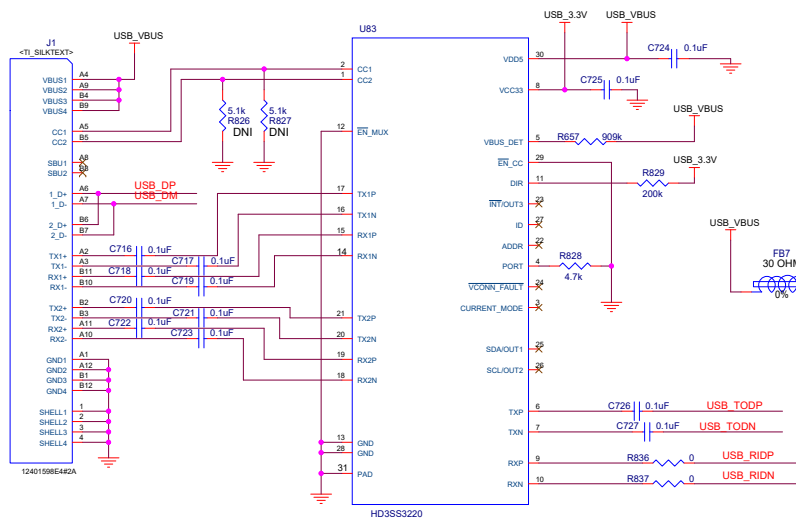
MGTAVTT_1V2
To be used for FPGA Transceiver

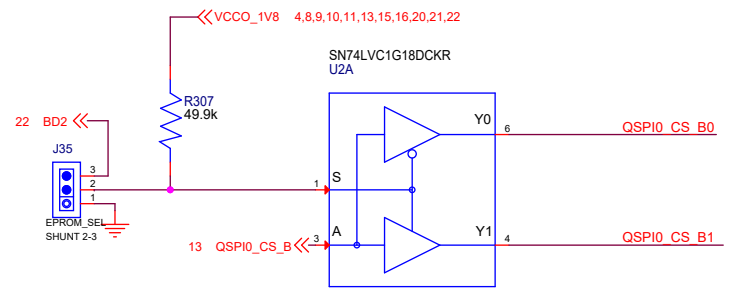
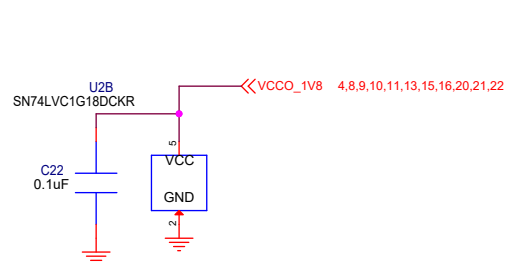
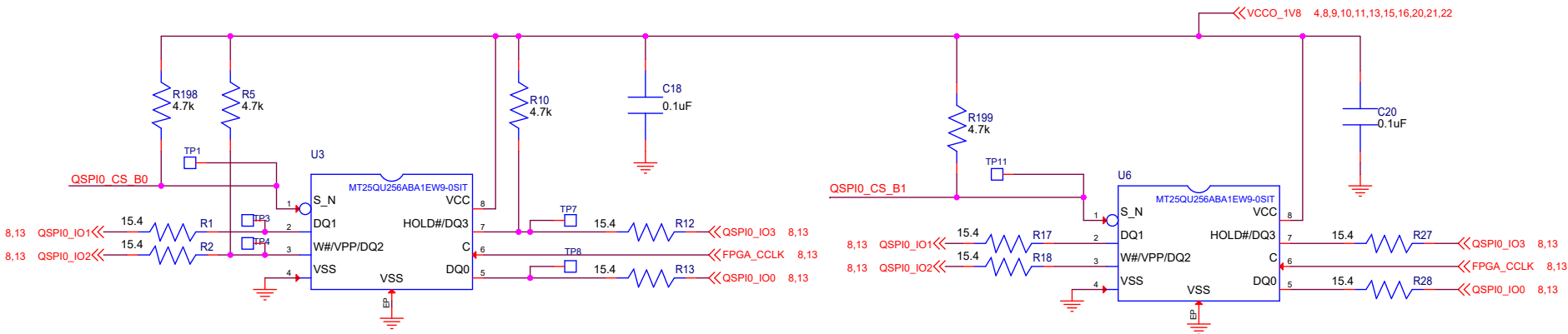


MGTAVCCAUX_1V8
To be used for FPGA Transceiver



VCCO_2V5
To be used for DDR Supply





STANDOFF ALUM HEX 2-56 x 3/4"

BARE BOARD_TSW14J58EVM

STANDOFF ALUM HEX 2-56 x 3/4"

STANDOFF ALUM HEX 2-56 x 3/4"

SCREW PANHEAD 2-56 x 1/4"

Z_FAN1
FAN SINK, 27mm x 27mm

STANDOFF ALUM HEX 2-56 x 3/4"

STANDOFF ALUM HEX 2-56 x 3/4"

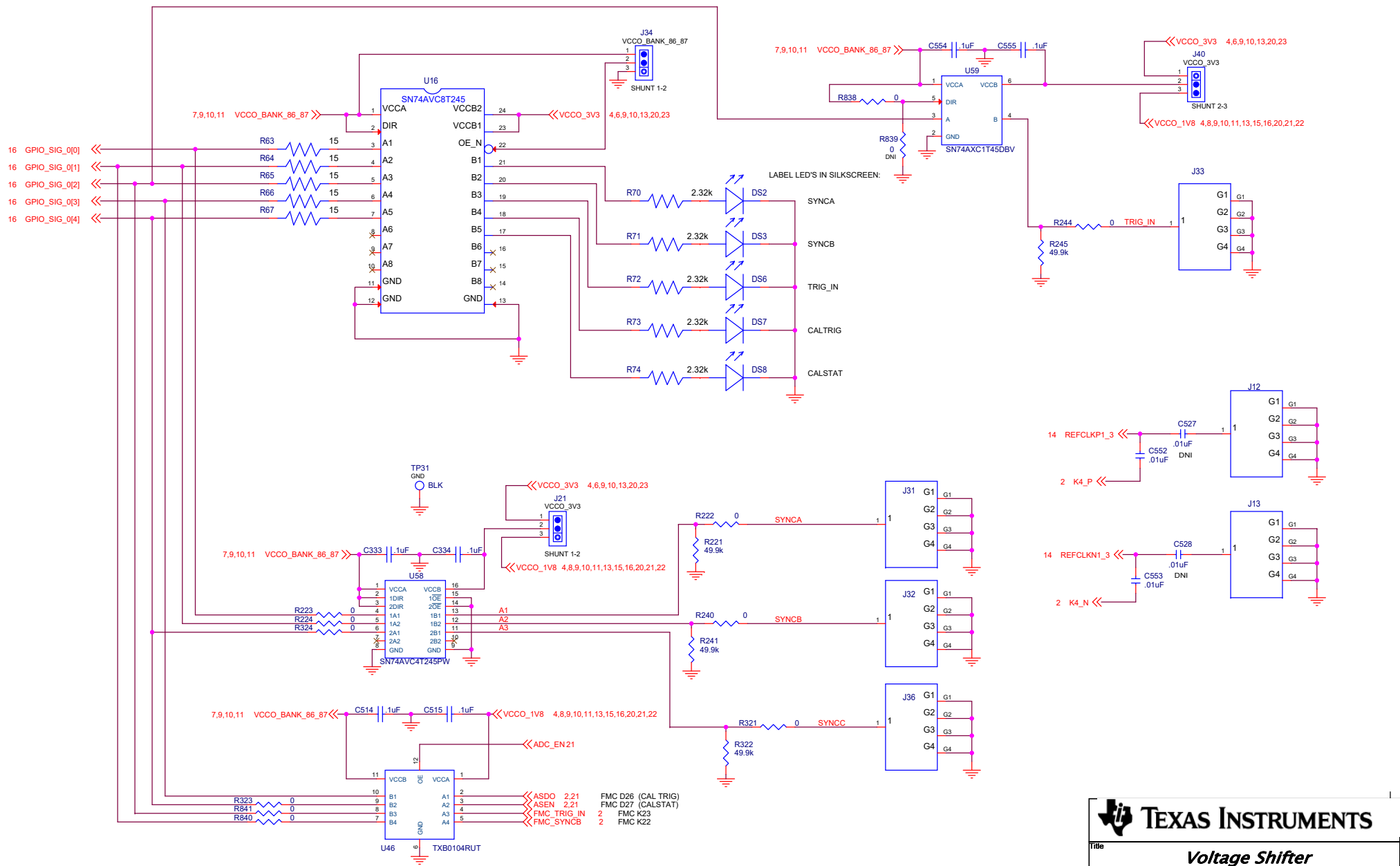
SCREW PANHEAD 2-56 x 1/4"

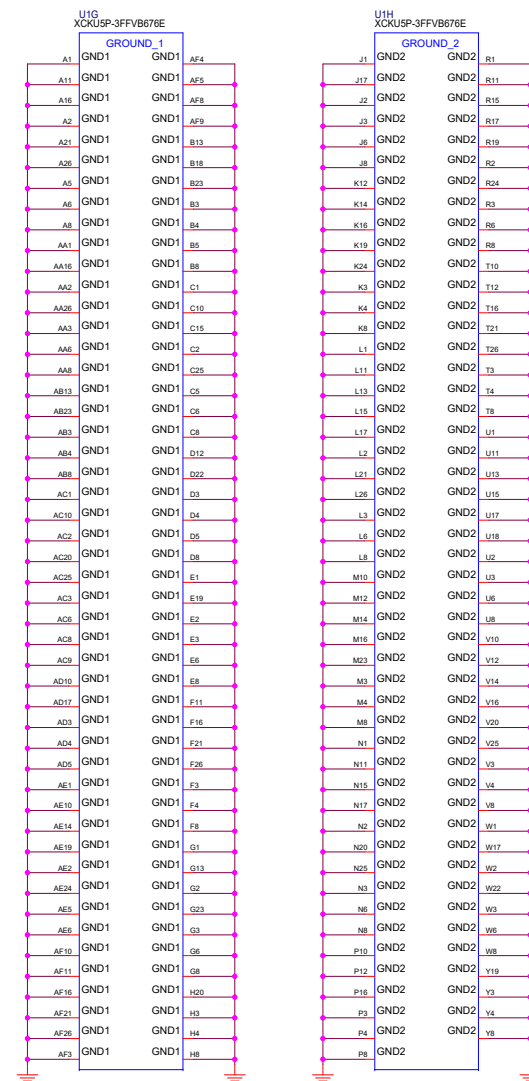
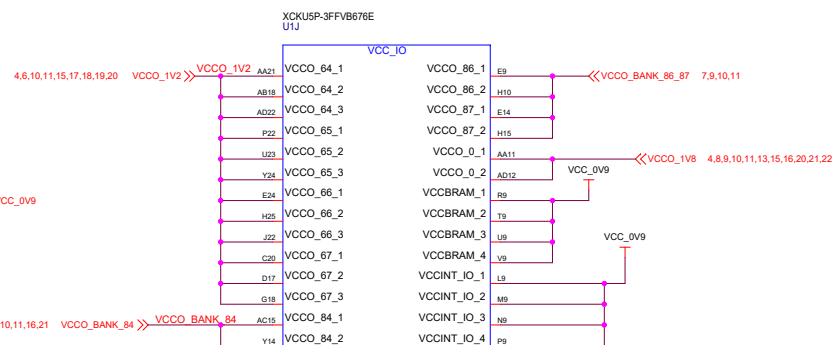
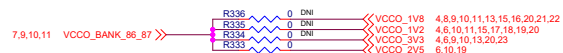
SCREW PANHEAD 2-56 x 1/4"

SCREW PANHEAD 2-56 x 1/4"

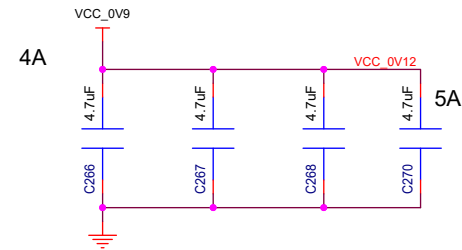
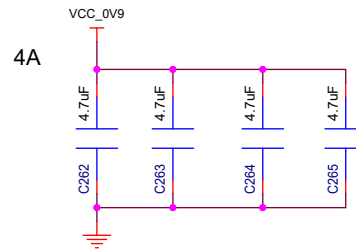
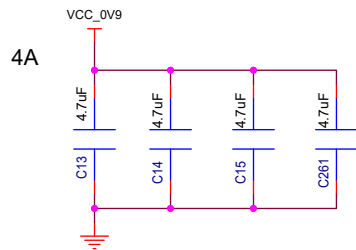
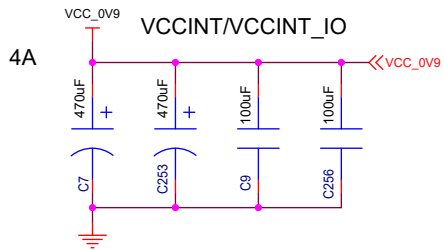
SCREW PANHEAD 2-56 x 1/4"

PGM FLASH		
Title PGM FLASH	Document Number DC182_TSW14J58EVM	Rev A10
Date: Wednesday, December 06, 2023 Sheet 8 of 23		

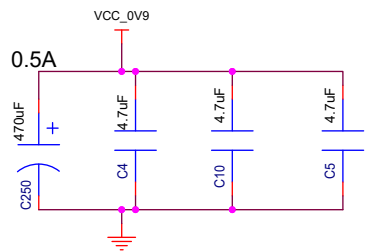




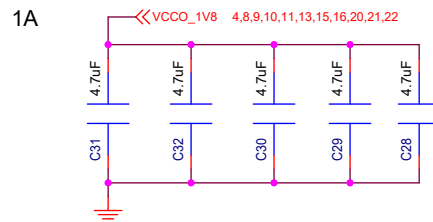
VCCINT/VCCINT_IO



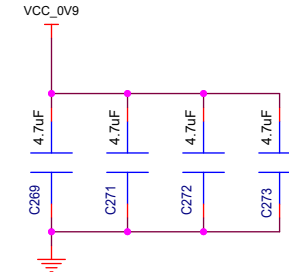
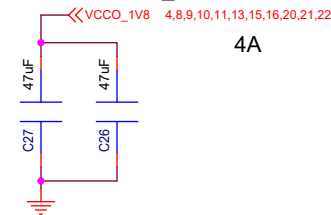
VCCBRAM



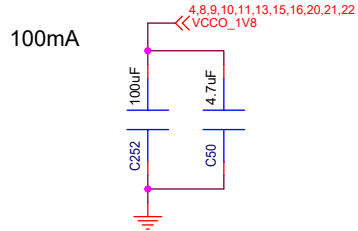
VCCAUX/VCCAUX_IO



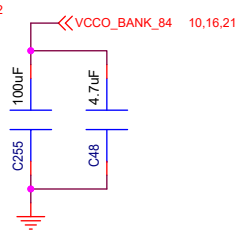
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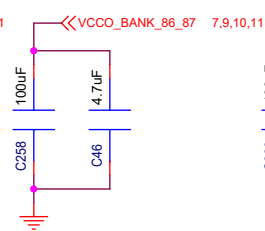
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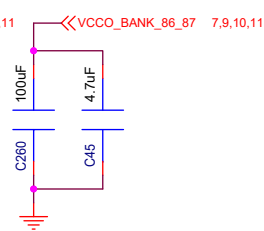
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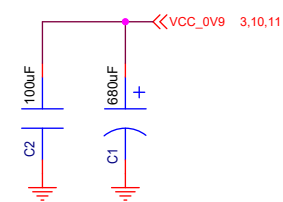
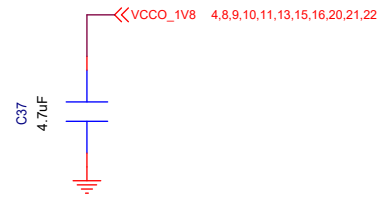
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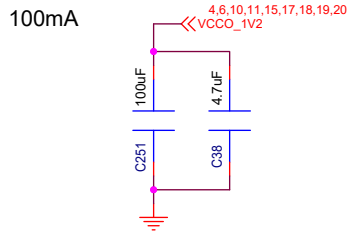
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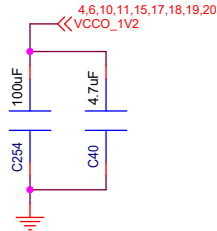
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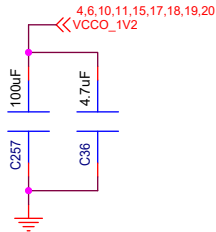
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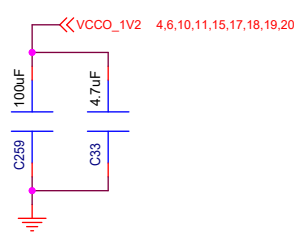
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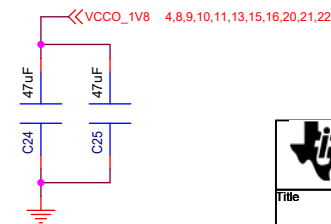
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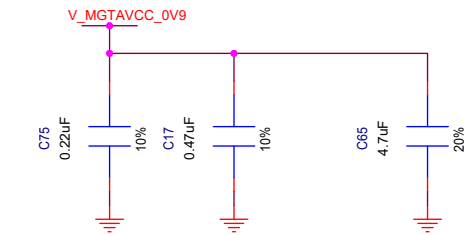
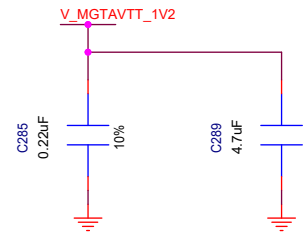
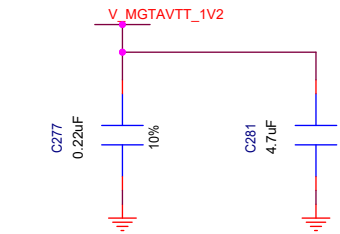
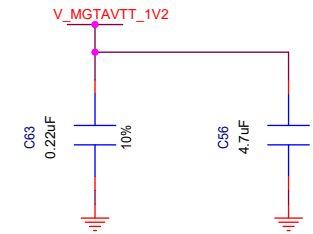
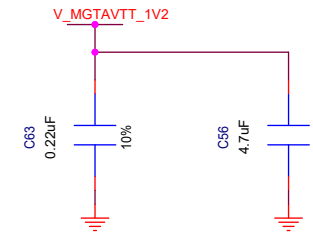
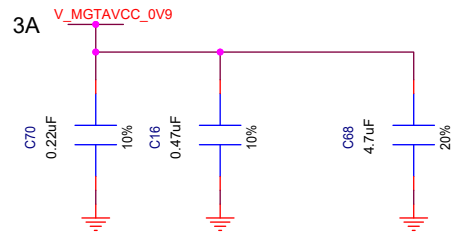
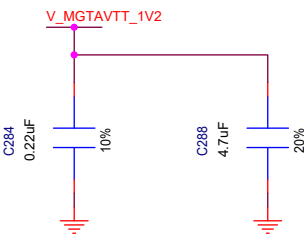
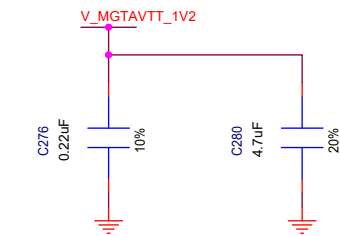
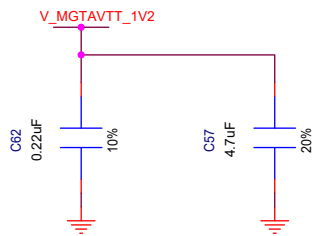
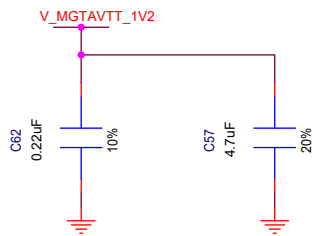
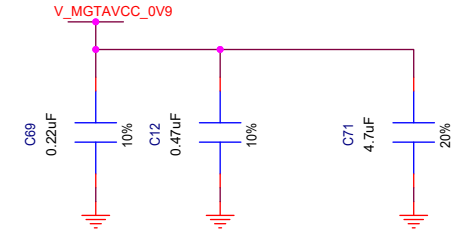
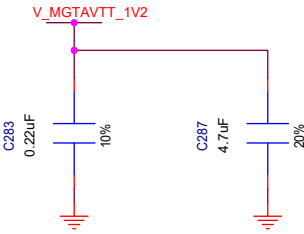
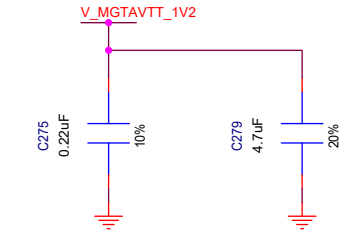
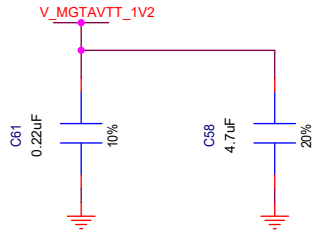
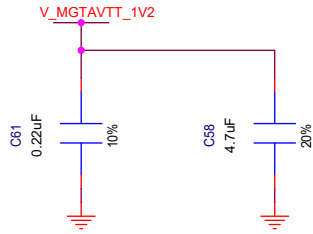
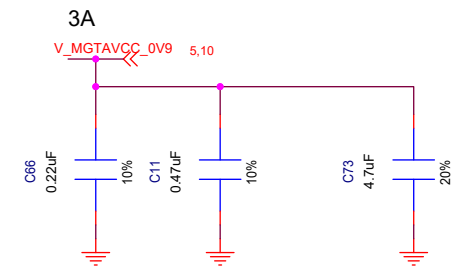
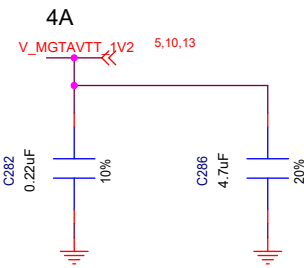
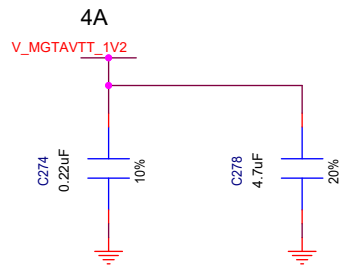
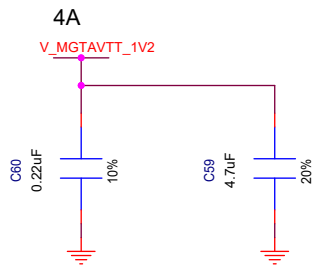
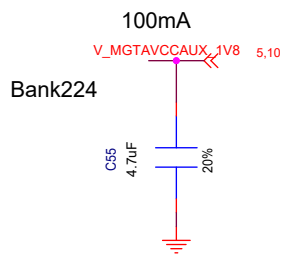
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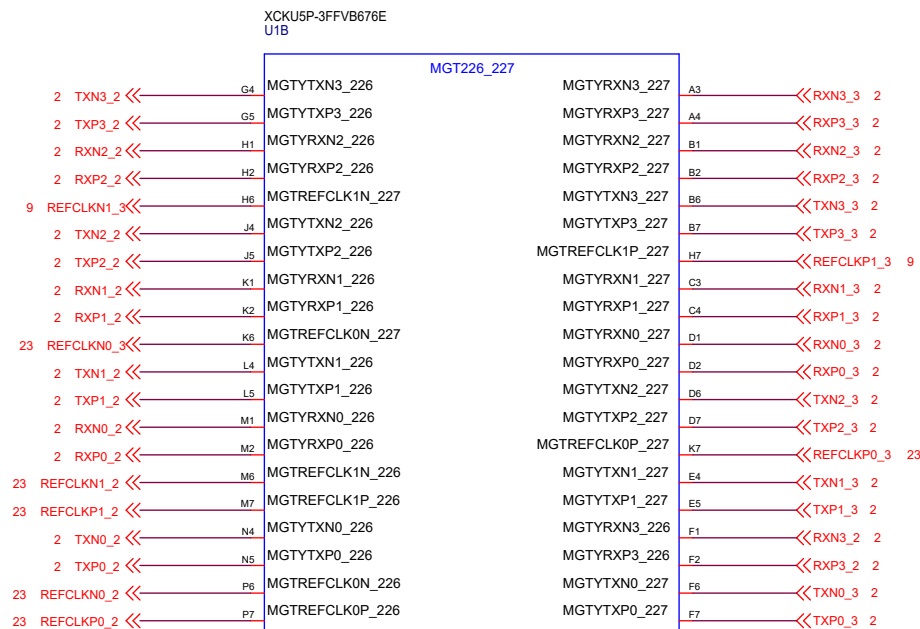
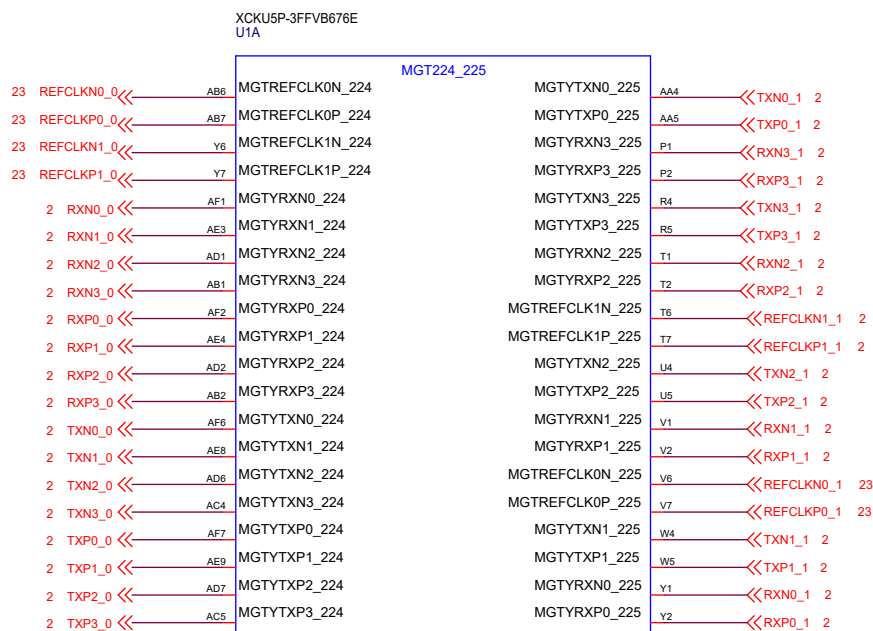


Bank

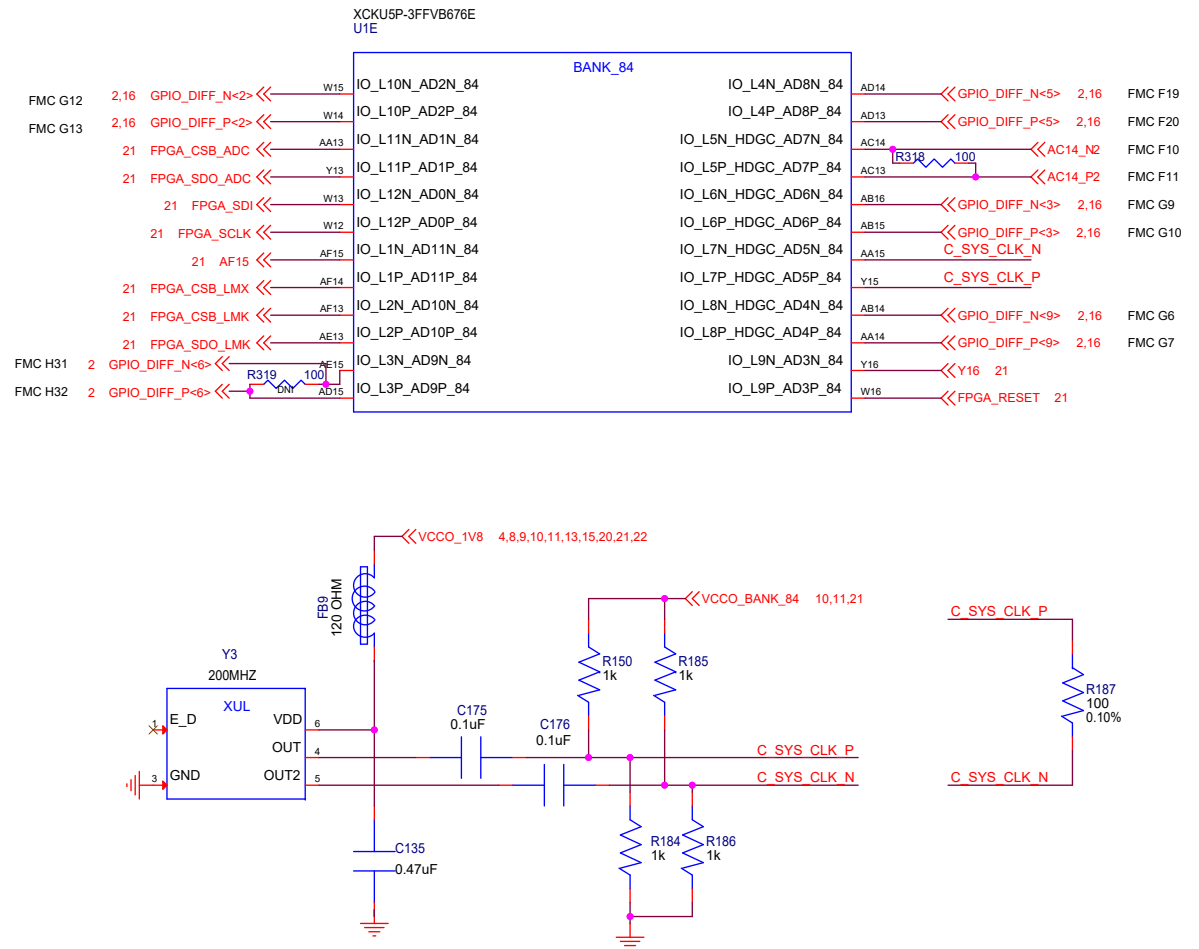
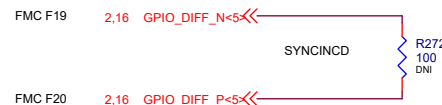
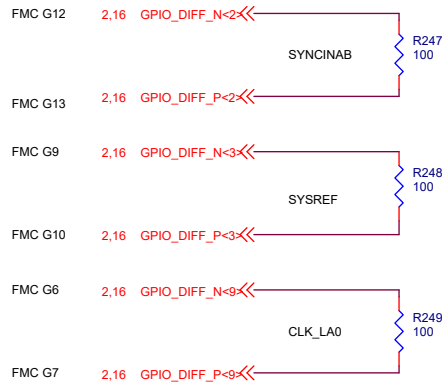
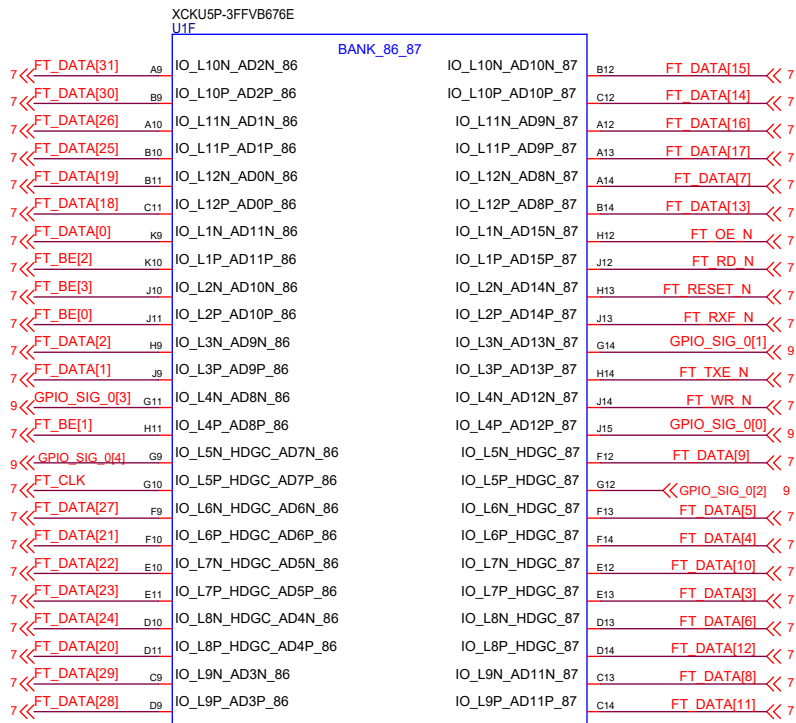


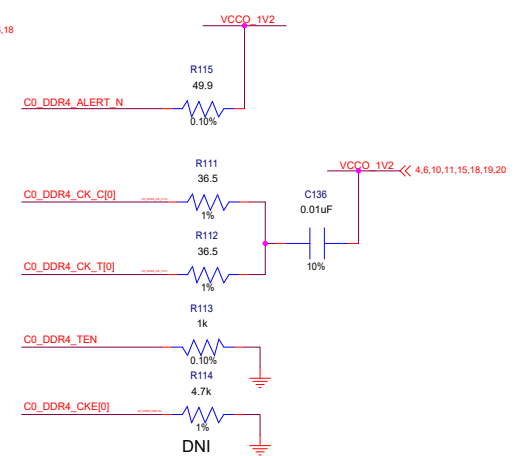
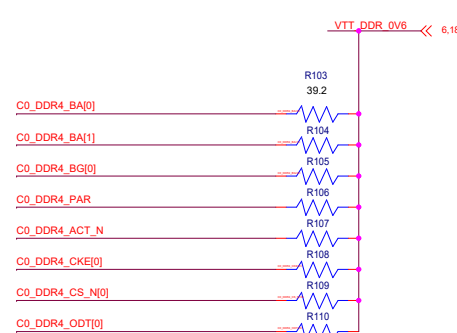
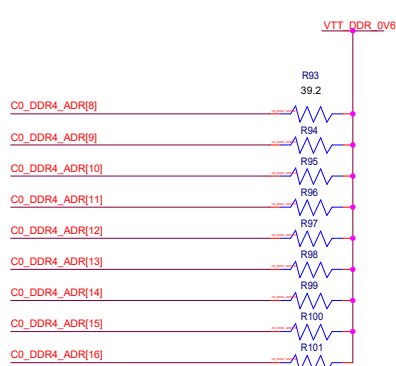
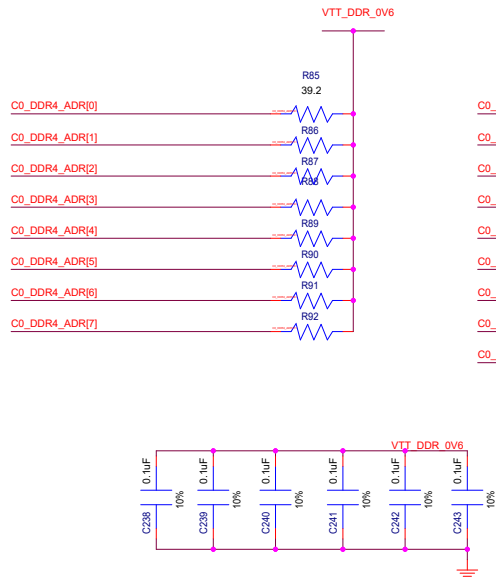
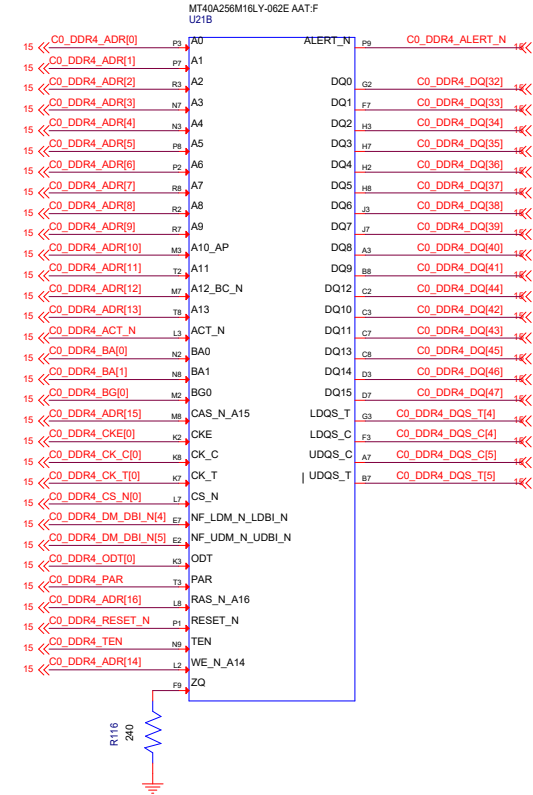
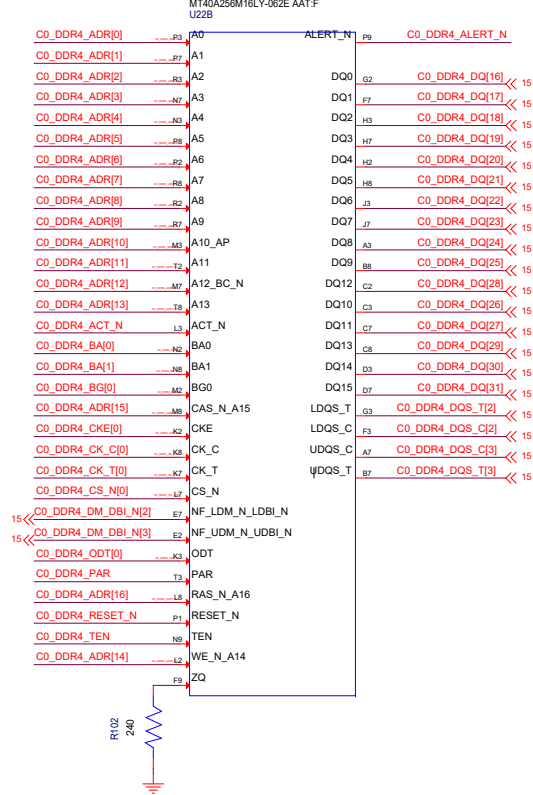
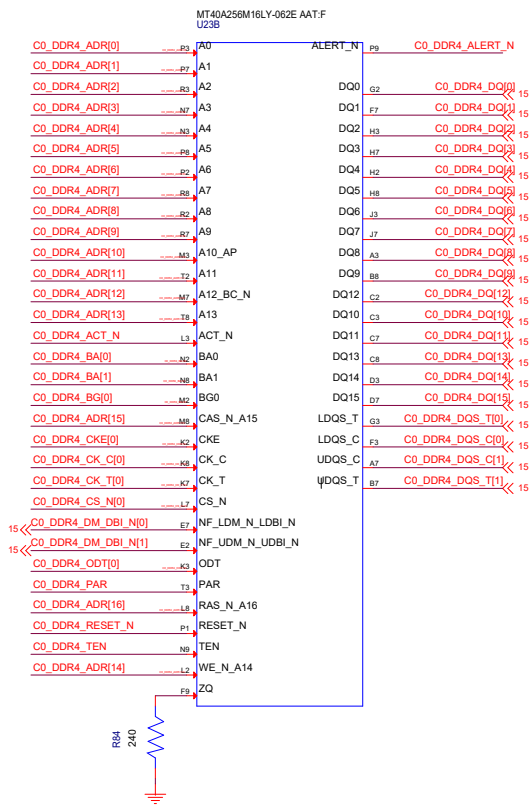
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FPGA Decoupling_1		
Size	Document Number	Rev
B	DC182_TSW14J58EVM	A10
Date:	Wednesday, December 06, 2023	Sheet 11 of 23



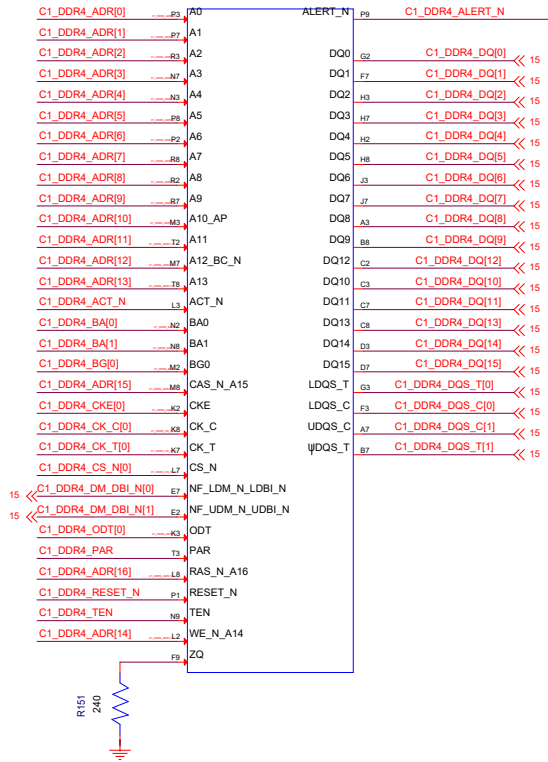


Ensure Clock and Signals are AC Coupled

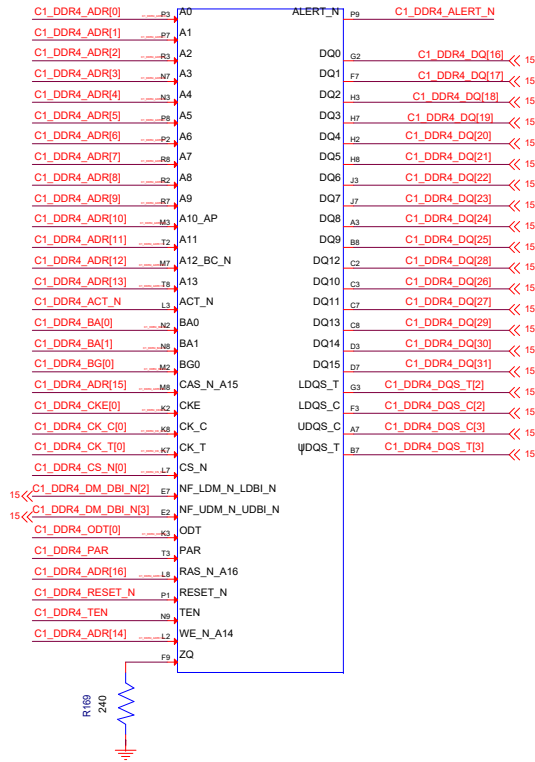




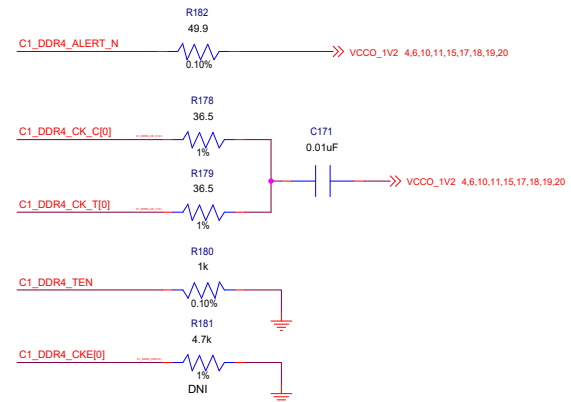
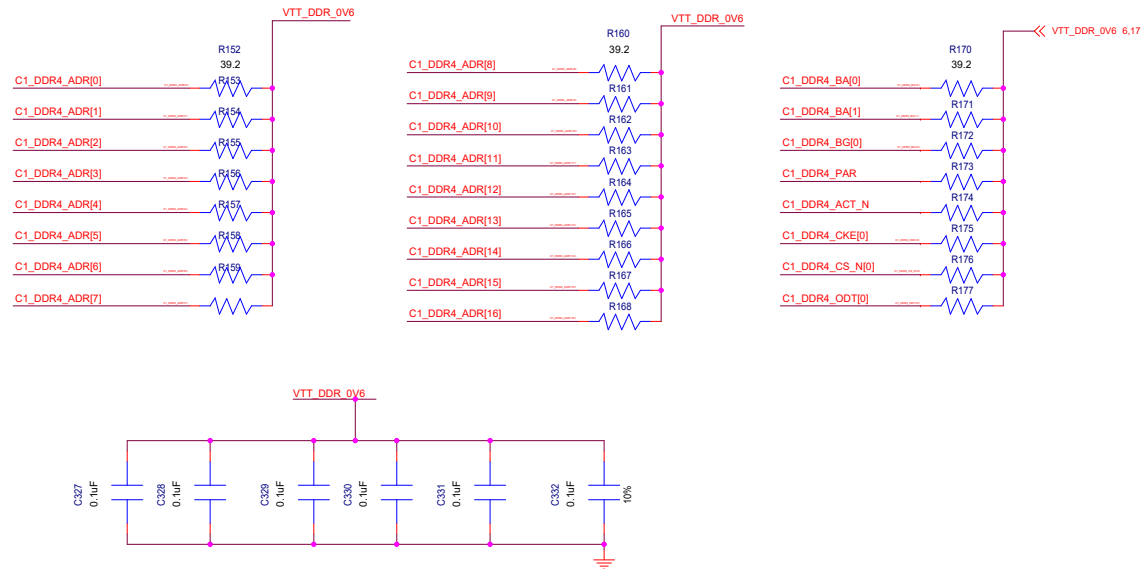
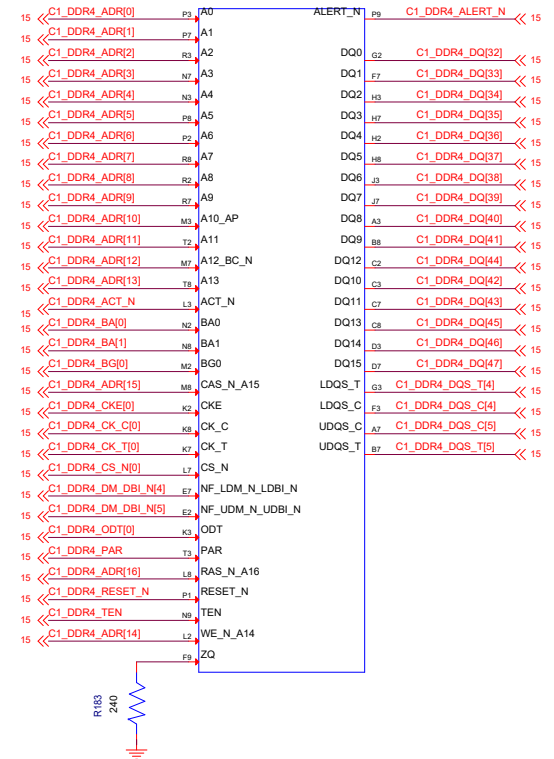
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U20B



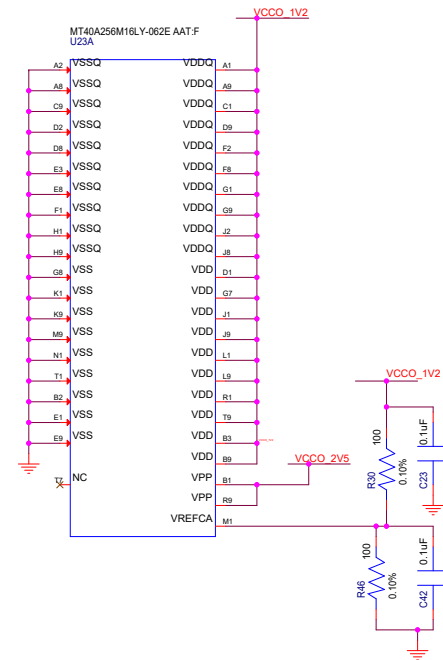
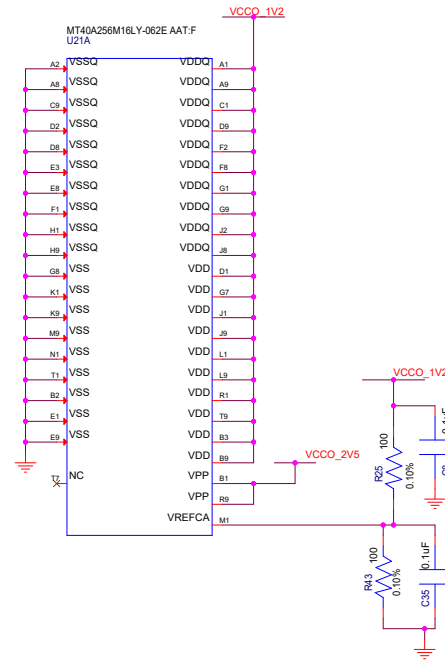
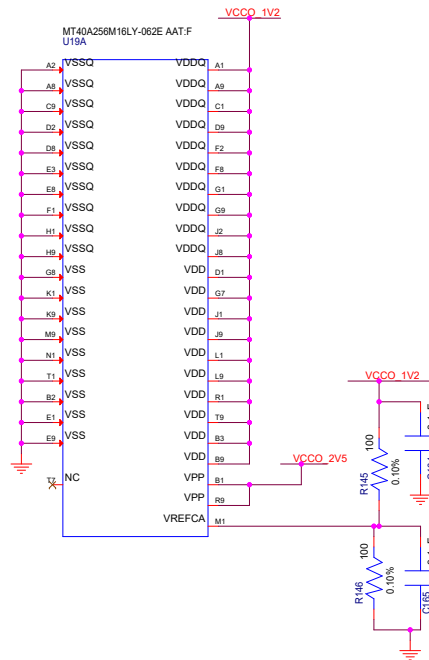
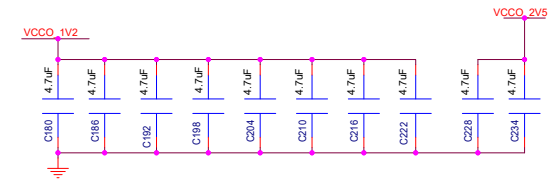
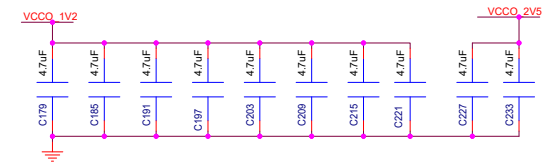
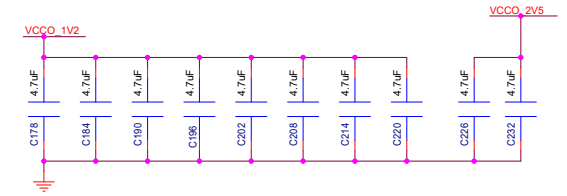
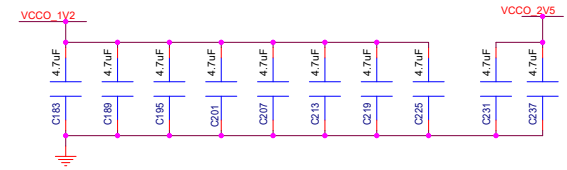
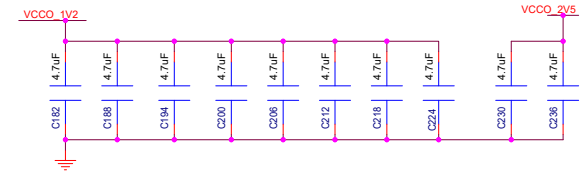
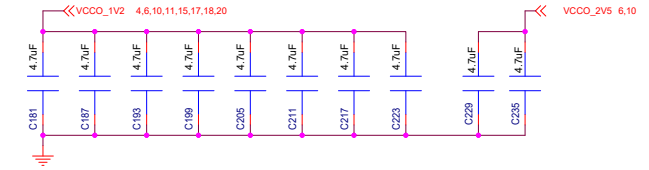
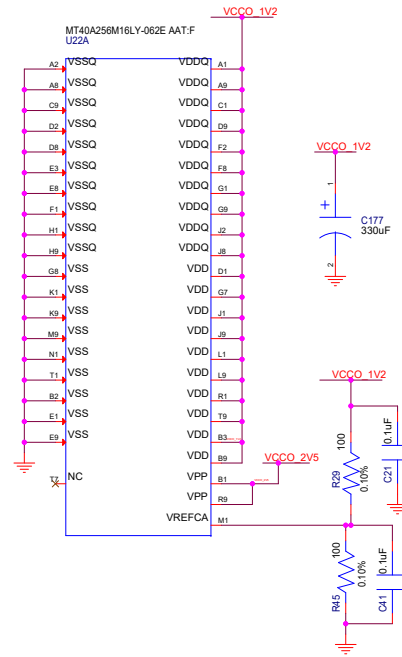
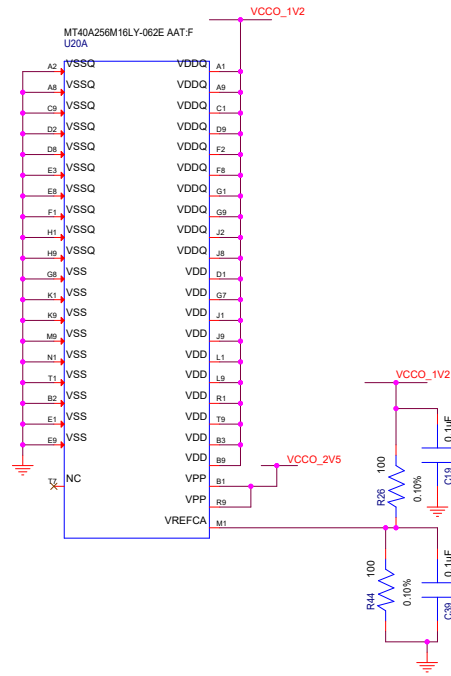
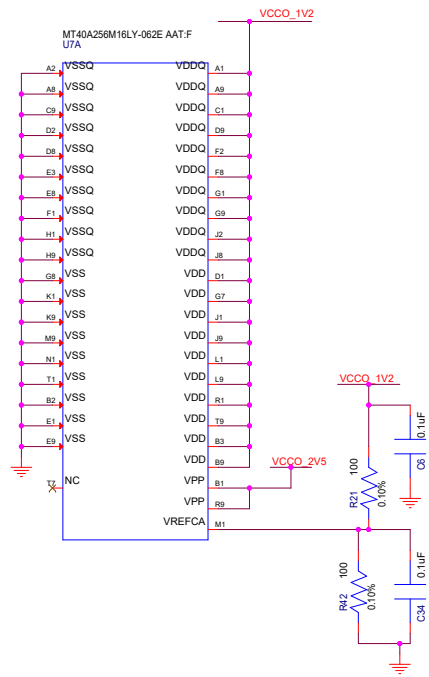
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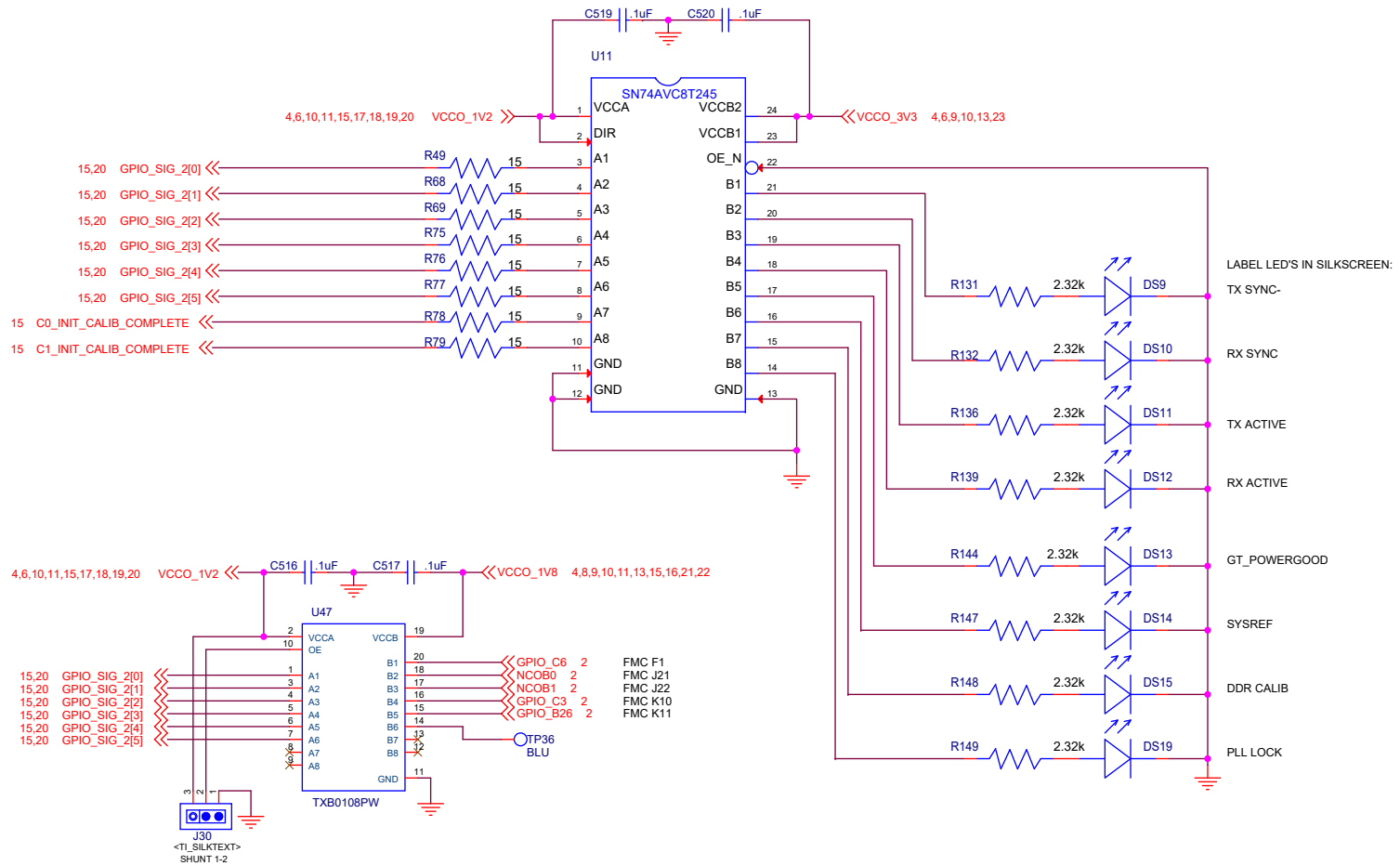


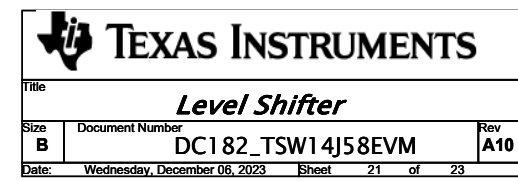
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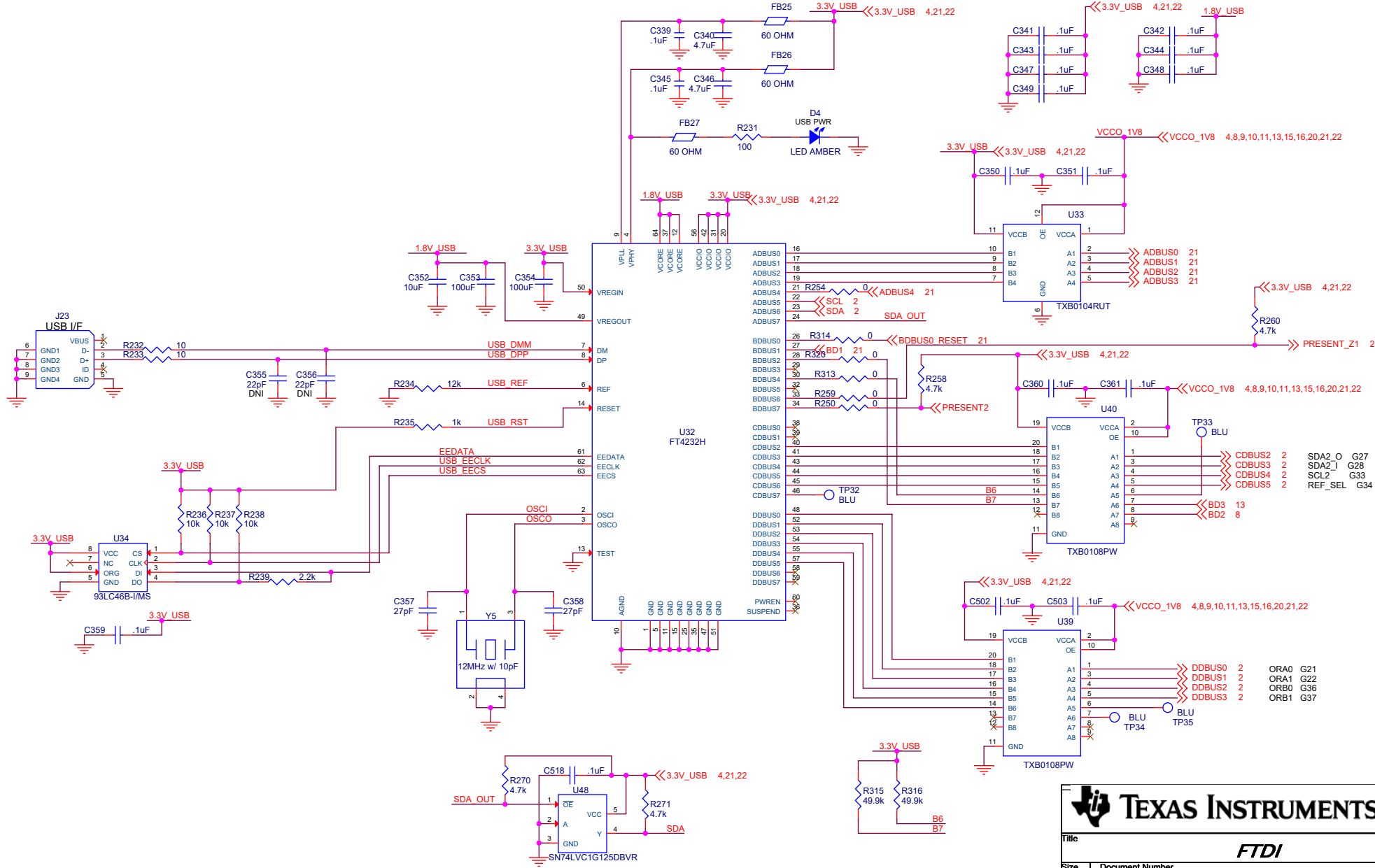


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