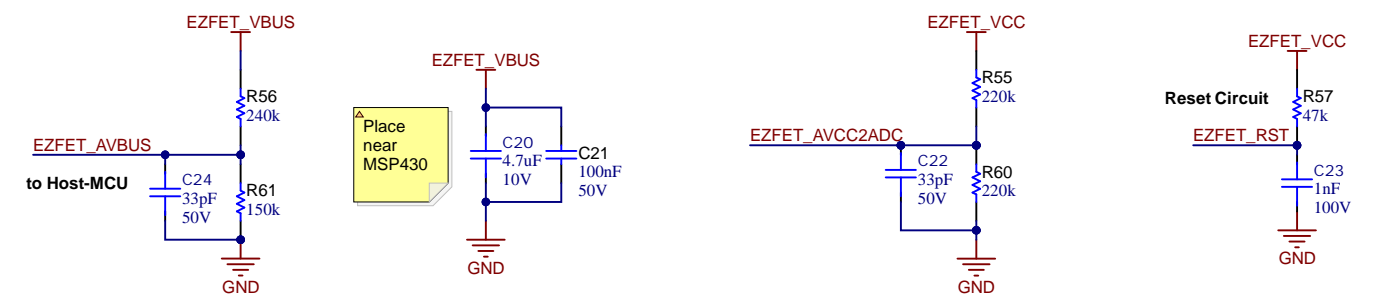
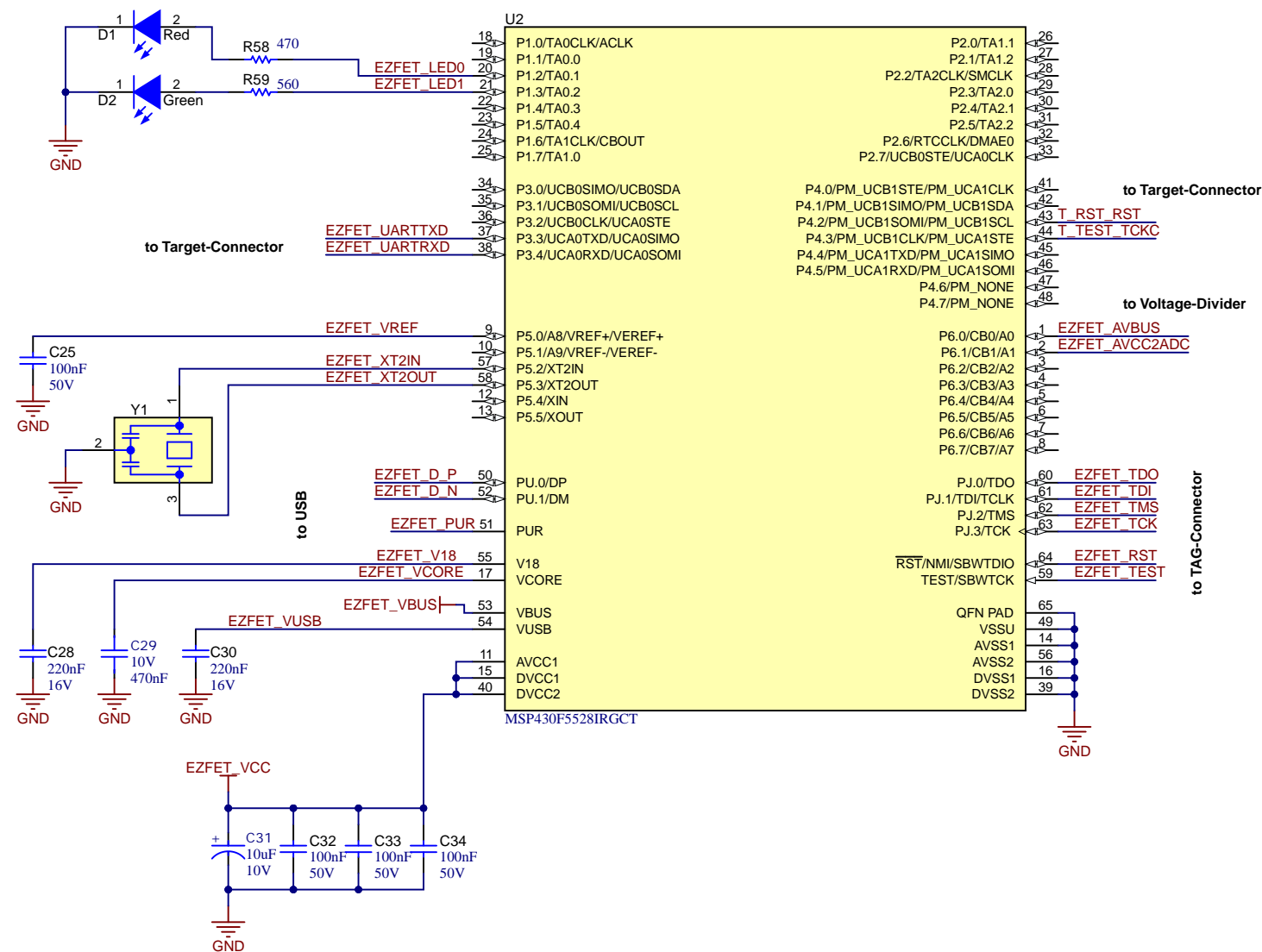
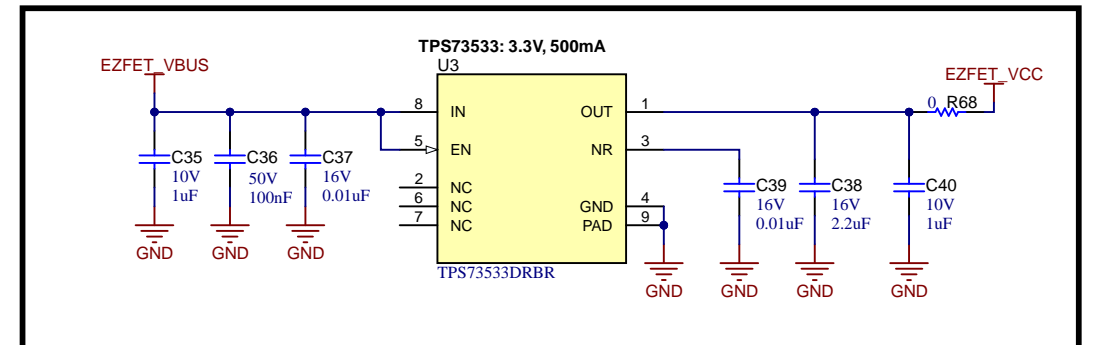


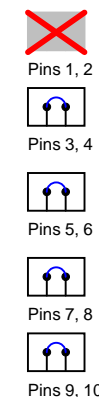
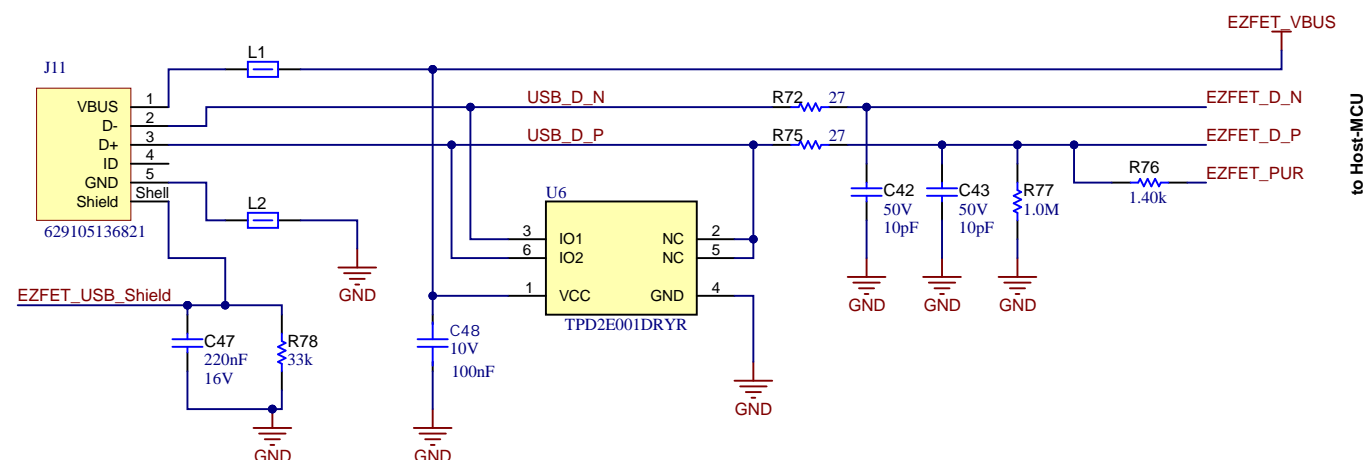
Host MCU for Emulation



3.3V Power (EZFET_VCC)



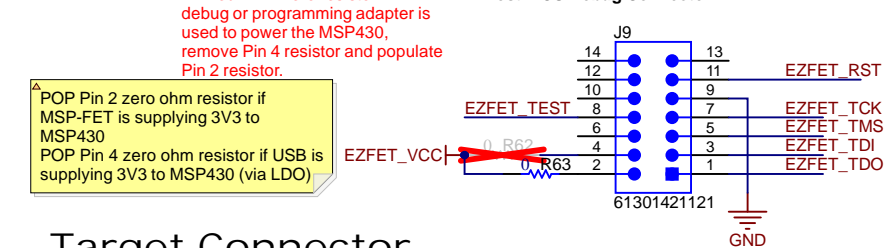
USB-Interface



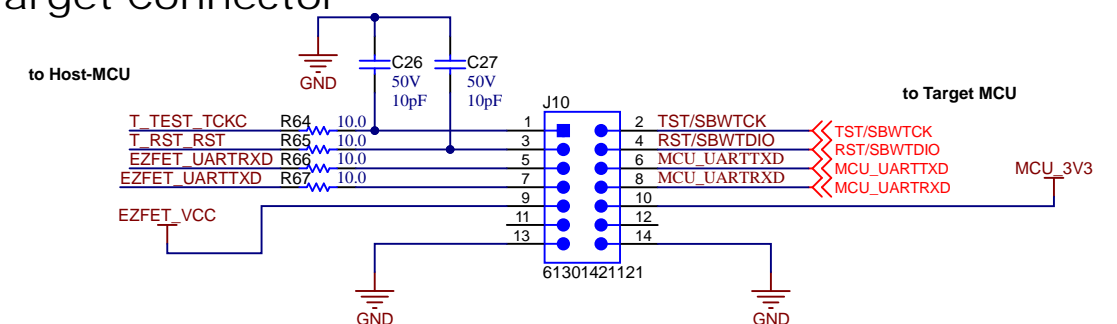
JTAG-Connector (Host Debug)


DNPed Pin 2 zero resistor. If debug or programming adapter is used to power the MSP430, remove Pin 4 resistor and populate Pin 2 resistor.

Host-MCU Debug Connector



Target Connector



Orderable: DRV8235EVM	Designed for: Public Release	Mod. Date: 1/31/2024	 TEXAS INSTRUMENTS http://www.ti.com © Texas Instruments 2024
TID #: N/A	Project Title: DRV8214/15_8234/35EVM		
Number: MD069	Rev: C	Sheet Title:	
SVN Rev: Unknown revision	Assembly Variant: 004	Sheet: 1 of 1	
Drawn By: Jacob Thompson	File: MD069C_ezFET_SchDoc	Size: B	
Engineer: Jacob Thompson	Contact: http://www.ti.com/support		

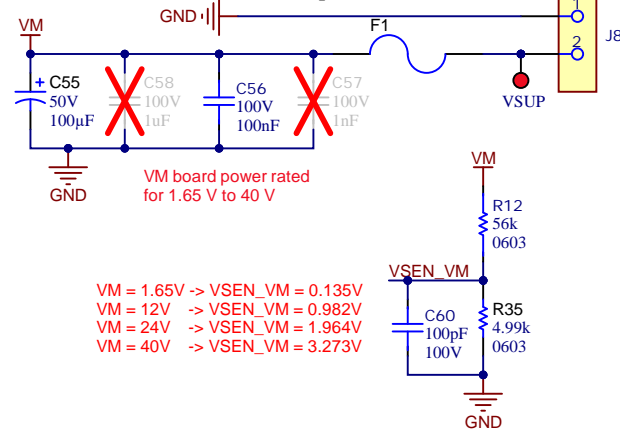
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3.3V LDO

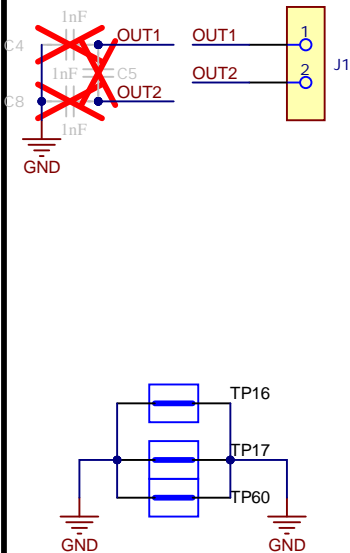
The diagram shows a 3.3V LDO regulator (U4: LM9036M-3.3/NOPB) with the following components and connections:

- Input:** VM connected to pin 8. A 100nF capacitor (C6) is connected between pin 8 and GND. A 50V capacitor is connected between pin 8 and GND. A red 'X' is placed over the input section.
- Output:** MCU_3V3 connected to pin 1. A 22μF capacitor (C7) is connected between pin 1 and GND. A 10V capacitor is connected between pin 1 and GND. A red 'X' is placed over the output section.
- Other pins:** Pin 2 is connected to GND. Pin 3 is connected to GND. Pin 4 is connected to GND. Pin 5 is connected to GND. Pin 6 is connected to GND. Pin 7 is connected to GND.

The diagram is crossed out with a large red 'X'.



GND ● GND
 VM ● VM
 TP8 ○ OUT1
 TP10 ○ OUT2

[illegible]

The top diagram shows the nFAULT pin configuration. It is pulled up to DRV_3V3 by resistor R24 (10k). The pin is connected to the IPROPI pin of the MCP23017. A network consisting of resistor R2 (1.50k) and capacitor C3 (1nF) is connected between the IPROPI pin and ground (GND).

The middle diagram shows the configuration for the I2C pins. Resistor R1 (10k) is crossed out, indicating it is not used. Resistor R6 (2.21k) is connected between DRV_3V3 and the SDA pin. Resistor R7 (2.21k) is connected between DRV_3V3 and the SCL pin. The RC_OUT pin is shown without a pull-up resistor.

The bottom diagram shows the configuration for the A0 and A1 pins. Resistor R13 (10k) is crossed out, indicating it is not used. Resistor R8 is connected between A0 and ground (GND), with a value of 0 indicated. Similarly, resistor R14 (10k) is crossed out, and resistor R10 is connected between A1 and ground (GND), with a value of 0 indicated.

Pin connection diagram for the P1 header. The diagram shows two rows of pins. The left row (TP28-TP39) includes nFAULT, RC_OUT, IPROPI, VREF, SCL, SDA, IN1, IN2, nSLEEP, A0, A1, and a ground connection. The right row (P1) includes pins 1-26, with labels MSP_nFAULT, MSP_RC_OUT, MSP_IPROPI, MSP_VREF, MSP_SCL, MSP_SDA, MSP_IN1, MSP_IN2, MSP_nSLEEP, and a ground connection. Connections are shown for TP28 to pin 1, TP29 to pin 4, TP30 to pin 5, TP31 to pin 7, TP32 to pin 9, TP33 to pin 11, TP34 to pin 13, TP35 to pin 15, TP36 to pin 17, TP37 to pin 19, TP38 to pin 21, TP39 to pin 23, and TP40 to pin 25. A 3V3 supply is connected to pin 26 and the MCU_3V3 pin.

Reset Circuit

MCU 3V3

R19 47k

C59 1nF 100V

RST/SBWDIO

J6

1 2 3

PUSH

S1

3 4 1 2

430481025816

SELECT PUSH BUTTON FUNC

The resistors on the ID[2:0] nets inform the firmware which device ID variant is on this board

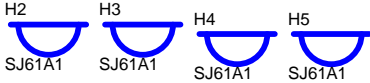
Device	ID1	ID2
DRV8213	1	1
DRV8214	1	0
DRV8234	0	0
DRV8215	0	1
DRV8235	Hi-Z	0

Type	ID3
Prerelease	0
Release	1

The diagram illustrates the ID[2:0] net configuration. Three MCU_3V3 pins are connected to ID1, ID2, and ID3. Each ID net has a 10k resistor to GND. ID1 and ID2 also have 10k resistors to MCU_3V3. ID3 has a 10k resistor to MCU_3V3. A common ground is connected to all three 10k resistors to GND.



PCB Number: MD069
PCB Rev: C



LBL1
PCB Label
THT-14-423-10
Size: 0.65" x 0.20 "

Label Table	
Variant	Label Text
001	DRV8214EVM
002	DRV8234EVM
003	DRV8215EVM
004	DRV8235EVM

ZZ1
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ4
Label Assembly Note
This Assembly Note is for PCB labels only

Orderable: DRV8235EVM		Designed for: Public Release	Mod. Date: 1/24/2024
TID #: N/A		Project Title: DRV8214/15_8234/35EVM	
Number: MD069	Rev: C	Sheet Title:	
SVN Rev: Unknown revision		Assembly Variant: 004	Sheet: 2 of 2
Drawn By: Jacob Thompson		File: MD069C_Hardware.SchDoc	Size: B
Engineer: Jacob Thompson		Contact: http://www.ti.com/support	

1

2

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