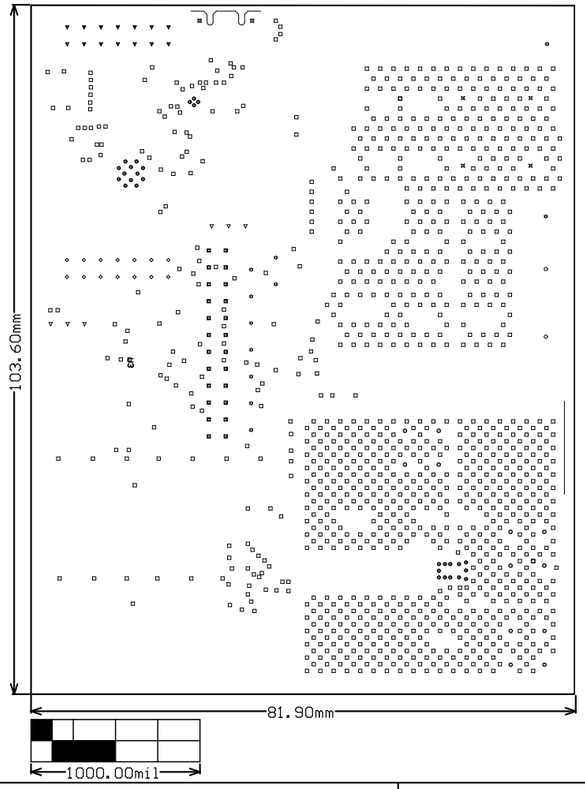
Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
◎	28	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	
□	1087	13.78mil (0.350mm)	PTH	Round	Top Layer - Bottom Layer	
◇	14	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	
▣	24	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer	+/-3.15mil
▽	6	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer	
▼	14	43.31mil (1.100mm)	PTH	Round	Top Layer - Bottom Layer	+/-1.97mil
○	2	51.18mil (1.300mm)	PTH	Round	Top Layer - Bottom Layer	
✪	12	62.99mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	+3.94mil/-0.00mil
⌘	4	62.99mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	
✡	11	63.00mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	
⊠	2	23.62mil (0.600mm)	PTH	Slot	Top Layer - Bottom Layer	
	1204 Total					

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		2.80mil		
	Dielectric 1	FR-4	11.40mil	4.2	
2	Signal Layer 1		1.40mil		
	Dielectric 2	FR-4	31.00mil	4.2	
3	Signal Layer 2		1.40mil		
	Dielectric 3	FR-4	11.40mil	4.2	
4	Bottom Layer		2.80mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING: 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-VO REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL WAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL WAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE:
DRV8145S/H-QIEVM (VQFN)

DESIGNED FOR:
Public Release

FILE NAME:
MD044A_DRV8145-QIEVM_VQFN.PcbDoc

ENGINEER:
Michael Erdahl

LAYOUT BY:
Michael Erdahl

SCALE: 1.12

ALTIUM DESIGNER VERSION:
22.10.1.41

ALL ARTWORK VIEWED FROM TOP SIDE | BOARD #: MD044 | REV: A | SVN REV: 9497b7228a77c0994b878eeba39881ad4daca2c0 [Locally Modified]
LAYER NAME = [illegible]ions | TID #: N/A
PLOT NAME = Fabrication Drawing | GENERATED : 10/19/2022 2:54:32 PM | TEXAS INSTRUMENTS

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