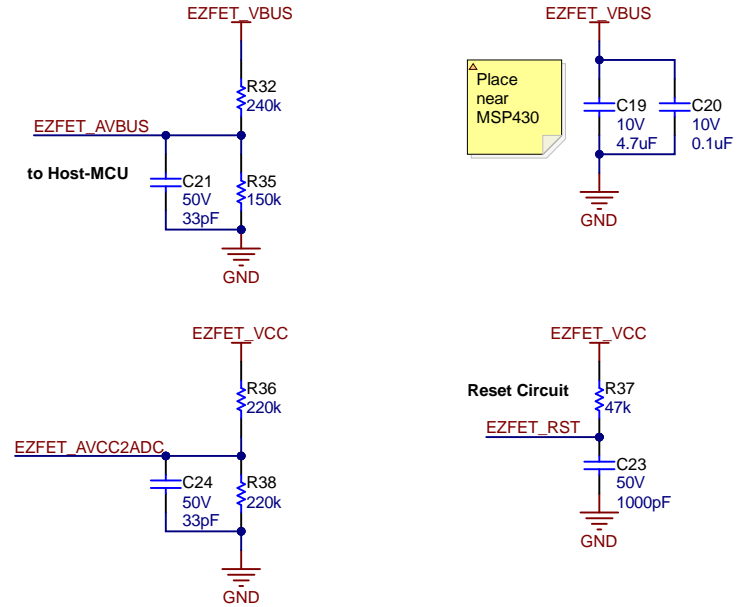
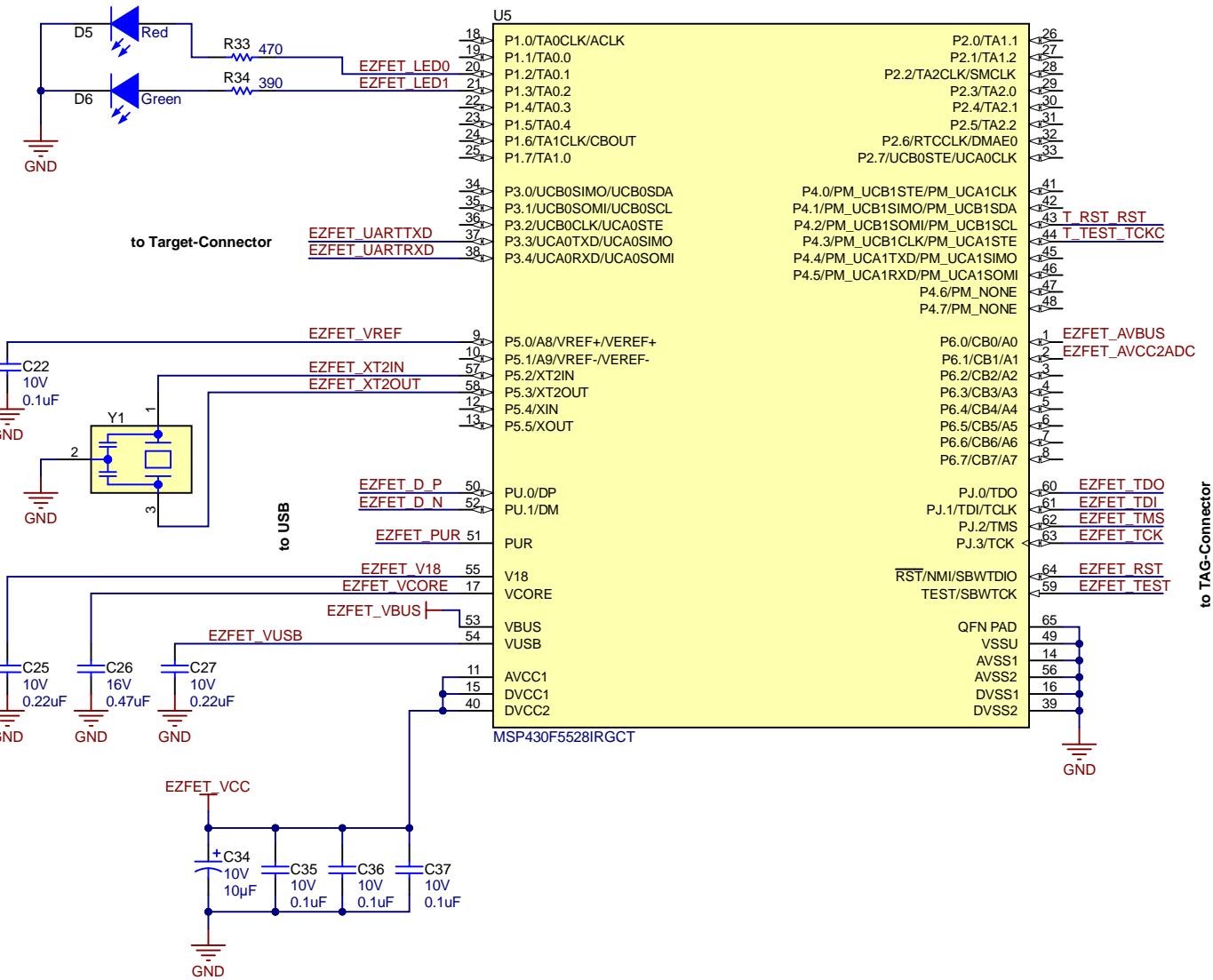
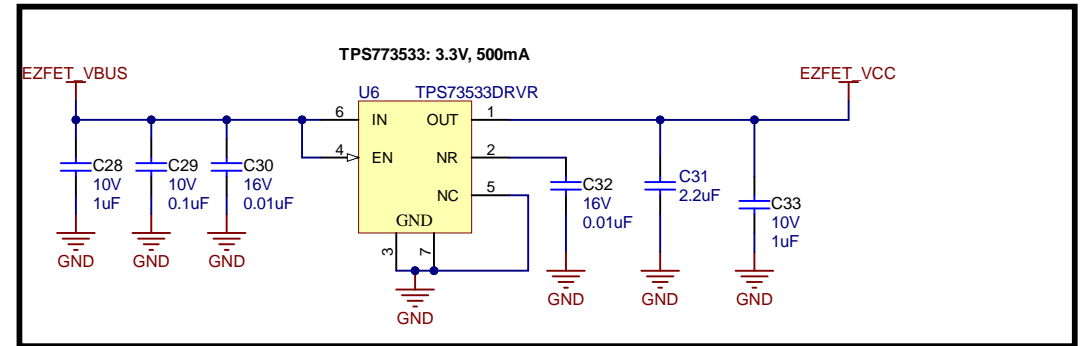


## Host MCU for Emulation

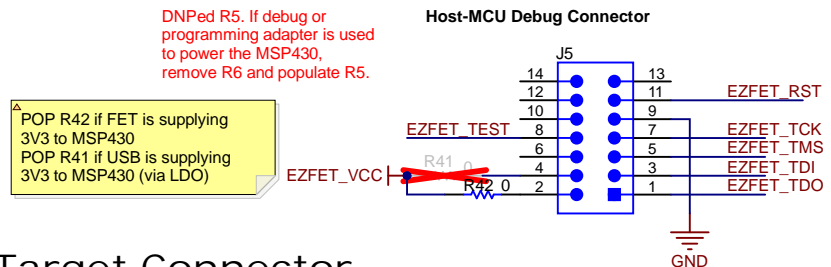


## 3.3V Power (EZFET\_VCC)

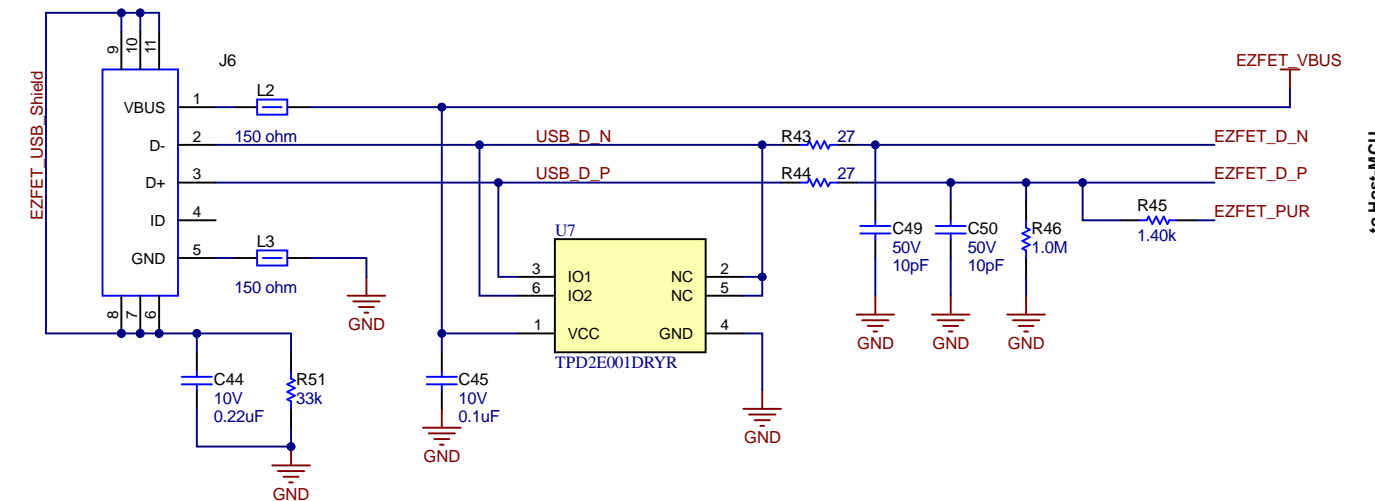


## JTAG-Connector (Host Debug)

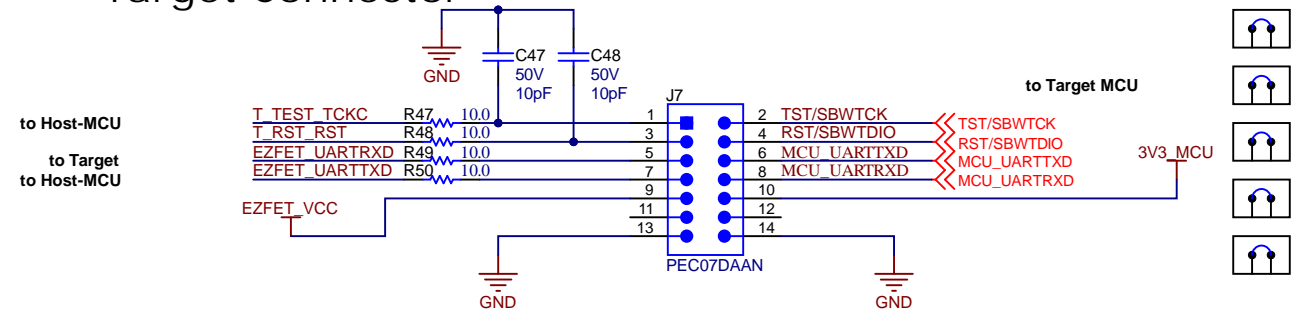
DNPed R5. If debug or programming adapter is used to power the MSP430, remove R6 and populate R5.



## USB-I-Interface



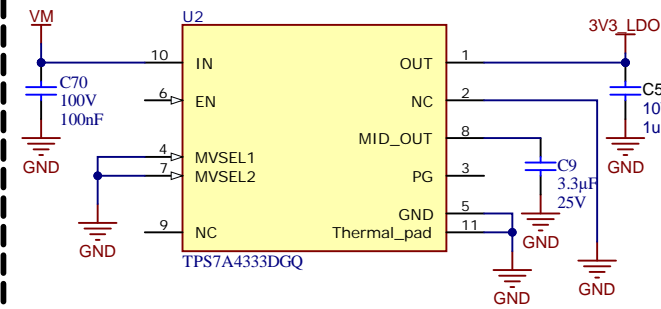
## Target Connector



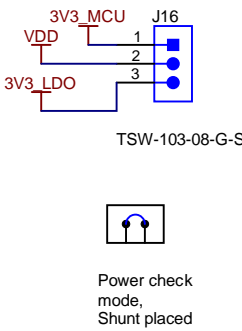
Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Orderable: DRV8263H-Q1EVM	Designed for: Public Release	Mod. Date: 8/16/2024
TID #: N/A	Project Title: DRV8263S/H-Q1EVM VQFN	
Number: MD093	Rev: E1	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: 002	Sheet: 1 of 3
Drawn By:	File: ezFET.SchDoc	Size: B
Engineer: Jacob Thompson	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	<a href="http://www.ti.com">http://www.ti.com</a>

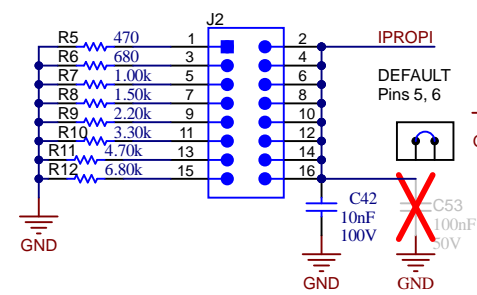
### 3.3V LDO



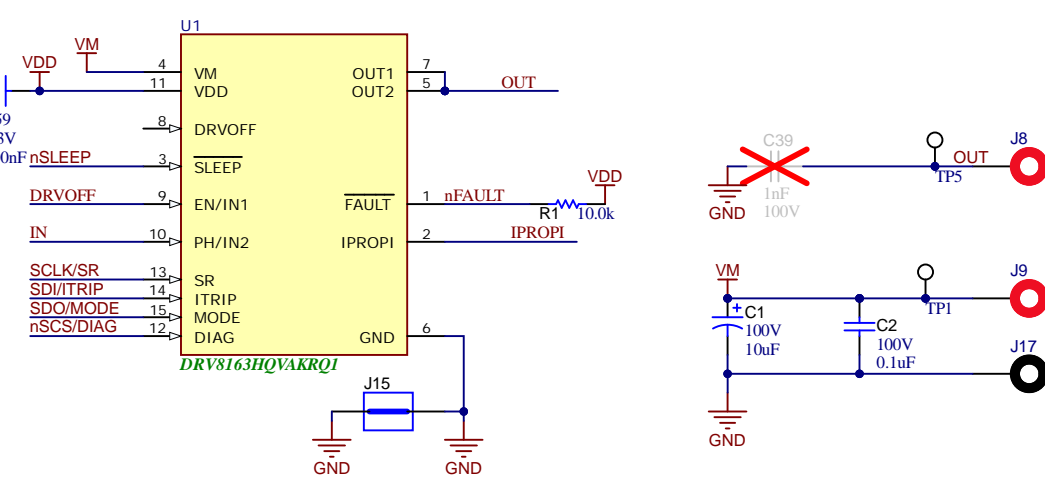
## Power Check



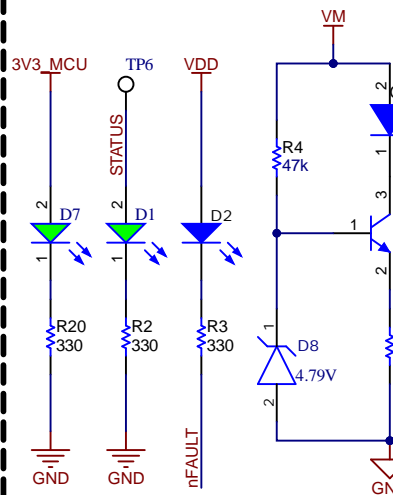
$$ITRIP = V(TRIP)/R(IPROPI) * A\_IPROPI$$



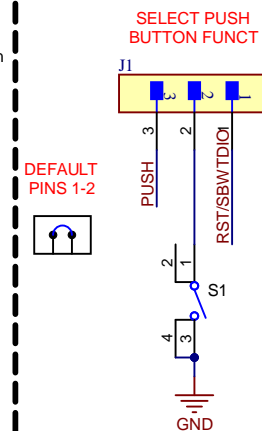
## DRV8163S/H-Q1 VQFN



## LEDS



## BUTTON




## ANALOG CONTROL SIGNALS (H-variant only)

ITRIP  
Levels  
1 0v  
2 1.65v  
3 1.98v  
4 2.31v  
5 2.64v  
6 2.97v


ITRIP	
PINS	ITRIP
1, 2	LVL1
3, 4	LVL2
5, 6	LVL3
7, 8	LVL4
9,10	LVL5
DNI	LVL6

DEFAULT  
Pins 3, 4




DIAG	
PINS	DIAG
1, 2	LVL1
3, 4	LVL2
5, 6	LVL3
7, 8	LVL4
9,10	LVL5
DNI	LVL6

DEFAULT  
Pins 3, 4



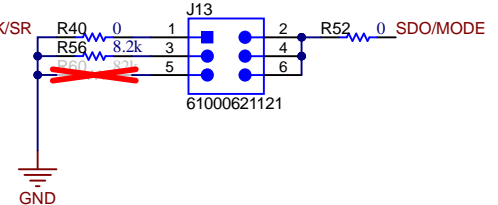
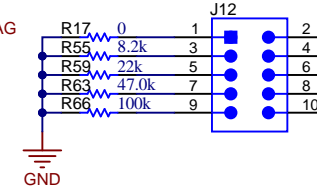
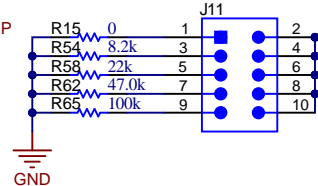
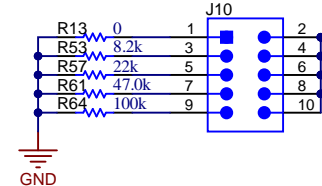

PINS	SR
1, 2	LVL1
3, 4	LVL2
5, 6	LVL3
7, 8	LVL4
9,10	LVL5
DNI	LVL6

DEFAULT  
Pins 3, 4

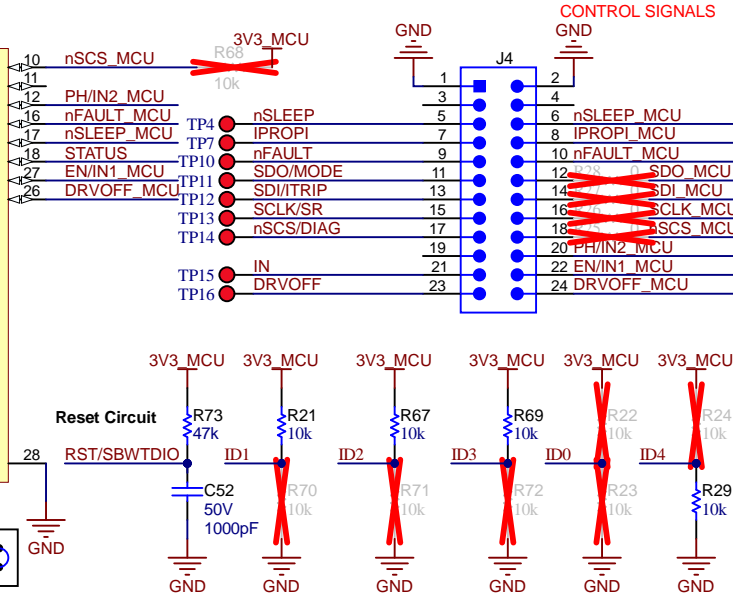
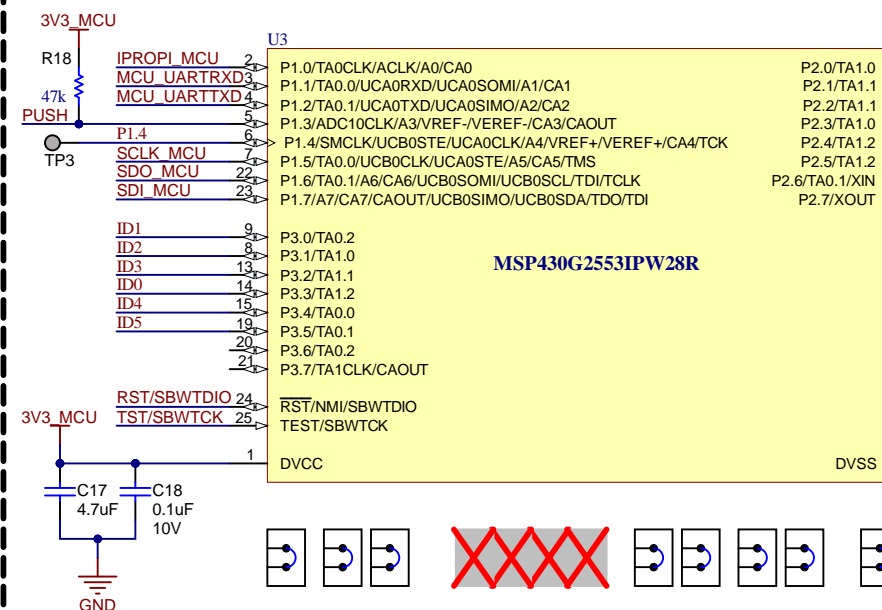


MOD	
PINS	MODE
1, 2	LVL1
3, 4	LVL2
5, 6	LVL3
DNI	LVL4

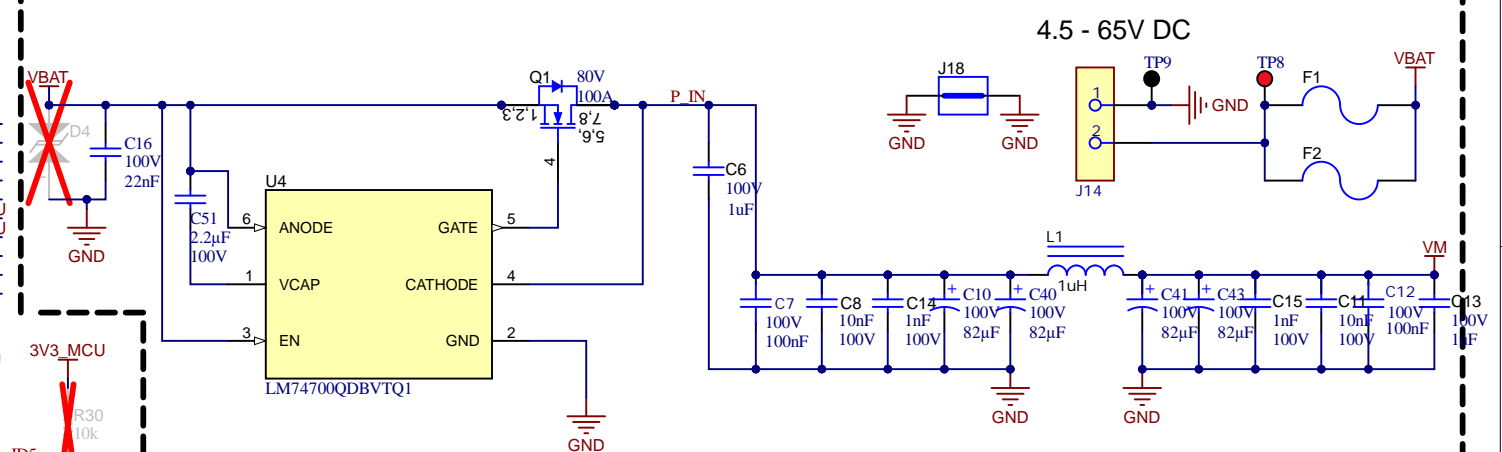
DEFAULT  
Pins 5,6



## MSP430



## MAIN INPUT SUPPLY REVERSE PROTECTION & FILTER



MP1

RBS-37BK

MP2

RBS-37BK

MP3

RBS-37BK

MP4

RBS-37BK

FID1

FID2

FID3

PCB Number: MD093

PCB Rev: E1

PCB

LOGO

Texas Instruments



PCB

LOGO

FCC disclaimer

PCB

LOGO

WEEE logo



CAUTION HOT SURFACE



CAUTION HOT SURFACE

PCB

LOGO

CAUTION. READ USER GUIDE BEFORE USE

LBL1

PCB Label

THT-14-423-10

Size: 0.65" x 0.20 "

ZZ1

Label Assembly Note

This Assembly Note is for PCB labels only

ZZ2

Assembly Note

These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Variant/Label Table	
Variant	Label Text
001	DRV8263S-Q1EVM
002	DRV8263H-Q1EVM