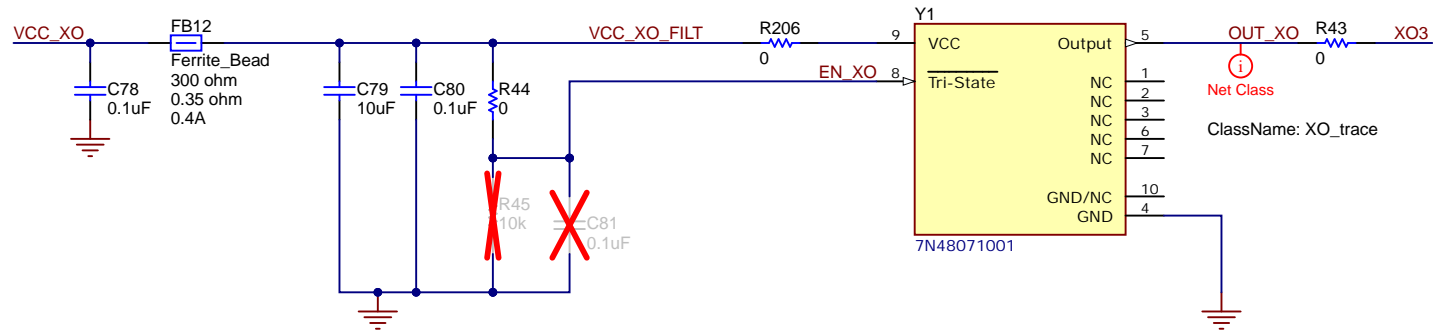
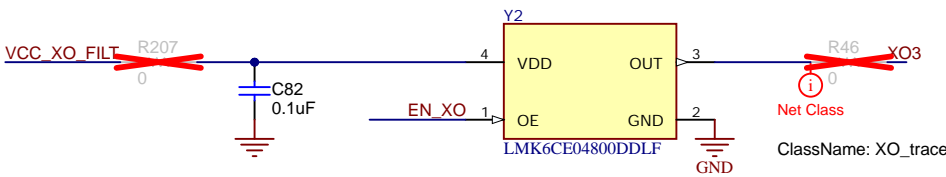


3.3V LVCMOS XO (multiple footprints)

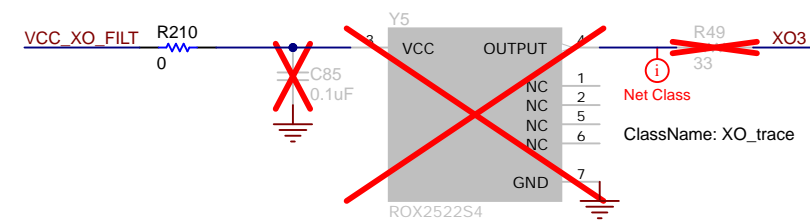
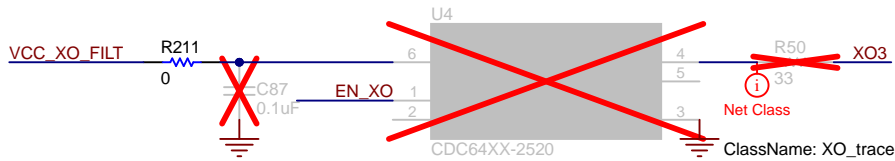
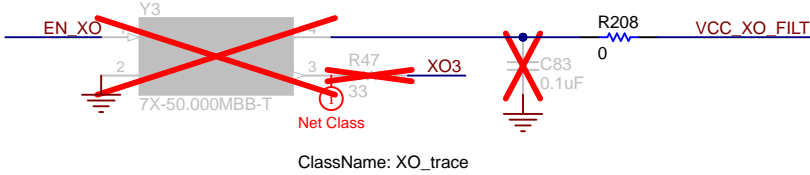
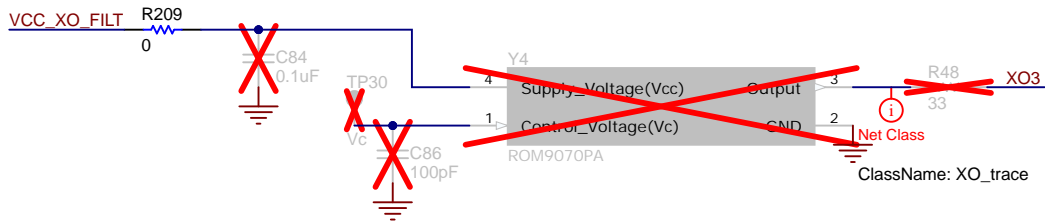
48 MHz TCXO
Connected to LMK device by default.



48 MHz BAW Oscillator
Not connected to LMK device by default.

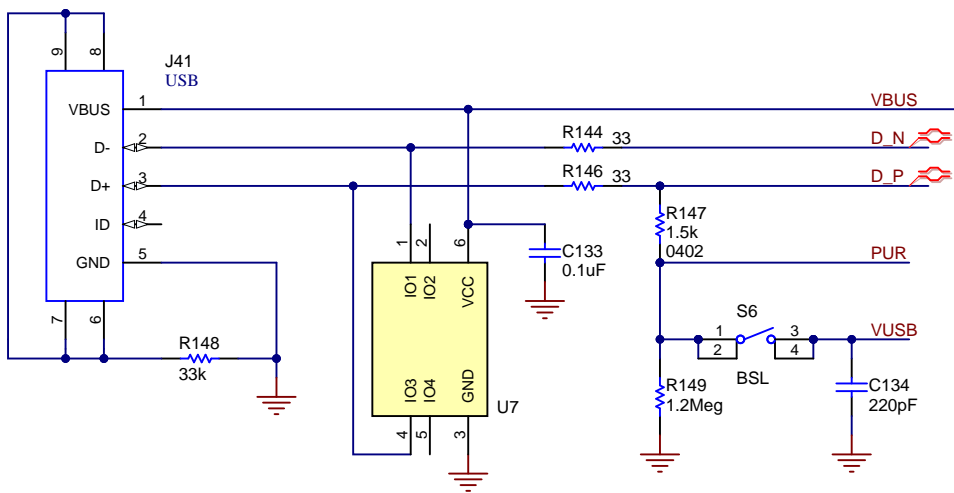


Other footprint options available (not populated):

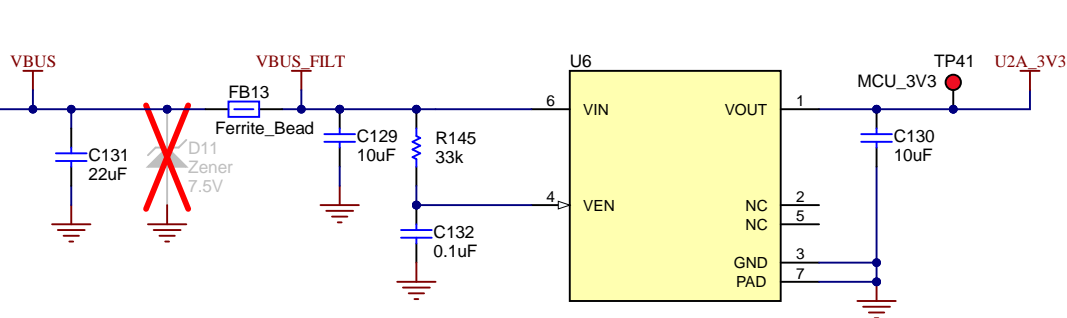


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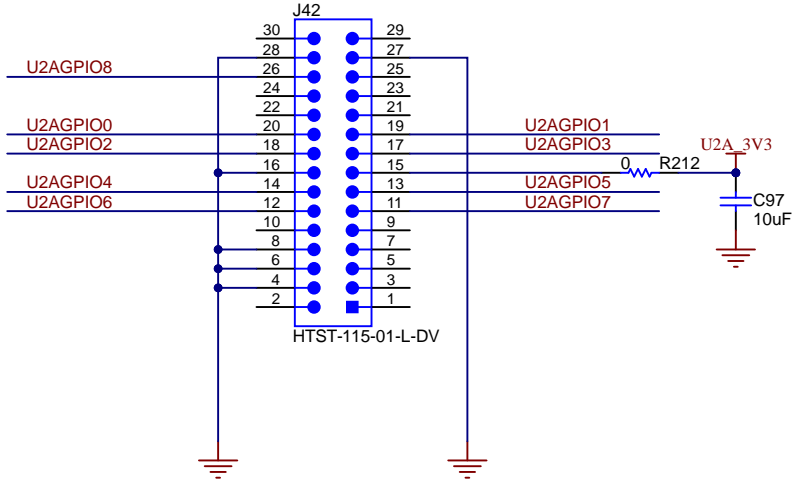
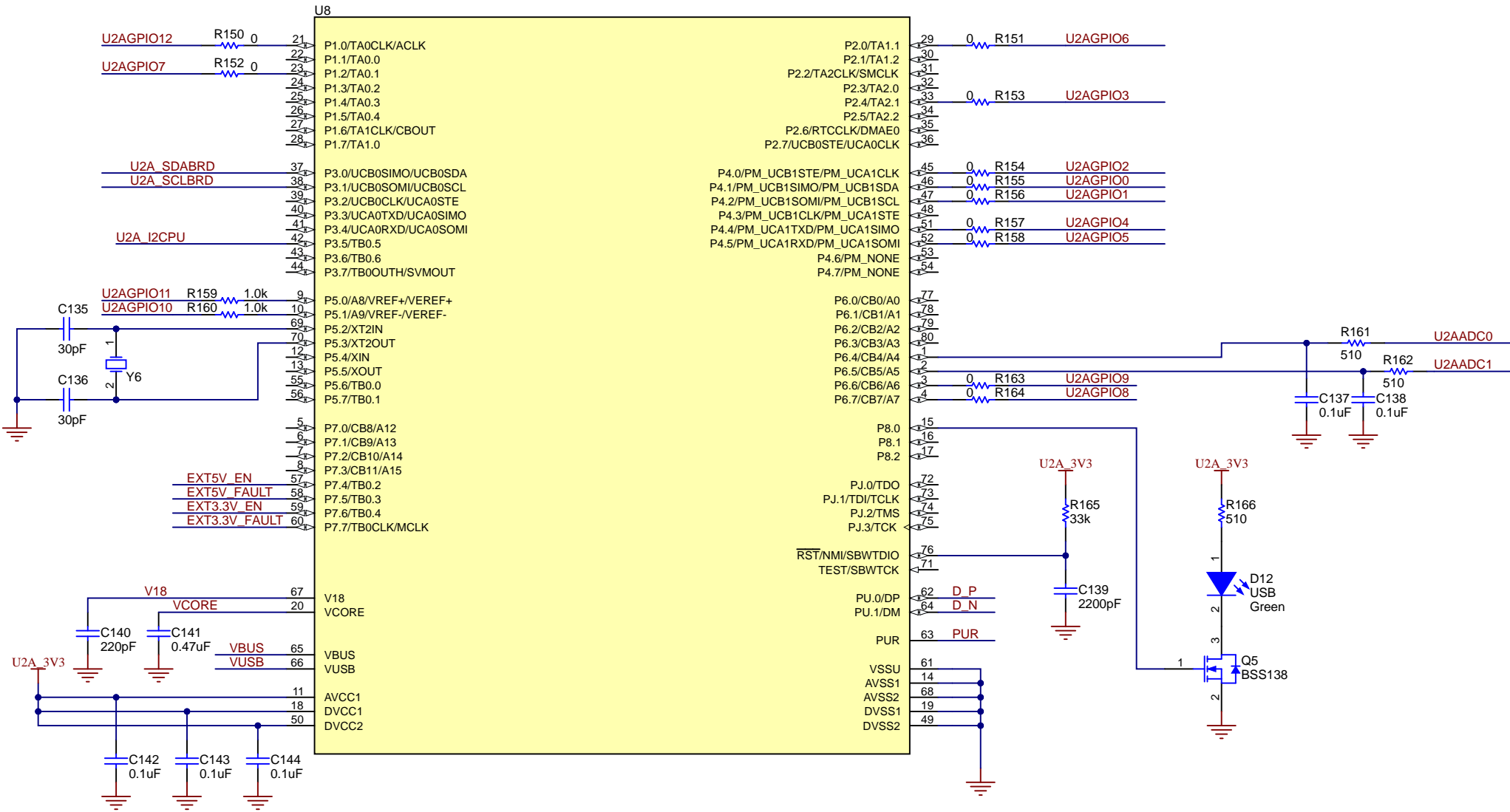
USB MINI-B CONNECTOR



3.3V, 150mA REGULATOR

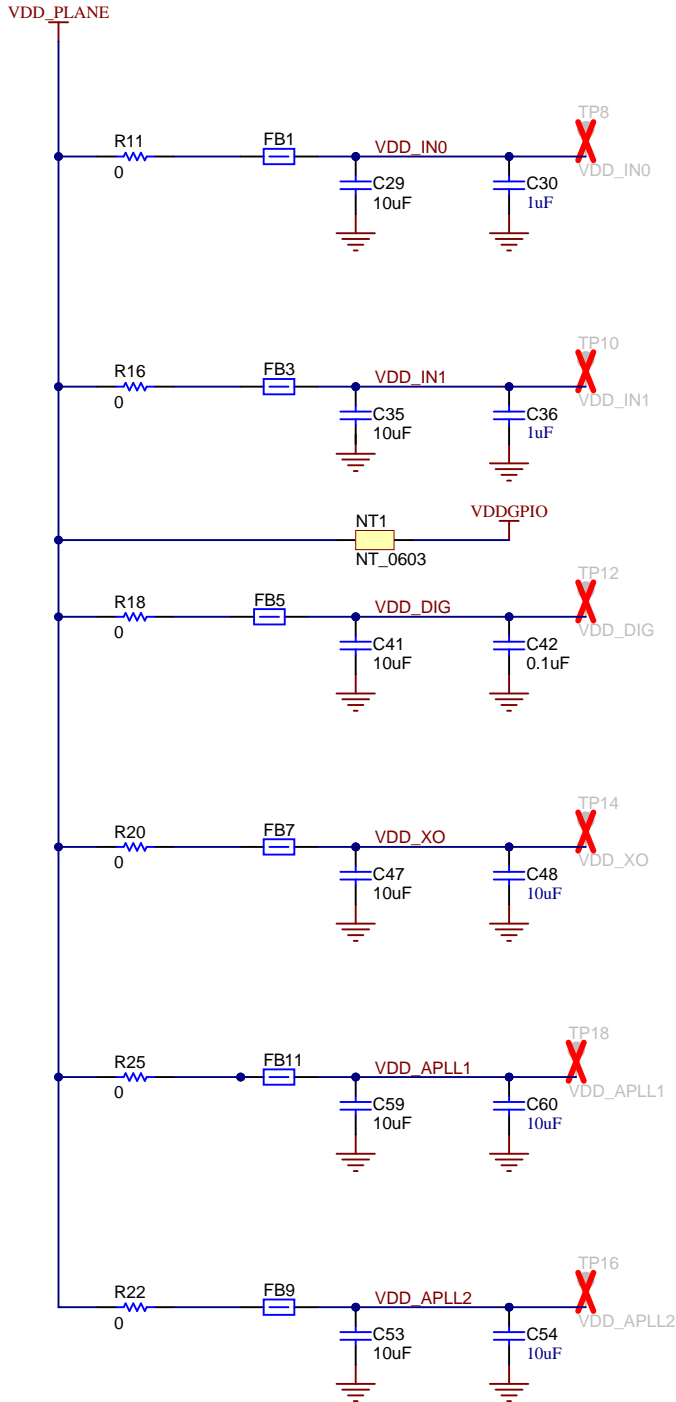


MSP430 MCU -- "USB2ANY" (U2A) CONTROLLER

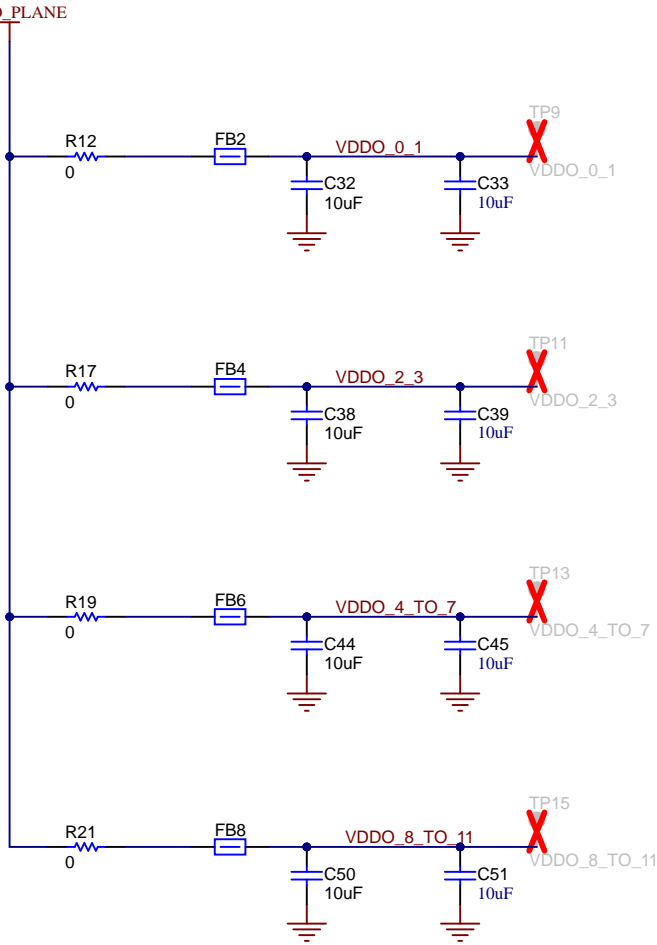


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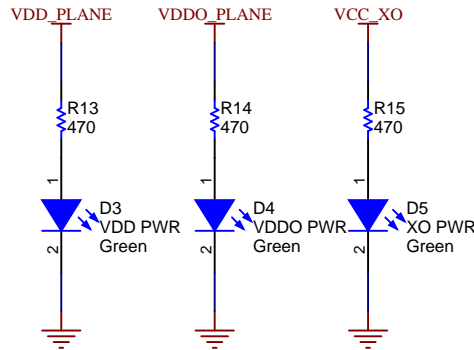
VDD CORE SUPPLY DIST & FILTERING



VDDO OUTPUT SUPPLY DIST & FILTERING



POWER LED INDICATORS (DUT, XO, TCXO)



GND TEST POINTS

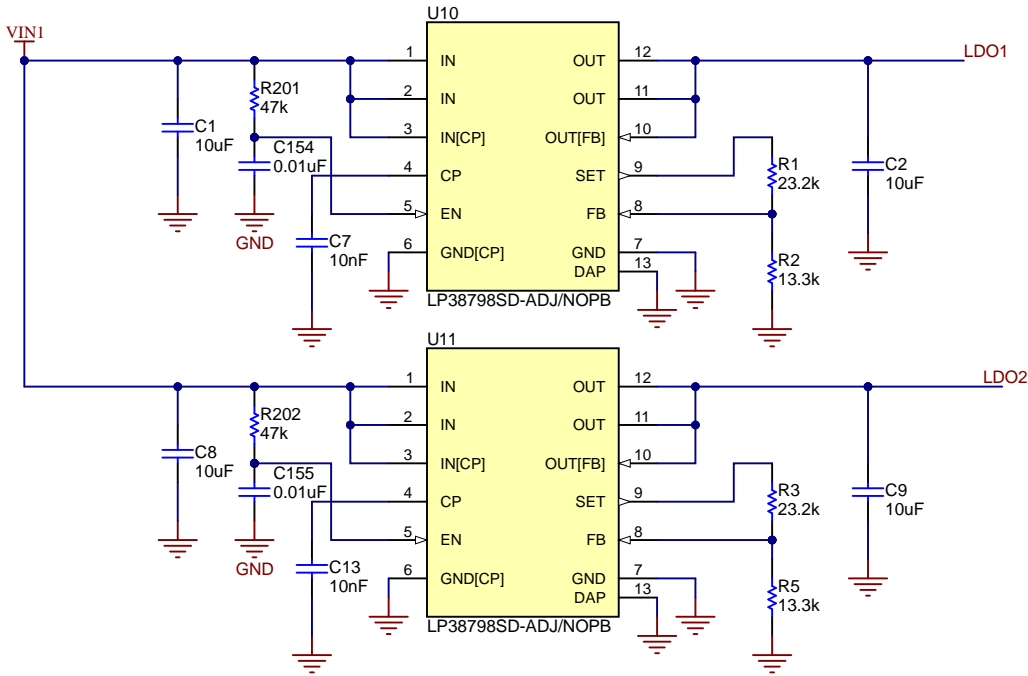


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Orderable: ChangeMe in variant		Designed for: Public Release		Mod. Date: 7/7/2025	
TID #: N/A		Project Title: LMK5B12212EVM			
Number: DC210		Rev: B		Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001		Sheet: 2 of 3	
Drawn By:		File: DC210B_PowerDist.SchDoc		Size: B	
Engineer: Riley Nguyen		Contact: http://www.ti.com/support		http://www.ti.com	
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1-A LDO REG (LDO1, LDO2) for DUT VDD & VDDO rails

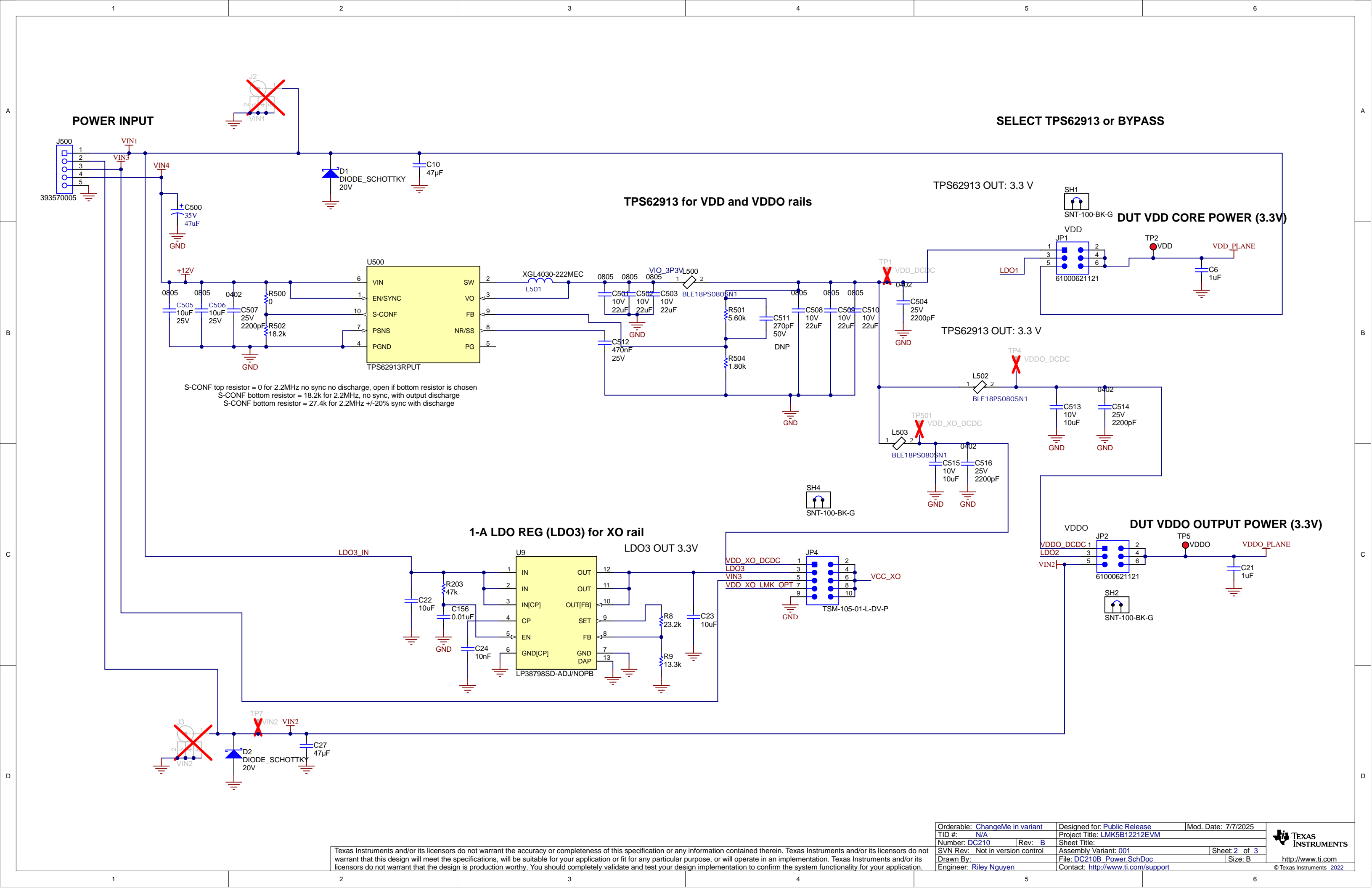


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TID #: N/A	Project Title: LMK5B12212EVM	
Number: DC210	Rev: B	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 2 of 3
Drawn By:	File: DC210B_Power_Alternate.SchDoc	Size: B
Engineer: Riley Nguyen	Contact: http://www.ti.com/support	

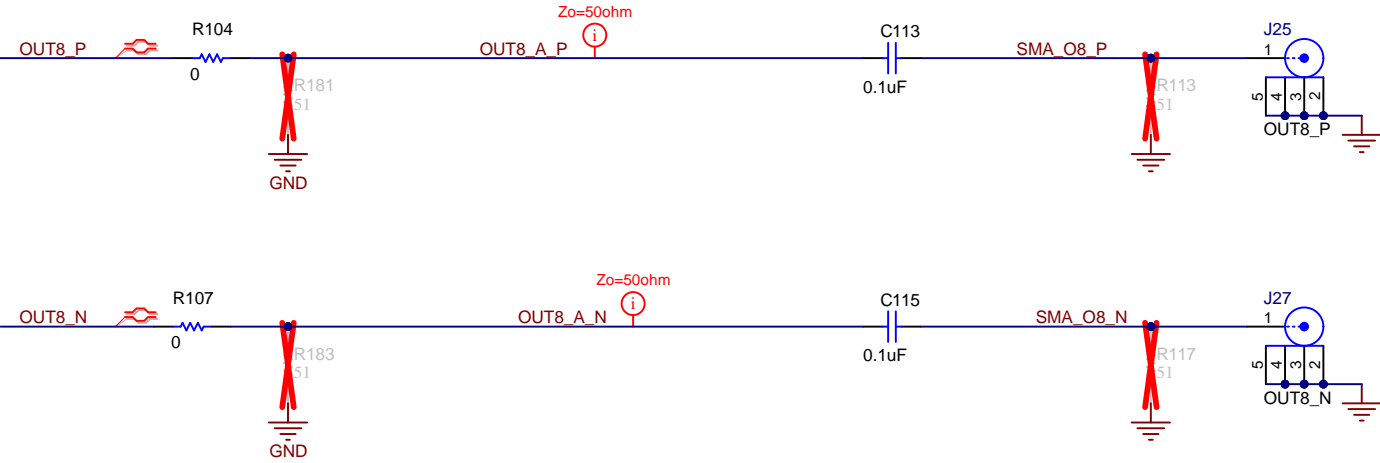
 **TEXAS
INSTRUMENTS**

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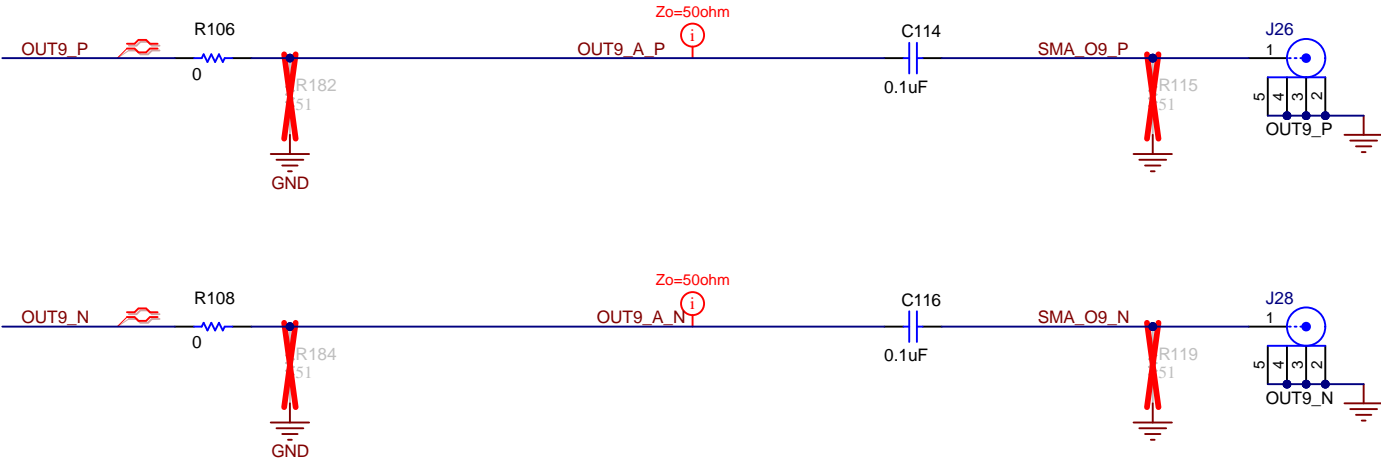


OUT8-OUT11 CLOCK OUTPUTS

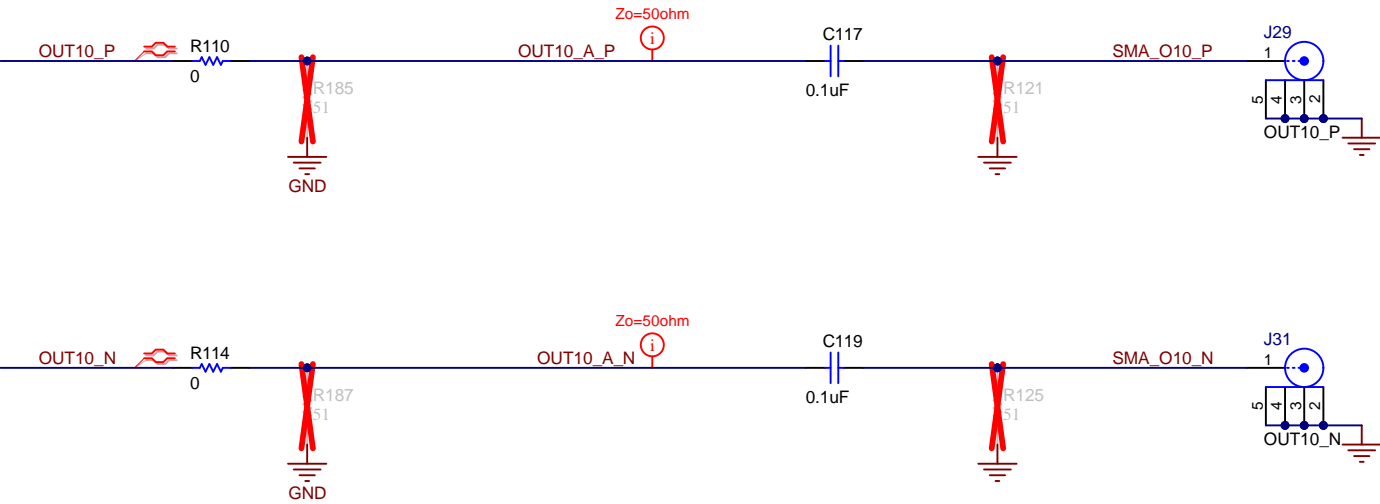
OUT8, Supported formats: LVDS, HSDS, and HCSL; Source may be VCO2 or VCO3
Default: AC-coupled (for HSDS outputs)



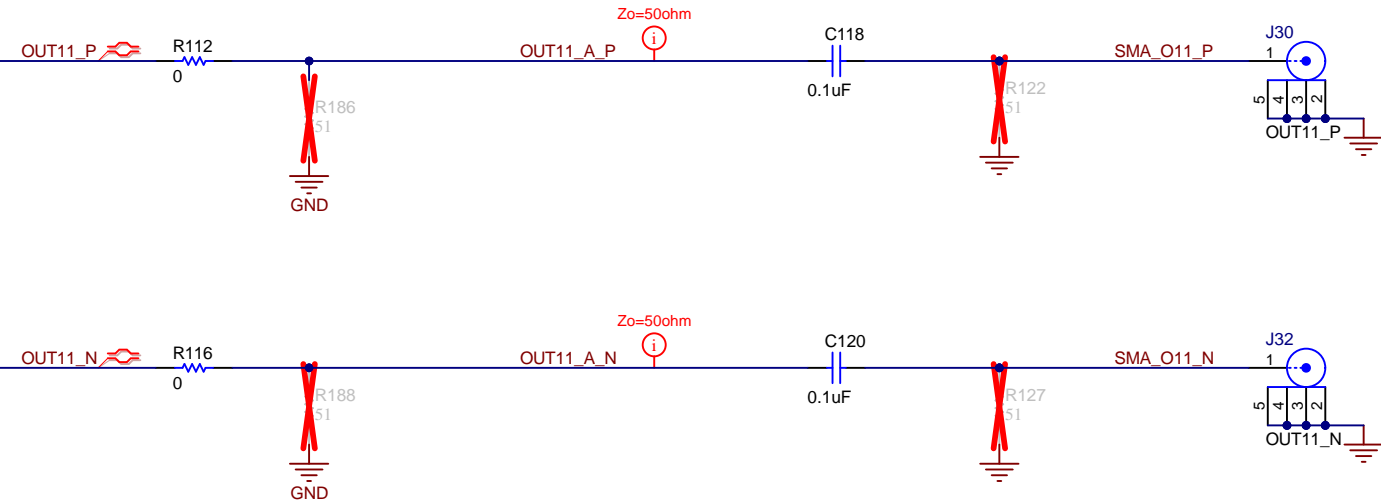
OUT9, Supported formats: LVDS, HSDS, and HCSL; Source may be VCO2 or VCO3
Default: AC-coupled (for HSDS outputs)



OUT10, Supported formats: LVDS, HSDS, and HCSL; Source may be VCO2 or VCO3
Default: AC-coupled (for HSDS outputs)




OUT11, Supported formats: LVDS, HSDS, and HCSL; Source may be VCO2 or VCO3
Default: AC-coupled (for HSDS outputs)



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TID #: N/A	Project Title: LMK5B12212EVM	
Number: DC210	Rev: B	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 2 of 3
Drawn By:	File: DC210B_Outputs_C.SchDoc	Size: B
Engineer: Riley Nguyen	Contact: http://www.ti.com/support	



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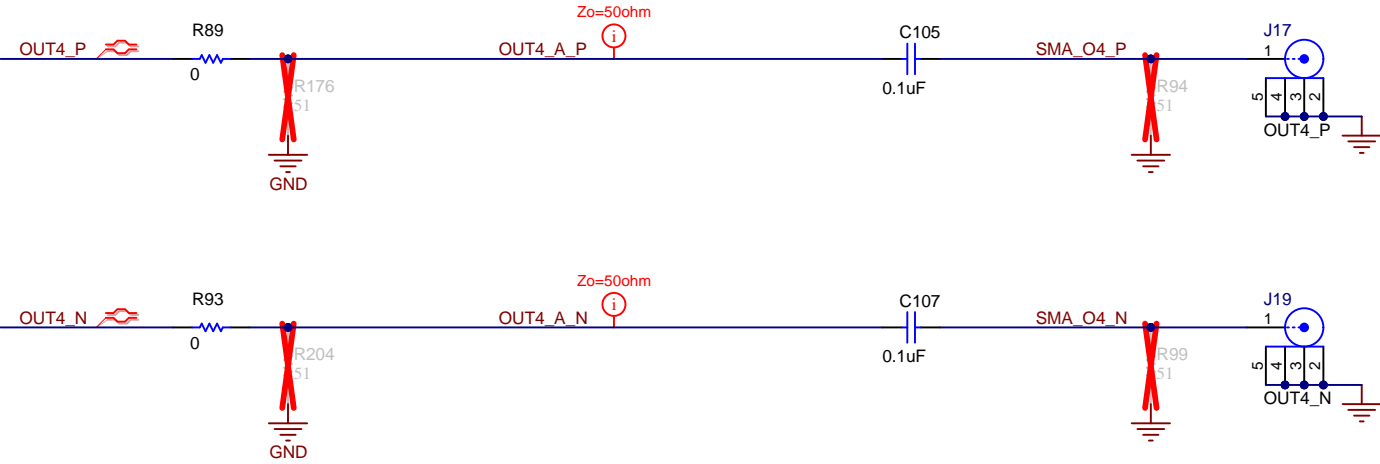
<http://www.ti.com>

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OUT4 to OUT7 CLOCK OUTPUTS

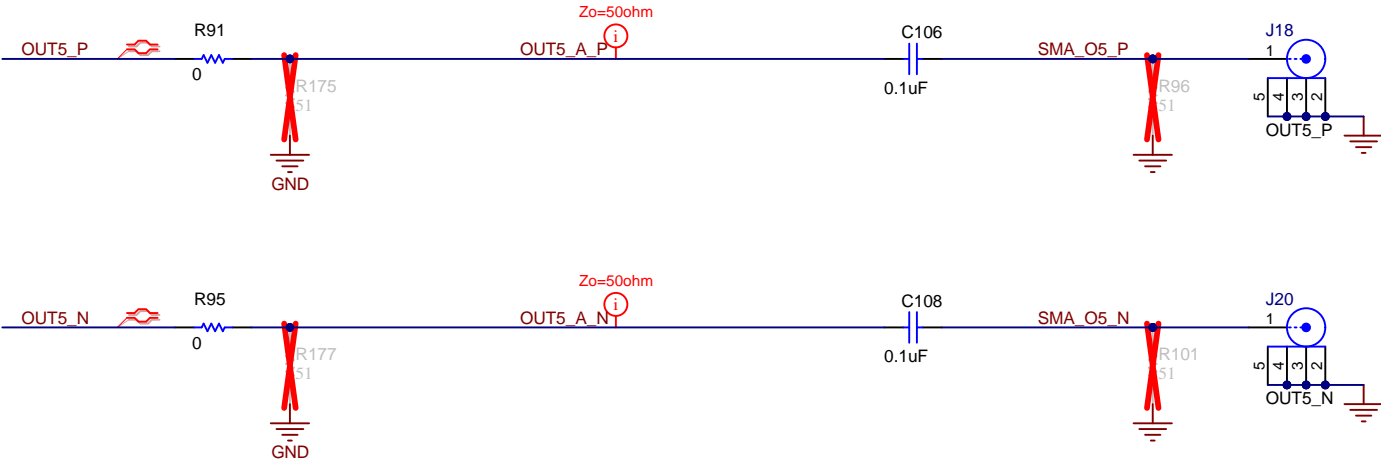
OUT4, Supported formats: LVDS, HSDS, and HCSL Source may be VCO2 or VCO3

Default: AC-coupled (for HSDS outputs)



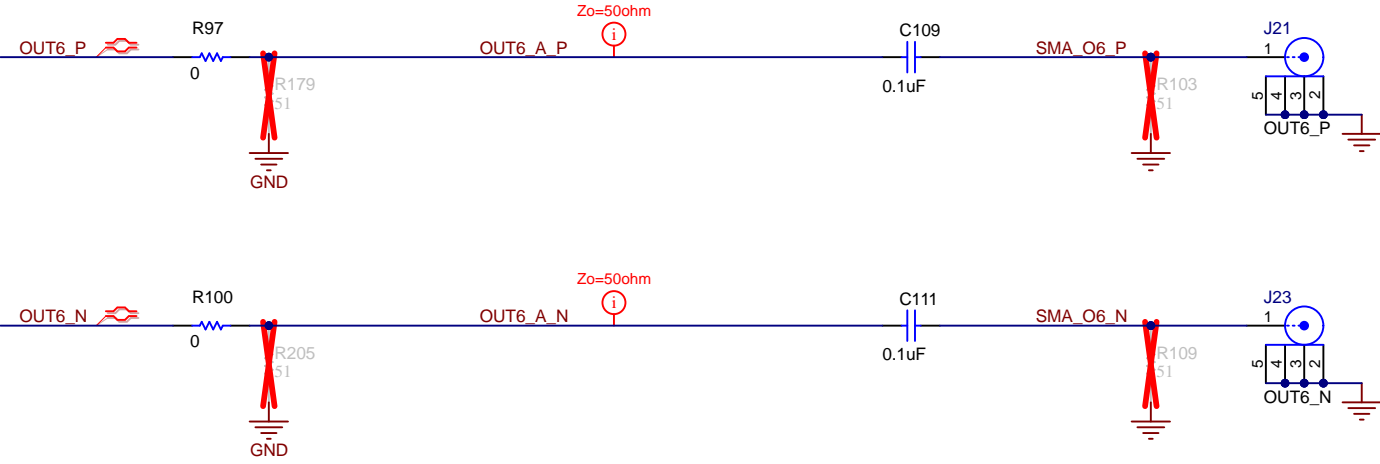
OUT5, Supported formats: LVDS, HSDS, and HCSL; Source may be VCO2 or VCO3

Default: AC-coupled (for HSDS outputs)



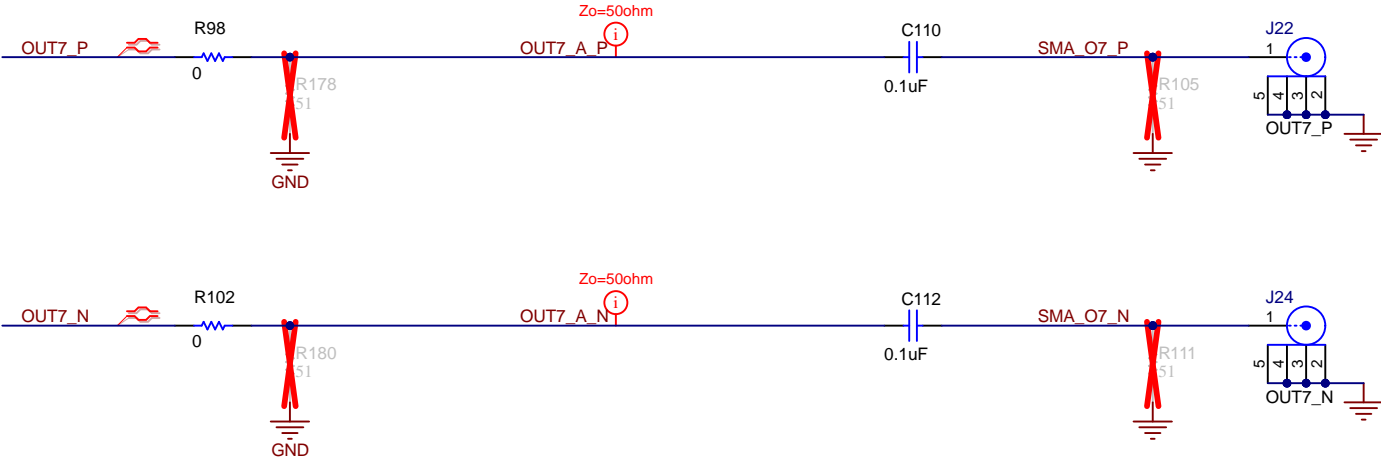
OUT6, Supported formats: LVDS, HSDS, and HCSL Source may be VCO2 or VCO3

Default: AC-coupled (for HSDS outputs)




OUT7, Supported formats: LVDS, HSDS, and HCSL; Source may be VCO2 or VCO3

Default: AC-coupled (for HSDS outputs)



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TID #: N/A	Project Title: LMK5B12212EVM	
Number: DC210	Rev: B	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 2 of 3
Drawn By:	File: DC210B_Outputs_B.SchDoc	Size: B
Engineer: Riley Nguyen	Contact: http://www.ti.com/support	

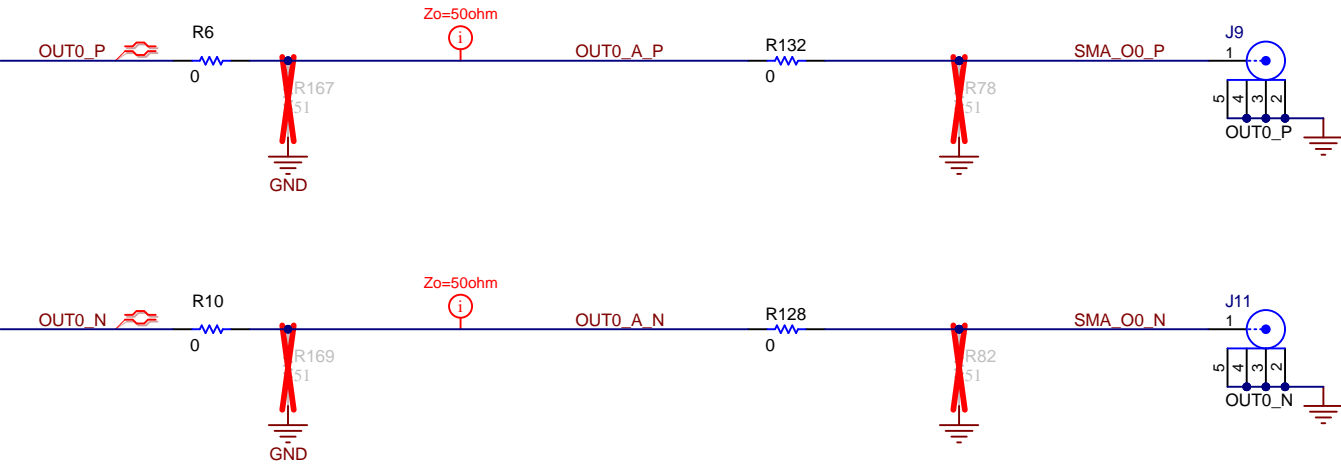


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OUT0-OUT3 CLOCK OUTPUTS

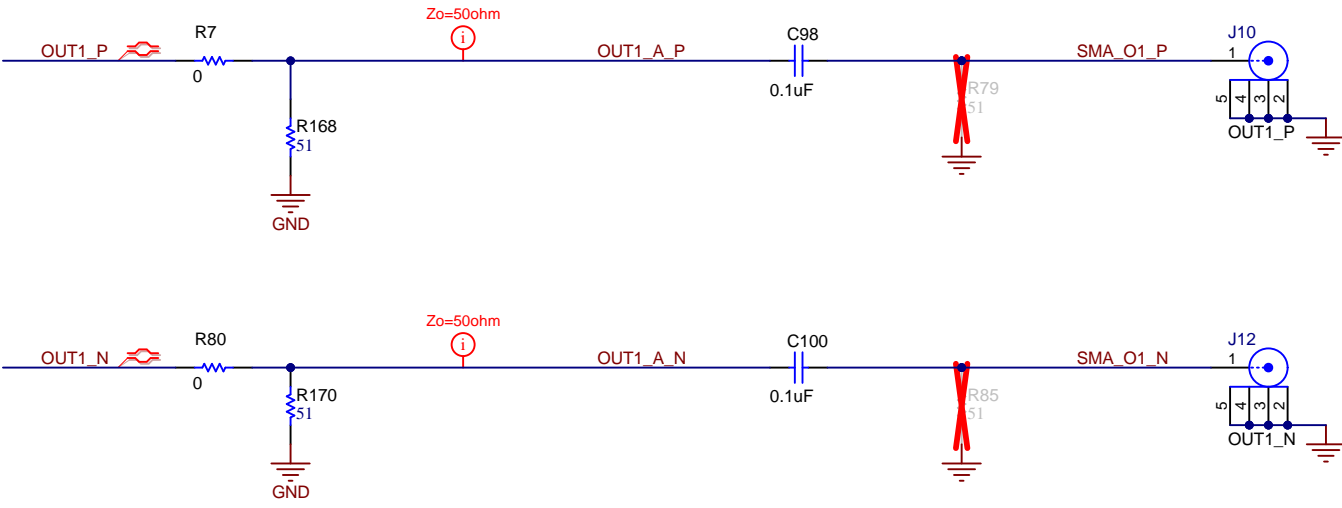
OUT0, Supported formats: CMOS, LVDS, HSDS, and HCSL. Source may be XO, REF0-1, or VCO1-3

Default: DC-coupled, no termination (for 1 Hz outputs)



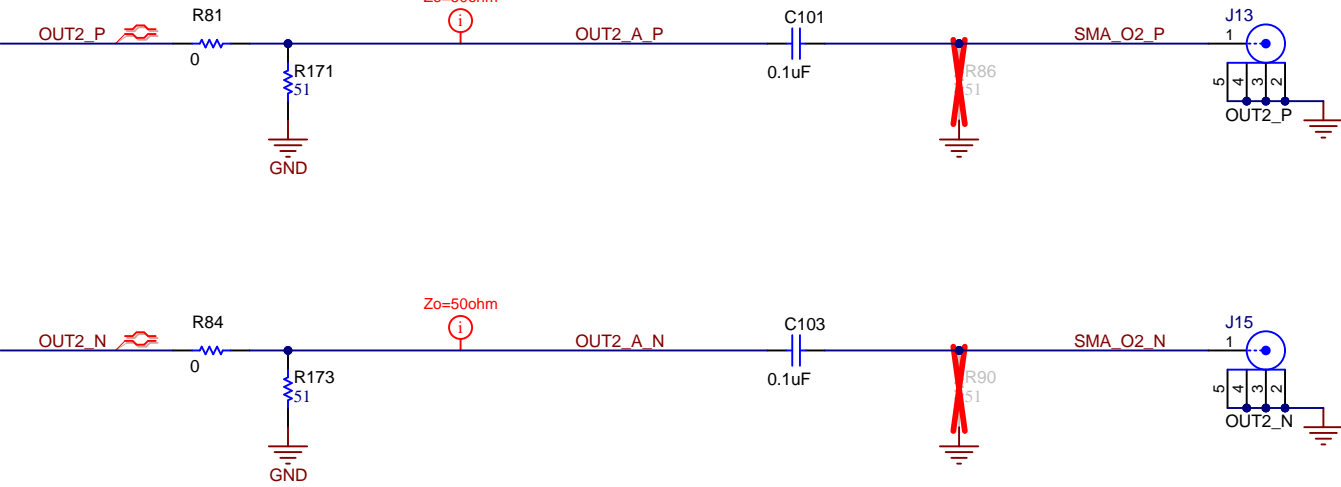
OUT1, Supported formats: CMOS, LVDS, HSDS, and HCSL. Source may be XO, REF0-1, or VCO1-3

Default: 50-ohms to GND on each P and N then AC-coupled (for HCSL outputs)



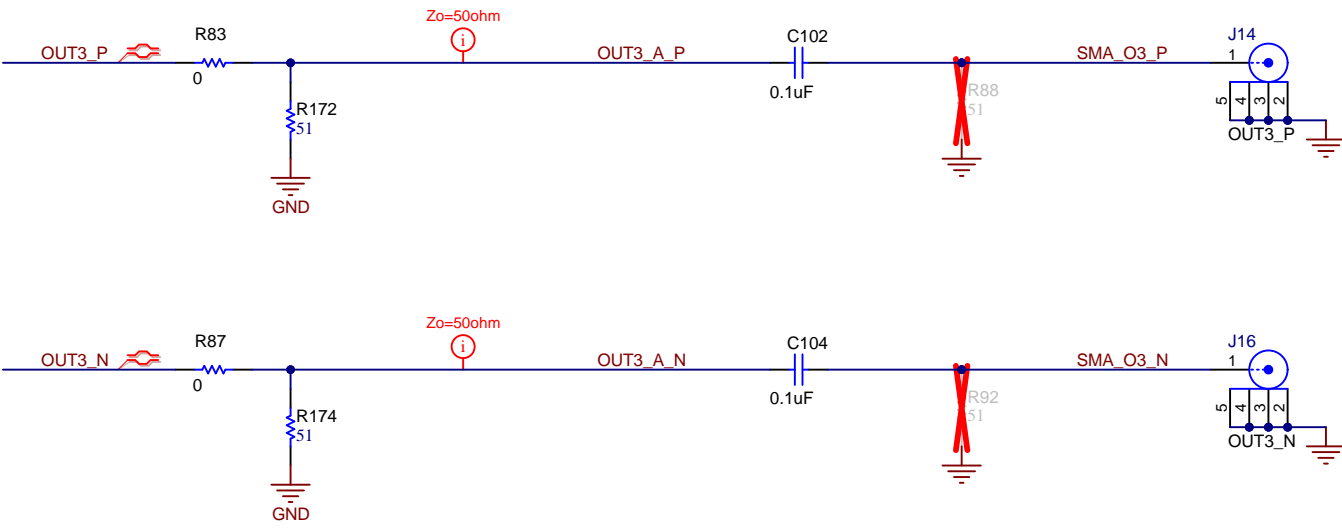
OUT2, Supported formats: LVDS, HSDS, and HCSL. Source may be VCO1, VCO2, or VCO3

Default: 50-ohms to GND on each P and N then AC-coupled (for HCSL outputs)



OUT3, Supported formats: LVDS, HSDS, and HCSL. Source may be VCO1, VCO2, or VCO3

Default: 50-ohms to GND on each P and N then AC-coupled (for HCSL outputs)



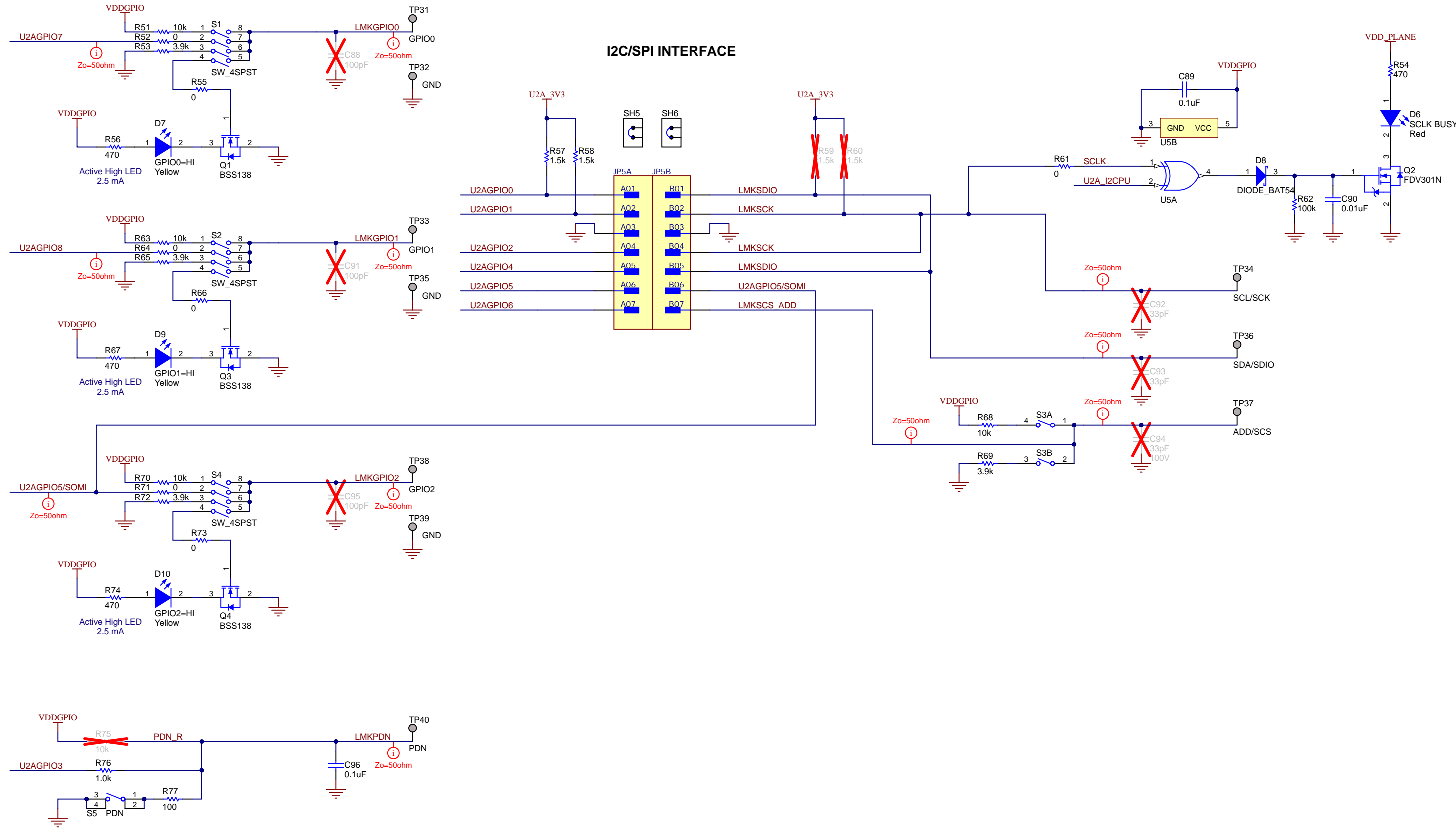
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TID #: N/A		Project Title: LMK5B12212EVM			
Number: DC210		Rev: B		Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001		Sheet: 2 of 3	
Drawn By:		File: DC210B_Outputs_A.SchDoc		Size: B	
Engineer: Riley Nguyen		http://www.ti.com			
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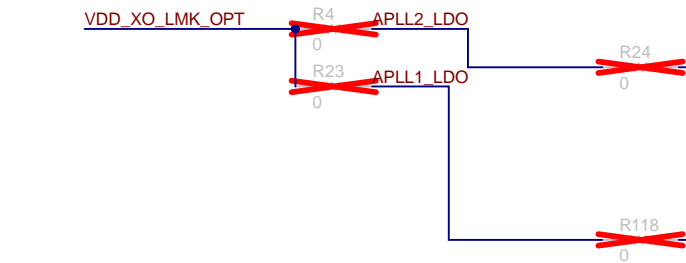
GPIO LEDs

I2C/SPI INTERFACE

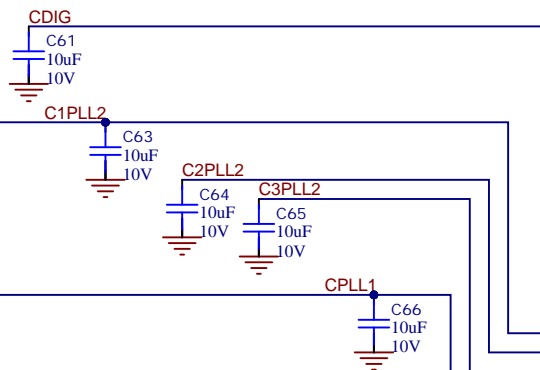


Optional XO Supply using APLL LDOs (1.8 - 2.6 V)

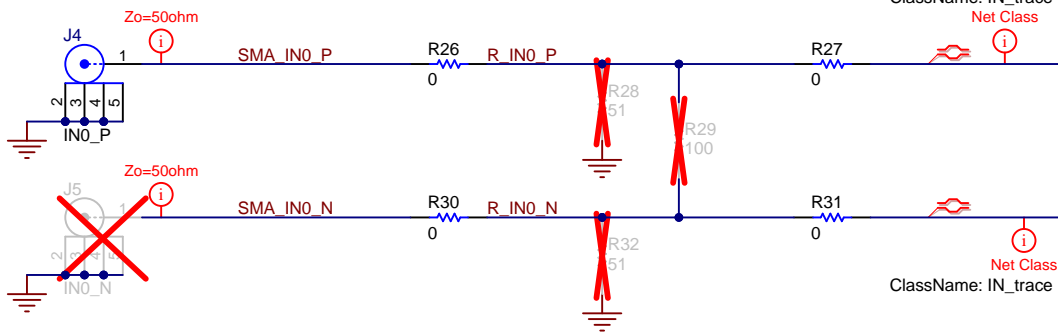
Default: XO supply from DCDC. R4 and R23 are DNI. Refer to JP4.



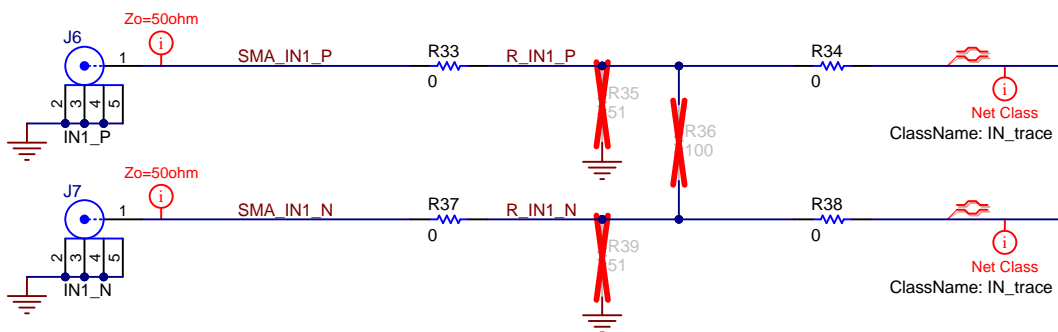
DUT LDO BYPASS CAPS



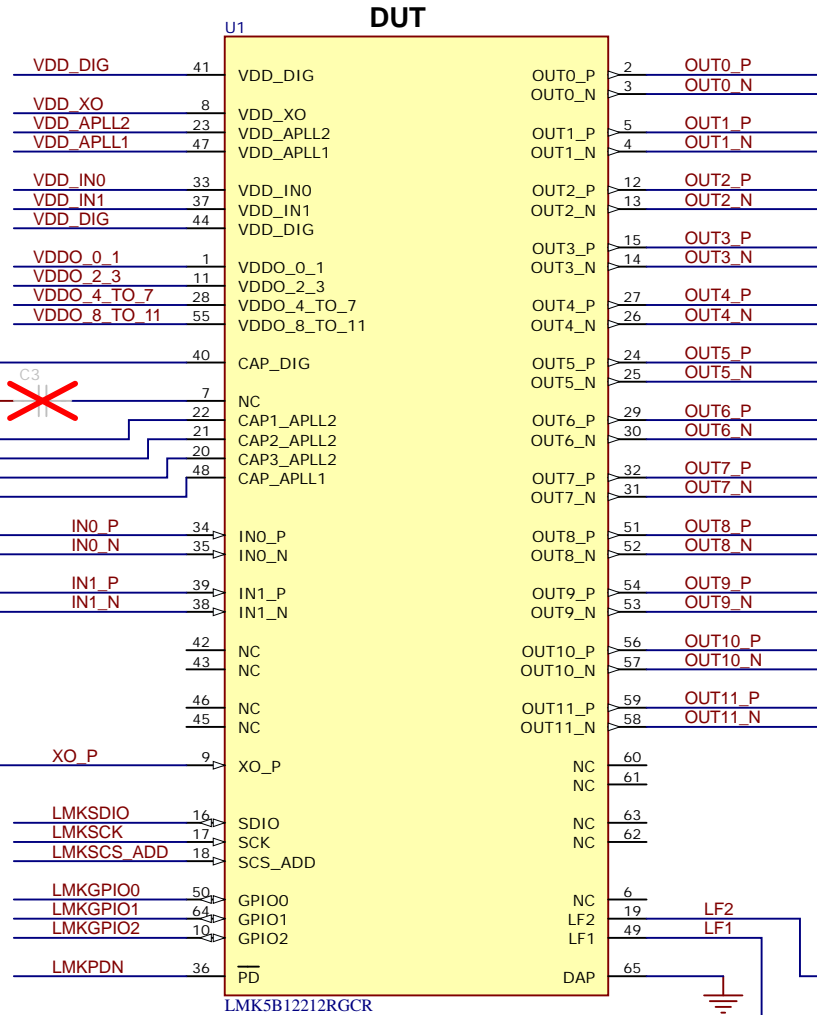
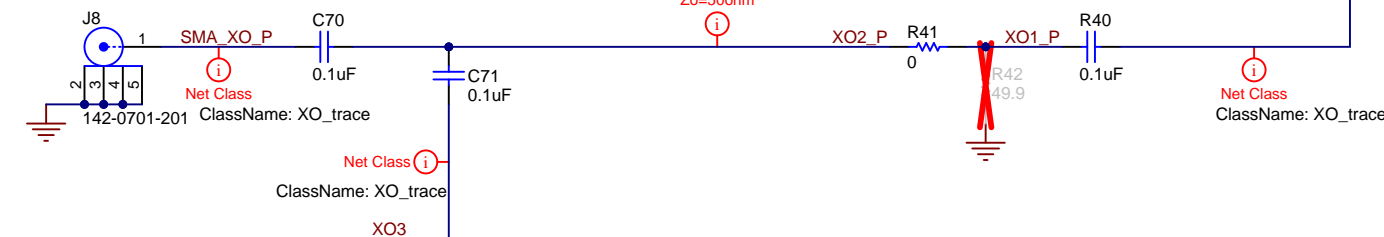
DPLL INPUT 0



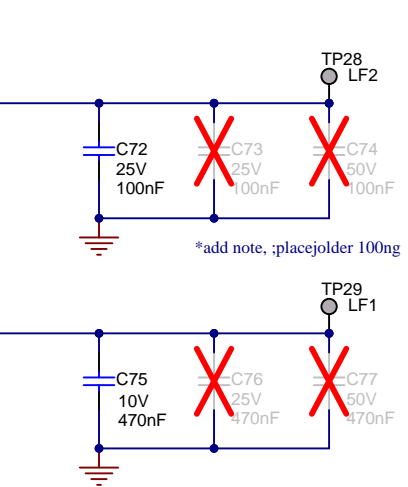
DPLL INPUT 1



EXT. SMA XO CLK



LOOP FILTER C2 SELECTION



STANDOFF HARDWARE

H1



SJ61A6

H2



SJ61A6

H3



SJ61A6

H4



SJ61A6

H5



SJ61A6

H6



SJ61A6

MH1



MTG_HOLE



FID1



FID2



FID3



FID4



FID5



FID6

PCB Number: DC210

PCB Rev: A

Printed Circuit Board

PCB

LOGO

Texas Instruments

PCB

LOGO

WEEE logo

PCB

LOGO

FCC disclaimer



LBL1

PCB Label

THT-14-423-10

Size: 0.65" x 0.20 "

ZZ1

Label Assembly Note

This Assembly Note is for PCB labels only

Variant/Label Table	
Variant	Label Text
001	LMK5C22212AEVM
002	LMK5B12212EVM

ZZ2

Assembly Note

These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ5

Assembly Note

Default Shunt (SH) settings for JP* headers: Connect Shunts (SH) on JP1(1-2=DC/DC to VDD), JP2(1-2=DC/DC to VDDO), JP4(1-2=DC/DC to XO), JP5(1-2=SDA, 3-4=SCL).

ZZ6

Assembly Note

Place serial number sticker on top side of PCB.

ZZ7

Assembly Note

This Assembly SMA connectors must be installed per manufacturers procedure.