



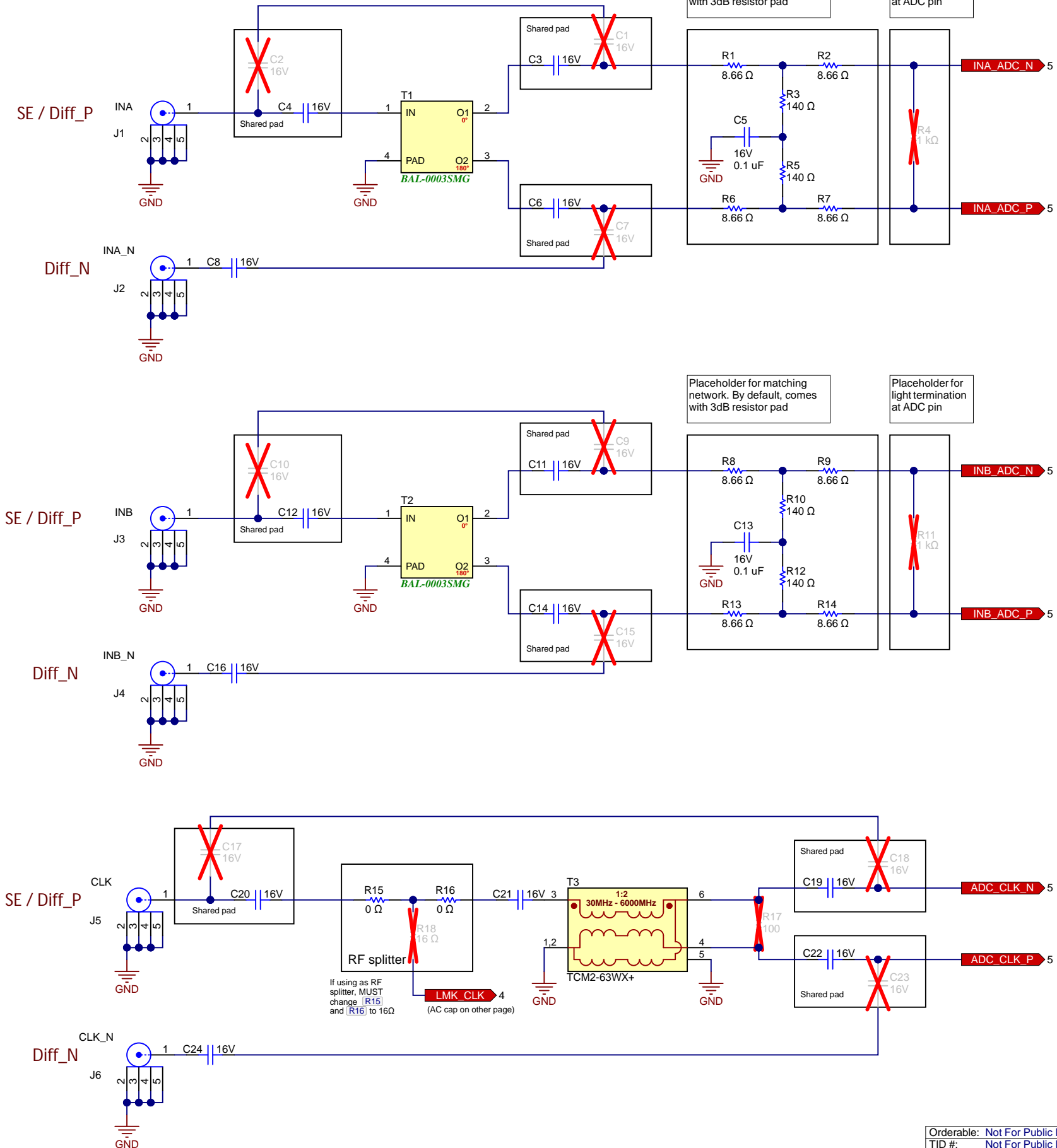
ADC EVM RF Input




Clock input

Differential by default

Note: LMK requires reference clock on input **J12**



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Orderable: Not For Public Release	Designed for: Not For Public Release	Mod. Date: 3/3/2025	 http://www.ti.com © Texas Instruments 2024
TID #: Not For Public Release	Project Title: ADC3RF7xEVM		
Number: -	Rev: A	Sheet Title: ADC EVM RF Input	
SVN Rev: cfec0883921a2ab84ee9a9a5c9e5b22a51022	Sheet: 2 of 20		
Drawn By: CW	File: ADC3RF7x_ADC_Input_AB_RevA_SchDoc Size: B		
Engineer: CW	Contact: http://www.ti.com/support		

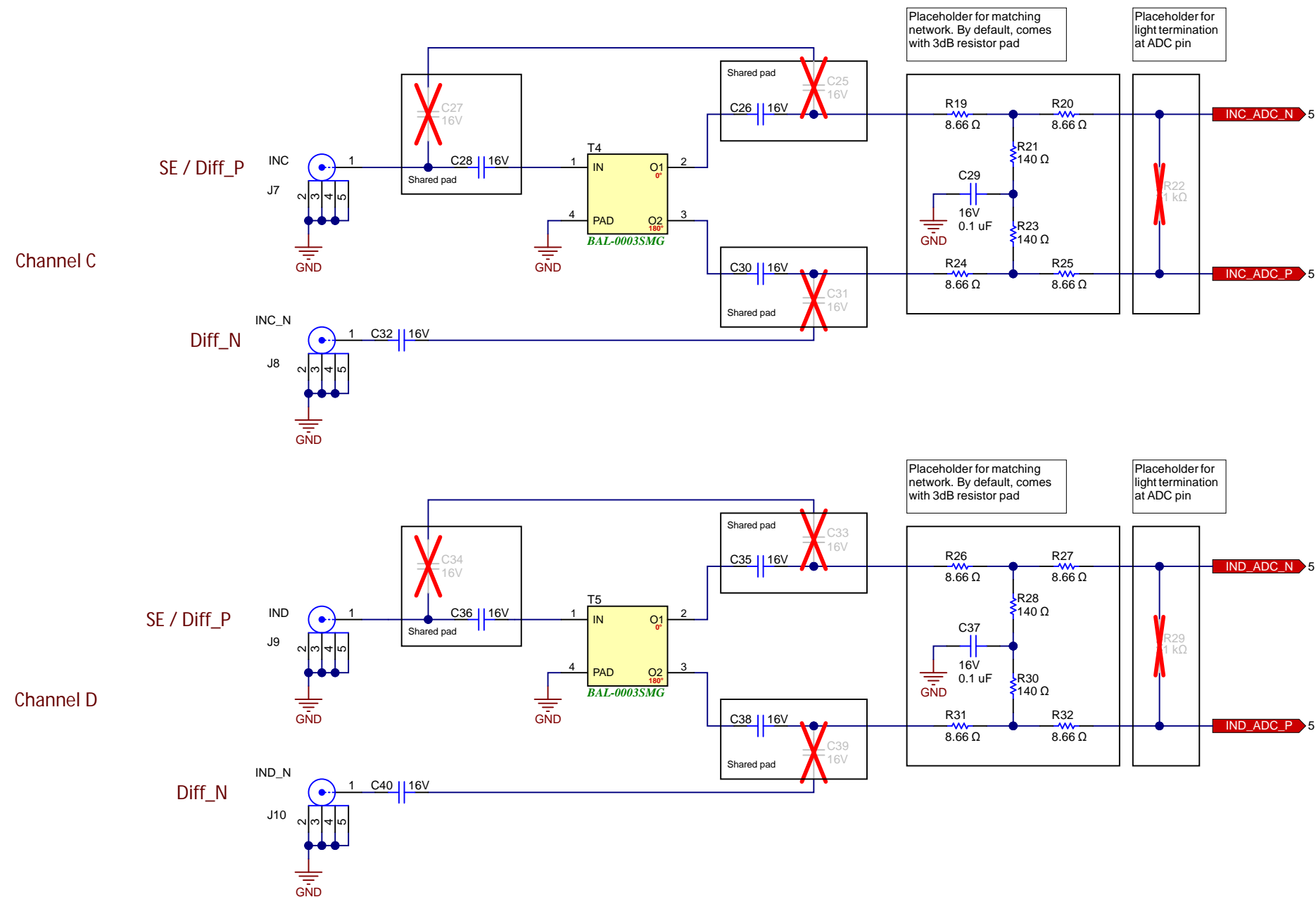
ADC EVM RF Input

A


E

C

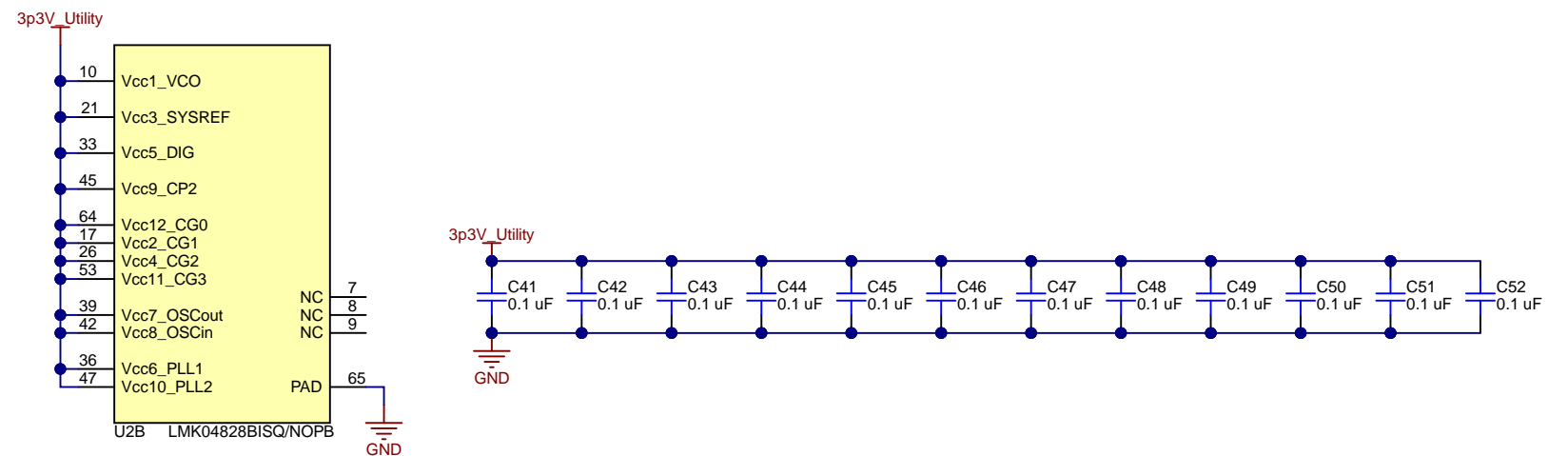
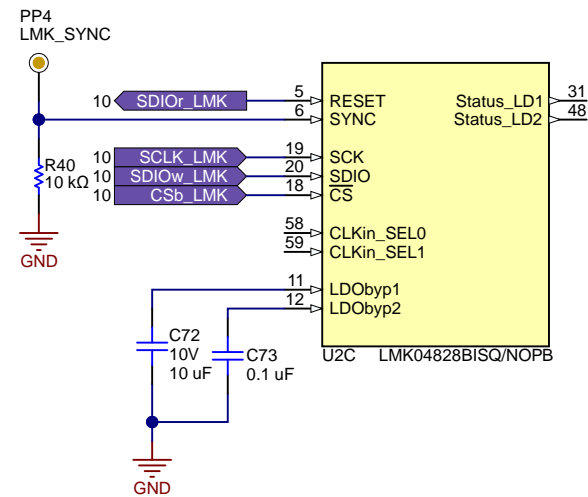
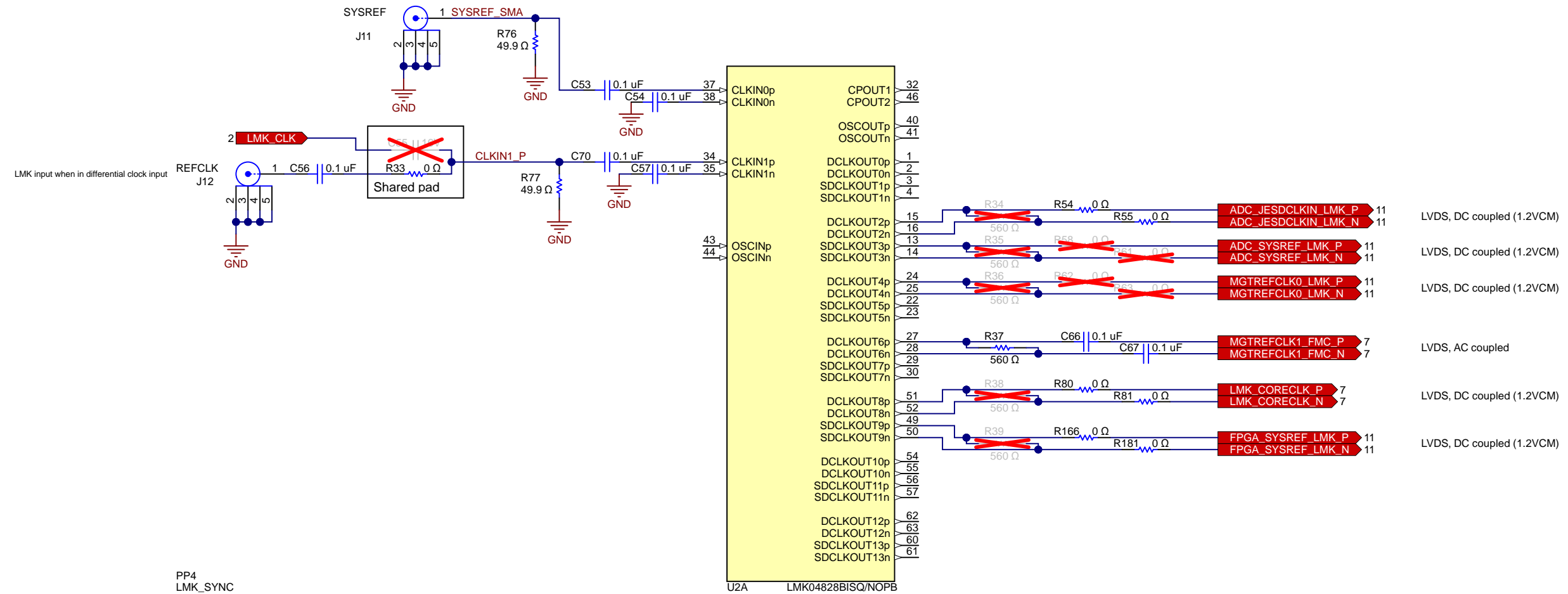
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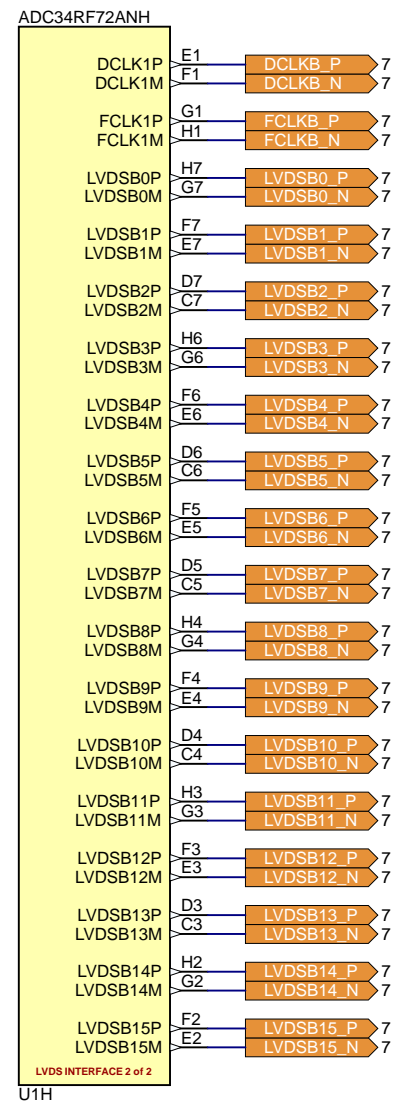
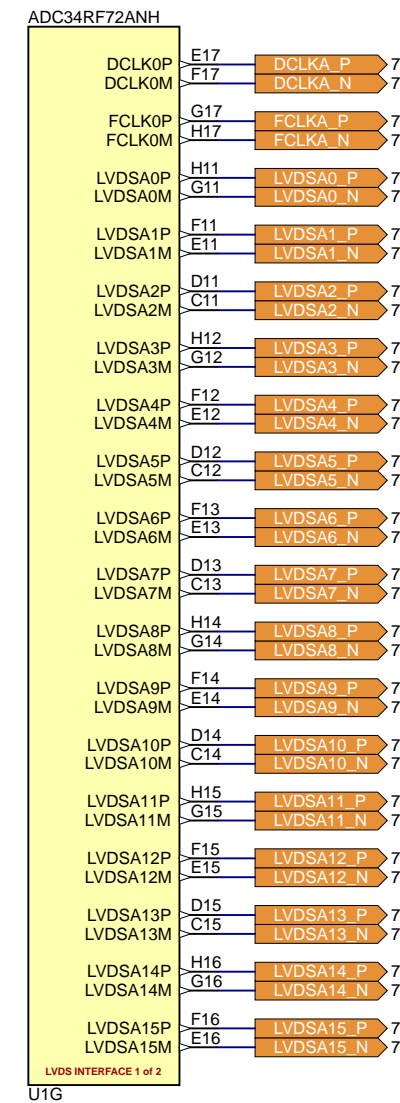
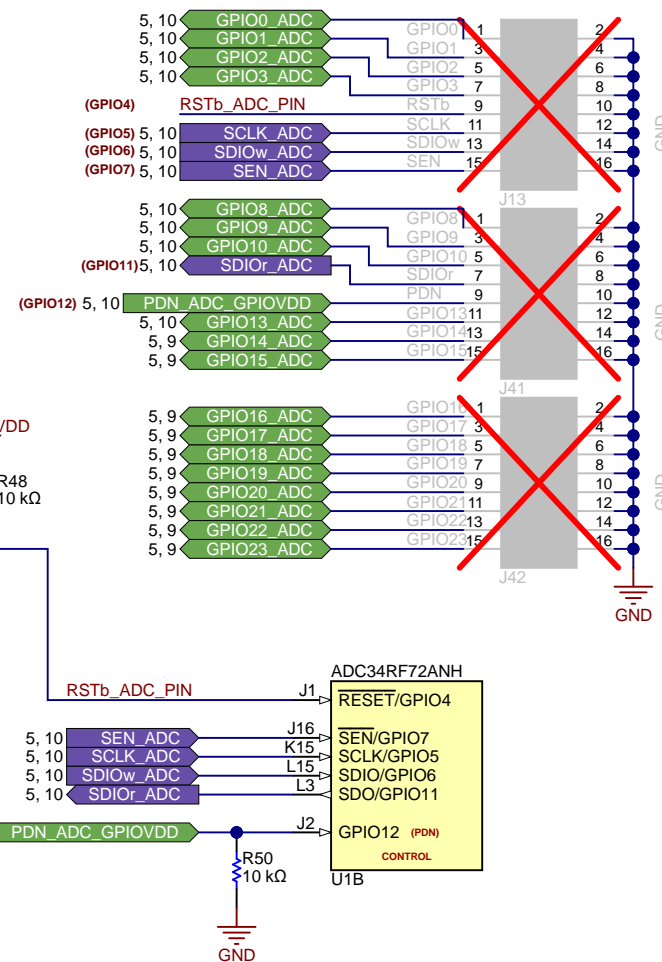
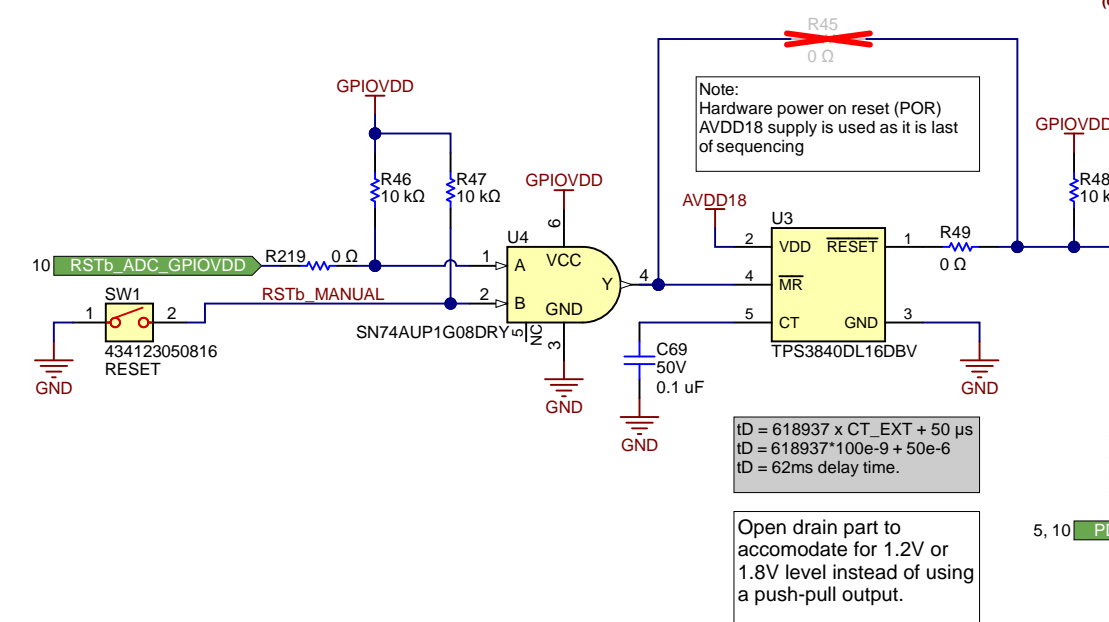
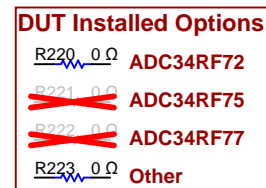
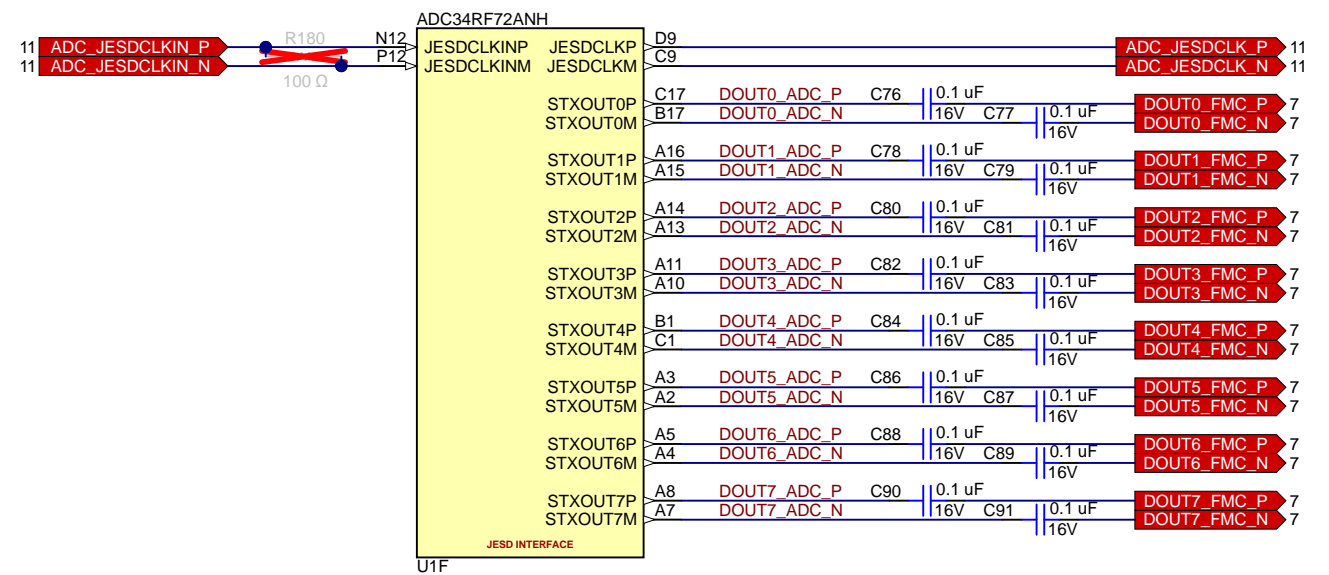
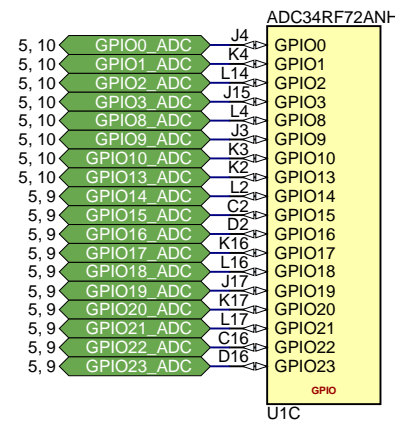
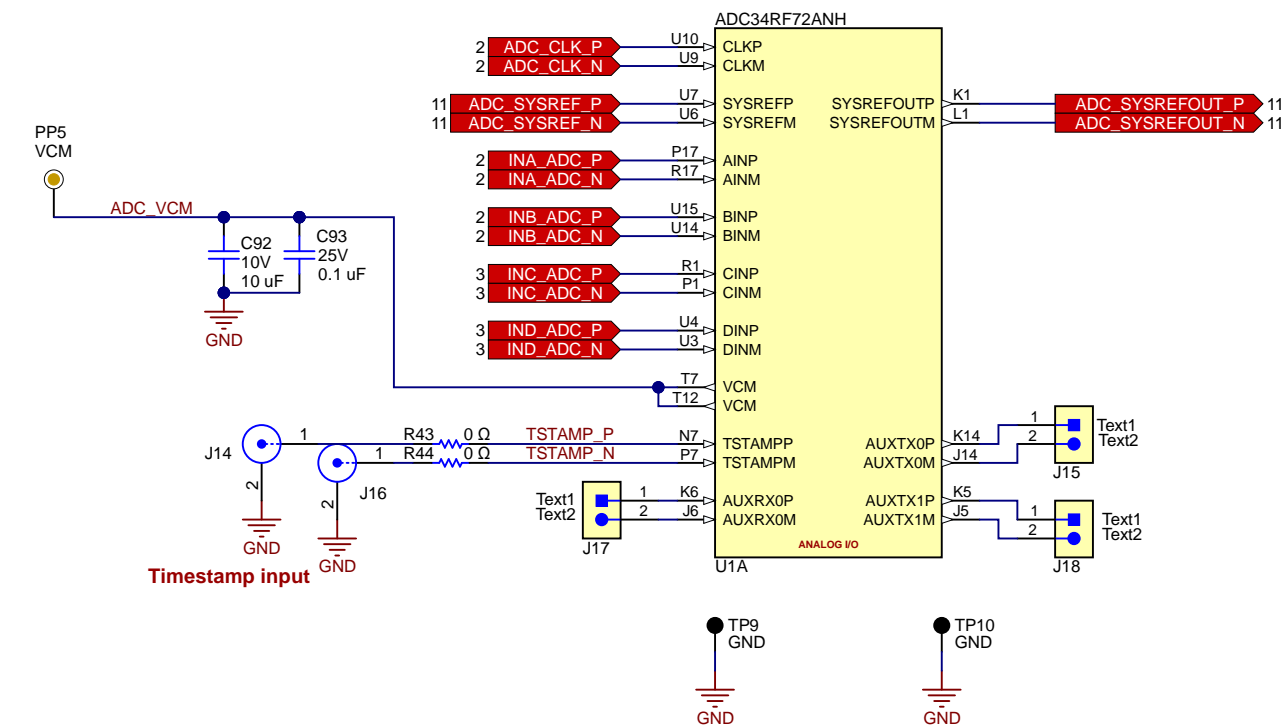
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TID #: Not For Public Release	Project Title: ADC34RF7xEVM		
Number: -	Rev: A	Sheet Title: ADC EVM RF Input	
SVN Rev: 3549342212367fc0980d4322093f5980c001	ADC34RF7x-ADC34RF72 Sheet: 3 of 20		
Drawn By:	File: ADC34RF7x_ADC Input_CD_RevA.SchDoc Size: B		
Engineer: CW	Contact: www.ti.com/support		

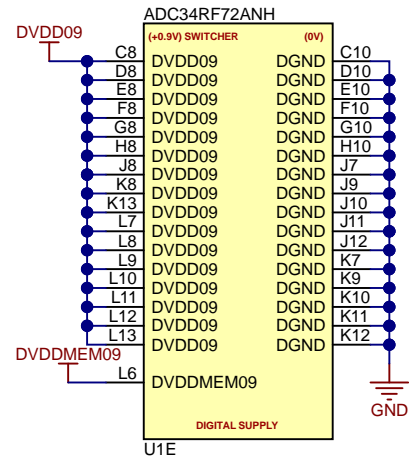
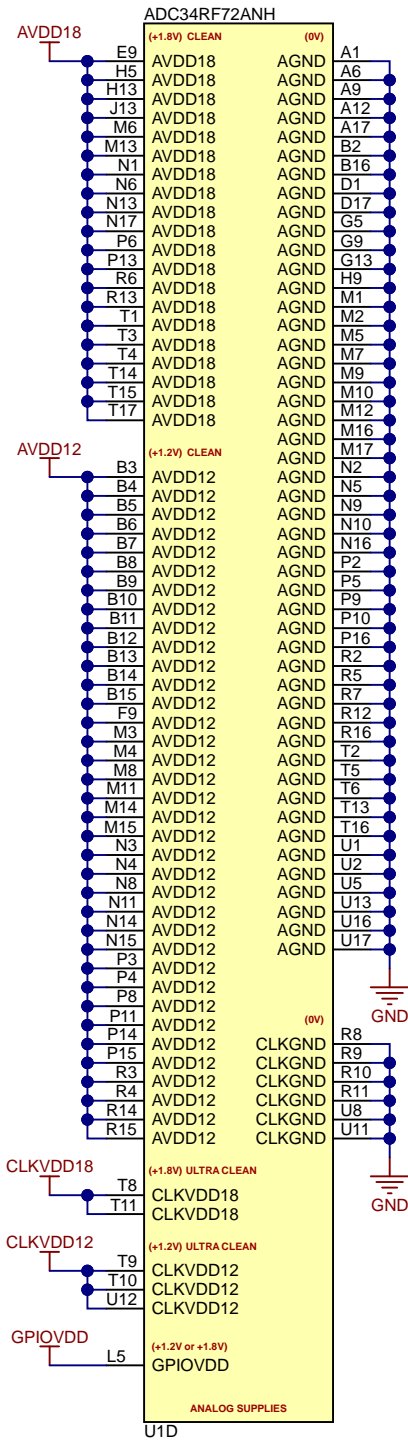
LMK04828 FPGA Clocks and SYSREF



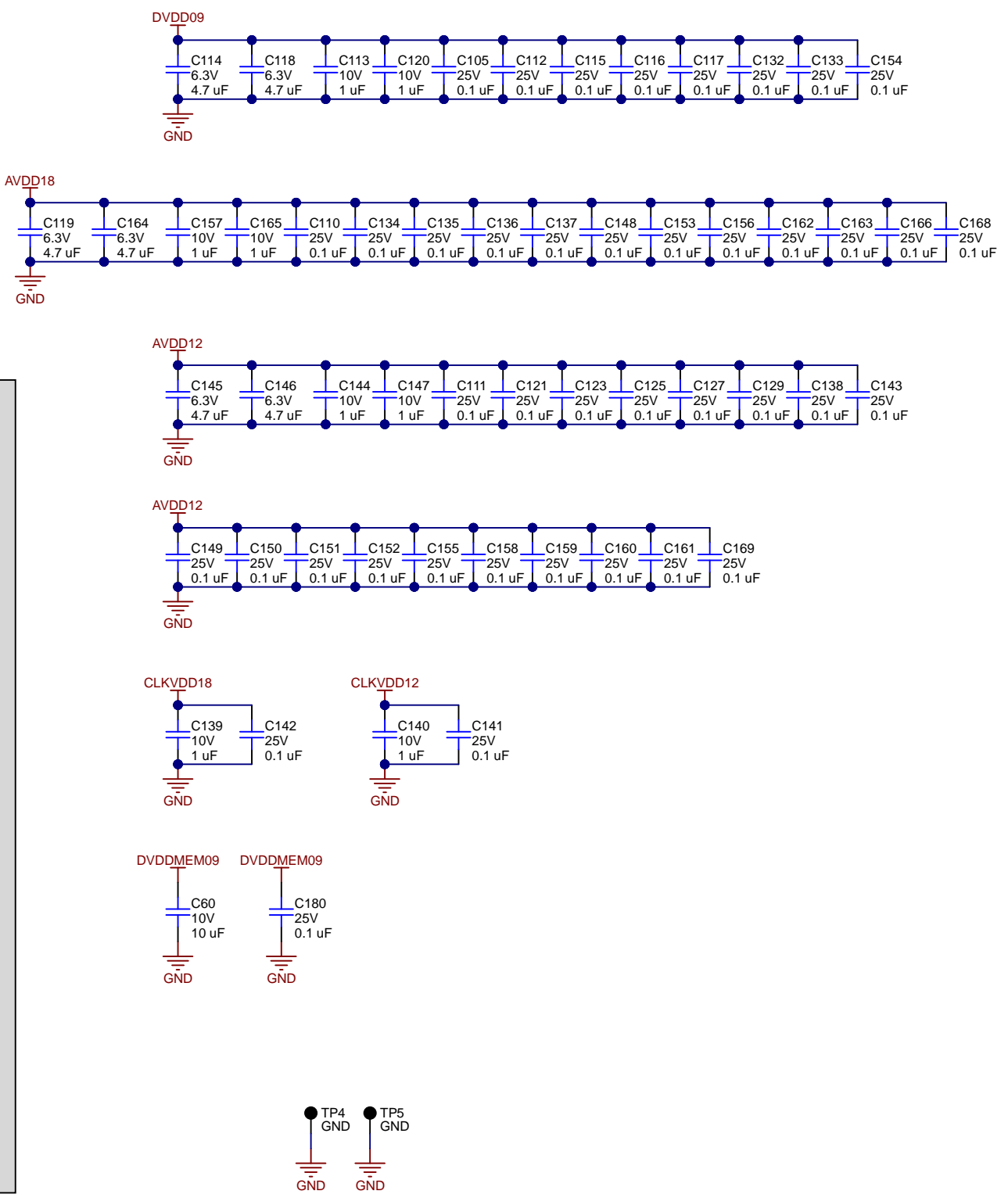
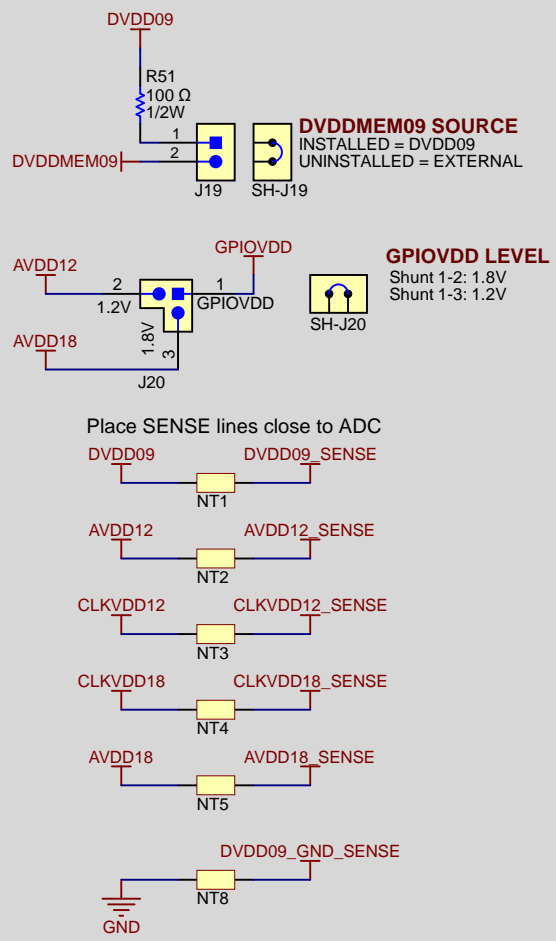
ADC Input, SERDES and Digital Pins



ADC EVM Power

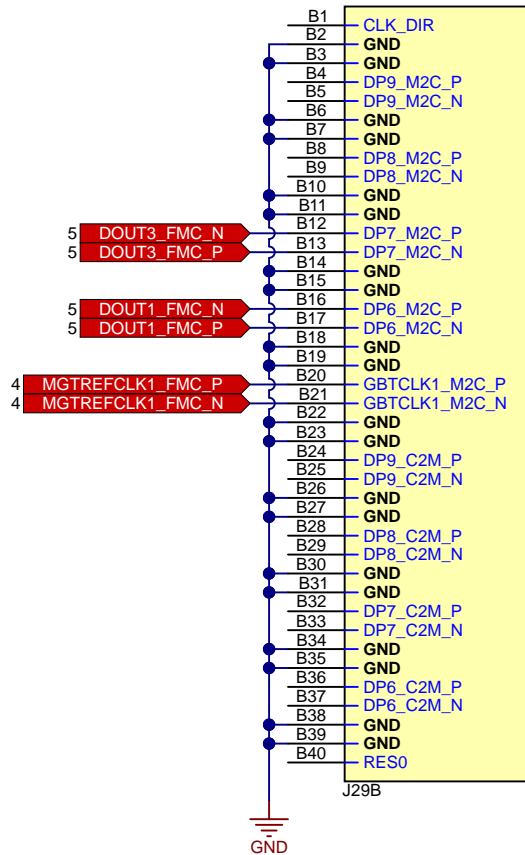
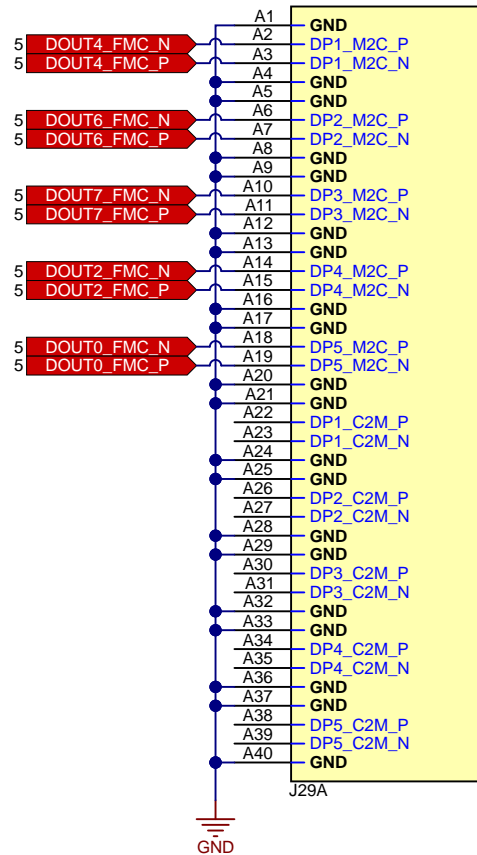


NET TIES & SOLDER OPTIONS

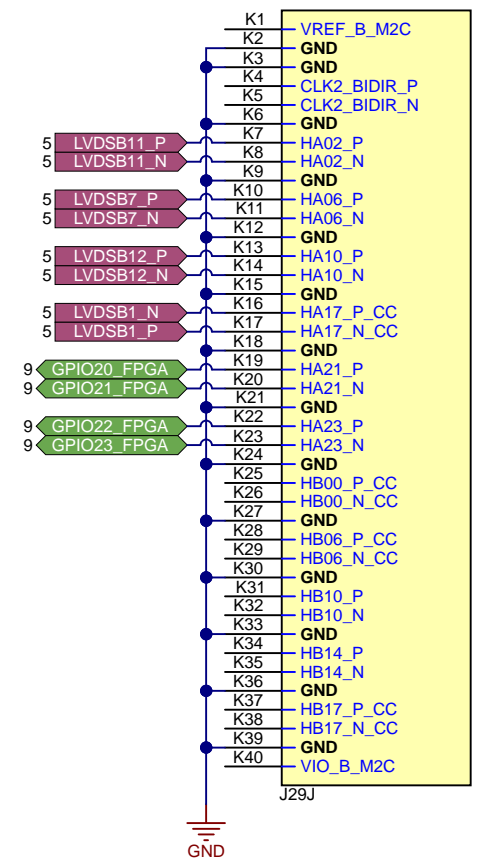
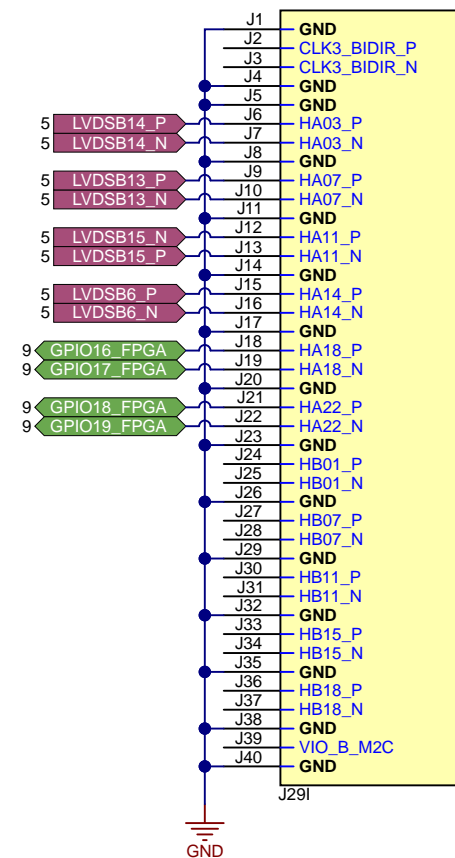
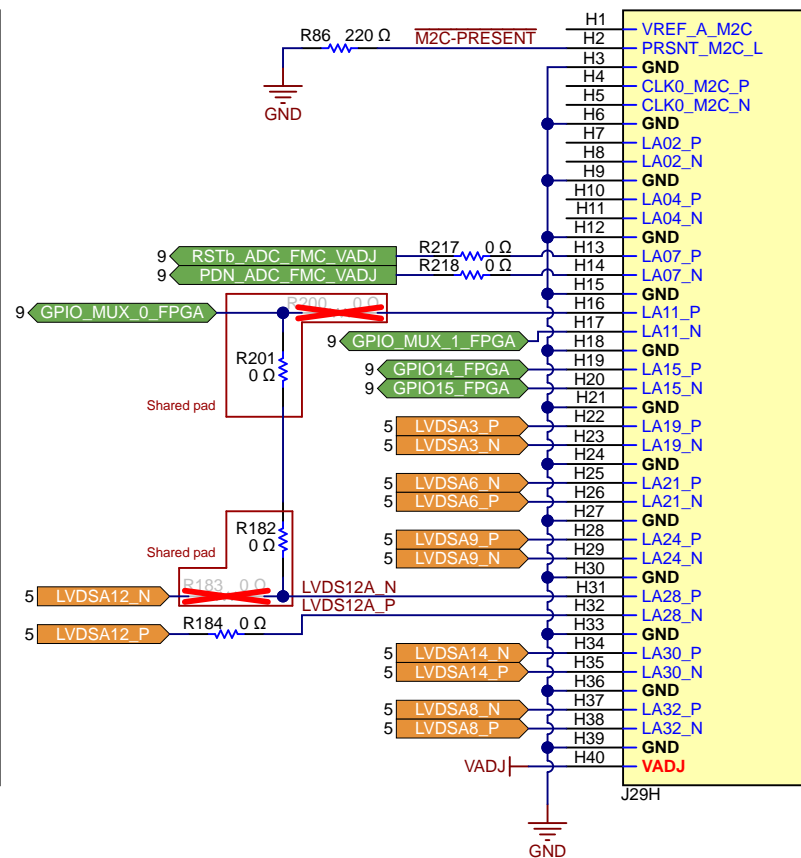
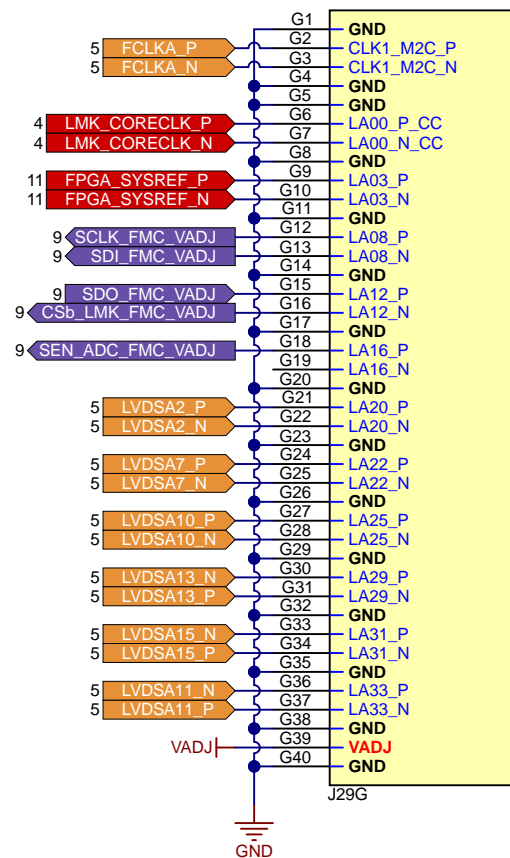
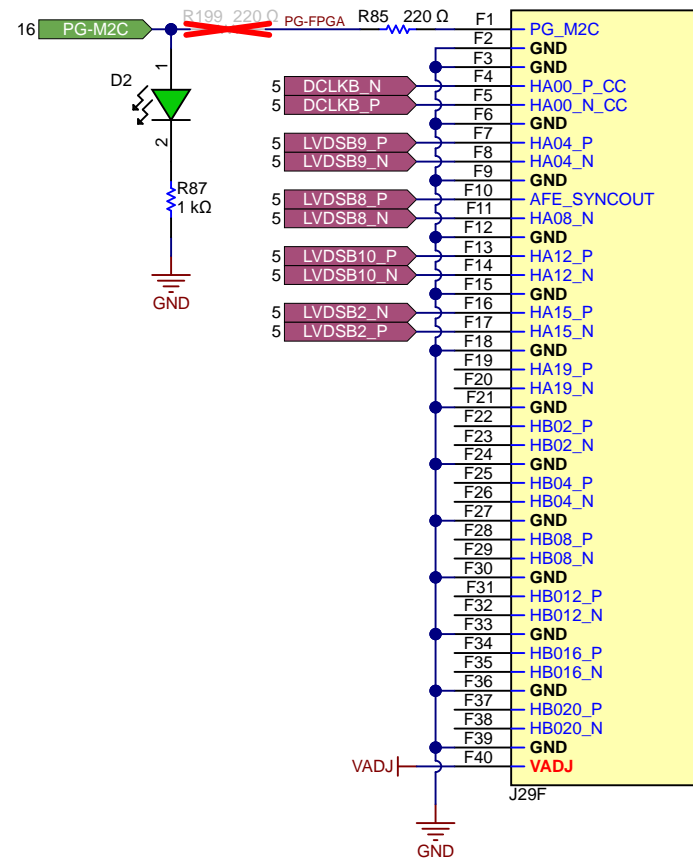
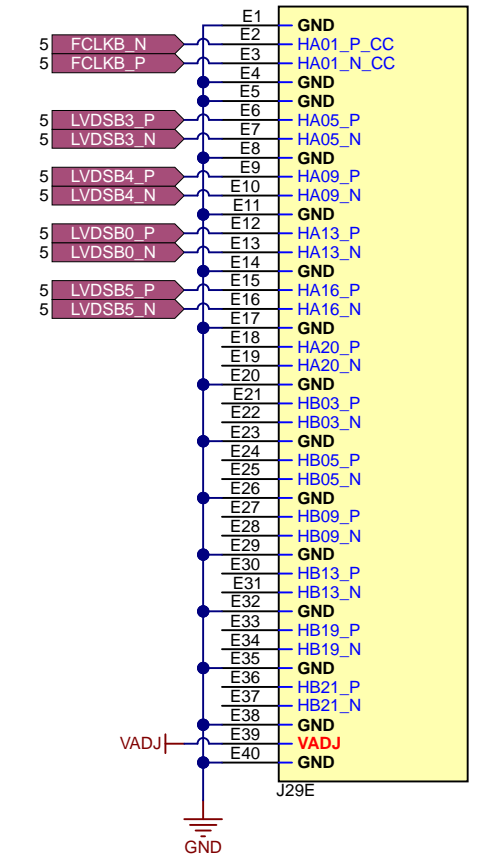
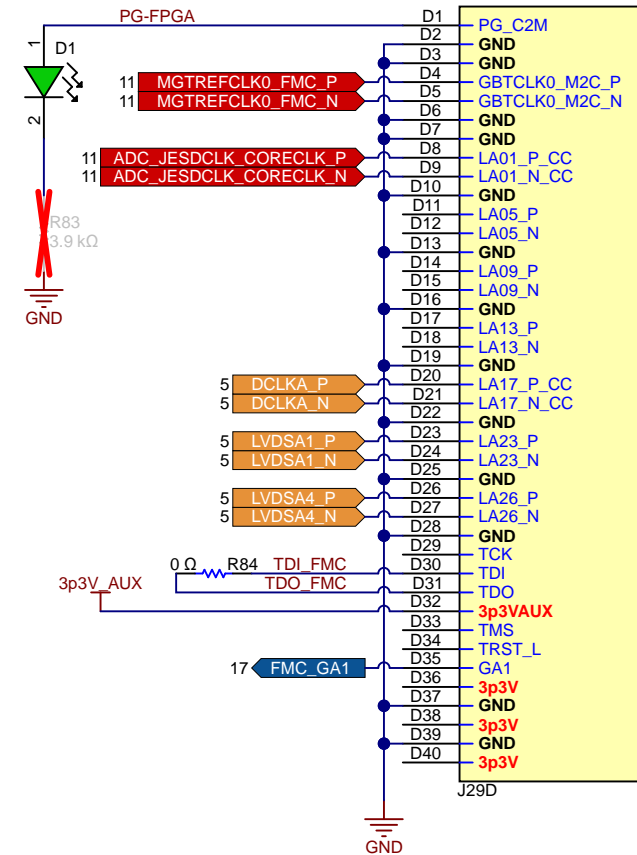
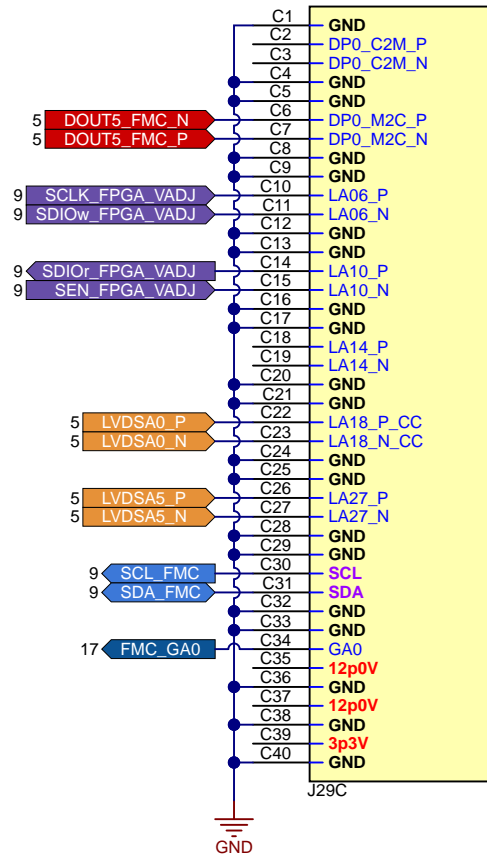


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FMC Connector



FPGA as SPI Peripheral

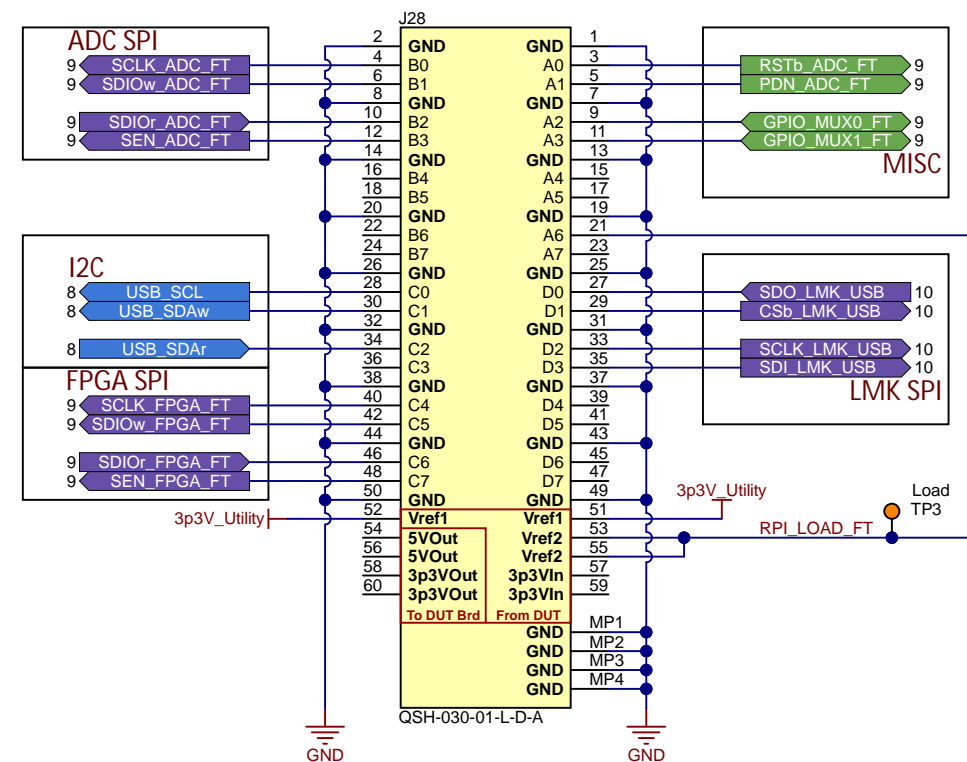


USB Interface

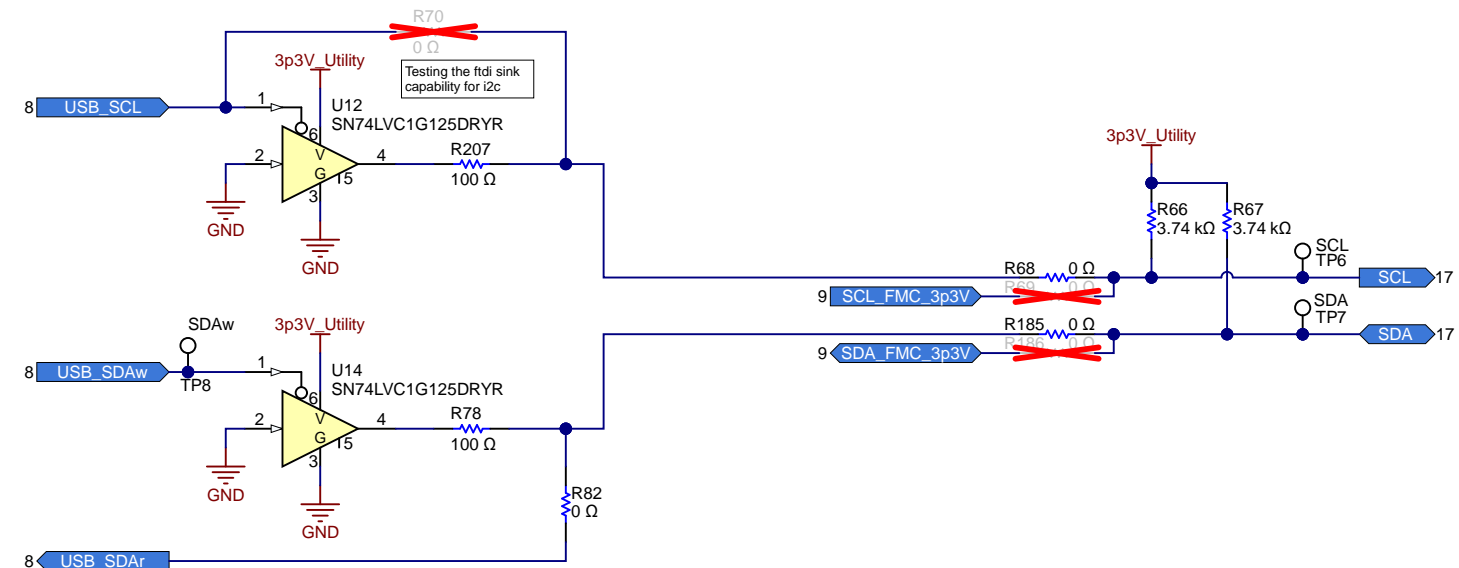
Note: FTDI pinout matches TII dualsite board for ADC(site1) & LMK

*Note: All SDIO naming convention is from the perspective of the FTDI host controller.

SDIOw = Serial Data In (FTDI → ADC/LMK)
SDIOr = Serial Data Out (ADC/LMK → FTDI)



Vref1: Passes 3.3V to RPi autoload board



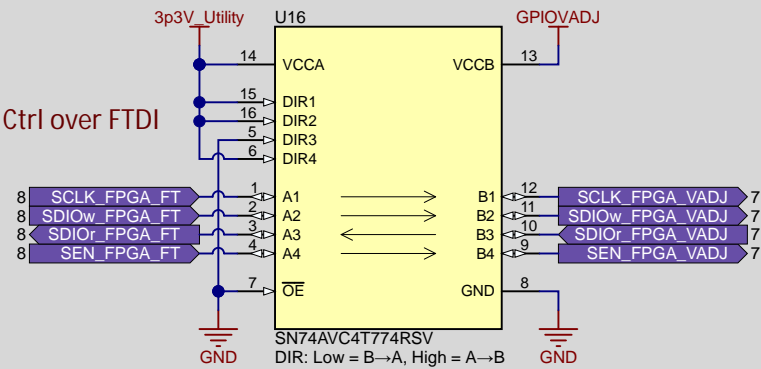
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TID #: Not For Public Release	Project Title: ADC34RF7x EVM	
Number: -	Rev: A	Sheet Title: USB Interface
SVN Rev: 3549342212367fc0980a04322b19c5686c043	ADC34RF72	Sheet: 8 of 20
Drawn By: CW	File: ADC34RF7x_USB_RevA.SchDoc	Size: B
Engineer: CW	Contact: http://www.ti.com/support	



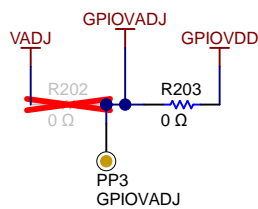
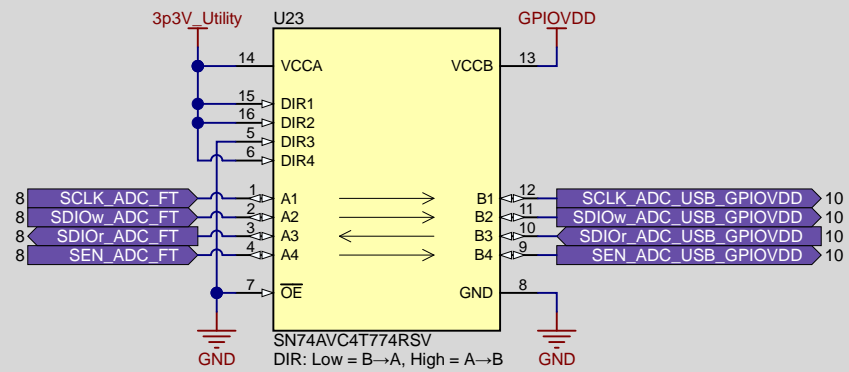
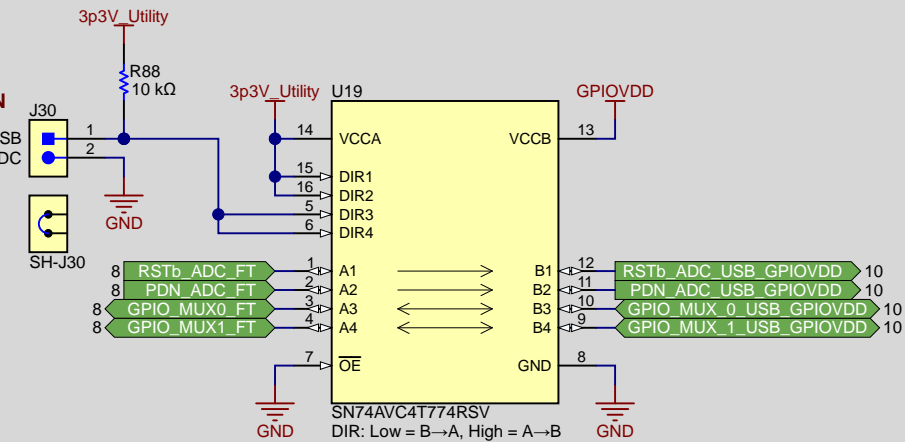
FTDI Level Shifting

FPGA Ctrl over FTDI

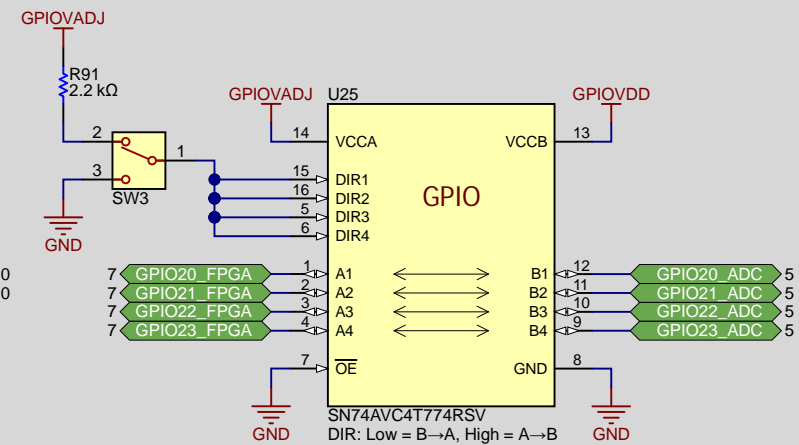
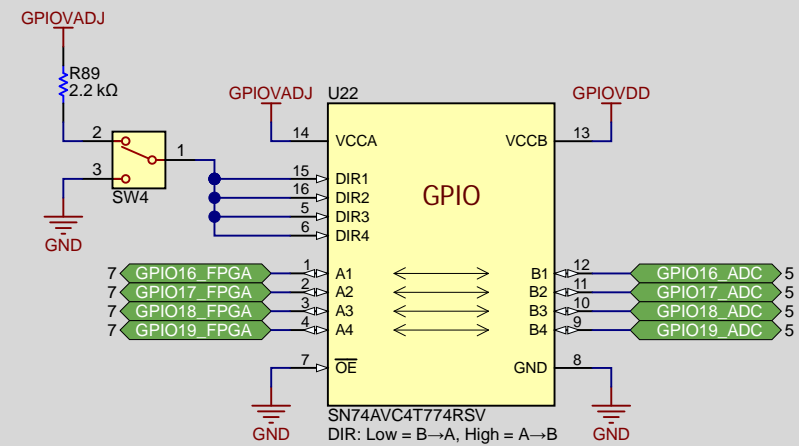
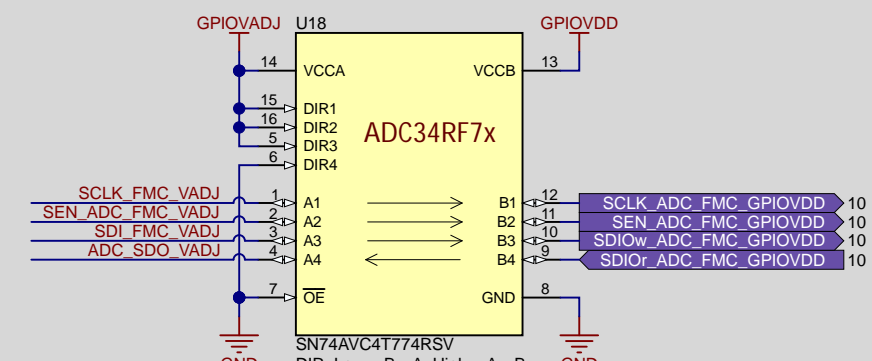
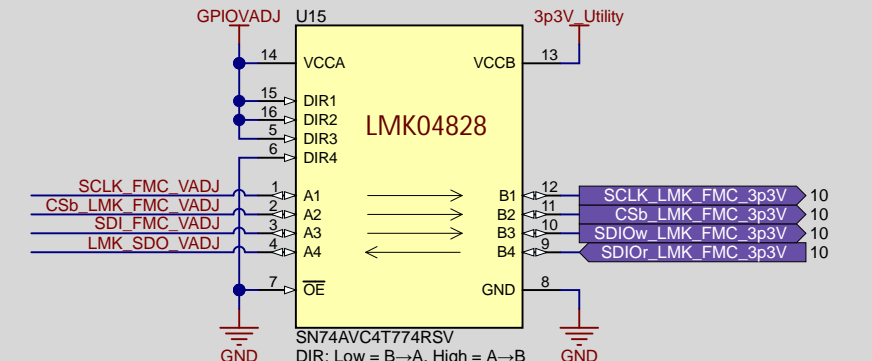
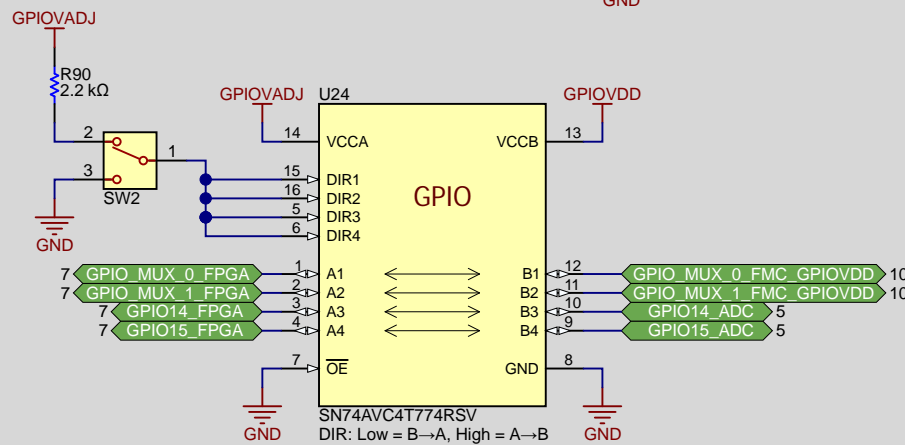
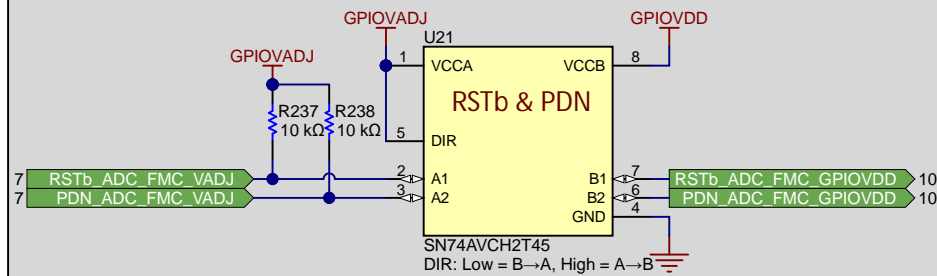
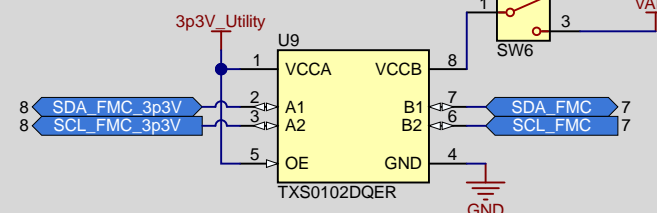
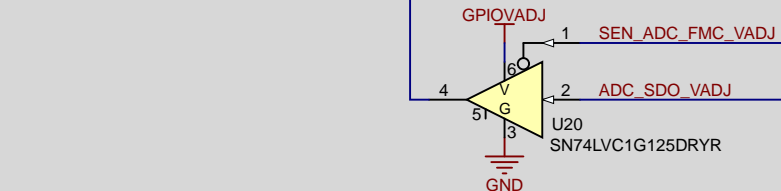
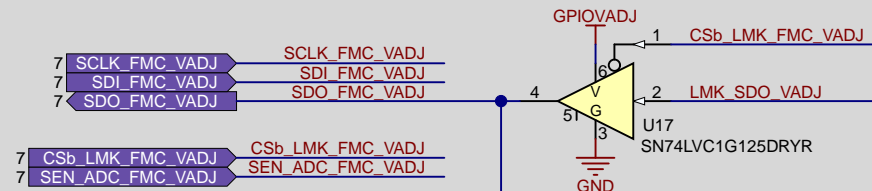


USB GPIO DIRECTION

INSTALLED = ADC TO USB
UNINSTALLED = USB TO ADC

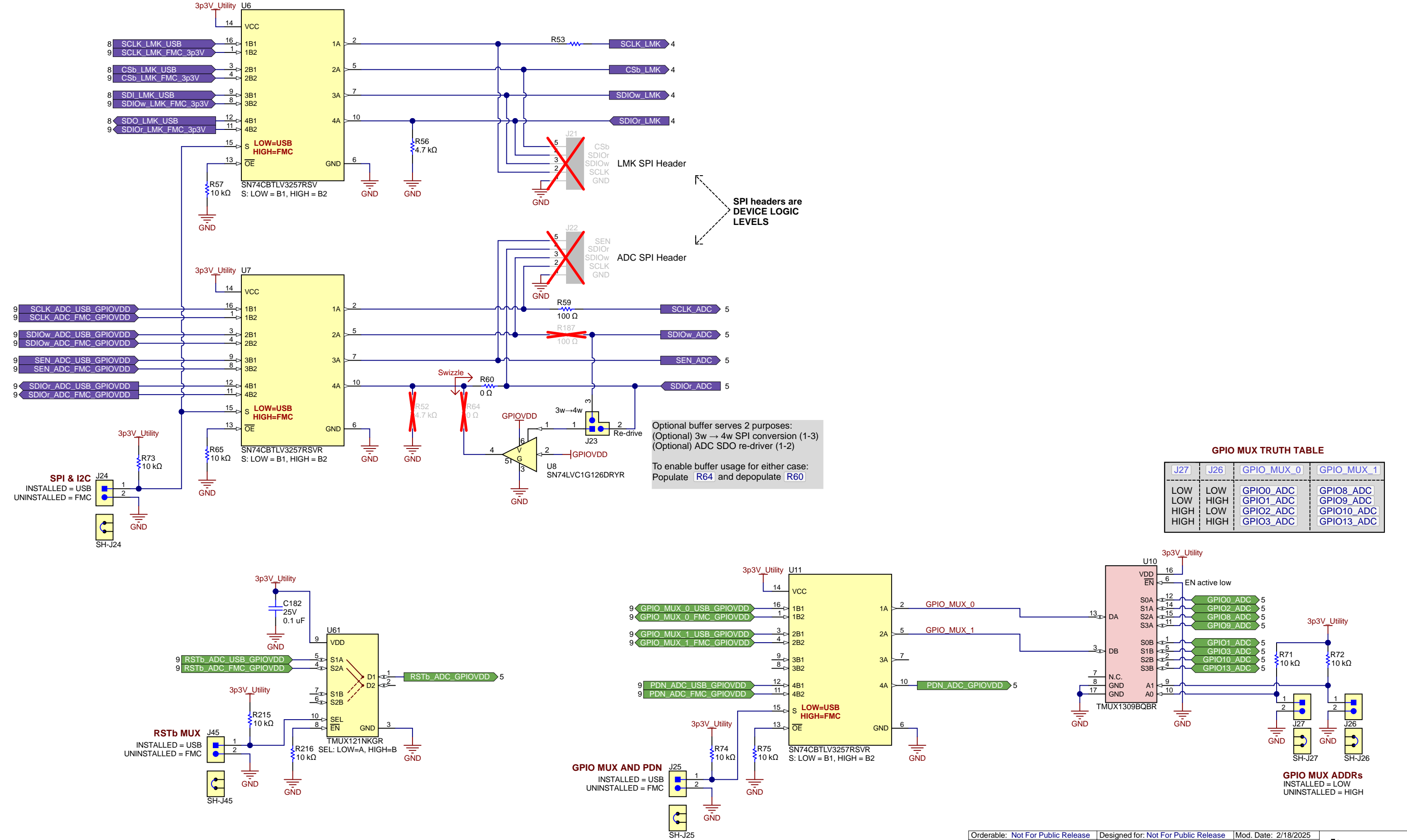


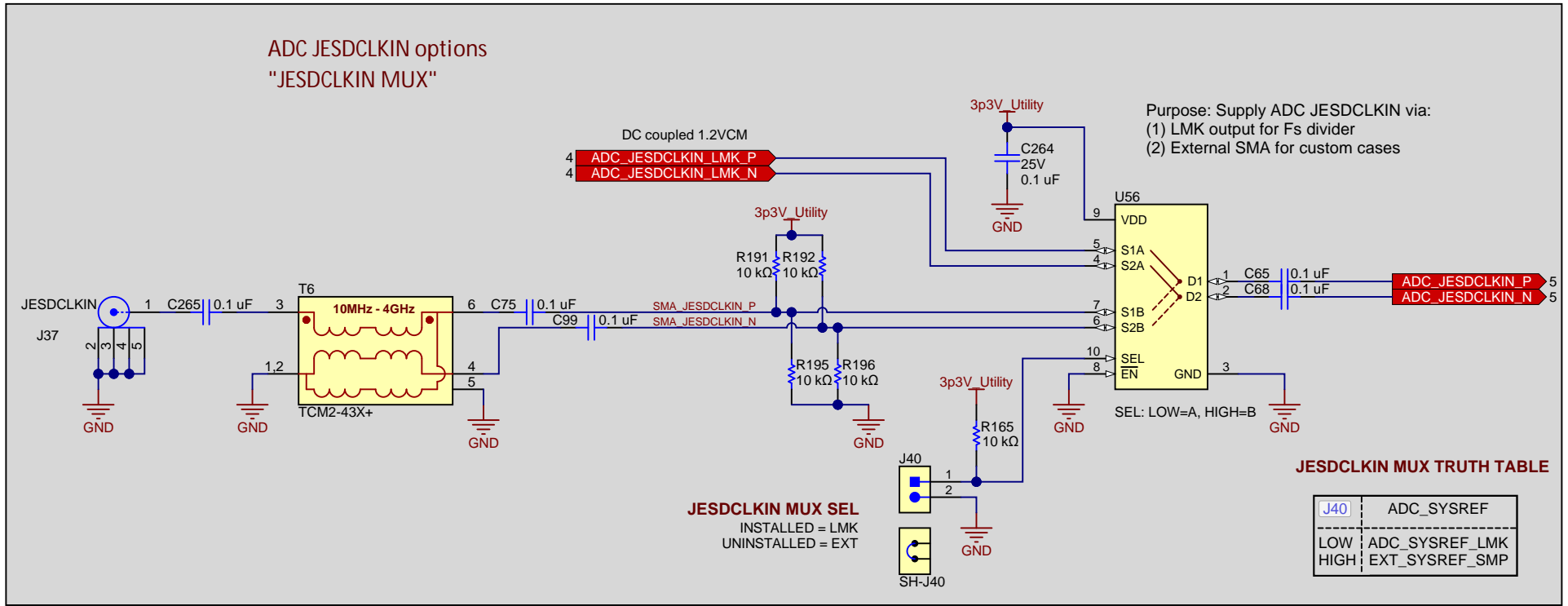
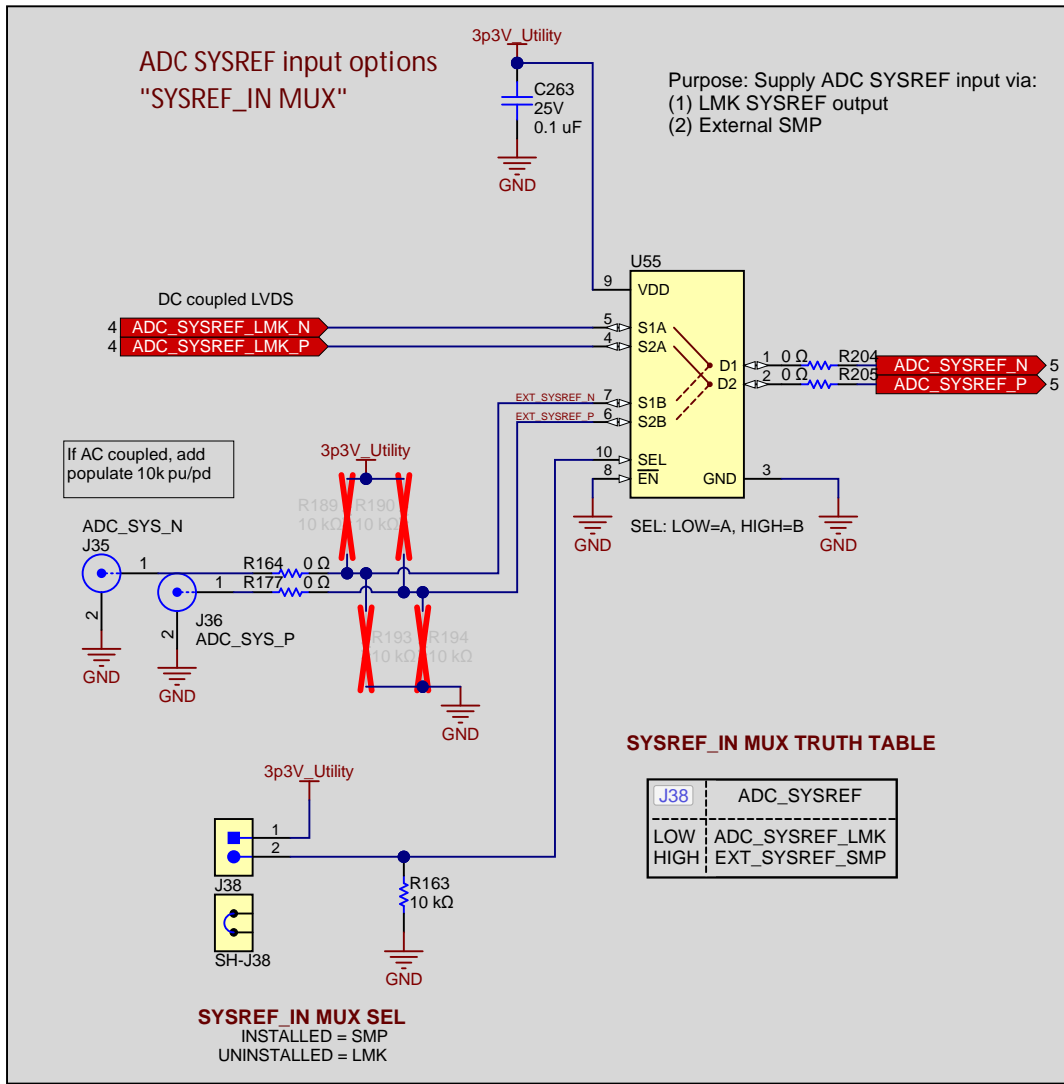
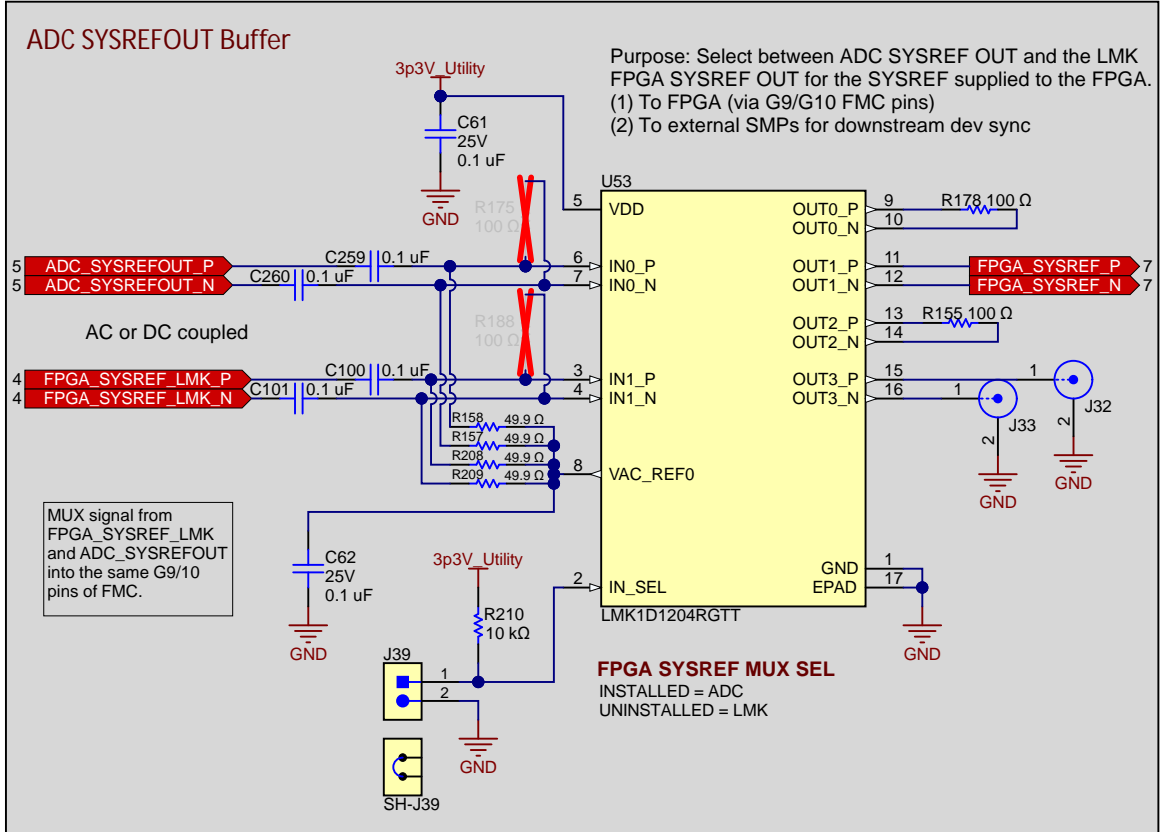
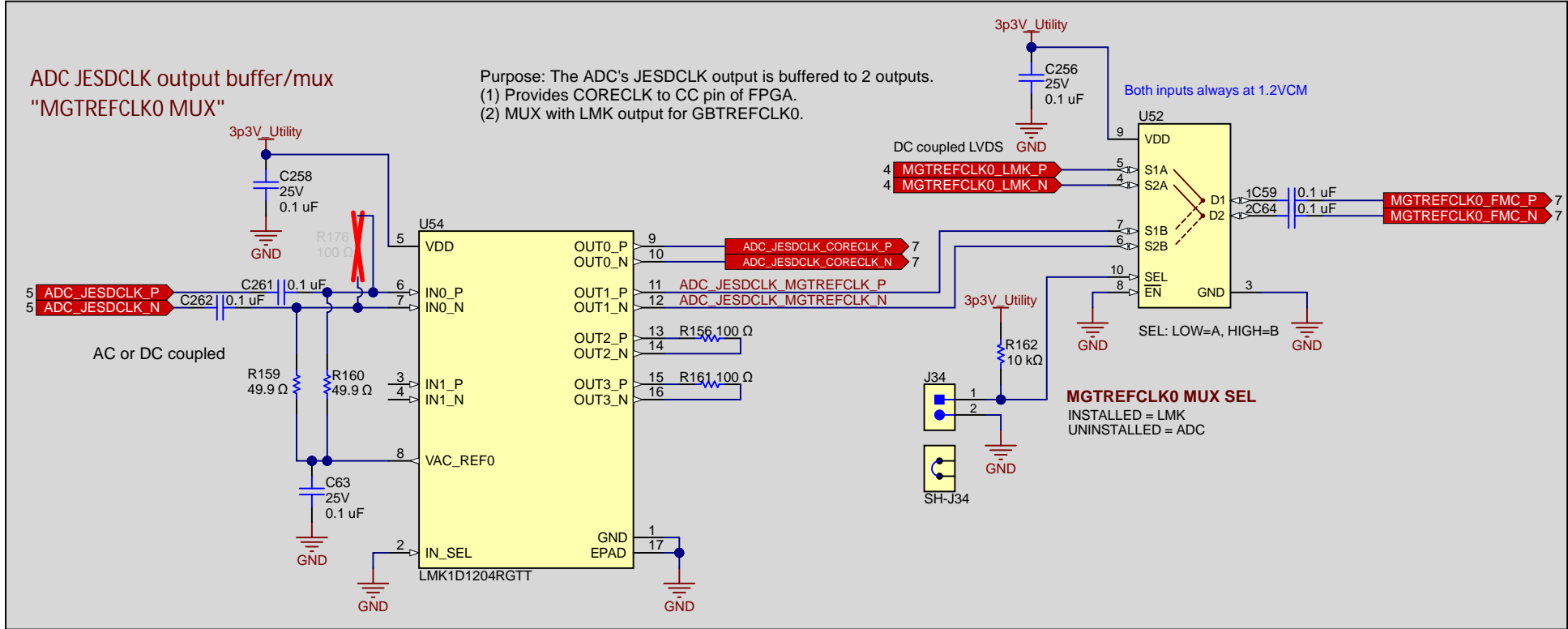
FPGA Level Shifting



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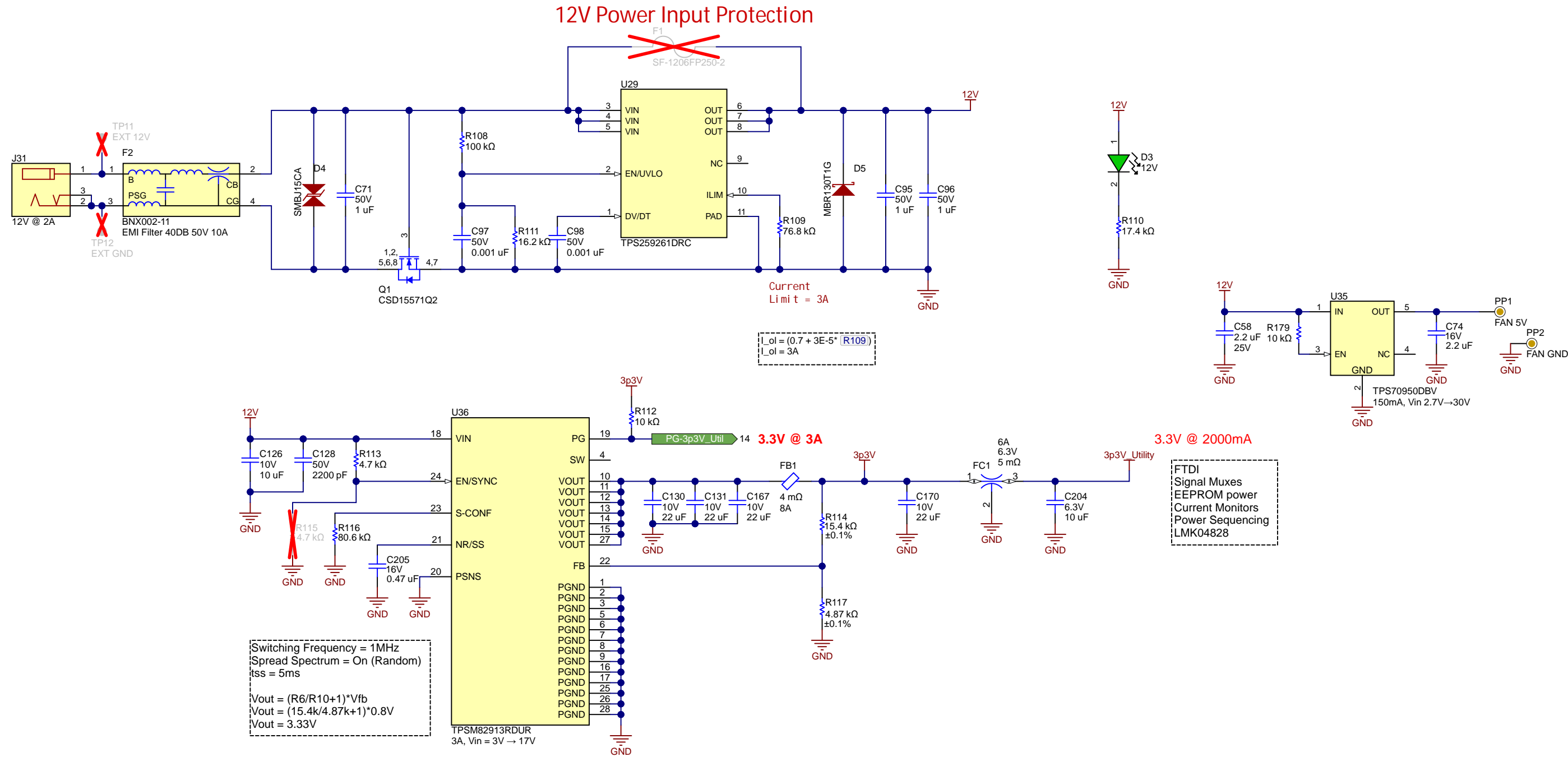
MUXes



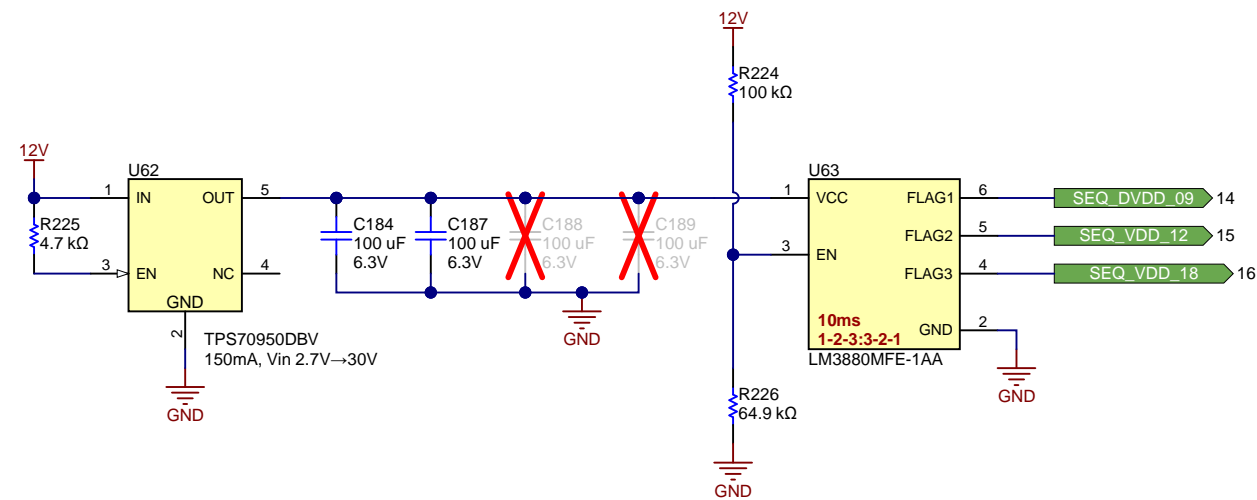



POWER UP SEQUENCE

- DVDD (0.9V)
- AVDD12 (1.2V) → CLKVDD12 (1.2V)
- AVDD18 (1.8V) → CLKVDD18 (1.8V)

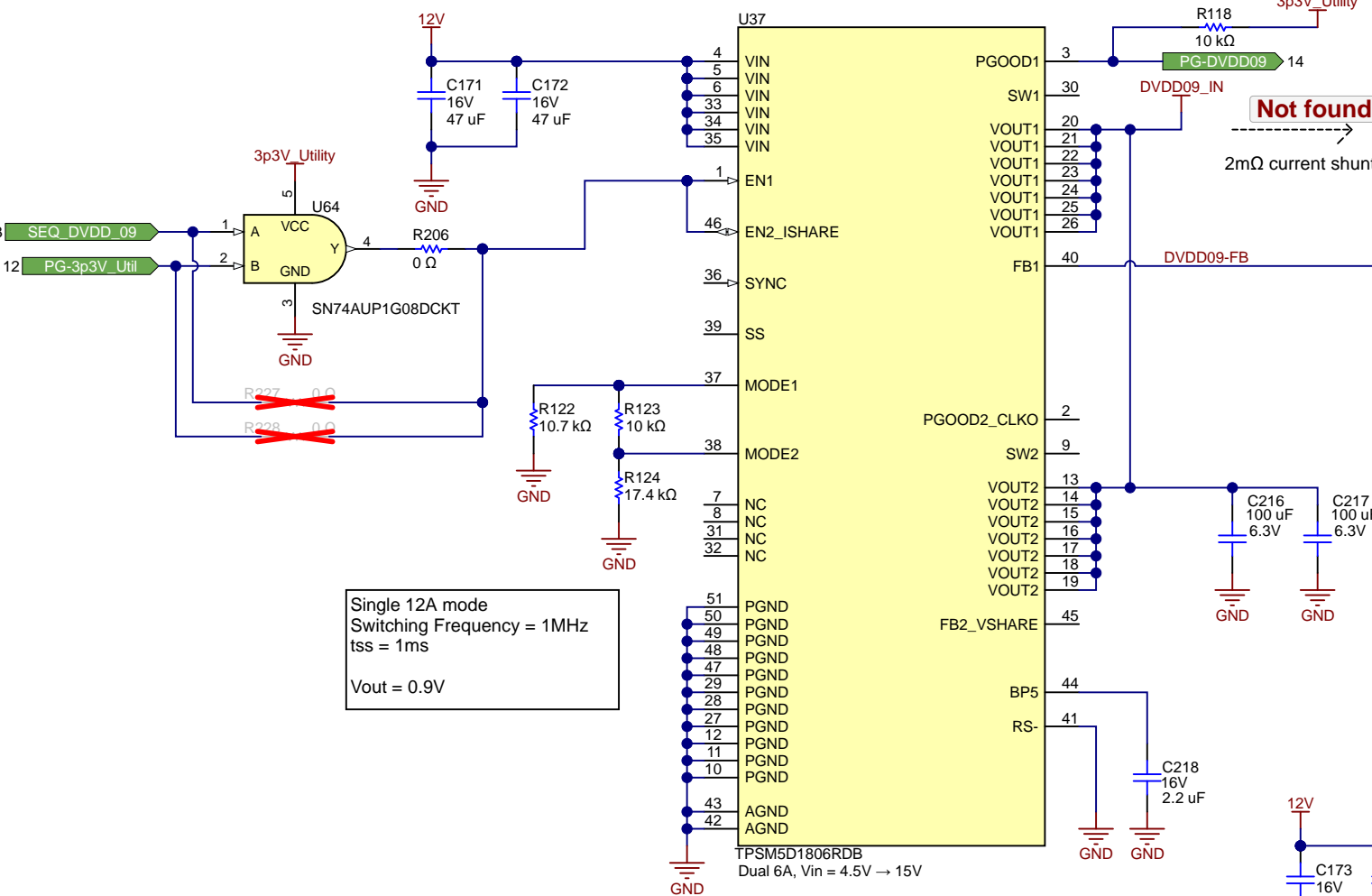


Power Sequencer

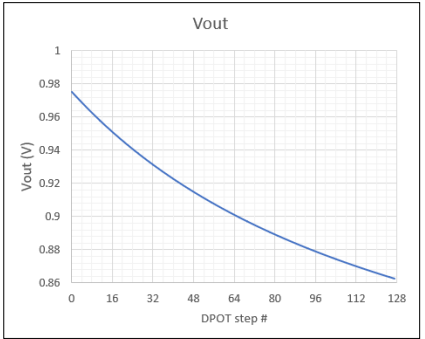
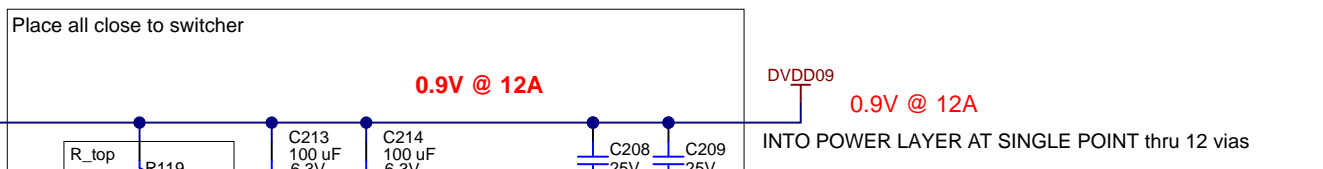


Orderable: Not For Public Release	Designed for: Not For Public Release	Mod. Date: 3/13/2025	 TEXAS INSTRUMENTS http://www.ti.com © Texas Instruments 2024
TID #: Not For Public Release	Project Title: ADC34RF7xEVM		
Number: -	Rev: A	Sheet Title: Power Sequencer	
SVN Rev: cfec0883921a2ab84ee9	A1a06002a5b4510221DC34RF7xEVM [Last Modified]		
Drawn By:	File: ADC34RF7x_Power Sequencer.SchDoc	Sheet: 13 of 20	
Engineer: CW	Contact: http://www.ti.com/support		

EVM Power 2
DVDD09, DC-DC before LDOs



To switch over to uFit power connector, break **R206**, **R119** and **Not found** (2mΩ current shunt) for DVDD



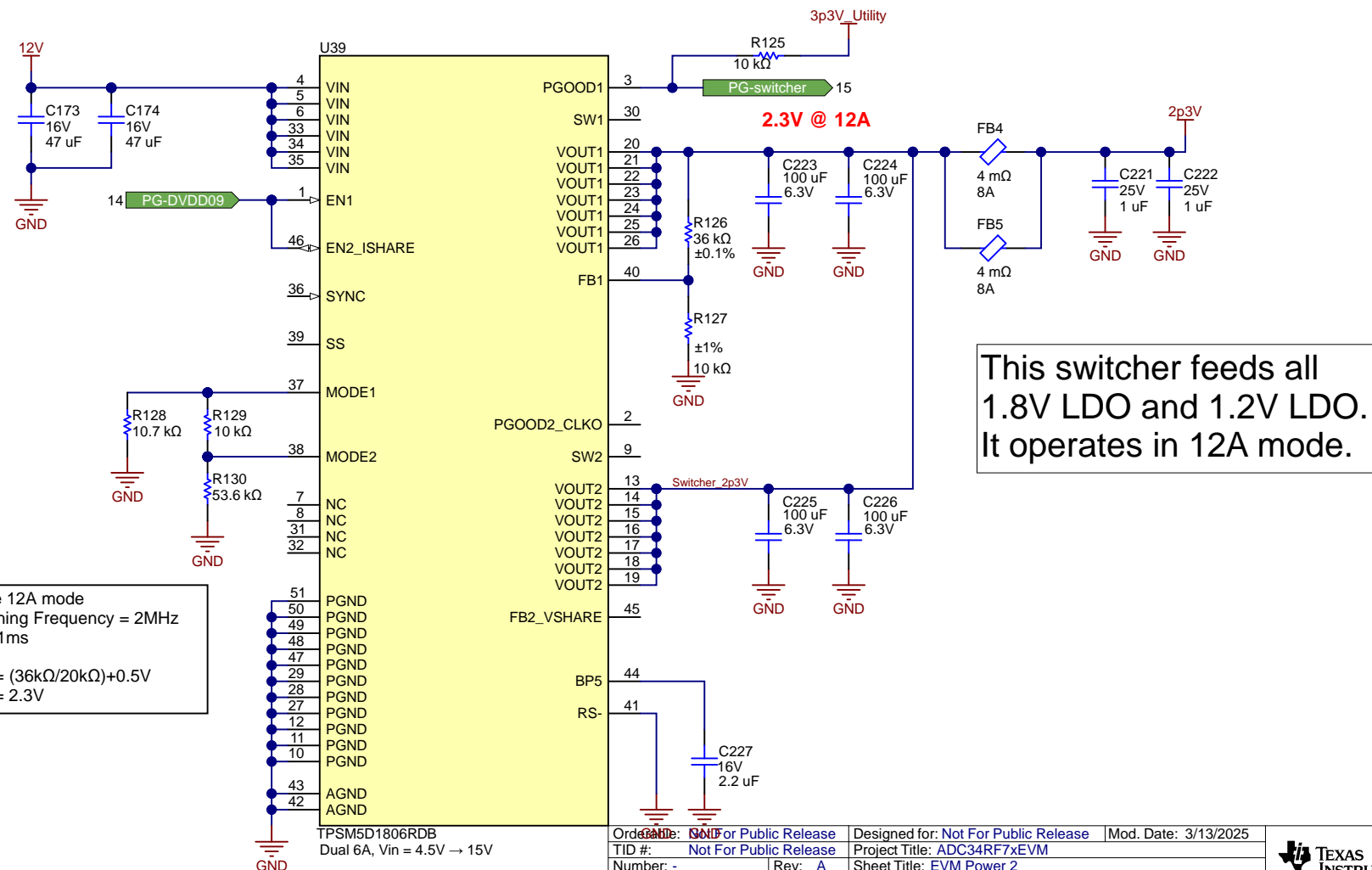
**TODO change feedback res values to achieve 0.7V through 1.1V

R_bot = 11kΩ // (11kΩ+5kΩ) = 6.518kΩ
Vout = (5.23kΩ/(2*6.518kΩ))+0.5=0.901V

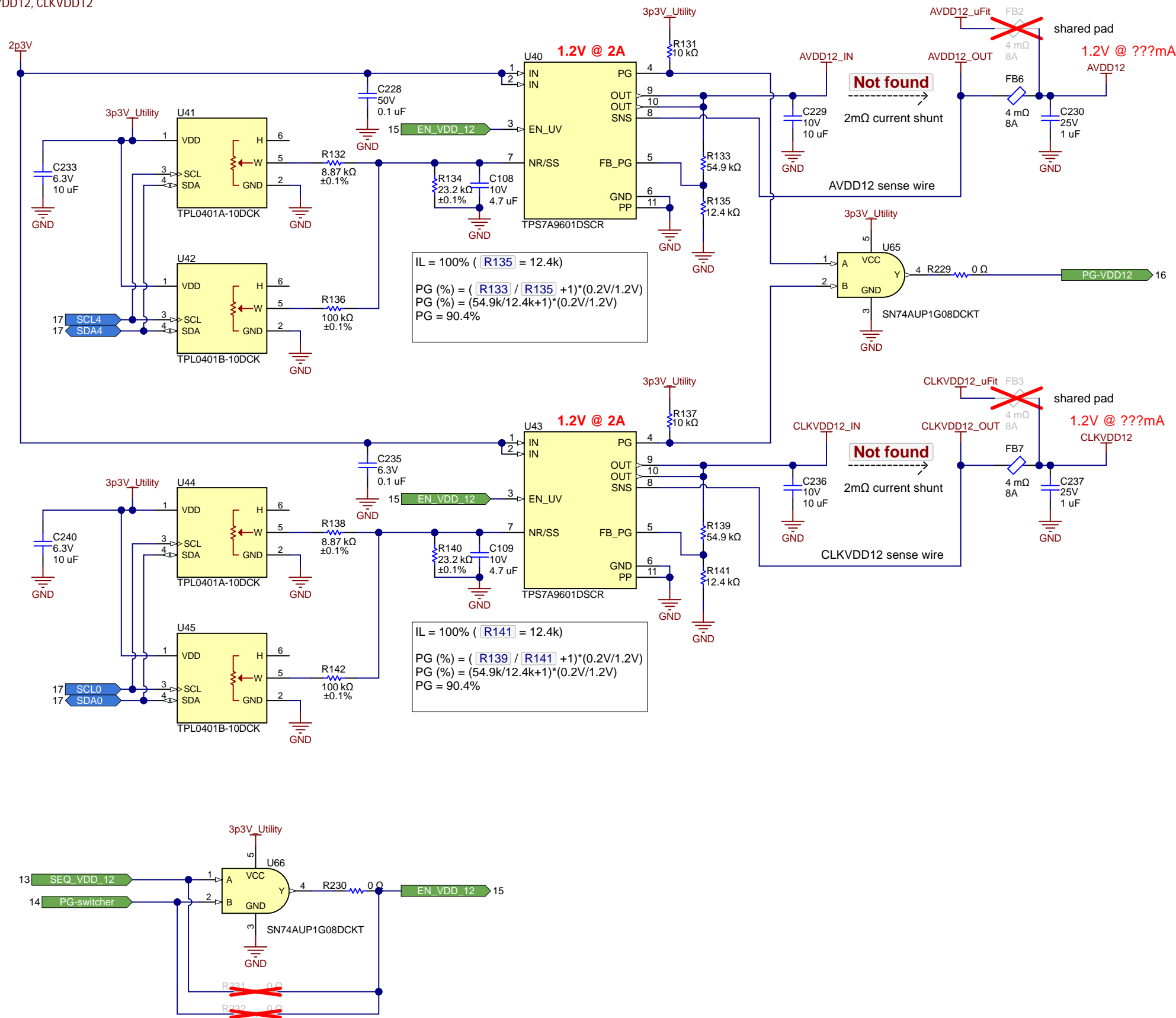
R_wiper=10kΩ; R_bot = 7.218kΩ, Vout = 0.862V
R_wiper=0Ω; R_bot = 5.5kΩ, Vout = 0.975V

Resolution at mid-scale ≈ 8uV

R_wiper refers to R_WL (Resistance from pin 5 to pin 2)



This switcher feeds all 1.8V LDO and 1.2V LDO. It operates in 12A mode.



POWER UP SEQUENCE

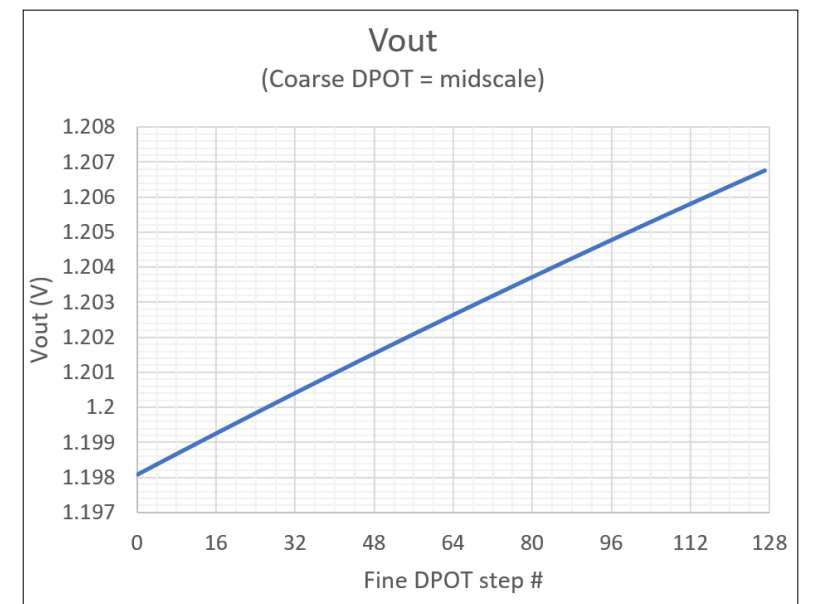
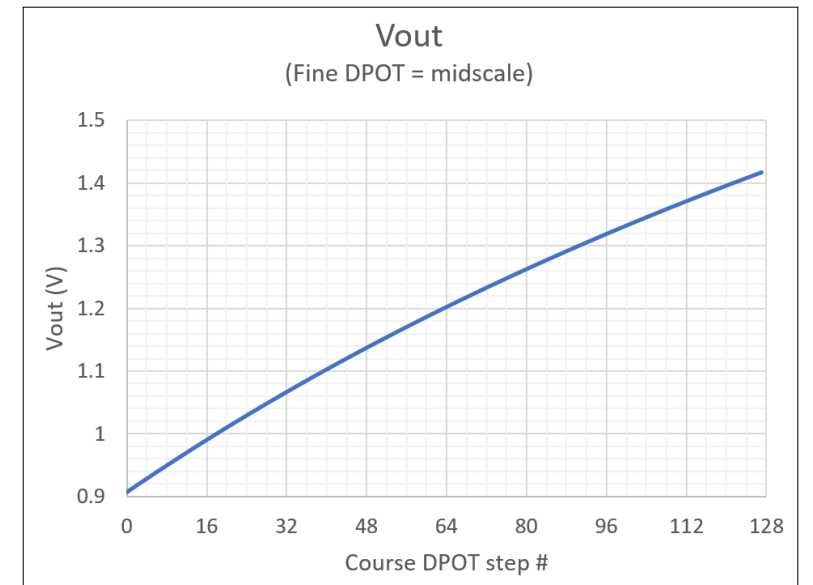
1. DVDD (0.9V)
2. AVDD12 (1.2V) → CLKVDD12 (1.2V)
3. AVDD18 (1.8V) → CLKVDD18 (1.8V)

FOR ALL 1.2V MARGINING LDOs

$$R_{NRSS} = 23.2k\Omega, R_{EQ_{COARSE}}(nom) = 13.87k\Omega, R_{EQ_{FINE}}(nom) = 105k\Omega$$

$$R_{EQ_{DPOTS}}(nom) = \frac{13.87k\Omega * 105k\Omega}{13.87k\Omega + 105k\Omega} = 12.2516k\Omega$$

$$R_{EQ_{DPOTS_{NRSS}}}(nom) = \frac{12.2516k\Omega * 23.2k\Omega}{12.2516k\Omega + 23.2k\Omega} = 8.0176k\Omega \rightarrow V_{out} = 150\mu A * 8.0176k\Omega = 1.202V$$



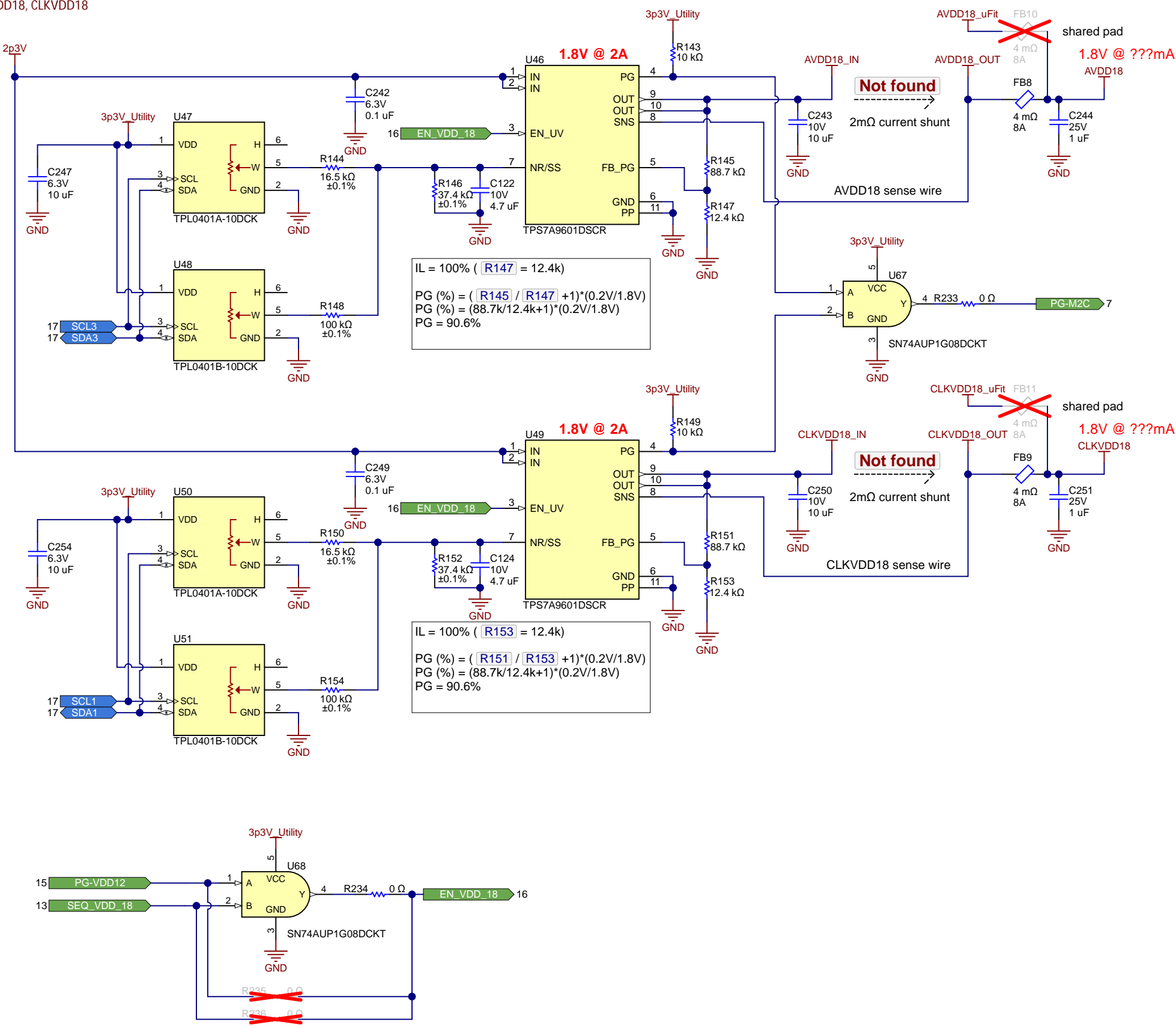
EVM Power 4
AVDD18, CLKVDD18

A

B

C

D

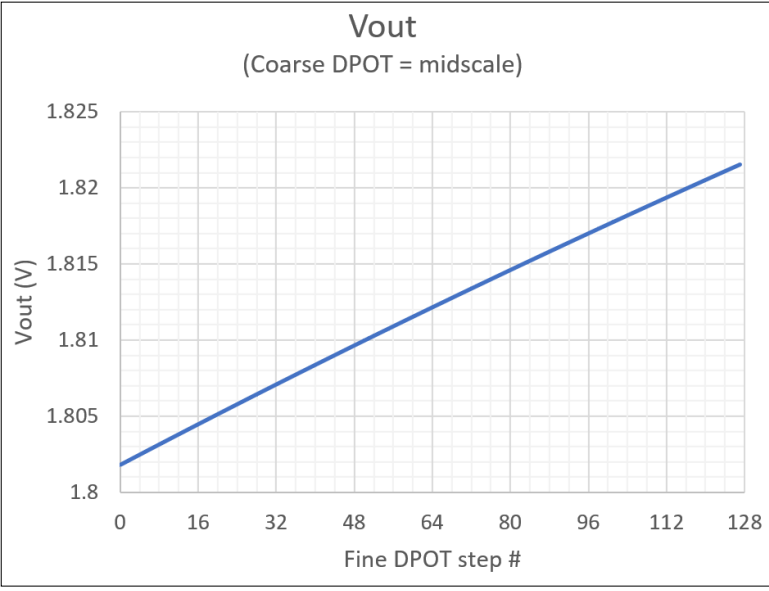
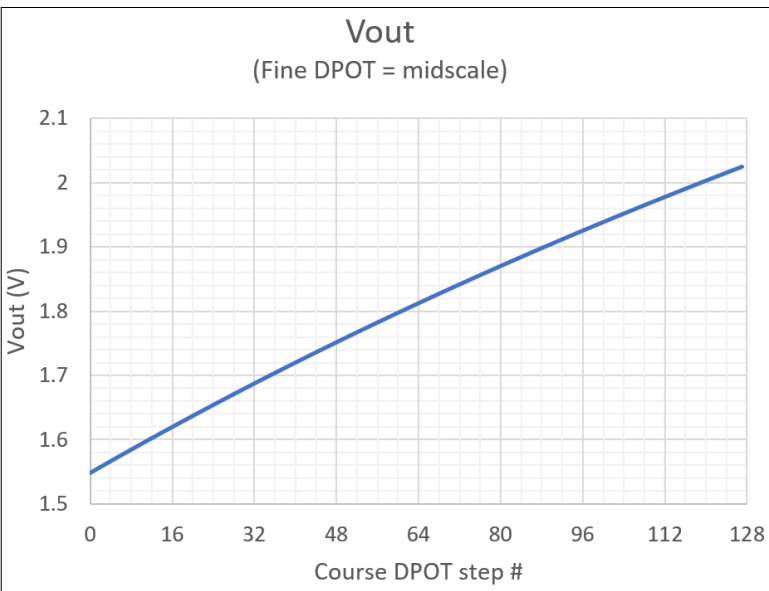


POWER UP SEQUENCE

1. DVDD (0.9V)
2. AVDD12 (1.2V) → CLKVDD12 (1.2V)
3. AVDD18 (1.8V) → CLKVDD18 (1.8V)

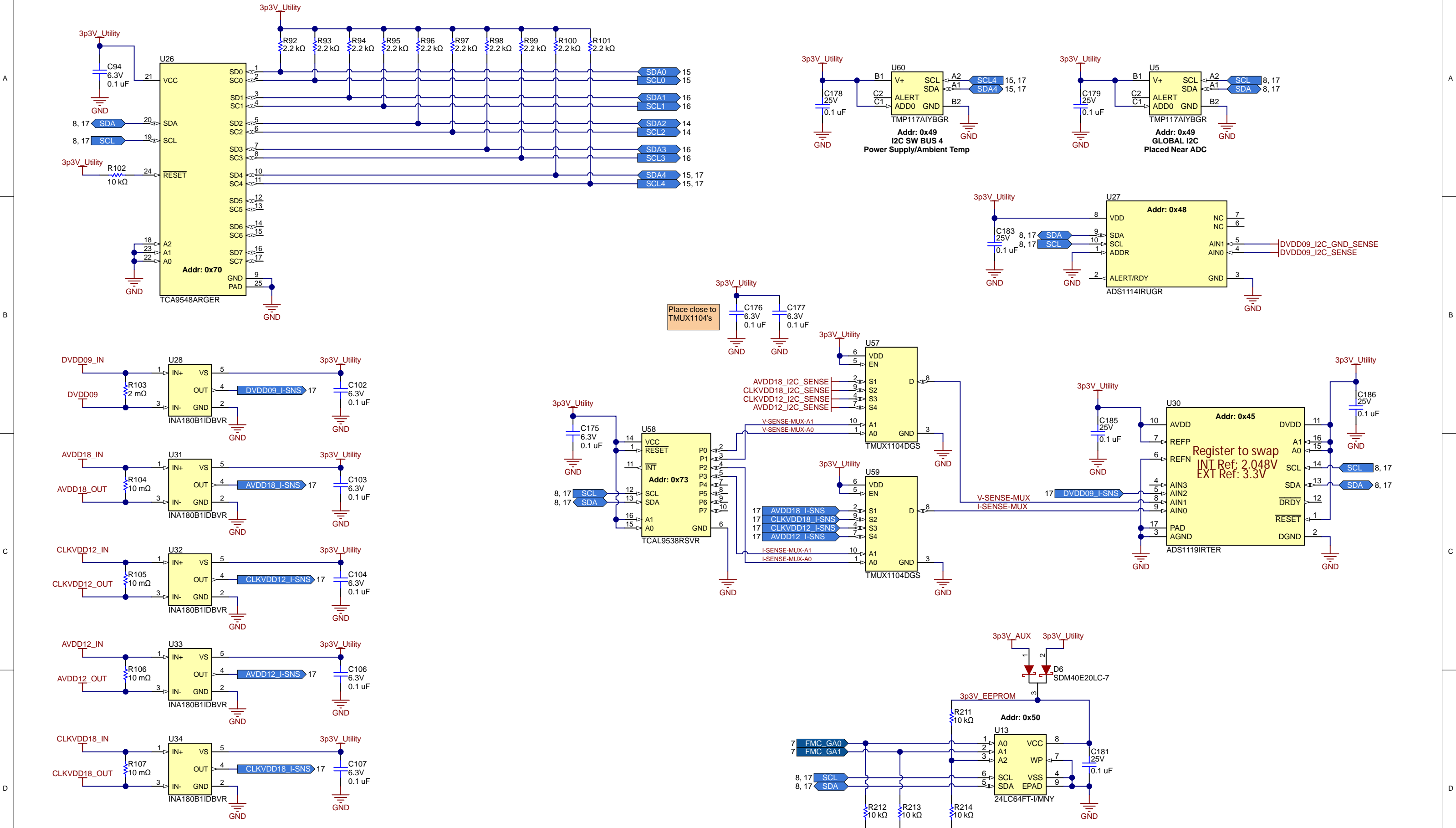
FOR ALL 1.8V MARGINING LDOs

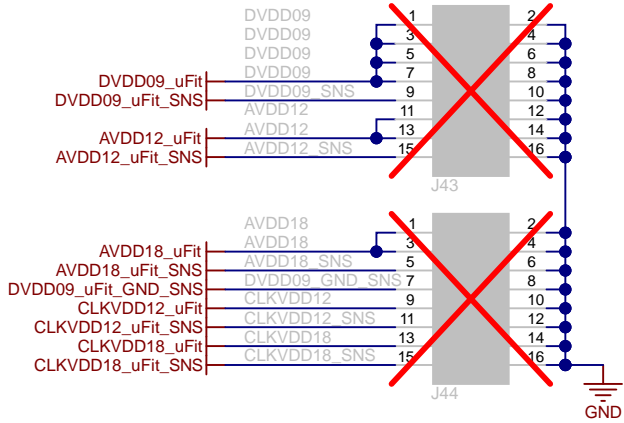
$$R_{NRSS} = 37.4k\Omega, R_{EQCOARSE}(nom) = 21.5k\Omega, R_{EQFINE}(nom) = 105k\Omega$$
$$R_{EQDPOTS}(nom) = \frac{21.5k\Omega * 105k\Omega}{21.5k\Omega + 105k\Omega} = 17.8458498k\Omega$$
$$R_{EQDPOTSNRSS}(nom) = \frac{17.8458498k\Omega * 37.4k\Omega}{17.8458498k\Omega + 37.4k\Omega} = 12.0811k\Omega \rightarrow V_{out} = 150\mu A * 12.0811k\Omega = 1.812V$$



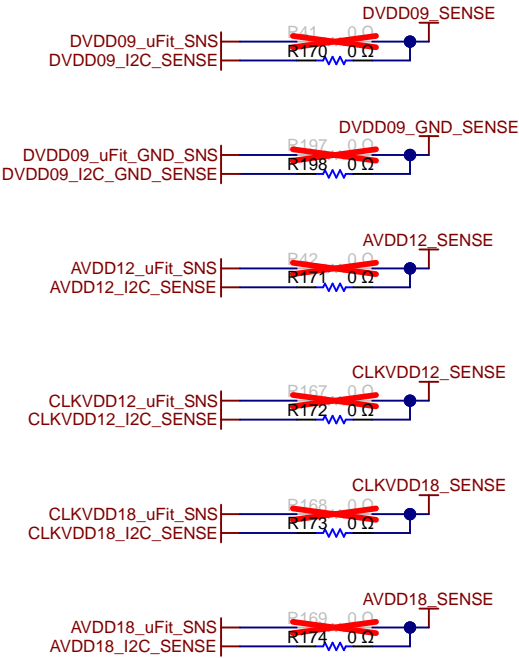
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I2C Devices





Place 0 ohm resistor close to existing sense line to leave minimal stub



Misc Hardware/Logos

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

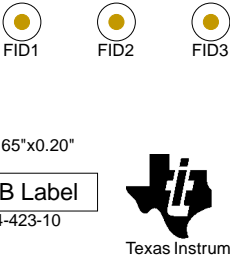
ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

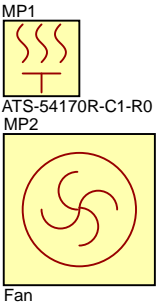
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Variant/Label Table	
Variant	Label Text
001	ADC3xRF7x_RevE2

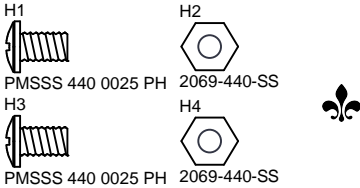
Size: 0.65"x0.20"
LBL1
PCB Label
THT-14-423-10



PCB
LOGO
FCC disclaimer



PCB Number: -
PCB Rev: A



Orderable: Not For Public Release		Designed for: Not For Public Release		Mod. Date: 2/24/2025	
TID #: Not For Public Release		Project Title: ADC34RF7xEVM			
Number: -		Rev: A		Sheet Title: Misc Hardware/Logos	
SVN Rev: 3549342212367fc0980ad16322031e356605c93		ADC34RF72		Sheet: 19 of 19	
Drawn By: CW		File: ADC34RF7x_Misc_RevA.SchDoc		Size: B	
Engineer: CW		Contact: http://www.ti.com/support			

Rev History & Variants

Revision History

Rev	Release Date	Notes
E1	Jun. 14, 2024	Initial Release
E2	Aug. 09, 2024	<ul style="list-style-type: none">• Swap GPIO3 and GPIO11 (fixes default SDO mapping)• Simplify SPI pullup/pulldown• Changes defaults for onboard power• Differential clock input (RF72 only) and single ended analog inputs• Fix LED current limit resistors• Swap AIN0 and AIN1 inputs on ADS1114• Combines I2C buses with optional break point• I2C bus pullup decreased to 3.74kΩ• Added second TMP117 on I2C bus 4 near power supply• Replaced all INA226 with INA180 shunts• Uses I2C IO expander for switching supply sense MUXes• EEPROM uses low Vf diode for powering through 3p3V_Utility and 3p3V_AUX (if connected to supporting FMC)• Updated DNI list to remove uncommonly used headers which are in high density areas• SYNCb routed to H31 through shared pad
E3	Jan. 28, 2025	<ul style="list-style-type: none">• Separates RESETb onto unique MUX for individual control• Allows break from RESETb to only use manual switch into watchdog• Adds 0Ω series R onto PDN and RESETb paths from FMC

Variant(s)

Variant	Notes
001	<ul style="list-style-type: none">• ADC34RF72
002	<ul style="list-style-type: none">• ADC32RF77

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Engineer: CW	Contact: http://www.ti.com/support	