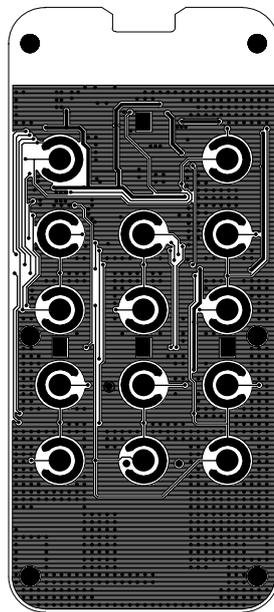


DRILL CHART: TOP to BOTTOM  
ALL UNITS ARE IN MILLIMETERS

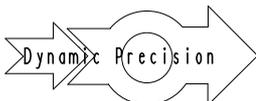
FIGURE	SIZE	PLATED	QTY
◻	0.3	PLATED	776
·	1.0	NON-PLATED	2
▲	1.0	NON-PLATED	1
⊙	2.5	NON-PLATED	6
▣	2.3x1.75	NON-PLATED	4

ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	Title <b>ZLLRC</b>		Layer <b>DRM</b>	PCB No.	Revision <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI		Latest Revision Prepared By PIOTR PRZYSTUP		Sheet of Size <b>1</b> of 10 <b>A4</b>
	First Revision Checked By ESPEN WIUM		Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013



ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	Title <b>ZLLRC</b>		Layer <b>PA1</b>	PCB No.	Revision <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI		Latest Revision Prepared By PIOTR PRZYSTUP		Sheet of <b>2</b> of <b>10</b>
	First Revision Checked By ESPEN WIUM		Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013

A

A

B

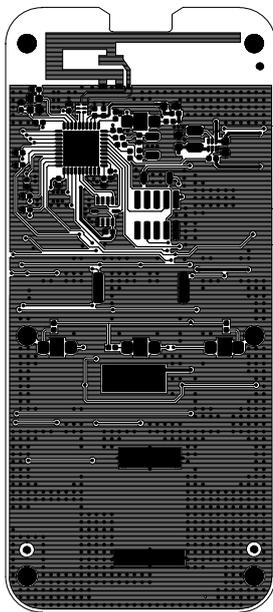
B

C

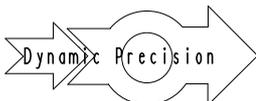
C

D

D



ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	Title <b>ZLLRC</b>		Layer <b>PA2</b>	PCB No.	Revision <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI		Latest Revision Prepared By PIOTR PRZYSTUP		Sheet of <b>3</b> of 10
	First Revision Checked By ESPEN WIUM		Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013

A

A

B

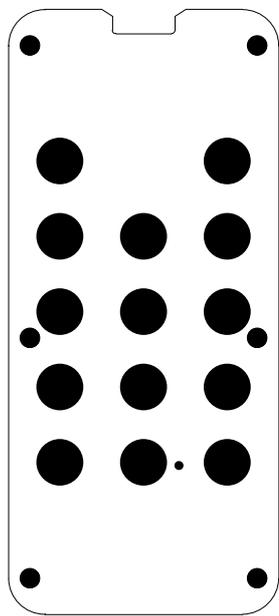
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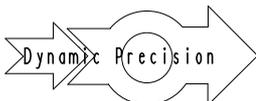
C

D

D



ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	Title <b>ZLLRC</b>		Layer <b>PL1</b>	PCB No.	Revision <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI		Latest Revision Prepared By PIOTR PRZYSTUP		Sheet of <b>4</b> of 10
	First Revision Checked By ESPEN WIUM		Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013

A

A

B

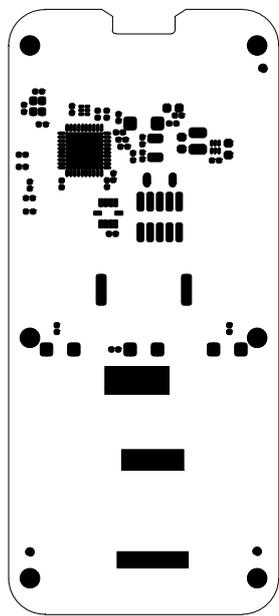
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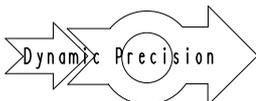
C

D

D



ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	<b>Title</b> <b>ZLLRC</b>		<b>Layer</b> <b>PL2</b>	<b>PCB No.</b>	<b>Revision</b> <b>1.1</b>
	<b>First Revision Prepared By</b> ANDRZEJ GRUCHALSKI		<b>Latest Revision Prepared By</b> PIOTR PRZYSTUP		<b>Sheet</b> <b>of</b> <b>5</b> <b>10</b>
	<b>First Revision Checked By</b> ESPEN WIUM		<b>Latest Revision Checked By</b> ESPEN WIUM		<b>Latest modification date</b> 03 April 2013

A

A

B

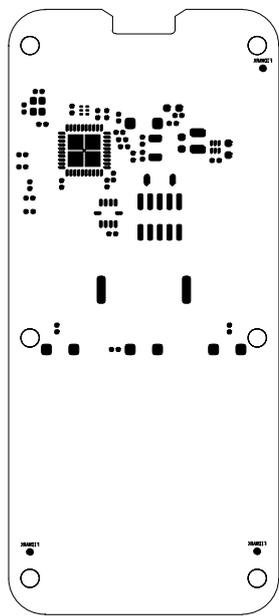
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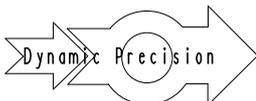
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D

D



ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	<b>Title</b> <b>ZLLRC</b>		<b>Layer</b> <b>SP2</b>	<b>PCB No.</b>	<b>Revision</b> <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI		Latest Revision Prepared By PIOTR PRZYSTUP		Sheet of Size <b>6</b> of <b>10</b> <b>A4</b>
	First Revision Checked By ESPEN WIUM		Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013

A

A

B

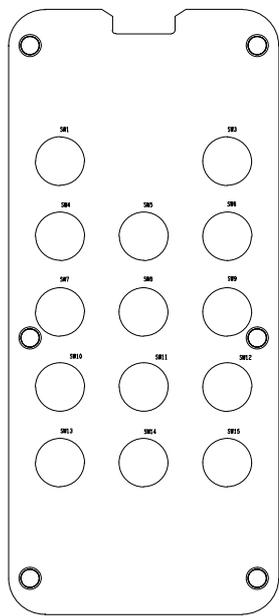
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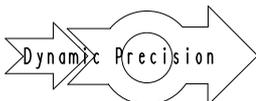
C

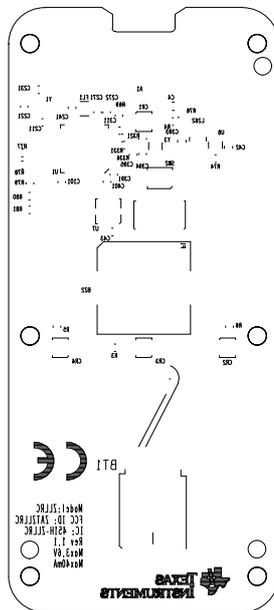
D

D

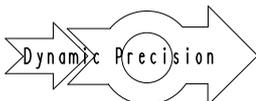


ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	<b>Title</b> <b>ZLLRC</b>		<b>Layer</b> <b>SS1</b>	<b>PCB No.</b>	<b>Revision</b> <b>1.1</b>
	<b>First Revision Prepared By</b> ANDRZEJ GRUCHALSKI		<b>Latest Revision Prepared By</b> PIOTR PRZYSTUP		<b>Sheet</b> <b>of</b> <b>7</b> <b>10</b>
	<b>First Revision Checked By</b> ESPEN WIUM		<b>Latest Revision Checked By</b> ESPEN WIUM		<b>Latest modification date</b> 03 April 2013



ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	<b>Title</b> <b>ZLLRC</b>		<b>Layer</b> <b>SS2</b>	<b>PCB No.</b>	<b>Revision</b> <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI		Latest Revision Prepared By PIOTR PRZYSTUP		Sheet <b>8</b> of 10
	First Revision Checked By ESPEN WIUM		Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013

A

A

B

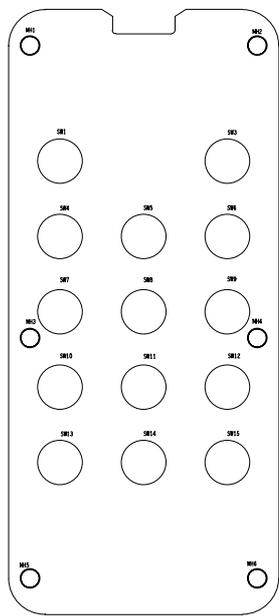
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C

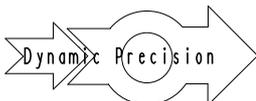
C

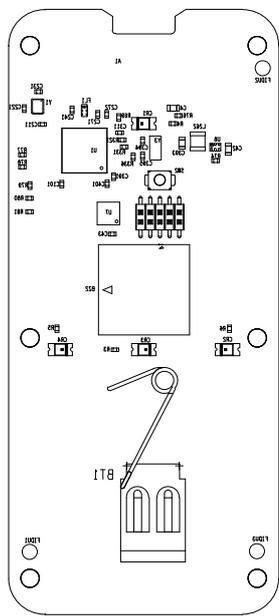
D

D

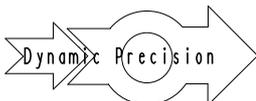


ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	<b>Title</b> <b>ZLLRC</b>		<b>Layer</b> <b>AD1</b>	<b>PCB No.</b>	<b>Revision</b> <b>1.1</b>
	<b>First Revision Prepared By</b> ANDRZEJ GRUCHALSKI		<b>Latest Revision Prepared By</b> PIOTR PRZYSTUP		<b>Sheet</b> <b>of</b> <b>9</b> <b>10</b>
	<b>First Revision Checked By</b> ESPEN WIUM		<b>Latest Revision Checked By</b> ESPEN WIUM		<b>Latest modification date</b> 03 April 2013



ALL DRAWINGS SEEN FROM LAYER1 (TOP) UNLESS OTHER STATED

	<b>Title</b> <b>ZLLRC</b>		<b>Layer</b> <b>AD2</b>	<b>PCB No.</b>	<b>Revision</b> <b>1.1</b>
	First Revision Prepared By ANDRZEJ GRUCHALSKI		Latest Revision Prepared By PIOTR PRZYSTUP		Sheet of <b>10</b> of <b>10</b>
	First Revision Checked By ESPEN WIUM		Latest Revision Checked By ESPEN WIUM		Latest modification date 03 April 2013

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