Application Report
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PMP9762 Test Report — Efficient, Step-Down, High-Power LED Driver With Synchronization for Fire Alarms

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Low Power DC-DC

ABSTRACT

This application report demonstrates the design and test results of an efficient, step-down, high-power LED driver for generating the strobe light used in fire alarms. The LED driver is enabled by an external synchronization signal, which allows multiple circuits to strobe at exactly the same time. Alternatively, an on-board timing circuit allows simple testing with a pre-configured strobe at a 1% duty cycle every second. The TPS62130 step-down converter is used in this application to provide a high efficiency and easily implemented dimming of a single 3-A LED from a quasi-regulated 12-V input voltage.

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1 PMP9762 Specifications

This TI Design demonstrates driving a 3-A LED with pulses of current to create a strobe effect, such as is found in fire alarms. A common 12-V semi-regulated input source voltage is used and a synchronization signal from an outside clock source is accepted.

Cree's XP-L series of LEDs is used, because of its small size and high current operation. A single LED is used, which has a forward voltage of about 3.5 V at 3 A and 25°C. See Reference 1 for details of the LED.

The TPS62130 is chosen as the LED driver, because it accepts a wide 3-V to 17-V input voltage range and outputs 3 A of current in a very small 3-mm × 3-mm package, while delivering around 90% efficiency. See Reference 2 for details of the IC.

Table 1 shows the performance specifications for PMP9762.

Table 1. Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Unit
Input Voltage		4.5	12	17	V
LED Current		0		3	A
Peak Efficiency	I_{LED} = 3 A		90%		
PWM Dimming Duty Cycle	Applied to JP1	0%	1%	100%(1)	
Analog Dimming Voltage	Applied to J7	0		155	mV

(1) Duty cycles above 50% may need to reduce the LED current to avoid thermal limits of the LED.

2 Design Procedure

2.1 Setting the LED Current

The 3-A LED current is set by the voltage across a sense resistor, R2. This is the voltage at the FB pin and is controlled by the voltage on the SS/TR pin. Due to the tolerances in these circuits, the actual amount of LED current can vary from the calculated value. In most applications, this has a negligible impact on the perceived brightness of the LED.

First, the FB pin voltage is set to a lower level, such as 100 mV, to reduce the losses in the sense resistor:

$$R2 = \frac{V_{FB}}{I_{OUT}} = \frac{0.100\,V}{3\,A} = 0.0333\,\Omega \quad (1)$$

A common value of 33 mΩ is chosen for R2.

Next, the FB pin voltage is set by setting the SS/TR pin voltage:

$$V_{FB} \times \frac{1.25}{0.8} = V_{SS/TR} = 0.099\,V \times \frac{1.25}{0.8} = 0.155\ V \quad (2)$$

Finally, the SS/TR pin voltage is set by choosing a proper value for R1, based on the SS/TR pin's 2.5-µA current source:

$$R1 = \frac{V_{SS/TR}}{I_{SS/TR}} = \frac{0.155\,V}{2.5\,\mu A} = 62\,k\Omega \quad (3)$$

A common value of 61.9 kΩ is chosen for R1.

2.2 Inductor

An inductor (L1) must be selected that is within the recommended range in the TPS62130's datasheet (SLVSAG7). In order to use the low frequency setting and achieve higher efficiency, a 2.2-µH inductor is required. Coilcraft's XFL4020-222MEB is selected for its high current handling and high efficiency.

2.3 Output Capacitor

To maintain stability, an output capacitor (C3) must be selected within the recommended range. The recommended LC output filter combination is found in the TPS62130's datasheet with a more detailed LC stability matrix in Reference 3. This application uses the recommended 2.2-µH inductor and 22-µF ceramic output capacitor. A small value of output capacitance is acceptable, since the output voltage ripple is not critical for an LED driver.

2.4 Input Capacitor

A 10-µF input capacitor (C1) is required by the TPS62130's datasheet. To reduce the size of the capacitor, a 22-µF ceramic capacitor is chosen and has similar effective capacitance to a 10-µF capacitor in a larger case size due to DC bias performance. The datasheet also requires a 0.1-µF decoupling capacitor on AVIN (C7). Finally, 68 µF of bulk capacitance (C6) is added to overcome any high impedance that might be present between the input source and the PCB. Such capacitance may not be required in the final application.

3 Test Results

This section shows test data acquired from PMP9762. If not otherwise noted, Vin = 12 V, LED Current = 3 A, DEF = Low, FSW = High, EN = High, JP4 and JP5 = open. Due to the thermal limits of operating the LED at 3-A DC, DC efficiency and line regulation are taken at 1 A through analog dimming on J7. The 3-A data is measured with an oscilloscope under pulsed conditions (1% duty cycle at 1 Hz).

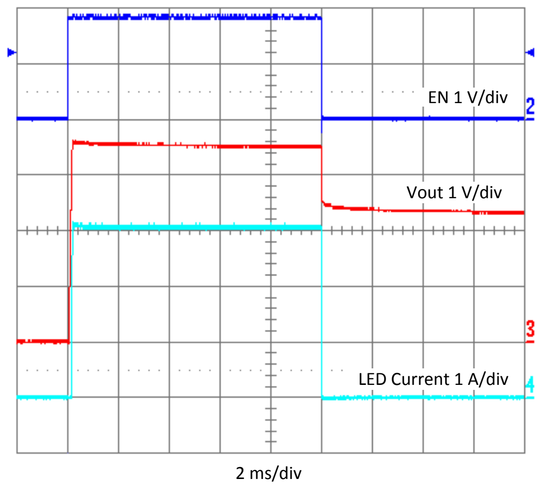

Figure 1. Start-Up on EN

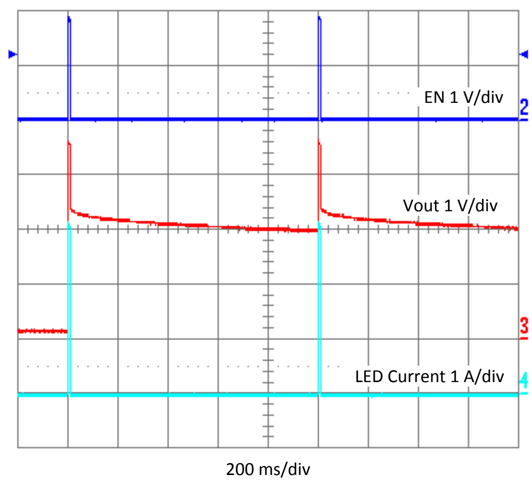

Figure 2. PWM Dimming on EN With 1% Duty Cycle at 1 Hz

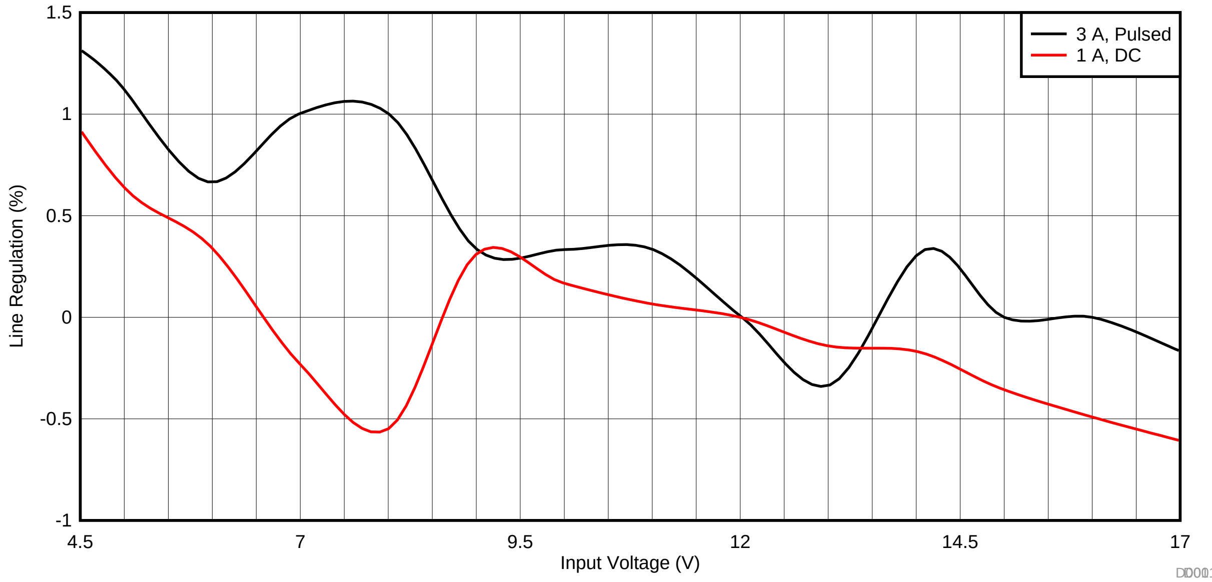

Figure 3. Line Regulation

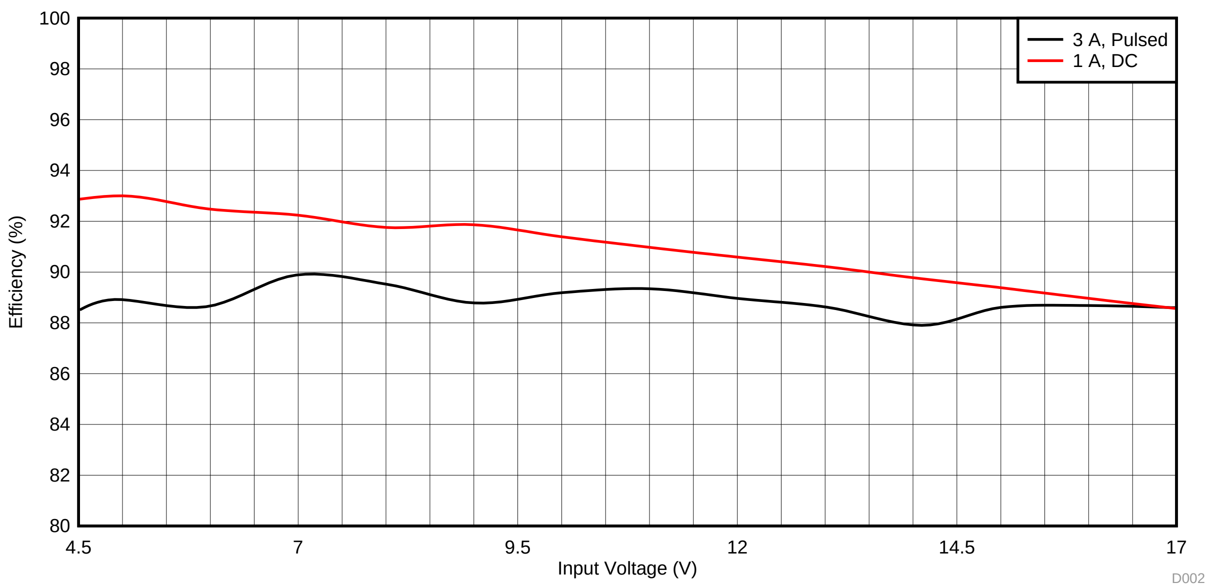

Figure 4. Efficiency vs Input Voltage

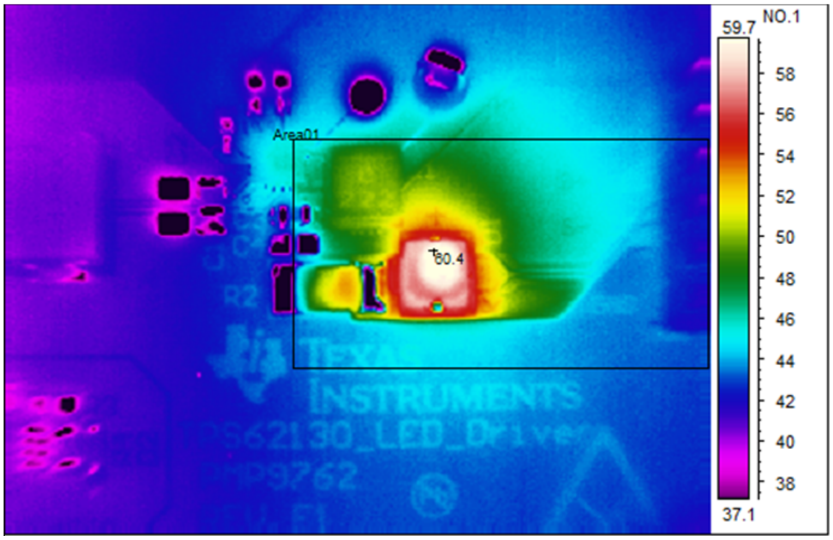

Figure 5. Thermal Performance (1-A LED Current, DC)

4 Schematic

Figure 6 shows the schematic.

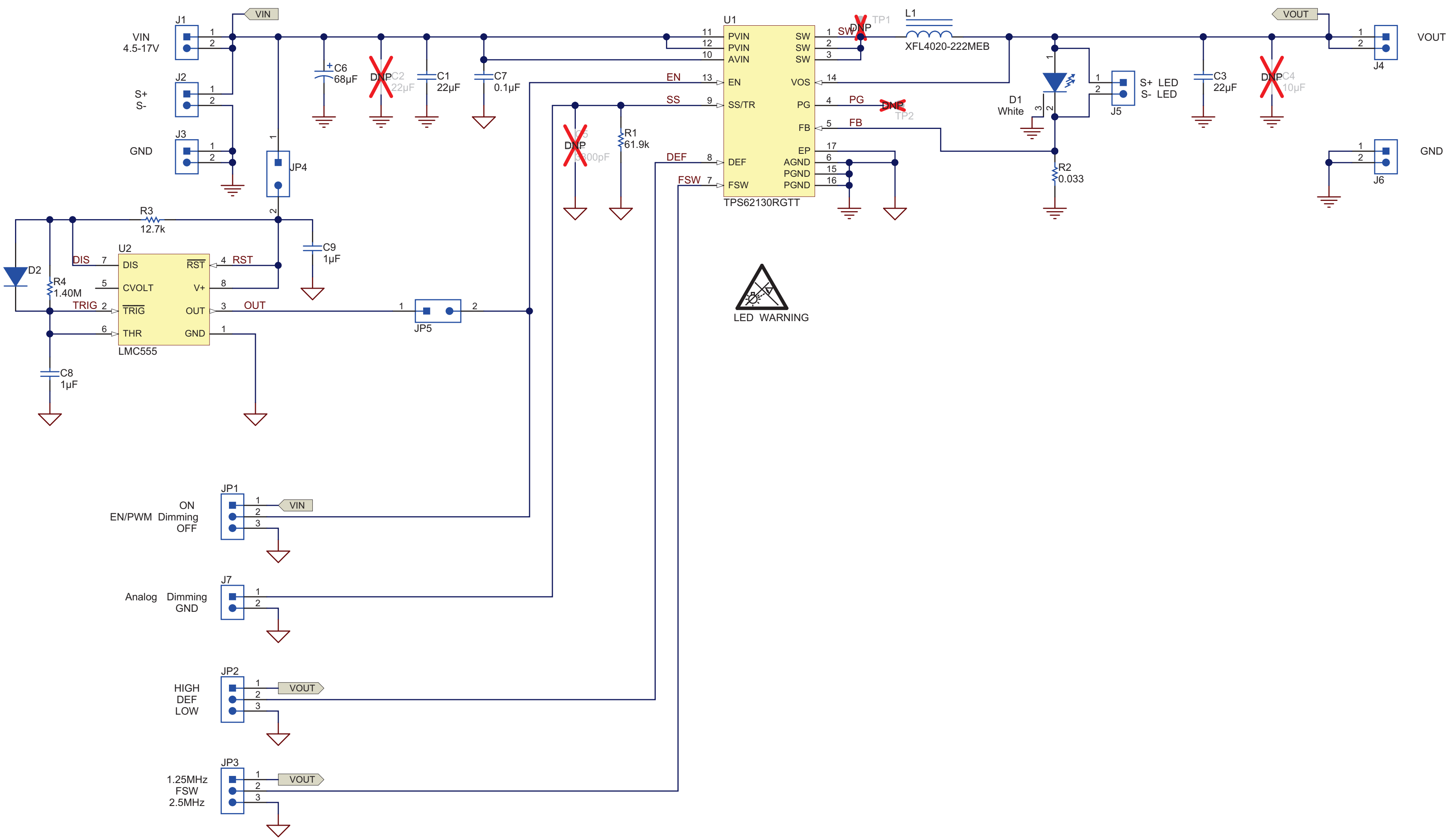

Figure 6. Schematic

4.1 Jumpers and Connectors

This section describes the jumpers and connectors on PMP9762 and how each should be used. The function of uninstalled components is also explained.

J1 – VIN	Positive input connection from the input supply.
J2 – S+/S–	Input voltage sense connections. Measure the input voltage at this point.
J3 – GND	Return connection from the input supply.
J4 – VOUT	Output voltage connection.
J5 – S+ LED/S– LED	LED forward voltage sense connection. Measure the LED's forward voltage at this point.
J6 – GND	Output return connection.
J7 – Analog Dimming	Apply a voltage from 0 to 155 mV to this pin to analog dim the LED. Otherwise, do not connect.
JP1 – EN/PWM Dimming	EN/PWM dimming input jumper. JP4 and JP5 must be open to use the jumper on JP1. Place the supplied jumper across ON and EN to turn on the IC. Place the jumper across OFF and EN to turn off the IC. The EN/PWM Dimming pin can also be used to dim the LED. In this case, apply the PWM signal to this pin without any jumper installed. A 100-Hz PWM signal is recommended for non-visible dimming. For the strobe effect, a 1-Hz signal is recommended.
JP2 – DEF	DEF pin input jumper. Place the supplied jumper across HIGH and DEF to set the LED current at 5% above nominal. Place the jumper across LOW and DEF to set the LED current at the nominal level.
JP3 – FSW	FSW pin input jumper. Place the supplied jumper across 1.25 MHz and FSW to operate the IC at a reduced switching frequency of nominally 1.25 MHz. Place the jumper across 2.5 MHz and FSW to operate the IC at the full switching frequency of nominally 2.5 MHz. A higher switching frequency allows the use of small external components for the output filter but provides lower efficiency.
JP4 – Timer_EN	Timer enable input jumper. Install the supplied jumper to supply power to timer IC. JP1 must be removed to use the timer circuit.
JP5 – Timer_OUT	Timer output jumper. Install the supplied jumper to connect the output of the timer to the EN pin of the TPS62130. The timer outputs a 1% duty cycle pulse at a 1-Hz rate at 12 Vin. JP1 must be removed to use the timer circuit.

4.2 Uninstalled Components

C2 – Cin	Extra input capacitance may be added here to reduce the input voltage ripple.
C4 – Cout	Extra output capacitance may be added here to reduce the output voltage ripple.
C5 – Css/tr	A small capacitor may be installed here to slow down the start-up of the TPS62130. This reduces inrush current but decreases dimming linearity.

5 Bill of Materials (BOM)

The bill of materials (BOM) is given in three sections: components required to assemble the LED driver circuit as it would be used in the final application, components used for the 555 timer circuit, and other components (connectors, uninstalled components, and so forth).

Table 2. Bill of Materials for LED Driver Circuit

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
C1	1	22µF	CAP, CERM, 22 µF, 25 V, ±20%, X5R, 0805	0805	GRM21BR61E226ME44	Murata
C3	1	22µF	CAP, CERM, 22 µF, 6.3V, ±20%, X5R, 0603	0603	JMK107BBJ226MA-T	Taiyo Yuden
C7	1	0.1µF	CAP, CERM, 0.1 µF, 25 V, ±10%, X5R, 0402	0402	GRM155R61E104KA87D	Murata
D1	1	White	LED, White, SMD	LED, 3.45x3.45mm	XPLAWT-00-0000-000BV20E3	Cree
L1	1	2.2µH	Inductor, Shielded, Composite, 2.2 µH, 3.7 A, 0.02 Ω, SMD	4x2x4mm	XFL4020-222MEB	Coilcraft
R1	1	61.9k	RES, 61.9 k, 1%, 0.1 W, 0603	0603	RC0603FR-0761K9L	Yageo America
R2	1	0.033	RES, 0.033, 1%, 0.5 W, 2010	2010	WSL2010R0330FEA	Vishay-Dale
U1	1		Buck Step Down Regulator with 3 to 17 V Input	3 x 3 mm	TPS62130RGTT	Texas Instruments

Table 3. Bill of Materials for 555 Timer Circuit

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
C8, C9	2	1µF	CAP, CERM, 1 µF, 25 V, ±10%, X7R, 0805	0805	GRM21BR71E105KA99L	Murata
D2	1	75V	Diode, Switching, 75 V, 0.3 A, SMD, 2-Leads, Body 1.2x0.8mm	SMD, 2-Leads, Body 1.2x0.8mm	1N4148WT	Fairchild Semiconductor
R3	1	12.7k	RES, 12.7 k, 1%, 0.1 W, 0603	0603	RC0603FR-0712K7L	Yageo America
R4	1	1.40Meg	RES, 1.40 M, 1%, 0.1 W, 0603	0603	CRCW06031M40FKEA	Vishay-Dale
U2	1		CMOS Timer, 8-pin Mini SOIC, Pb-Free	MUA08A	LMC555CMM/NOPB	Texas Instruments

Table 4. Bill of Materials for Other Components

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer
PCB	1		Printed Circuit Board		PMP9762	Any
C6	1	68µF	CAP, TA, 68 µF, 25 V, ±20%, 0.095 ohm, SMD	7361-38	TPSV686M025R0095	AVX
J1–J7, JP4, JP5	9		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
JP1, JP2, JP3	3		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
C2	0	22µF	CAP, CERM, 22 µF, 25 V, ±20%, X5R, 0805	0805	GRM21BR61E226ME44	Murata
C4	0	10µF	CAP, CERM, 10 µF, 16 V, ±20%, X5R, 0603_950	0603_950	GRM188R61C106MAALD	Murata
C5	0	3300pF	CAP, CERM, 3300 pF, 25 V, ±10%, X7R, 0603	0603	GRM188R71E332KA01D	Murata
TP1, TP2	0	Yellow	Test Point, Compact, Yellow, TH	Yellow Compact Test point	5009	Keystone

6 Board Layout

Figure 7 through Figure 11 illustrate the board layout.

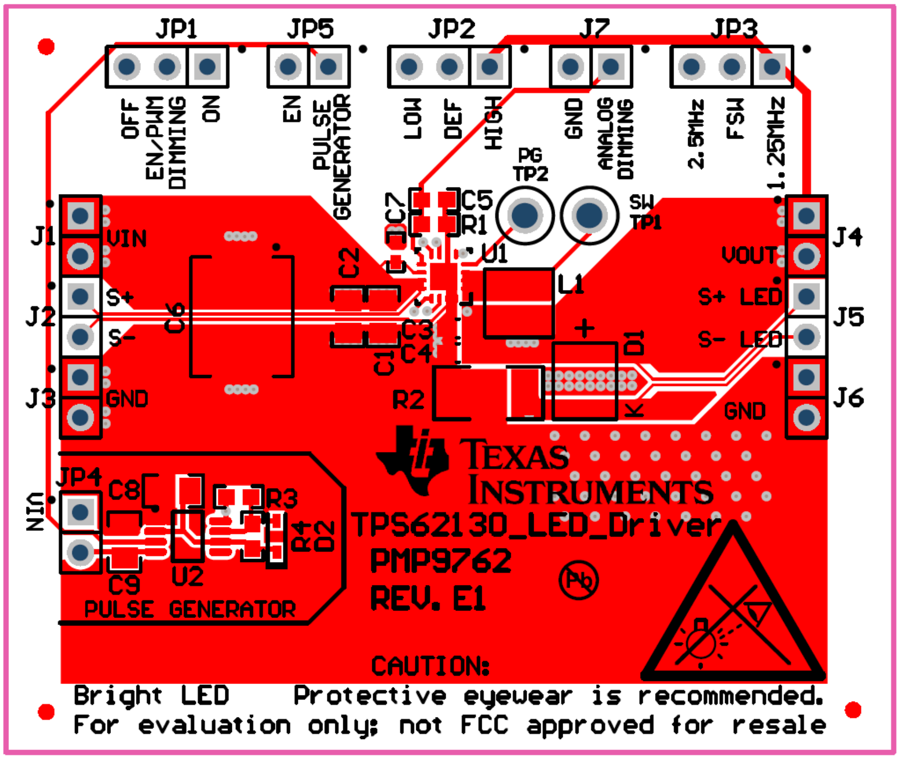

Figure 7. Assembly Layer

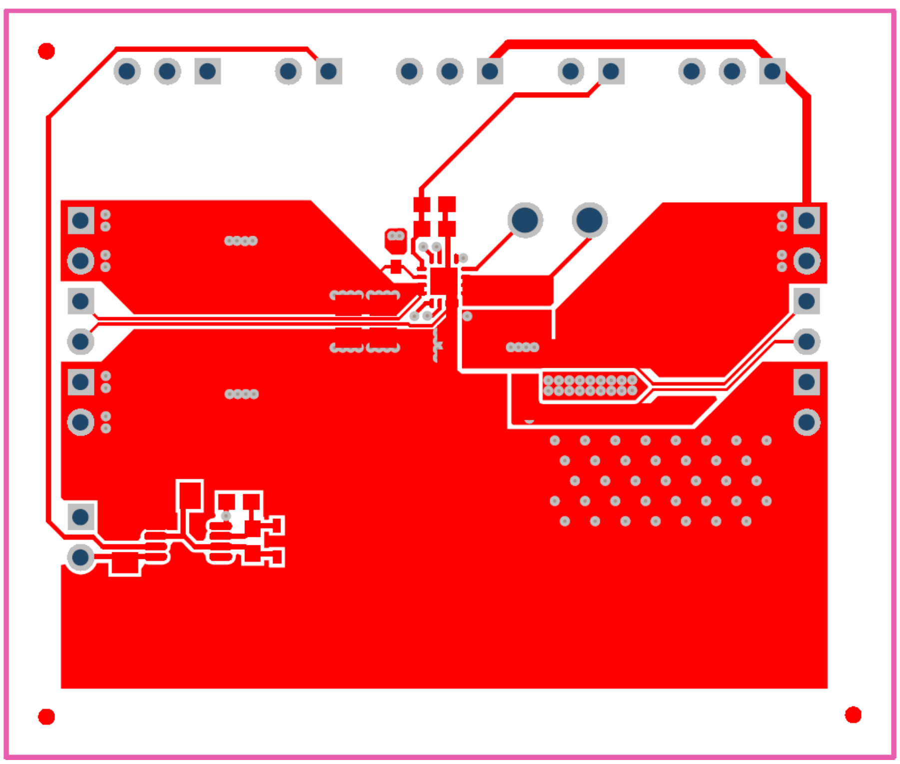

Figure 8. Top Copper Layer

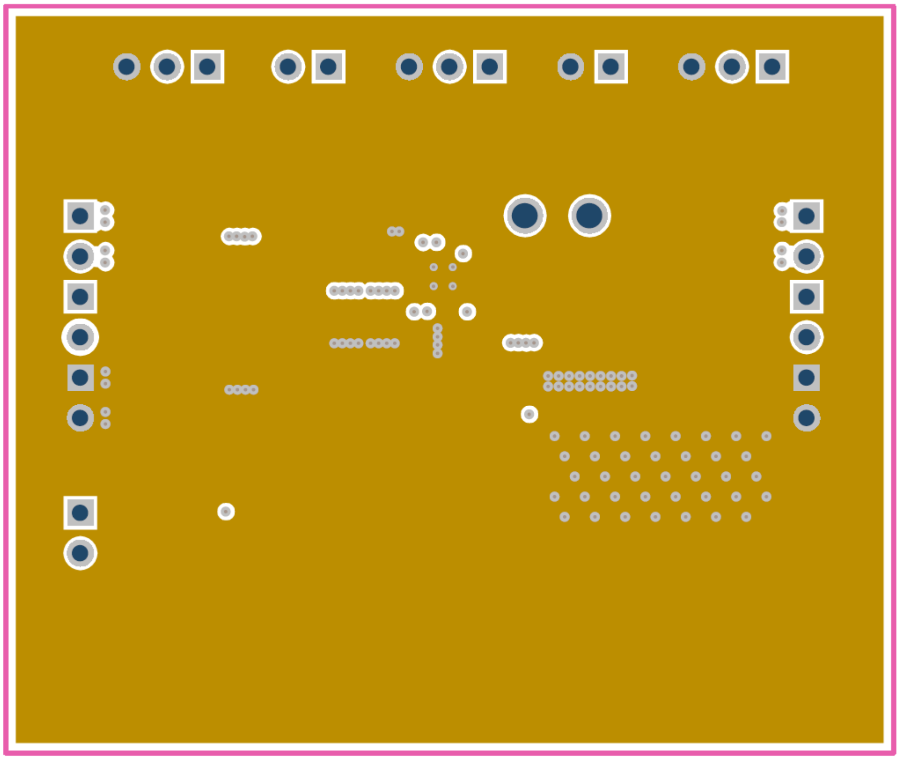

Figure 9. Inner Copper Layer 1

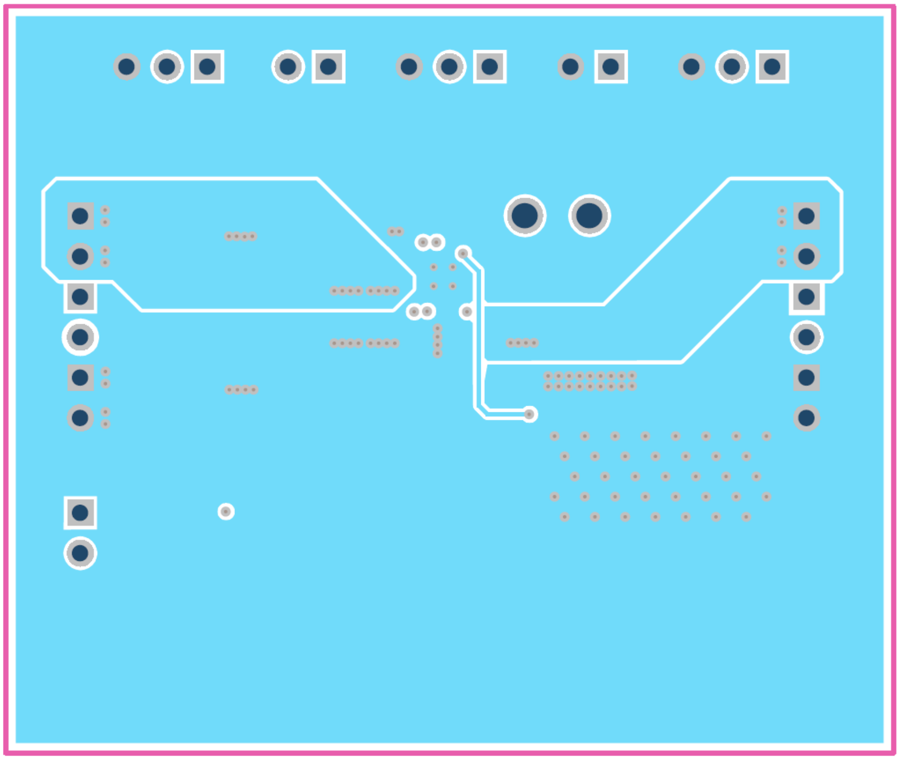

Figure 10. Inner Copper Layer 2

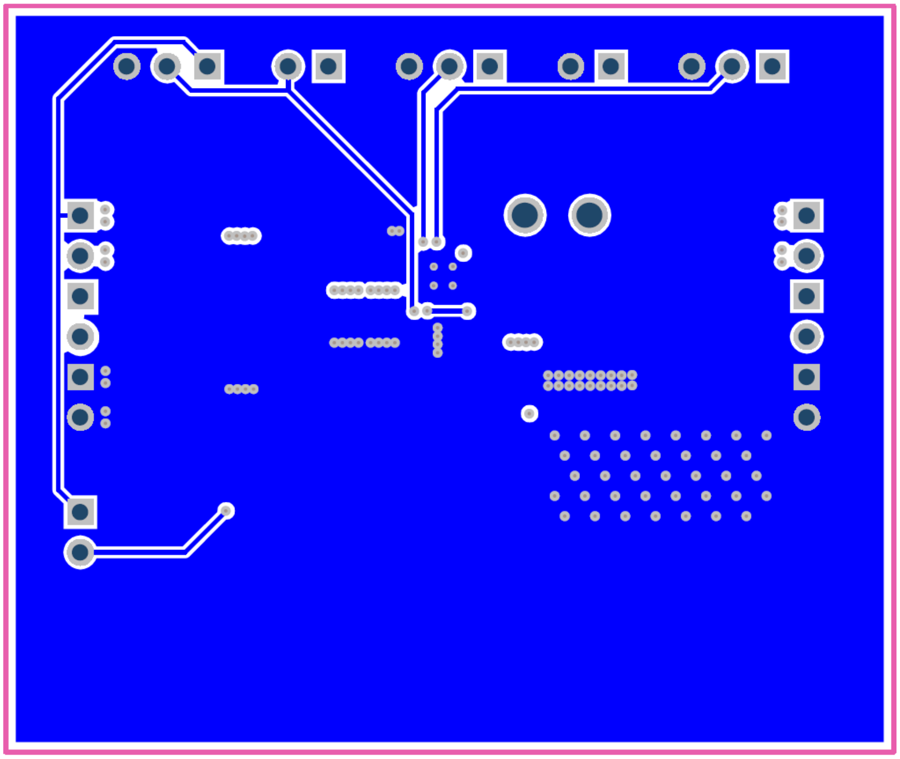

Figure 11. Bottom Copper Layer

7 References

1. http://www.cree.com/LED-Components-and-Modules/Products/XLamp/Discrete-Directional/XLamp-XPL
2. TPS62130 3-17V 3A Step-Down Converter in 3x3 QFN Package data sheet (SLVSAG7)
3. Optimizing the TPS62130/40/50/60 Output Filter, Application Report (SLVA463)
4. Using the TPS62150 as Step-Down LED Driver With Dimming, Application Report (SLVA451)

555 Timer Circuit

A.1 555 Timer Circuit Operation

A 555 timer is configured in astable mode to create a 1% duty cycle pulse at 1 Hz for easy evaluation in the typical use case. This timer circuit would typically not be implemented in the final product, as a master clock source is given to synchronize all fire alarms to a common signal.

Astable operation outputs a square wave with a configurable period and duty cycle. The threshold and trigger inputs monitor the C8 capacitor voltage. When the capacitor voltage reaches 2/3 of the supply voltage (8 V), the THRES pin trips and makes the output low. Now, the capacitor discharges through the DISC pin. When the capacitor voltage decreases to 1/3 of the supply voltage (4 V), then the THRES pin trips and makes the output high again. This repeats continuously. Diode D2 is added to make the capacitor charging be faster than the discharging in order to achieve duty cycles of less than 50%.

The resistors and capacitors set the circuit's timings. The capacitor is chosen to be a common 1 µF. The capacitor charges through R3 and D2 and discharges through R4. The output is high when the capacitor charges and low when it discharges.

A.2 555 Timer Circuit Schematic

Figure 12 is the 555 timer circuit schematic.

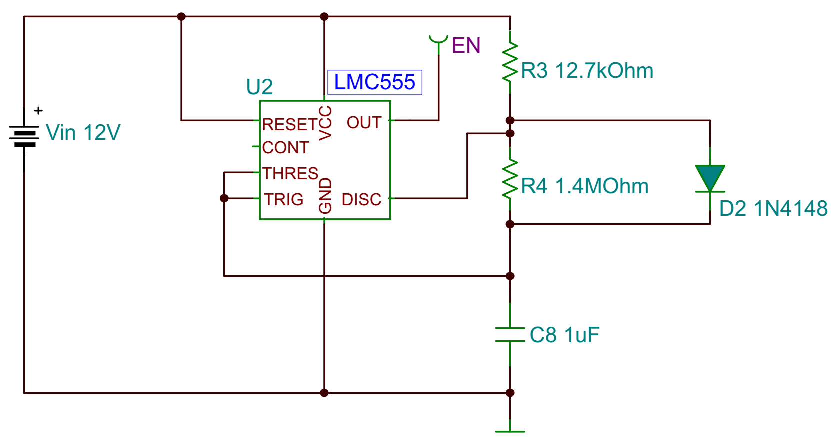

Figure 12. 555 Timer Circuit

A.3 PMP9762 555 Timer Simulation Results

Figure 13 and Figure 14 illustrate two PMP9762 555 timer simulation results.

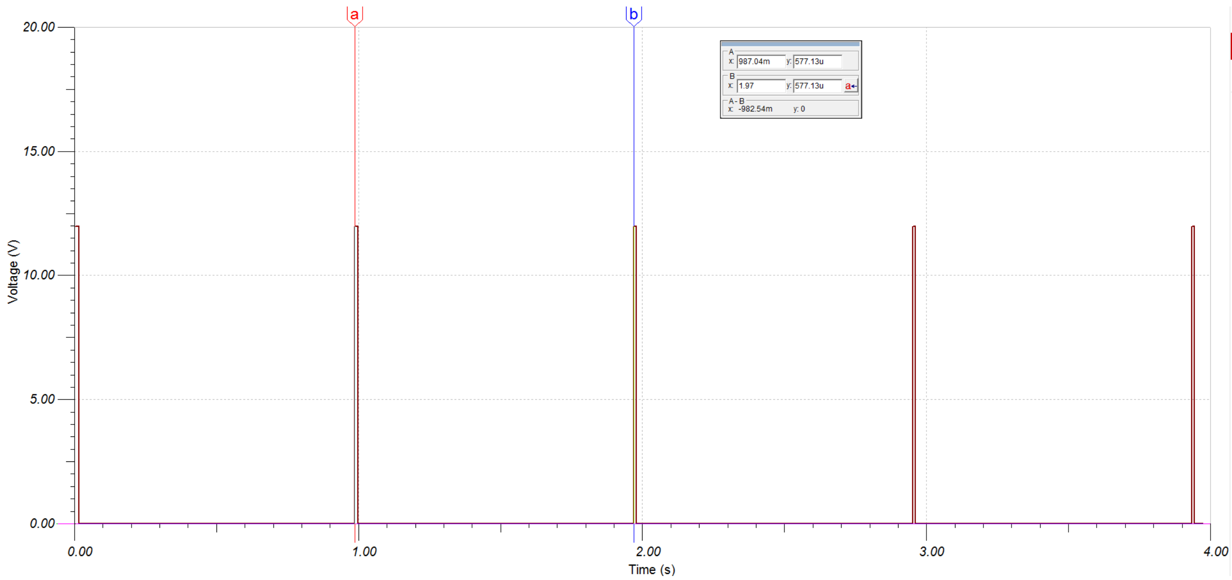

Figure 13. 982 msec Simulated Period for Output of Timer Circuit

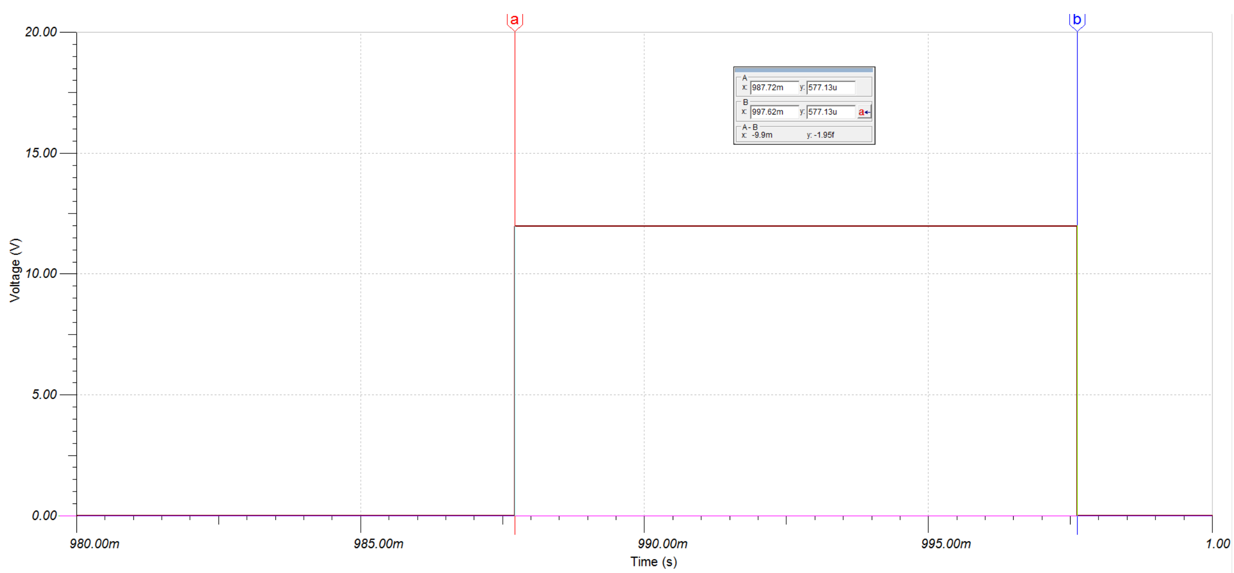

Figure 14. 9.9 msec Simulated On time for Output of Timer Circuit

A.4 PMP9762 555 Timer Test Results

Figure 15 and Figure 16 show PMP9762 555 timer test results.

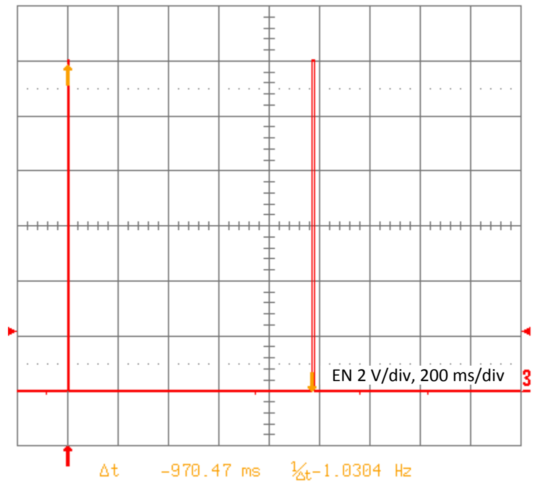

Figure 15. 970 msec Measured Period for Output of Timer Circuit

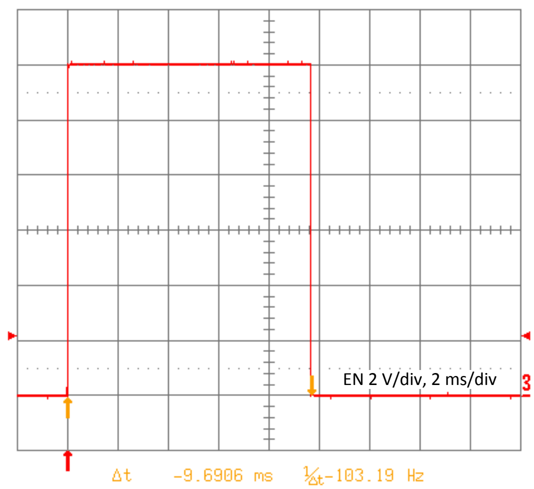

Figure 16. 9.69 msec Measured On Time for Output of Timer Circuit