

# Configuring the bq27000/200 for Gas Gauge Applications

Bill Jackson

Battery Management

## ABSTRACT

Users of the bq27000 and bq27200 ICs can program ten EEPROM locations to optimize setups for particular battery and host requirements. This application report describes how to configure these ICs for those requirements.

## 1 Programming the EEPROM

Users of the bq27000 and bq27200 ICs can program ten EEPROM locations to optimize setups for particular battery and host requirements. These EEPROM locations are mapped directly to RAM locations 0x76 to 0x7f. The host can only write to these locations during a special test mode. This test mode is entered by writing 0xdd to address 0x6e. This action allows write access to these RAM locations and allows transferring the RAM contents into EEPROM. The bq27000/200 processing is inhibited while address 0x6e contains 0xdd and when EEPROM programming is complete, address 0x6e must be written back to 0x00. The bq27000/200 processor is reset by this action, and the new EEPROM values take effect at that time.

The actual EEPROM programming is accomplished by reading each address (after previously writing it with the desired data) and then applying a programming pulse of 21 volts amplitude for a 10-ms to 100-ms duration. After all programming changes have been accomplished, the test system must write 0x00 to address 0x6e. This action disables write access to the EEPROM values, resets the bq27000/200, and allows normal execution to resume.

### 1.1 Initial Last Measured Discharge

The initial last measured discharge (ILMD) value is the design capacity of the battery. The high byte of last measured discharge (LMD) is set equal to ILMD on a full reset. LMD is then used for the 100% full-capacity reference. The bq27000/200 subsequently updates this value with the learned capacity of the battery. It is recommended to program the ILMD with a value slightly smaller than the expected initial capacity of the battery. This reduces the perturbation that may occur later in the equipment lifetime due to some unexpected reset, where corruption of RAM values is evident. A reset without RAM corruption (the register backup input maintains the RAM content) leaves the LMD value at its learned value and does not cause it to be reinitialized to ILMD. Units for ILMD are  $256 \times 3.57 \mu\text{Vh}$  per least significant bit (LSB).

The EEPROM value for ILMD is programmed in address 0x76. The formula for determining the EEPROM value for ILMD is:

$$\text{ILMD} = \text{DesignCapacity(mAh)} \times \frac{R_S(\text{m}\Omega)}{256 \times 3.57 \mu\text{Vh}} \quad (1)$$

Example: If the battery design capacity is 1000 mAh and the sense resistor is 20 mΩ, the value to be programmed in ILMD would be:  $1000 \text{ mAh} \times 20 \text{ m}\Omega / (256 \times 3.57 \mu\text{Vh}) = 21.9$ . The next smaller value is 21 decimal, or 15 hexadecimal. Setting ILMD to 0x15 initializes LMD to 0x1500 (5376 decimal), or 960 mAh with a 20-mΩ sense resistor.

## 1.2 Scaled End-of-Discharge Voltage Final

Set the scaled end-of-discharge voltage final (SEDFV) voltage to the threshold where the battery is expected to have zero capacity. This threshold is typically about 3000 mV. Nominal available capacity (NAC) is adjusted to zero during a discharge if this voltage threshold is reached. Units for SEDVF are 8 mV, with a 2048-mV offset.

Program the EEPROM value for SEDVF in address 0x77. The formula for determining the EEPROM value for SEDVF is:

$$\text{SEDFV} = \frac{\text{DesignEDVF(mV)}}{8} - 256 \quad (2)$$

Example: To set the EDVF threshold to 3000 mV, the value to be programmed in SEDVF is:  $3000 \text{ mV}/8 - 256 = 119$  decimal or 77 hexadecimal.

## 1.3 Scaled End-of-Discharge Voltage First

Set the scaled end-of-discharge voltage first (SEDEV1) voltage to the threshold where the battery is expected to have 6.25% capacity remaining under typical load conditions. NAC is adjusted down to LMD/16 during a discharge (unless NAC is already a smaller value) when this voltage threshold is reached. If NAC reaches LMD/16 before the EDV1 threshold is reached and the discharge is a valid learning cycle discharge (VDQ = 1), NAC is held at the LMD/16 value until the EDV1 threshold is reached. Thus, NAC is synchronized to the 6.25% capacity level at the EDV1 threshold. This threshold also terminates a learning cycle. The learned capacity has  $\text{LMD} \times 6.25\%$  added to the measured discharge from full to EDV1; so, setting the EDV1 threshold to a value appropriate to 6.25% of LMD is critical. Units for SEDV1 are 8 mV, with a 2048-mV offset.

Program the EEPROM value for SEDV1 in address 0x78. The formula for determining the EEPROM value for SEDV1 is:

$$\text{SEDEV1} = \frac{\text{DesignEDV1(mV)}}{8} - 256 \quad (3)$$

Example: To set the EDV1 threshold to 3350 mV, the value to be programmed in SEDV1 is:  $3350 \text{ mV}/8 - 256 = 162.75$  decimal. The closest value is 163 decimal or a3 hexadecimal. Setting SEDV1 to 0xa3 sets the EDV1 threshold at 3352 mV.

## 1.4 Initial Standby Load Current

The initial standby load current (ISLC) value programmed in EEPROM should be the estimated standby load current. The bq27000/200 takes any nonzero current value that is less than or equal to two times the programmed standby load current value and computes a weighted average with the previous standby load current. This allows the reported standby current to reflect the actual measured standby current, and the value is used to compute standby time-to-empty. The bq27000/200 also disables learning a new LMD if a learning discharge cycle terminates at EDV1 when the average discharge current is less than or equal to two times the programmed standby load current value. This prevents learning an inflated capacity value under a standby load condition. Units for ISLC are 7.14  $\mu\text{V}$  per LSB.

Program the EEPROM value for ISLC in address 0x79. The formula for determining the EEPROM value for ISLC is:

$$\text{ISLC} = \frac{\text{DesignStdbyCurrent(mA)} \times R_S(\text{m}\Omega)}{7.14 \mu\text{V}} \quad (4)$$

Example: To set the ISLC value to 20 mA with a 20-m $\Omega$  sense resistor, the value to be programmed in ISLC is:  $20 \text{ mA} \times 20 \text{ m}\Omega/7.14 \mu\text{V} = 56$  decimal or 3a hexadecimal. The bq27000/200 disqualifies a learning cycle if the measured discharge current is less than or equal to 40 mA when EDV1 is detected.

## 1.5 Digital Magnitude Filter and Self-Discharge Rate

The digital magnitude filter (DMF) threshold sets the minimum signal level across the sense resistor that is to be measured. If the signal level measured by the bq27000/200 is less than this threshold, the signal is ignored and assumed to be zero. If the signal level is higher than this threshold, the signal is accepted as a valid measurement. The DMF prevents a small measurement offset due to IC characteristics as well as any additional offset due to PCB layout from accumulating a large error over a long time. During times with no charge or discharge, any small signal due to offset that is less than the DMF threshold is ignored. If the DMF value is set to zero, then all signal levels will be treated as valid. A typical value for the DMF threshold is 15–20  $\mu\text{V}$ . The formula for determining the EEPROM value for DMF is:

$$\text{DMF}[3 : 0] = \frac{\text{DesignThreshold}}{4.9 \mu\text{V}} \quad (5)$$

The self-discharge (SD) rate estimate sets the rate at 25°C that is used to estimate the self-discharge capacity loss in 1 day when the battery is not being charged. This rate is automatically compensated for temperature by doubling the programmed rate for every 10°C increase or halving the programmed rate for every 10°C decrease. A typical value for Lithium ion batteries is 0.2% per day at 25°C. The formula for determining the EEPROM value for SD is:

$$\text{SD}[3 : 0] = \frac{1.61}{\text{DesignSD}} \quad (6)$$

The EEPROM values for the digital magnitude filter and self-discharge (DMFSD) rate are combined into a single byte and programmed in address 0x7a.

Example: To set the DMF threshold to 15  $\mu\text{V}$  and the self-discharge rate to 0.2% per day, the value to be programmed in the upper nibble of DMFSD is:  $15 \mu\text{V}/4.9 \mu\text{V} = 3.06$  and the value to be programmed in the lower nibble of DMFSD is:  $1.61/0.2 = 8.05$ . The closest values are 3 and 8; so, the hexadecimal value for DMFSD would be 0x38. Setting DMFSD = 0x38 sets the DMF threshold to 14.7  $\mu\text{V}$  and the self-discharge rate to 0.2% per day at 25°C.

## 1.6 Taper Current

The taper current (TAPER) threshold sets the threshold that charging current must fall below for the bq27000/200 to detect that the battery has received a full charge. Voltage must also meet the qualifying threshold that is set in pack configuration (PKCFG) to qualify as a valid taper current charge termination. Typical values for the taper threshold are in the range of LMD/20 to LMD/10. The value programmed in the bq27000/200 should be a little higher in value than the expected charge termination current of the charger. If the charger terminates before the bq27000/200 can detect the charge termination, the bq27000/200 does not adjust the displayed capacity to the full (NAC=LMD) condition. Units for TAPER are 228  $\mu\text{V}$  per LSB.

The EEPROM value for TAPER is programmed in bits 6-0 in address 0x7b. Bit 7 of address 0x7b is reserved for enabling the capacity fade estimate. The formula for determining the EEPROM value for TAPER is:

$$\text{TAPER} = \frac{\text{DesignTaperCurrent}(\text{mA}) \times R_S(\text{m}\Omega)}{228 \mu\text{V}} \quad (7)$$

Example: To set the taper charge termination threshold to 100 mA:  $\text{TAPER} = 100 \text{ mA} \times 20 \text{ m}\Omega/228 \mu\text{V} = 8.8$ . The EEPROM value for TAPER should be programmed to 0x09 or 0x89, depending on the option chosen for bit 7. This programs the taper current value to 102.6 mA.

Bit 7 of TAPER is used to enable or disable application of a capacity fade estimate. This is useful if the battery may spend considerable time without a capacity learning cycle. If bit 7 = 0, capacity aging is disabled. If bit 7 = 1, two separate aging estimates are made. The primary adjustment is made if substantial charge and discharge activity occurs without a learning cycle. Every time CYCL (cycle count since last learning cycle) increments by 2, LMD is reduced by  $\text{ILMD} \times 256/1024$  (0.1% of design capacity). A secondary adjustment is made if considerable time passes with no significant charge or discharge activity. LMD is reduced by  $\text{ILMD} \times 256/1024$  (0.1% of design capacity) every time that NAC is reduced by

1.56% due to self-discharge. For example, if the self-discharge estimate is programmed for 0.2%/day, LMD is reduced by 0.1% of design capacity every 8 days of idle operation at 25°C. The rate doubles or halves every 10°C temperature change, just like the self-discharge estimate. Whenever a learning cycle occurs, LMD is replaced with the new learned value, CYCL is cleared, and the aging computations start over using the new learned LMD value as a starting point.

## 1.7 Pack Configuration

The pack configuration (PKCFG) value is used to set five different user options.

**PKCFG[7]** — Bit 7 sets the initial state of the GPIO pin when power is applied to the bq27000. The host can write to the MODE register to change the GPIO configuration at any time if the GPIO configuration needs to be dynamically changed. If bit 7 = 0, then the GPIO is initialized as an open-drain output. If bit 7 = 1, then the GPIO is initialized as an input. If the GPIO pin is unused, the preferred setup is to program bit 7 = 0 to set the GPIO pin as an output. The GPSTAT bit in MODE register is set to a 1 on power on reset (POR) and turns the open-drain FET output off.

**PKCFG[6:5]** — Bit 6 (QV1) and bit 5 (QV0) are used to set the qualification voltage threshold for a current taper charge termination. VOLT must be greater than or equal to the threshold determined by the QV1 and QV0 setup. The qualification voltage can be programmed to 3968 mV, 4016 mV, 4064 mV, or 4112 mV (see Table 3 in the bq27000/200 data sheet). The qualification voltage chosen should be as high as possible to minimize the chance for any premature termination resulting from a reduction in charge current due to some system or charger issue that may occur before the battery is full. For example, if the system has an operating mode that robs the charger of most of its available power and the remaining charge current for the battery is less than the taper current termination threshold, the taper qualification voltage threshold can prevent a possible false charge termination detection. The qualification voltage threshold should not be set so high that the tolerance of the charger voltage and measurement accuracy of the bq27000 could prevent the reported voltage from exceeding the taper qualification voltage threshold.

Example: If the charger were set for 4200 mV nominal, with a  $\pm 2\%$  tolerance, the minimum charger voltage would be 4116 mV. The voltage measurement accuracy of the bq27000 is  $\pm 20$  mV; so, an applied 4116-mV source could be measured as low as 4096 mV. The taper qualification threshold should be set to 4064 mV, as the highest 4112-mV setting is too high with worst-case tolerances. This selection requires setting QV1 (bit 6) = 1 and QV0 (bit 5) = 0.

**PKCFG[4-2]** — These bits are used to store an average board offset value. The value of the board offset is largely determined by the PCB layout. This offset value is added to the internal compensated offset to achieve a more accurate measurement of the voltage across the sense resistor. The board offset value is a signed number with a resolution of 2.45  $\mu\text{V}$  per bit. The maximum positive offset value that can be stored is 7.35  $\mu\text{V}$  with PKCFG[4-2] = 011. The maximum negative offset value that can be stored is -9.8  $\mu\text{V}$  with PKCFG[4-2] = 100. The offset can be computed by measuring the total offset of the board plus gauge with no charge or discharge current flowing and subtracting the offset of just the gauge alone. Built-in offset commands in the bq27000/200 allow measurement of these values. The total board plus gauge offset may be measured by performing a compute external offset (CEO) command. The user must first ensure that no charge or discharge current is flowing. Then, set MODE[5] = 1, and write the command key of 0x56 to address 0x00 to perform the CEO command. The result may be read after about 5.5 seconds in 0x5f-5e. The value is a signed number with LSB resolution of 1.225  $\mu\text{V}$ . The gauge offset value may be similarly obtained by performing a compute internal offset (CIO) command. This command is performed by setting MODE[4] = 1 and then writing the command key of 0x56 to address 0x00. After about 5.5 seconds, the result may be read from 0x5f-5e and subtracted from the CEO reading to obtain the board offset value. If the board offset exceeds the compensation range, use the maximum positive or negative compensation value as appropriate for maximum accuracy. An excessive board offset indicates that a better board design could be achieved with some improvement in measurement accuracy, especially of small charge and discharge currents. The board offset value should be measured several times on each of several different boards to determine a good average value to use for the production lot. Measurement of board offset for each unit should not be required.

**PKCFG[1]** — This bit (DCFIX) can be used to select a fixed discharge rate compensation value and allow the DCOMP location in EEPROM to be used for a customer identification or serial number. If DCFIX = 0, DCOMP specifies the discharge compensation value to be used in computing CACD, MLTTE, and ARTTE. If DCFIX = 1, then a fixed default compensation value for DCOMP is used, and the DCOMP location in EEPROM is free for the user to program to any desired value. The fixed default compensation value is equal to 6.25% of the discharge current that exceeds C/4. Many applications find the fixed discharge compensation value to be satisfactory and set DCFIX = 1.

**PKCFG[0]** — This bit (TCFIX) can be used to select a fixed temperature compensation value and allow the TCOMP location in EEPROM to be used for a customer identification or serial number. If TCFIX = 0, TCOMP specifies the temperature compensation value to be used in computing CACT, MLTTE, and ARTTE. If TCFIX = 1, then the TCOMP location in EEPROM is free for the user to program to any desired value. The fixed default temperature compensation value is 0.68% of the initial LMD value (design capacity) per degree C below 12°C. This setting also disables learning of new capacity values if the temperature is less than or equal to 12°C. Many applications find the fixed temperature compensation value to be satisfactory and set TCFIX = 1.

The EEPROM bit values for the desired PKCFG options should be combined into a single hexadecimal value and then programmed in address 0x7c.

Example: To program PKCFG for unused GPIO pin, with a 4064-mV taper qualification voltage, board offset of -4.9 μV, and use TCOMP and DCOMP for customer identification information, the programming should be set to 01011011, or 0x5b.

## 1.8 Initial Maximum Load Current

The initial maximum load current (IMLC) register contains the end-equipment maximum expected load current. On reset, this value is transferred to the MLI register and used to calculate maximum load time-to-empty (MLTTE). The gauge learns a new maximum load if the current exceeds the initial maximum load. The units for IMLC are 457 μV per LSB. The equation for determining the EEPROM value is:

$$\text{IMLC} = \frac{\text{DesignMaxCurrent(mA)} \times R_S(\text{m}\Omega)}{457 \mu\text{V}} \quad (7)$$

Example: To set the IMLC value to 1200 mA with a 20-mΩ sense resistor, the value to be programmed in IMLC is: 1200 mA × 20 mΩ/457 μV = 52.5. The closest value is 53 decimal or 35 hexadecimal. This sets the initial MLI value to 1211 mA. If AI ever exceeds 1211 mA, the higher AI value replaces the 1211-mA initial value. To avoid having some extraordinary value getting stuck in MLI, the value in MLI is reduced to the average of the previous value and the IMLC value every time the gauge is charged to full, but only if a previous discharge to less than 50% has occurred.

The user can optionally use this byte in EEPROM to store a customer identification or serial number. If used this way, MLTTE should be ignored. No other functions of the gauge are affected.

## 1.9 Discharge Rate Compensation

The discharge rate compensation (DCOMP) value in EEPROM sets the factors used to calculate the reduction in NAC due to load current. The resulting CACD value is the available capacity, compensated for discharge rate. The EEPROM value can alternatively be used for a customer identification or serial number if DCFIX (bit 1 in PKCFG) is set to 1. When this option is used, a default compensation of 6.25% of the discharge current that exceeds C/4 is used for the discharge rate compensation factor, and the value in the DCOMP location is ignored. The default discharge rate compensation is equivalent to programming DCOMP with 0x42.

DCOMP is used to prevent an overstated run time when a heavy load is applied. When a learning cycle terminates, LMD is adjusted up or down to a value that corresponds to the load current applied at the time that EDV1 is detected. This LMD adjustment automatically compensates NAC to the discharge rate applied at the time EDV1 is detected during a learning cycle discharge. If EDV1 is detected on a non-learning discharge, there is no LMD adjustment, but NAC may have been adjusted at EDV1 due to a heavy load when EDV1 was detected. To properly compute CACD, the discharge compensation adjustment, DCMP, must comprehend the LMD and NAC adjustments that occur from time to time. The

DCMPADJ value in the equations is used to correct the compensation computation based on the previous LMD and NAC adjustments. A discharge at a lighter load than during previous discharges projects less capacity than is actually available at the lighter load, but if the load should suddenly increase to the prior level, the bq27000 should accurately reflect the available capacity at the heavier load. This prevents a surprise loss of capacity without warning from the bq27000/200.

The DCOMP values should be chosen to accurately represent the reduction in capacity versus load characteristics of the battery. Two factors can be set. One is the discharge offset (DCOFF) value. If the load current is below this value, no capacity reduction occurs. The second factor is the discharge compensation gain factor (DCGN) that determines the slope or rate at which the capacity is reduced as the load current exceeds the discharge offset value.

The DCOFF thresholds are set at 0, C/2, C/4, and C/8 for values of DCOFF of 0, 1, 2, and 3, respectively. DCOFF values are stored as DCOMP[1:0]. The DCGN value is determined by DCOMP[7:2]. The value for DCGN is determined by the desired gain/slope for the capacity reduction in % reduction per unit of current that exceeds the DCOFF threshold. The formula for DCGN is:

$$\text{DCGN}[5 : 0] = 2.56 \times \text{DesignDschgCompensationGain\%} \quad (8)$$

Once the DCOFF and DCGN values have been determined, they can be combined into a single word and programmed in address 0x7e.

CACD may be computed from NAC by the following equations:

$$\text{DCMP} = \text{DCGN} \times \frac{\text{AI} - \text{DCOFF}}{256}, \text{ for AI (Average Discharge Current) } > \text{DCOFF} \quad (9)$$

$$\text{DCMP} = 0, \text{ for AI } \leq \text{DCOFF} \quad (10)$$

$$\text{CACD} = \text{NAC} - (\text{DCMP} - \text{DCMPADJ}), \text{ if DCMP } > \text{DCMPADJ} \quad (11)$$

$$\text{CACD} = \text{NAC}, \text{ if DCMP } \leq \text{DCMPADJ} \quad (12)$$

After an EDV1 detection, the DCMPADJ value is equal to the saved value of DCMP at the last EDV1 detection. This computation continues until a battery-full detection occurs. This adjusts CACD for any NAC adjustment at EDV1. After a full-battery detection, the DCMPADJ value is changed to the saved value of DCMP at EDV1 from the last learning cycle discharge. This computation continues until EDV1 is again detected. This adjusts CACD for any LMD adjustment during the last learning cycle.

The preceding equations are also used to compute the discharge compensated available capacity when computing ARTTE or MLTTE. The DCMP equation uses At Rate (AR) or Maximum Load Current (MLI) as appropriate, in place of AI, to determine the rate-compensated capacity available at the AR or MLI load current value.

Programming example: A battery for use in a system with load currents up to 1C rate has a flat discharge capacity curve for load currents up to about C/4. At a 1C rate, the available battery capacity is down about 5% from the C/4 rate. The DCOFF value of C/4 can be selected with a DCOFF value of 2. At 1C, the current exceeds the DCOFF value by 0.75C; so, the desired capacity reduction slope is 5%/0.75C or 6.67%/1C. This yields a DCGN value of:  $2.56 \times 6.67 = 17.07$ . The closest value is 17 decimal, or 11 hexadecimal. Setting DCGN to 17 yields a capacity reduction slope of 6.64%. Combining the binary values of 010001 for DCGN and 10 for DCOFF yields a DCOMP value of 01000110, or 0x46. This may be easier to compute by noting that shifting the DCGN into the third bit position in DCOMP is the same as multiplying the raw DCGN value by 4. This results in combining  $4 \times \text{DCGN}$  and DCOFF as follows:  $4 \times 17 + 2 = 70$  decimal or 46 hexadecimal.

CACD calculation example: ILMD is programmed for a design capacity of 978 mAh. The battery has not been previously discharged to EDV1, so DCMPADJ = 0. The bq27000 measures a load current of 600 mA. The discharge rate compensation reduction is:  $\text{DCMP} = 17 \times (600 - 978/4) / 256 = 17 \times 355 / 256 = 23.6$ . CACD computes to 23.6 mAh less than NAC. CACD is not allowed to increase while discharging; so, if the load current drops, CACD may remain at the previous CACD value. As discharging continues, NAC continues to drop, but CACD holds steady until NAC drops enough that the new computed CACD value is again less than the previous value. Then, CACD again starts decreasing as the discharge continues with the lighter load.

DCGN and DCOFF determination: The optimal discharge rate compensation coefficients can be determined from the typical discharge curves on the battery. Discharge curves at various discharge rates are generally available from the cell manufacturer. The capacity of the cells at the various discharge rates can be determined from the discharge curves. If the discharge curves show time instead of capacity, the capacity can be computed by multiplying the discharge rate by the discharge time to reach the chosen EDV0 voltage threshold. The curves are generally plotted at various C-rates. The 1C rate is normally the current in mA that equals the cell capacity in mAh at a C/5 discharge rate. These capacity values in mAh can be plotted versus current as shown in Figure 1.

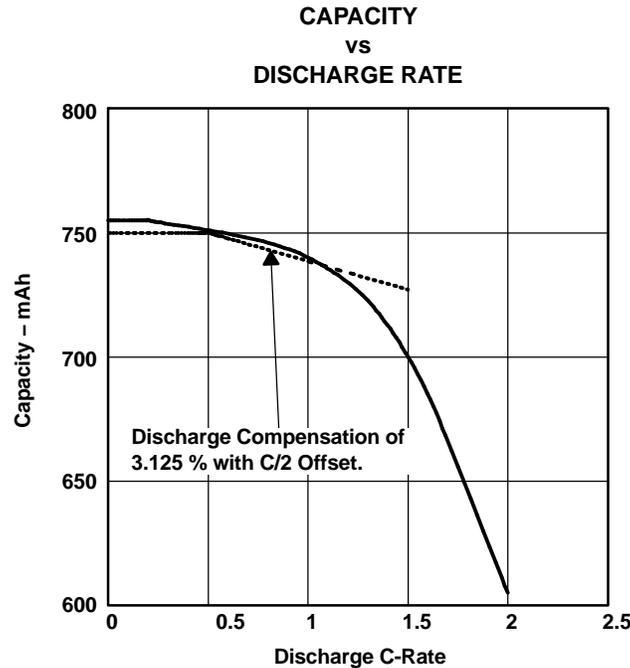


Figure 1. Capacity vs Discharge Rate

The cell capacitance at the minimum load current where learning is allowed (excluding standby load current) should be the value used to compute ILMD. Choose the DCOFF value (C/8, C/4, or C/2) and a DCGN (slope) that best matches the capacity versus load curve from the minimum load current value to the maximum (steady-state) load value expected. Figure 1 shows discharge compensation with DCOFF of C/2 and a slope of 3.125% reduction that would be appropriate for operation up to a discharge rate of 1.25 C. The ILMD value is programmed to 750 mAh in this example.

### 1.10 TEMPERATURE COMPENSATION

The temperature compensation (TCOMP) value in EEPROM sets the factors used to calculate the reduction in CACD due to temperature. The resulting CACT value is the available capacity, compensated for both discharge rate and temperature. The EEPROM value can alternatively be used for a customer identification or serial number if TCFIX (bit 0 in PKCFG) is set to 1. When this option is used, a default compensation of 0.6836% of design capacity per degree C below 12°C is used for the temperature compensation factor and the value in the TCOMP location is ignored. The 12°C threshold is also used to disqualify any learning cycles where the temperature is less than or equal to 12°C. The default temperature compensation is equivalent to programming TCOMP with 0x7c.

The battery impedance increases rapidly at cold temperature. This causes additional capacity loss at a given load current, because the battery drops to the minimum system operating voltage quicker than at warmer temperatures. If the temperature warms back up, the impedance decreases again and the available capacity increases. The temperature compensation is used to prevent overstating the available run time at cold temperatures. The increased impedance at cold temperature causes the EDV1 condition to be reached much sooner than at warmer temperatures and if TCOMP is properly set, CACT shows the actual available capacity at cold temperatures. NAC may be adjusted down when EDV1 is detected and

reflects the temperature compensated available capacity without any reduction due to TCOMP until the battery is again charged to full. To correctly compute CACT, the TCMP temperature compensation reduction value is saved if NAC is reduced when EDV1 is detected. The TCMP temperature compensation reduction is reduced by this value until the battery full condition is again detected. If the battery warms up after EDV1 is detected, it is possible for CACT to be larger than NAC.

Temperature compensation factors should be chosen that represent the battery capacity variation with temperature at the nominal expected load. Two factors can be set. The temperature compensation offset threshold TOFF sets the temperature threshold for disqualification of a learning cycle and also the temperature threshold above which there is no temperature compensation. The applied temperature compensation is proportional to the temperature drop below this threshold. The second factor is the temperature compensation gain threshold (TCGN). This factor sets the percentage of design capacity (DC), or initial LMD value that is used to reduce the available capacity for each degree that temperature is below TOFF. (Design capacity = Initial LMD value = ILMD × 256)

The TOFF threshold is the low nibble of TCOMP and reads directly in degrees C (or degrees K – 273). The upper nibble of TCOMP is the TCGN factor. The formula for TCGN is:

$$\text{TCGN}[3 : 0] = 10.24 \times \frac{\text{DesignTempCompensationGain}(\% \text{ofDC}/^{\circ}\text{C})}{^{\circ}\text{C}} \quad (13)$$

Once the TOFF and TCGN values have been determined, they can be combined into a single word and programmed in address 0x7f.

CACT may be computed from CACD by the following equations:

$$\text{TCMP} = \text{TCGN} \times \text{ILMD} \times \frac{273 + \text{TOFF} - T}{4}, \text{ for } T < 273 + \text{TOFF} \quad (14)$$

$$\text{TCMP} = 0, \text{ for } T \geq 273 + \text{TOFF} \quad (15)$$

$$\text{CACT} = \text{CACD} - (\text{TCMP} - \text{TCMPADJ}) \quad (16)$$

After NAC is reduced following an EDV1 detection, TCMPADJ equals the TCMP value when EDV1 was detected. This computation continues until a full-battery detection is made. This compensates for any NAC adjustment made at EDV1 due to cold temperature. After a full-battery detection, TCMPADJ is set to zero. This computation continues until a NAC reduction at EDV1 is again made.

The preceding equations are also used to compute the temperature compensated available capacity when computing ARTTE or MLTTE. The CACD value in the preceding equations is computed with a DCMP value that uses the appropriate AR or MLI value in place of AI for the computation.

Programming example: Desired temperature compensation is a 1% reduction in capacity for each degree below 10°C, with no reduction at warmer temperatures than 10°C. Learning new LMD values are disabled for temperatures at or below 10°C. TOFF is 10 decimal or a hexadecimal and is the lower nibble of TCOMP. TCGN = 10.24 × 1% DC per degree C = 10.24. The closest value is 10 decimal, or a hexadecimal. Setting TCGN = 10 yields a compensation value of 0.976% reduction in capacity per degree C below 10°C. Combining TCGN and TOFF yields a value of 0xaa to program in TCOMP.

CACT calculation example: ILMD is programmed for a design capacity of 996 mAh. ILMD is the high byte of the design capacity and has a value of 996 mAh/256. The temperature is 5°C, or 278°K, and the battery has just been charged to full (TCMPADJ = 0). TCMP = 10 × (996 mAh/256) × (273 + 10 – 278) / 4 = 48.6 mAh. This is a reduction of 9.73 mAh per °C or about 0.976% of the 996 mAh design capacity for each degree below 10°C.

TCGN and TOFF determination: The TCGN and TOFF values may be determined by first plotting the battery capacity versus temperature at the nominal load condition. TCGN and TOFF values may be chosen that give a best fit to this curve over the expected cold temperature operating range. This operation is much the same as determining DCGN and DCOFF from [Figure 1](#).

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265