

TLK313x CPRI Multi-hop Performance with the CDCM7005 Clock Jitter Cleaner

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ABSTRACT

Laboratory measurements were performed to determine the impact of reference clock phase noise on the performance of the TLK313x serializer/deserializer (SerDes) devices in a CPRI multi-hop configuration. The SerDes jitter-cleaner PLL was turned off, and the recovered clock, RXCLK_0, was externally jitter-cleaned with the CDCM7005 clock jitter cleaner before it was used to clock the serial transmitter.

The following key measurements were taken for 614.4Mbps, 1.2288Gbps, and 2.4576Gbps serial data rates, with the SerDes setup in the TBID mode (parallel interface clock rate = serial bit-rate/20):

1. Serial transmitter eye-pattern at every hop to determine compliance with the CPRI transmitter eye-mask.
2. Data continuity status as a function of the number of hops tested with the CRPAT long pattern.
3. Accumulated clock phase noise as a function of the number of hops.
4. SerDes PLL lock status at every hop.

It was observed that:

- the TLK313x/CDC7005 combination operated error-free in the 7-hop CPRI configuration at all the tested serial data rates with a large operating margin on the transmitter eye-mask. The worst-case total jitter recorded for the SerDes transmitter data after 7 hops was just 0.114UI at the 2.4576Gbps serial data rate, which provides better than 59% margin against the 0.279UI CPRI specification.
- at all the hops, the SerDes PLL remained locked after 24 hours of continuous error-free running.
- the TLK313x/CDCM7005 SerDes/clock combination proved to be capable of supporting more than the required 5 CPRI hops.

The results are applicable to any other non-CPRI multi-hop configurations similar to the one covered in this document.

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1 The Objectives

CPRI multi-hop configurations can suffer from performance degradation due to accumulated clock phase noise. The objective of this study is to understand the extent of the performance degradation when the TLK313x family of Texas Instruments SerDes devices is used with the Texas Instruments CDCM7005 clock jitter cleaner.

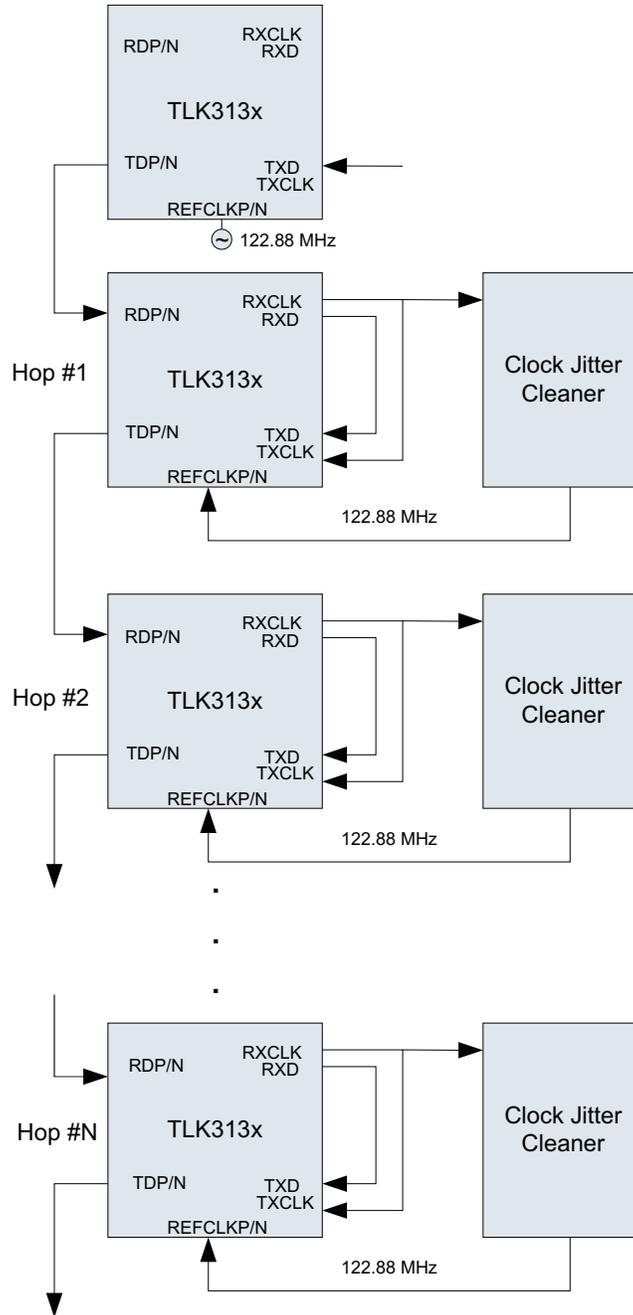


Figure 1. A typical CPRI Multi-hop SerDes/Clock Configuration

A typical CPRI multi-hop configuration using SerDes devices such as Texas Instruments TLK3131, TLK3132, and TLK3134, and clock jitter cleaners such as Texas Instruments CDCM7005, is shown in Figure 1. At every hop the recovered clock, RXCLK, is jitter-cleaned by the clock-jitter cleaner before it's used to clock the outgoing serial data TDP/TDN. This configuration reduces clock phase noise accumulation from hop to hop and hence reduces the transmitted serial data jitter at every hop.

2 Measurement Setup

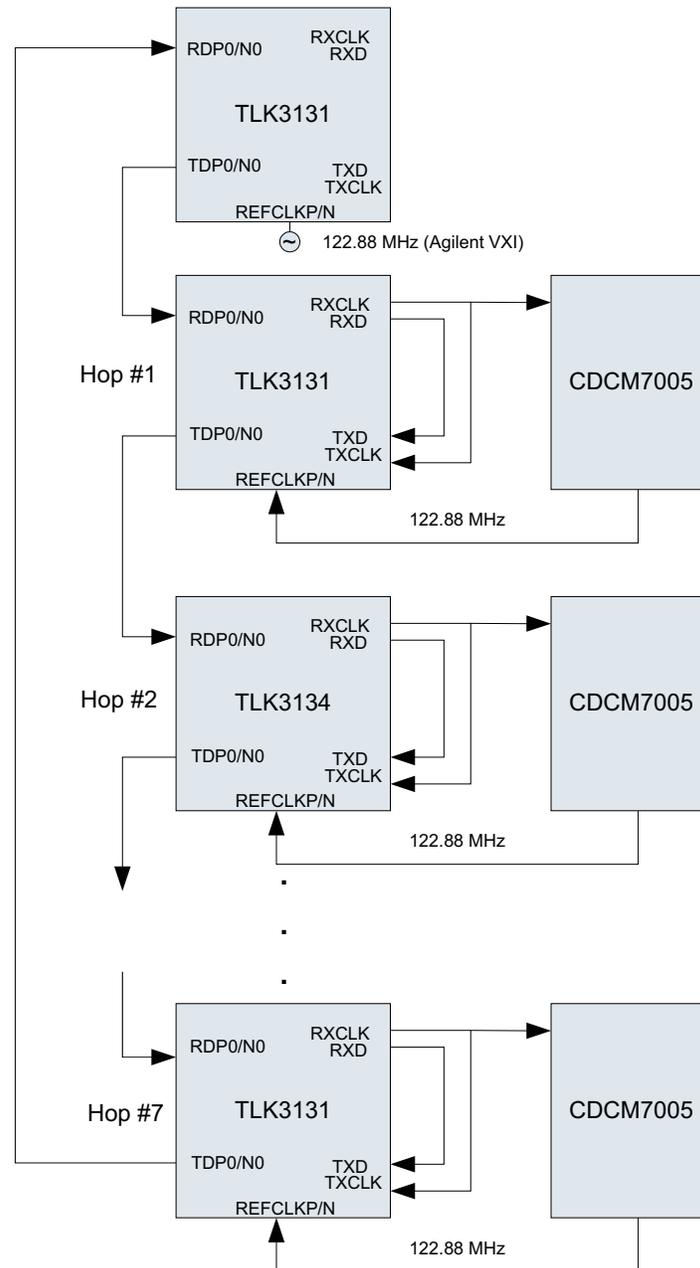


Figure 2. Measurement Setup for the Evaluation of CPRI SerDes/Clock Multi-hop Performance

The measurement setup used for the evaluation of the CPRI SerDes/clock multi-hop performance is as shown in Figure 2.

The first TLK3131 SerDes device was clocked with an external 122.88MHz clock from Agilent VXI. This device was setup to generate and verify a long continuous random test pattern (CRPAT) composed of 15360 bits. To form the first hop, the TDP0/TDN0 output of the first TLK3131 device was connected to the RDP0/RDN0 input of the second TLK3131 SerDes device which was itself set in the SLOOP mode. Again, the TDP0/TDN0 output of the second TLK3131 device was connected to the RDP0/RDN0 input of a TLK3134 device also set in the SLOOP mode to form the second hop. The process was repeated with four more TLK3134 devices and one TLK3131 device to form a total of seven hops. The TDP0/TDN0 output of the TLK3131 device on the seventh hop was connected back to the RDP0/RDN0 input of the first TLK3131 device for bit-error checking.

The MDIO script provided in Appendix 1 provides an example of how the lead (generator/verifier) TLK3131 device was configured and tested for the 2.4576Gbps serial data rate. The MDIO script provided in Appendix 2 provides more details on how the partner (downstream) TLK313x devices were configured and tested for the 2.4576Gbps serial data rate. The configuration and testing were similar for the other serial data rates.

The recovered clock, RXCLK_0, outputs of all the SerDes devices, other than the first TLK3131 device, were fed into the respective TXCLK inputs as well as into seven, separate CDCM7005 devices for jitter cleaning and clock multiplication. The jitter-cleaned 122.88MHz clock was tied to the REFCLKP/N input of each respective SerDes device. An external Epson Toyocom 491.52MHz voltage-controlled crystal oscillator (VCXO) was used with every CDCM7005 device to provide a 122.88MHz clock to every SerDes device on power-up. The clock frequency tolerance from this VCXO was ± 125 ppm.

Using Agilent E5052 Phase Noise Analyzer, the phase noise of the RXCLK_0 and jitter-cleaned REFCLKP/REFCLKN clocks were measured at every hop. The random jitter in ps-RMS was computed by integrating the phase noise over 10Hz to 20MHz frequency offset range. The random and total jitter of the TDP0/TDN0 output at every hop was measured using the jitter mode of the Agilent DCAj oscilloscope

3 Measurement Results

The performance results for the 614.4Mbps serial rate are shown in Figure 3 to Figure 9 and are summarized in Table 1.

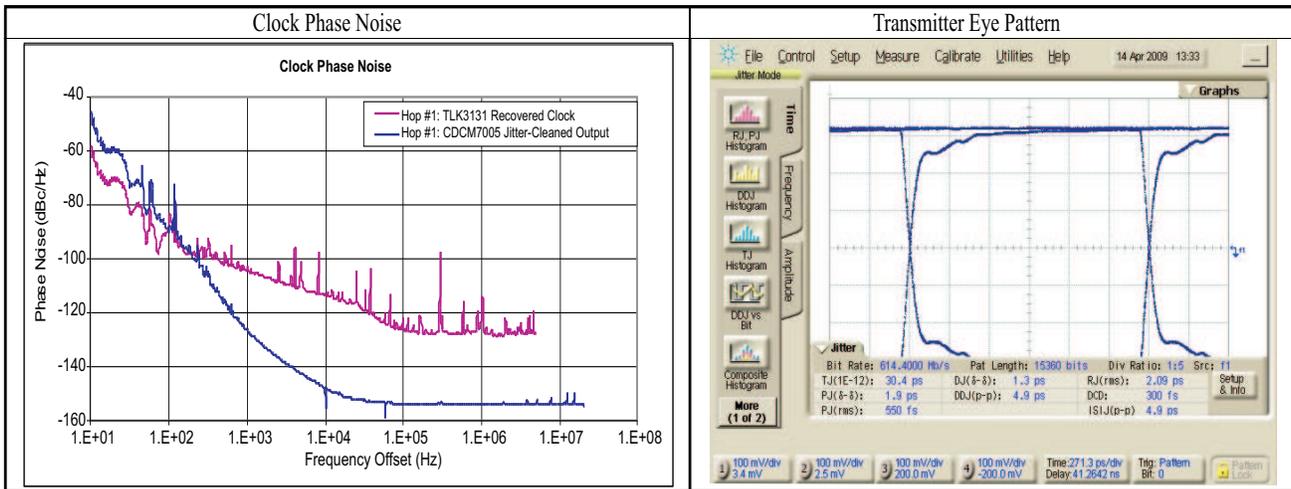


Figure 3. 614.4Mbps Serial Rate – Hop #1 Performance

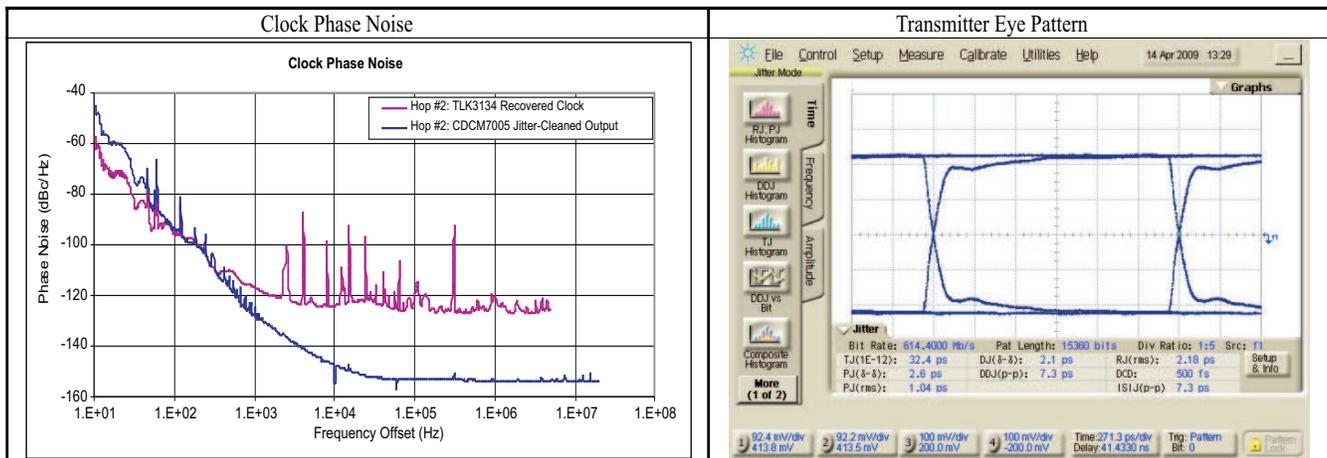


Figure 4. 614.4Mbps Serial Rate – Hop #2 Performance

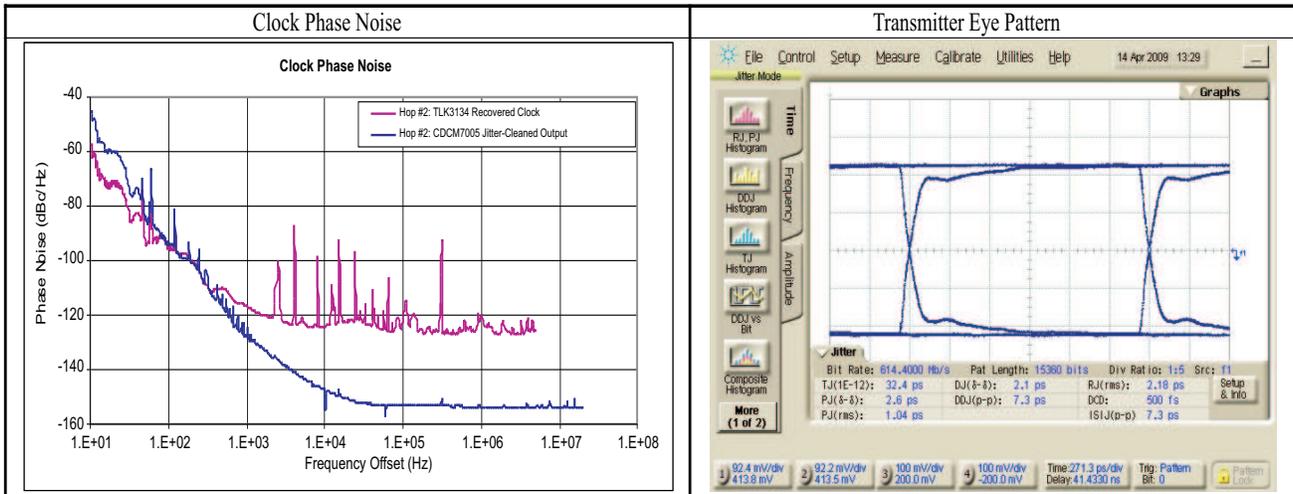


Figure 5. 614.4Mbps Serial Rate – Hop #3 Performance

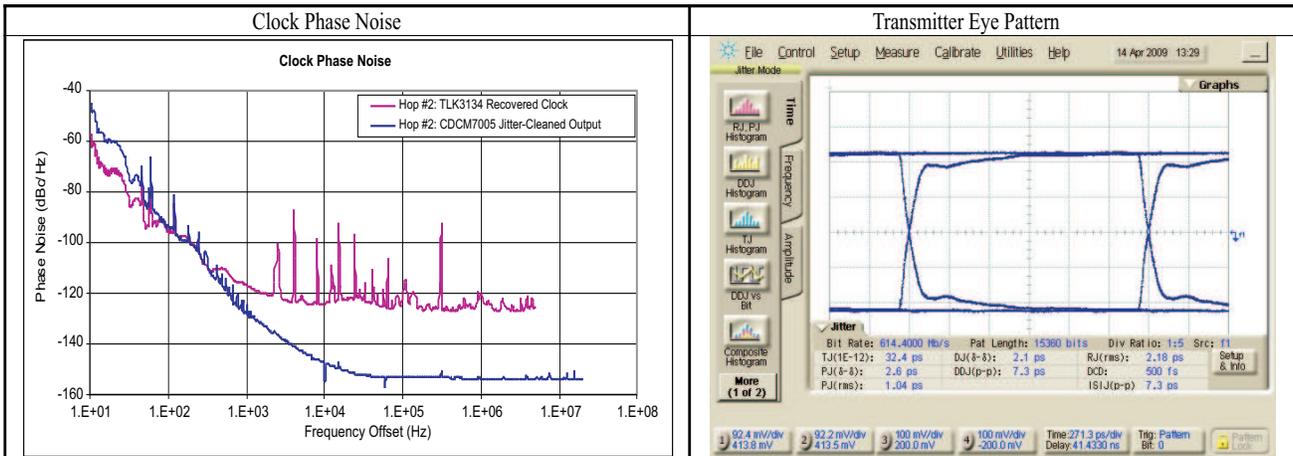


Figure 6. 614.4Mbps Serial Rate – Hop #4 Performance

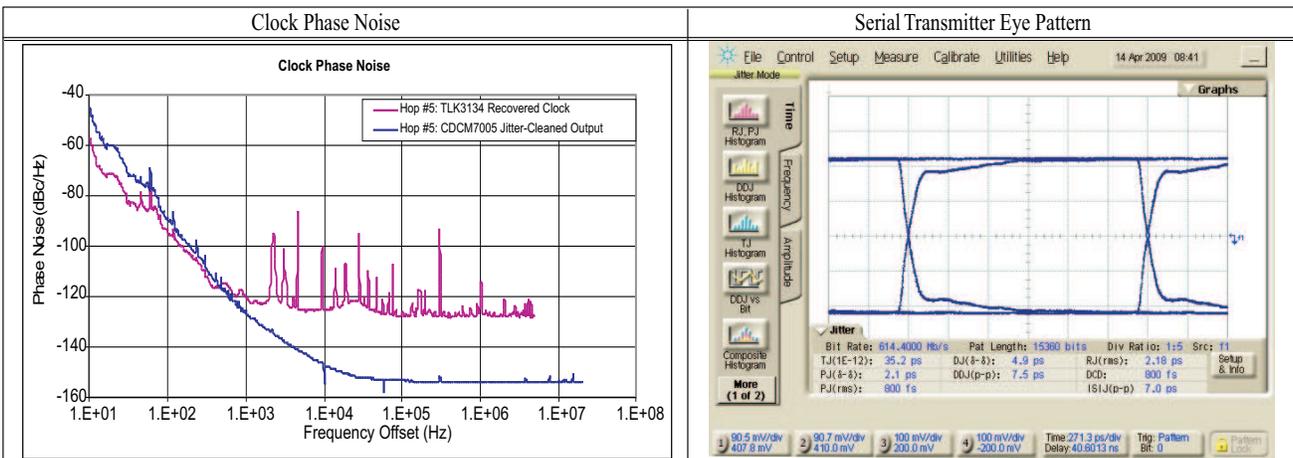


Figure 7. 614.4Mbps Serial Rate – Hop #5 Performance

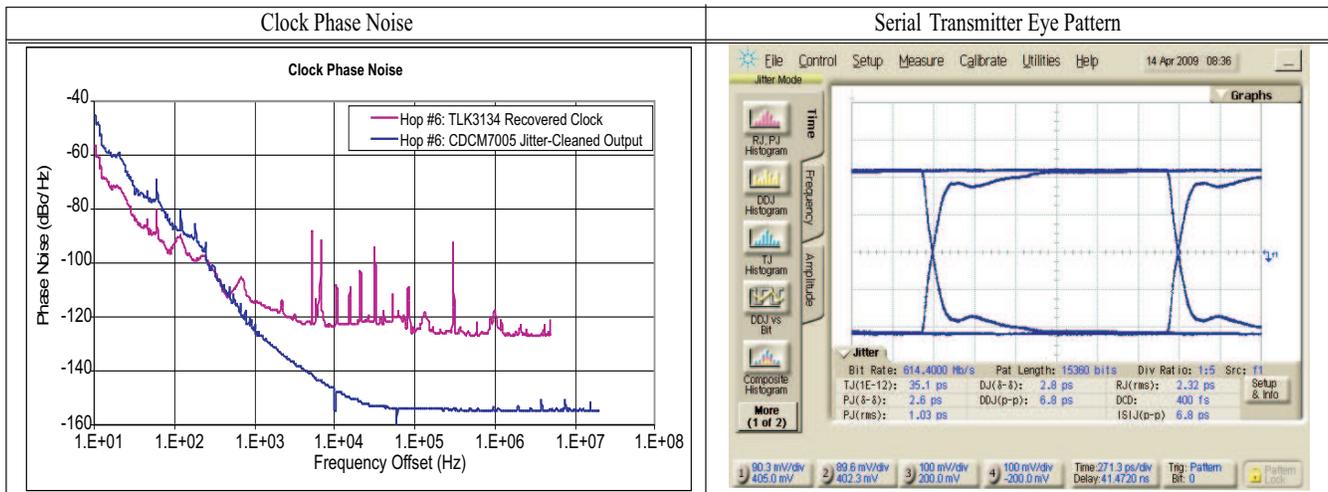


Figure 8. 614.4Mbps Serial Rate – Hop #6 Performance

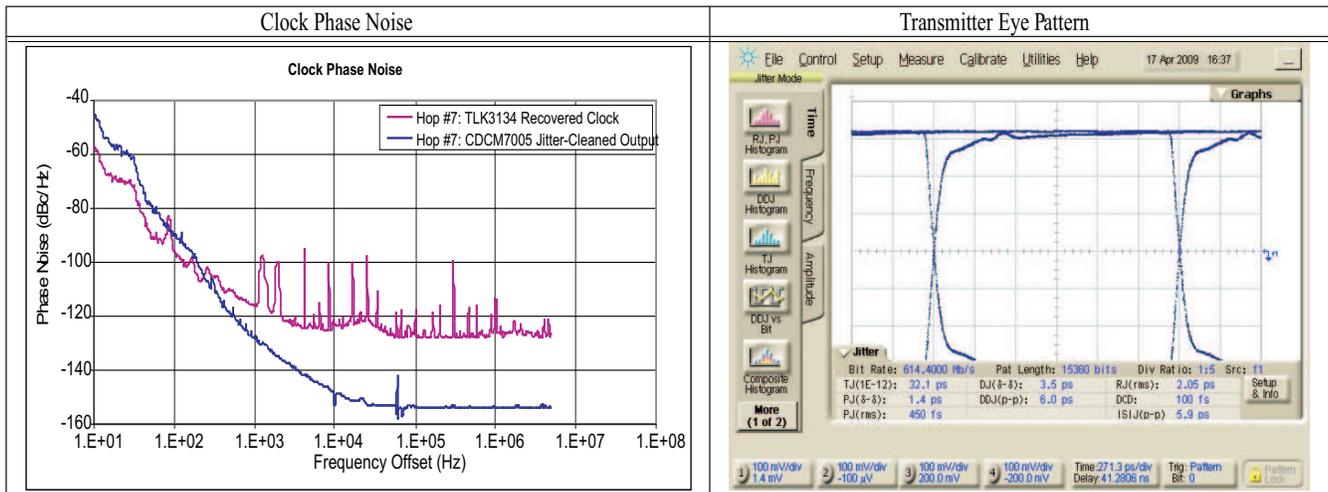


Figure 9. 614.4Mbps Serial Rate – Hop #7 Performance

Table 1. 614.4Mbps Serial Rate Performance Summary

| Hop # | 30.72MHz Recovered Clock Jitter (ps RMS) (10Hz to 20MHz Offset) | 122.88MHz CDCM7005 Output Clock Jitter (ps RMS) (10Hz to 20MHz Offset) | SerDes Serial Transmit Data Random Jitter (ps RMS) | SerDes Serial Transmit Data Total Jitter (ps pp [UI]) |
|-------|-----------------------------------------------------------------|------------------------------------------------------------------------|----------------------------------------------------|-------------------------------------------------------|
| 1 | 17.7 | 12.2 | 2.09 | 30.4 [0.019] |
| 2 | 20.5 | 12.0 | 2.18 | 32.4 [0.020] |
| 3 | 19.6 | 11.6 | 2.28 | 35.6 [0.022] |
| 4 | 18.9 | 12.2 | 2.33 | 35.9 [0.022] |
| 5 | 19.4 | 12.3 | 2.18 | 35.2 [0.022] |
| 6 | 20.4 | 12.0 | 2.32 | 35.1 [0.022] |
| 7 | 20.1 | 15.6 | 2.05 | 32.1 [0.020] |

The performance results for the 1.2288Gbps serial rate are shown in Figure 10 to Figure 16 and are summarized in Table 2.

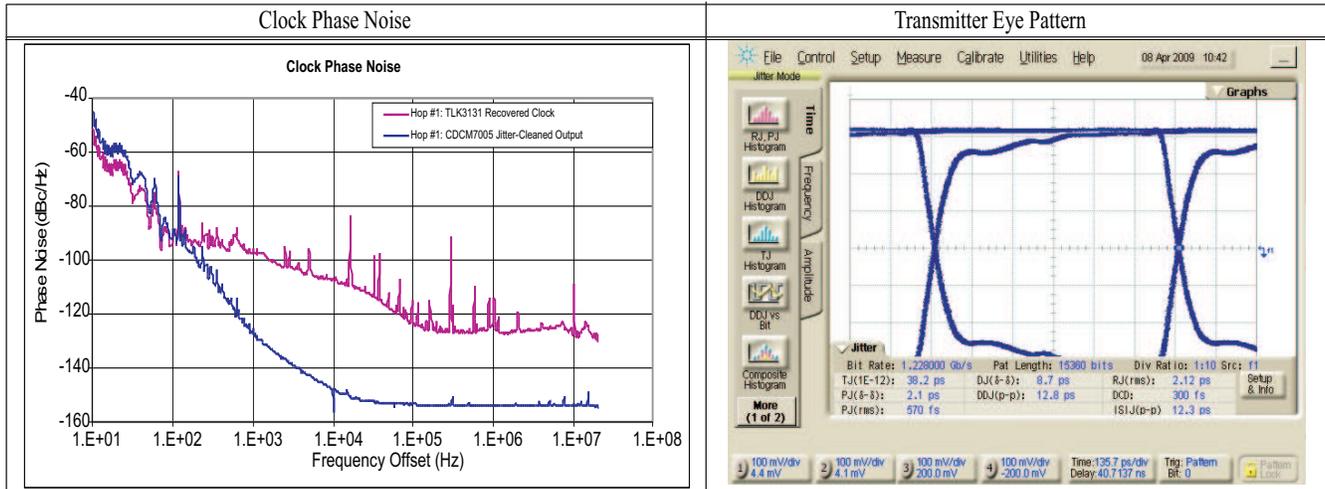


Figure 10. 1.2288Gbps Serial Rate – Hop #1 Performance

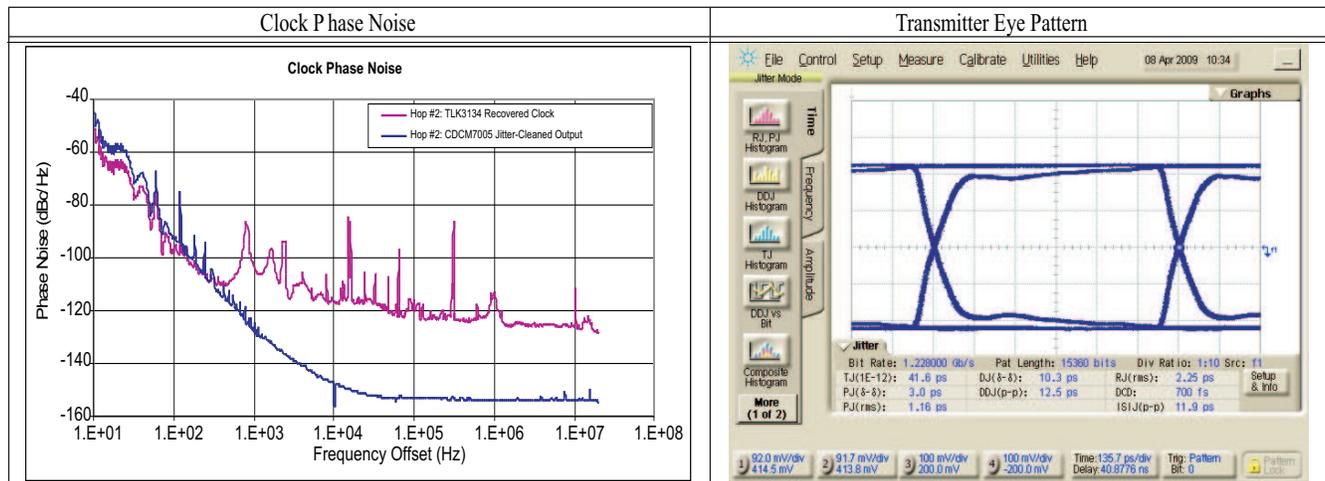


Figure 11. 1.2288Gbps Serial Rate – Hop #2 Performance

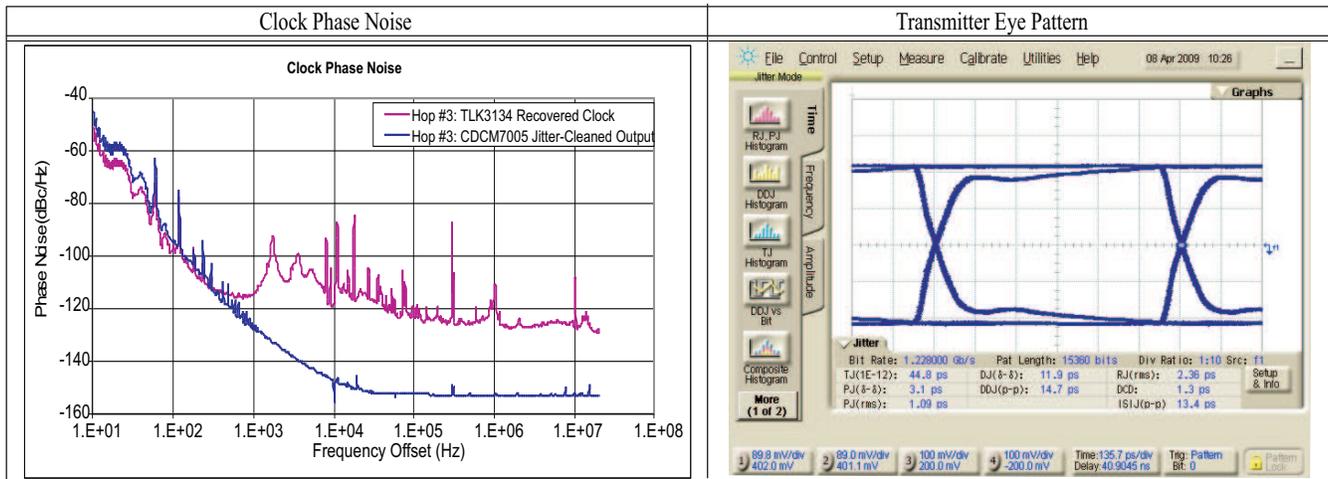


Figure 12. 1.2288Gbps Serial Rate – Hop #3 Performance

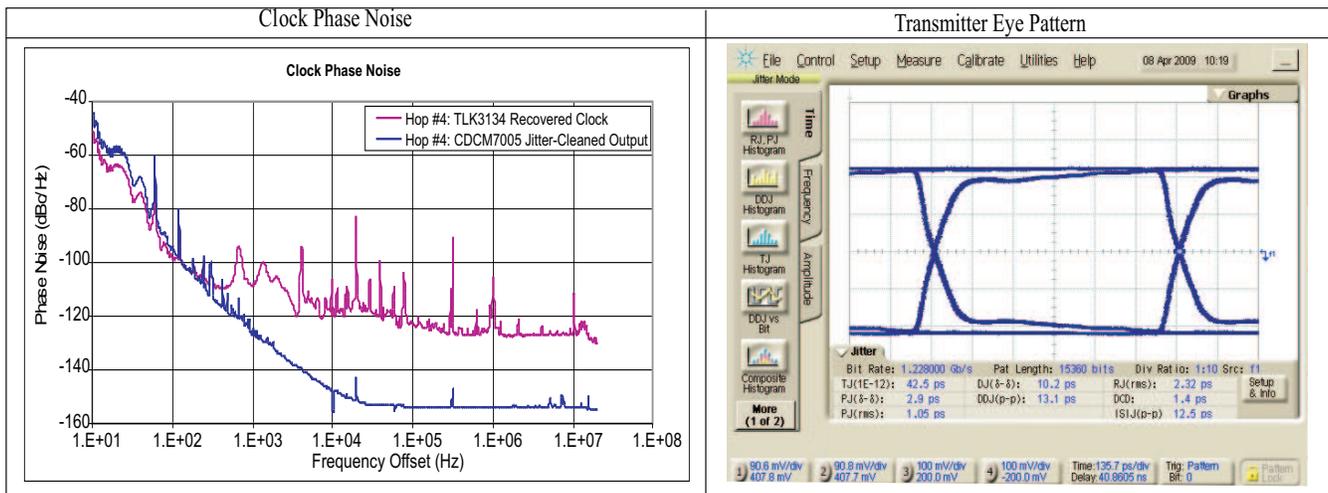


Figure 13. 1.2288Gbps Serial Rate – Hop #4 Performance

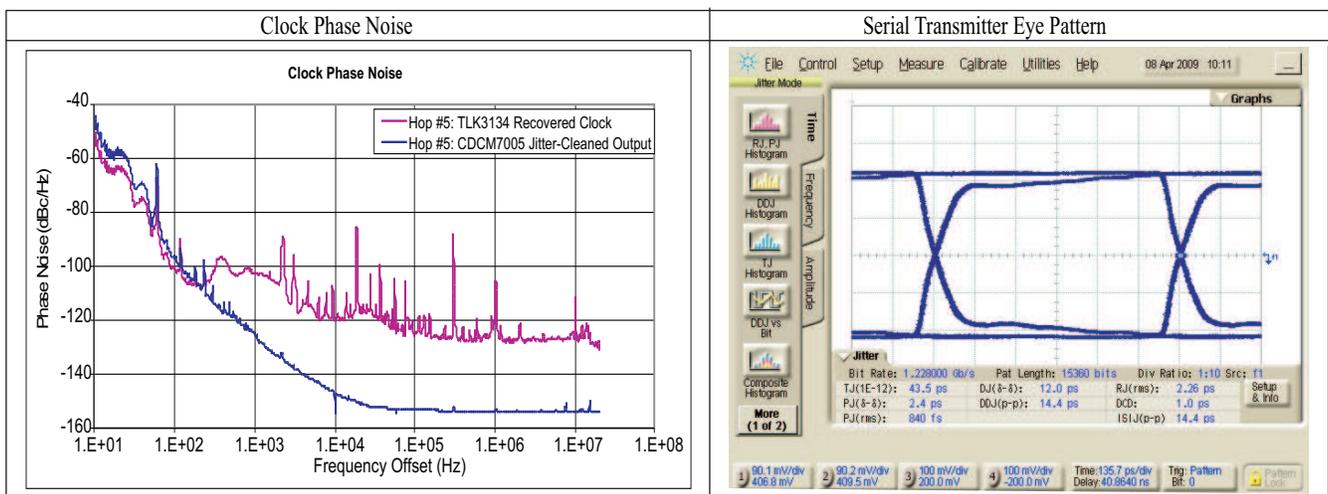


Figure 14. 1.2288Gbps Serial Rate – Hop #5 Performance

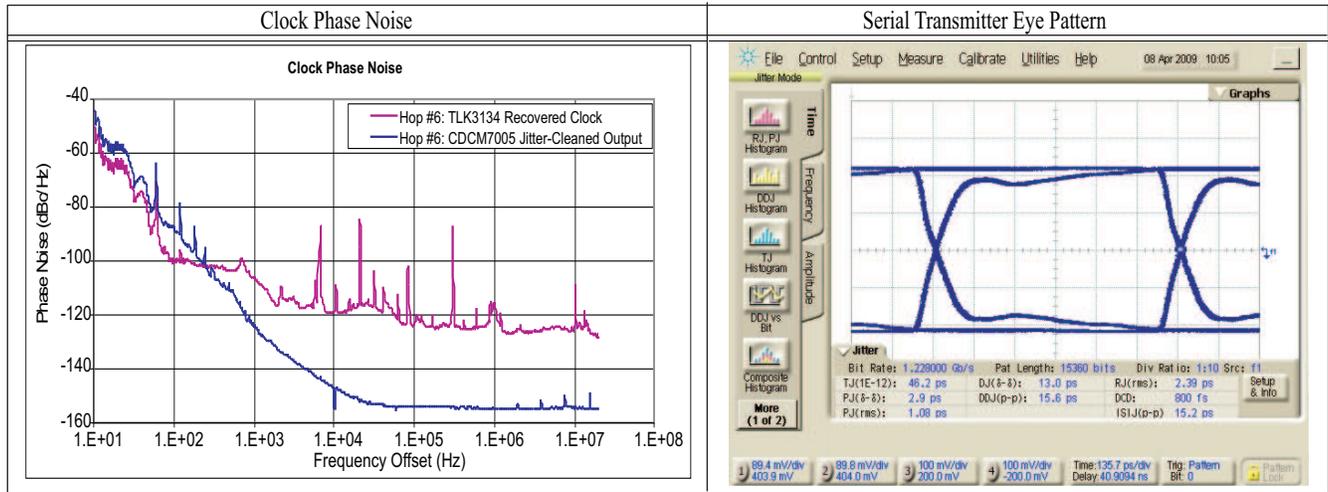


Figure 15. 1.2288Gbps Serial Rate – Hop #6 Performance

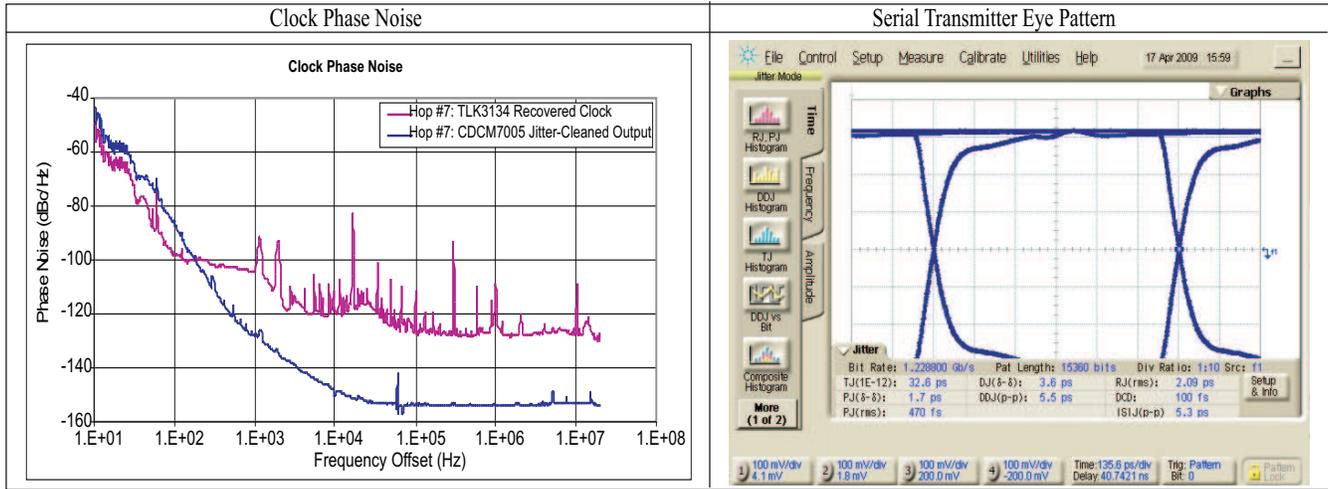


Figure 16. 1.2288Gbps Serial Rate – Hop #7 Performance

Table 2. 1.2288Gbps Serial Rate Performance Summary

| Hop # | 61.44MHz Recovered Clock Jitter (ps RMS) (10Hz to 20MHz Offset) | 122.88MHz CDCM7005 Output Clock Jitter (ps RMS) (10Hz to 20MHz Offset) | SerDes Serial Transmit Data Random Jitter (ps RMS) | SerDes Serial Transmit Data Total Jitter (ps pp [UI]) |
|-------|-----------------------------------------------------------------|------------------------------------------------------------------------|----------------------------------------------------|-------------------------------------------------------|
| 1 | 19.0 | 12.6 | 2.12 | 38.2 [0.047] |
| 2 | 21.3 | 12.9 | 2.25 | 41.6 [0.051] |
| 3 | 21.2 | 13.2 | 2.36 | 44.8 [0.055] |
| 4 | 20.4 | 13.8 | 2.32 | 42.5 [0.052] |
| 5 | 20.5 | 14.0 | 2.26 | 43.5 [0.053] |
| 6 | 22.0 | 14.4 | 2.39 | 46.2 [0.057] |
| 7 | 20.6 | 16.1 | 2.09 | 32.6 [0.040] |

The performance results for the 2.4576Gbps serial rate are shown in Figure 17 to Figure 23 and are summarized in Table 3.

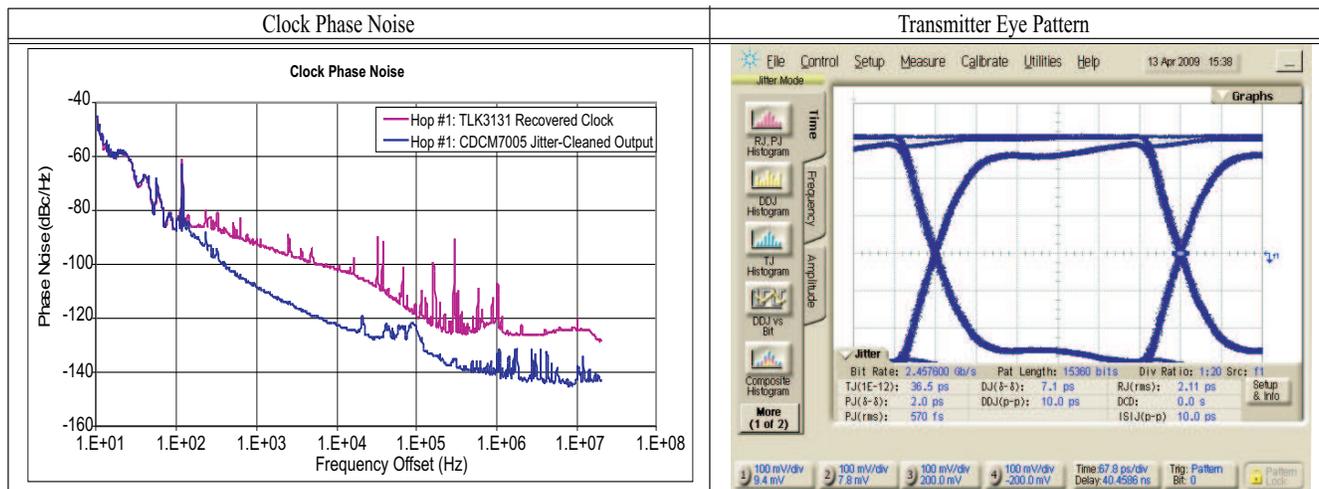


Figure 17. 2.4576Gbps Serial Rate – Hop #1 Performance

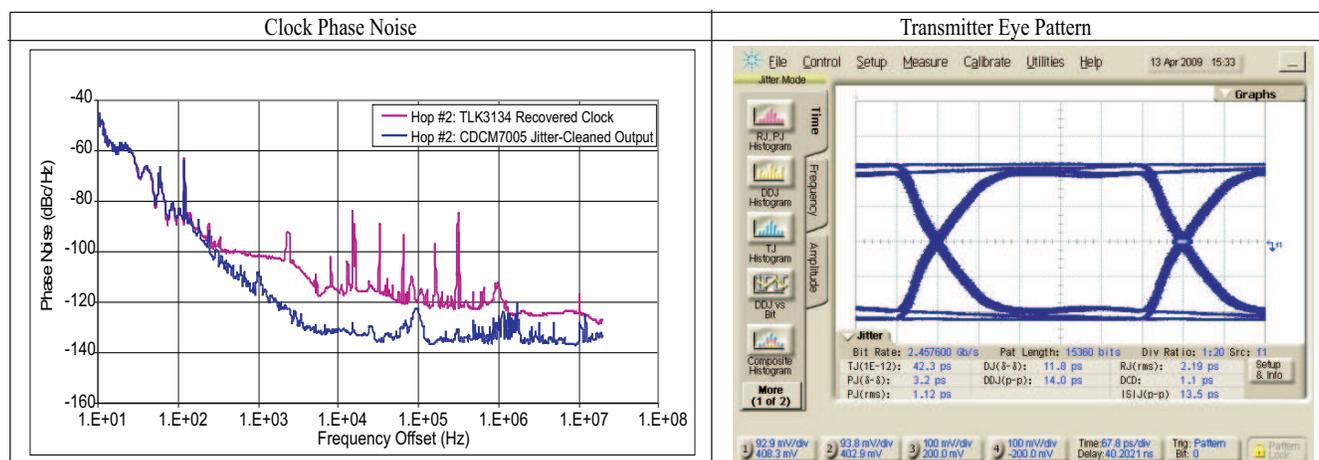


Figure 18. 2.4576Gbps Serial Rate – Hop #2 Performance

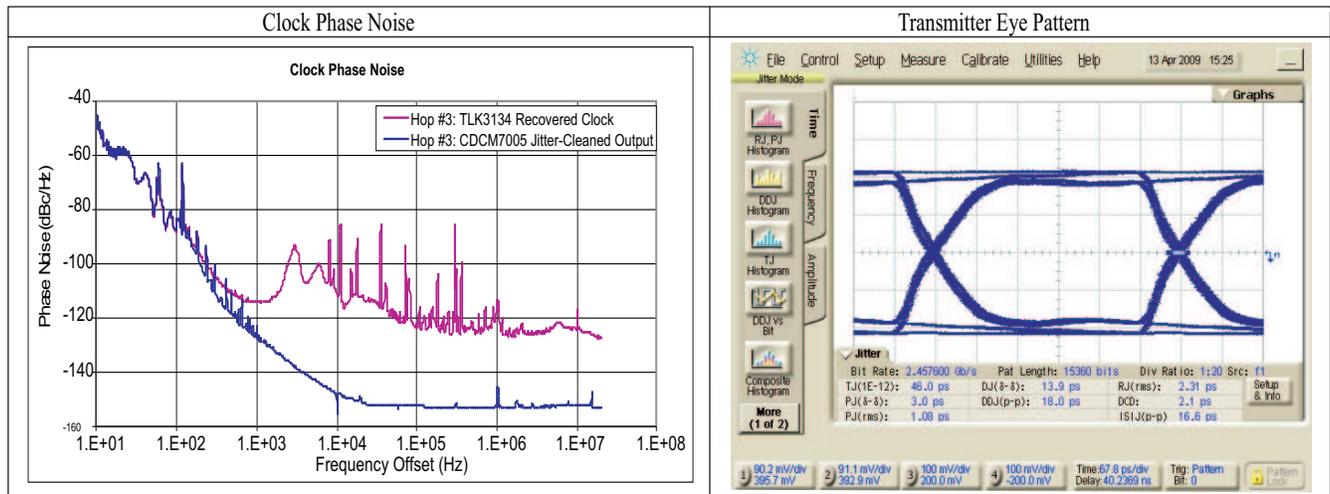


Figure 19. 2.4576Gbps Serial Rate – Hop #3 Performance

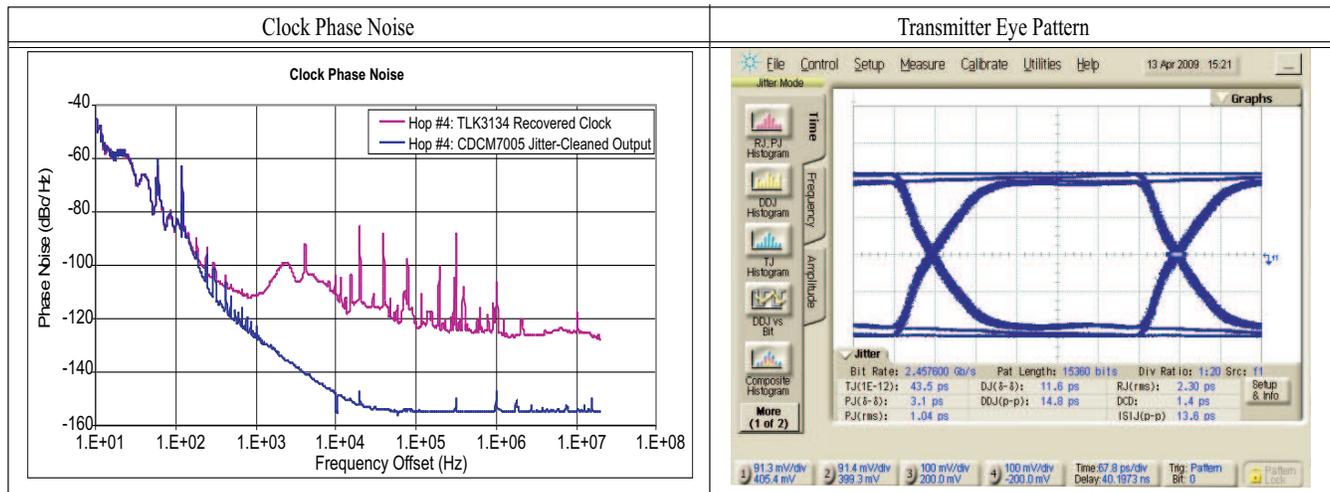


Figure 20. 2.4576Gbps Serial Rate – Hop #4 Performance

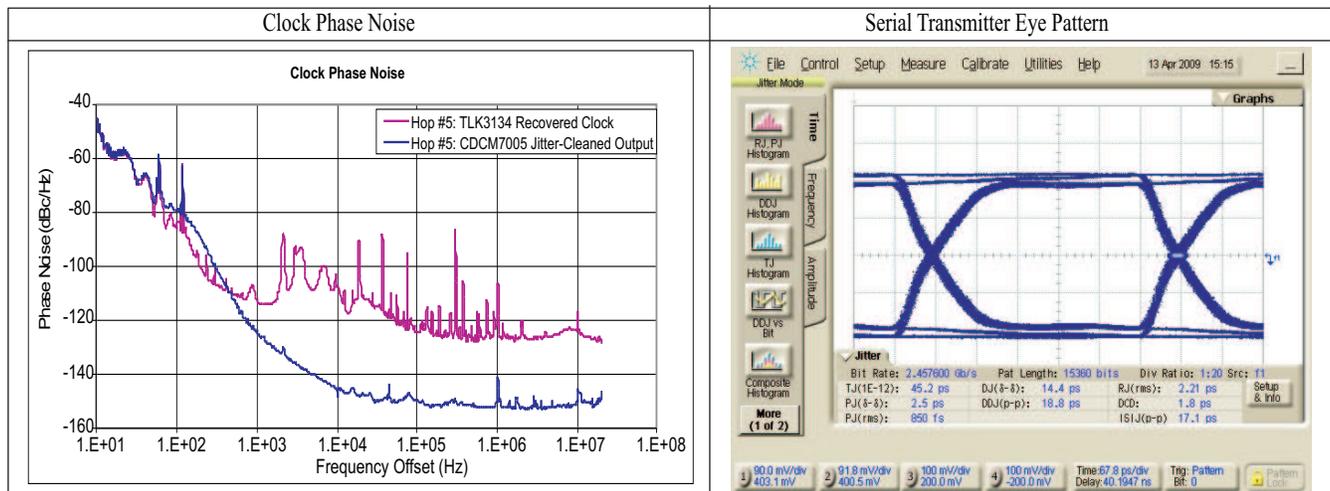


Figure 21. 2.4576Gbps Serial Rate – Hop #5 Performance

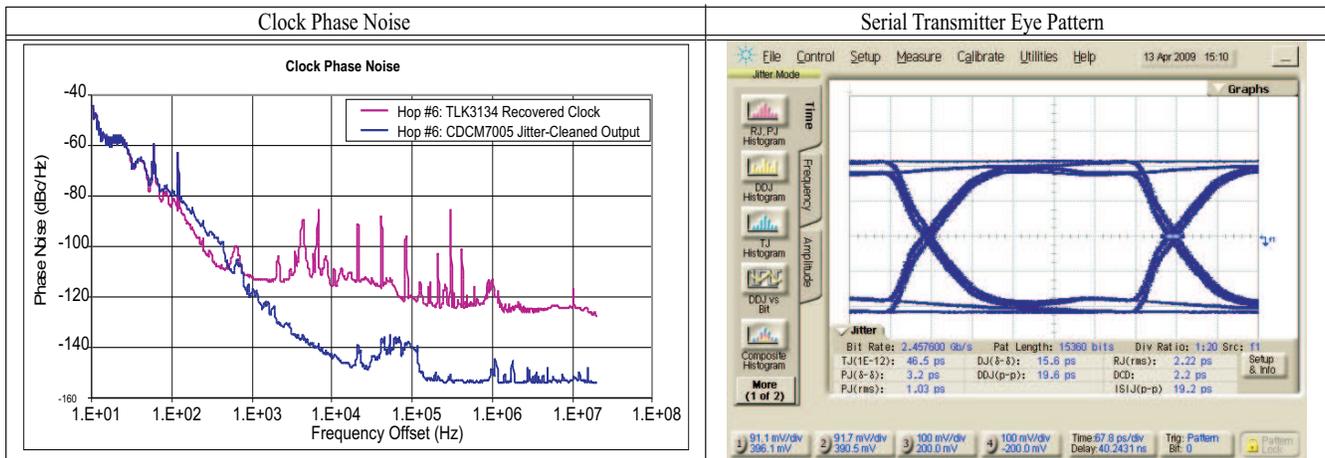


Figure 22. 2.4576Gbps Serial Rate – Hop #6 Performance

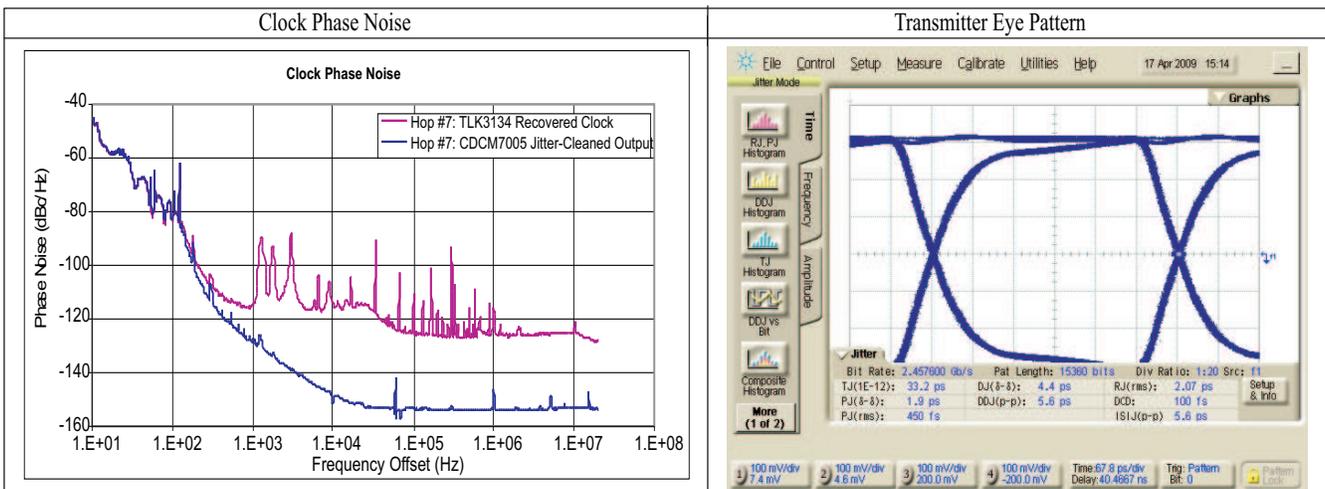


Figure 23. 2.4576Gbps Serial Rate – Hop #7 Performance

Table 3. 2.4576Gbps Serial Rate Performance Summary

| Hop # | 122.88MHz Recovered Clock Jitter (ps RMS) (10Hz to 20MHz Offset) | 122.88MHz CDCM7005 Output Clock Jitter (ps RMS) (10Hz to 20MHz Offset) | SerDes Serial Transmit Data Random Jitter (ps RMS) | SerDes Serial Transmit Data Total Jitter (ps pp [UI]) |
|-------|------------------------------------------------------------------|------------------------------------------------------------------------|----------------------------------------------------|-------------------------------------------------------|
| 1 | 14.9 | 13.1 | 2.11 | 36.5 [0.090] |
| 2 | 16.6 | 13.3 | 2.19 | 42.3 [0.104] |
| 3 | 16.5 | 13.6 | 2.31 | 46.0 [0.113] |
| 4 | 16.3 | 14.0 | 2.30 | 43.5 [0.107] |
| 5 | 16.6 | 14.6 | 2.21 | 45.2 [0.111] |
| 6 | 17.5 | 15.0 | 2.22 | 46.5 [0.114] |
| 7 | 16.1 | 15.3 | 2.07 | 33.2 [0.082] |

4 Conclusion

The TLK313x/CDCM7005 combination operated error-free in the 7-hop CPRI configuration at all the tested serial data rates with a large operating margin on the transmitter eye-mask. The worst-case total jitter recorded for the SerDes transmitter data after 7 hops was just 0.114UI at the 2.4576Gbps serial data rate which provides better than 59% margin against the 0.279UI CPRI specification.

At all the hops, the SerDes PLL remained locked after 24 hours of continuous error-free running.

Based on the above results, the TLK313x/CDCM7005 SerDes/clock combination has proven to be capable of supporting more than the required 5 CPRI hops.

Appendix A Configuration Script for the Lead SerDes Device

```

////////////////////////////////////
// TLK3131_LEAD_REF122_FULLL_245G.txt
////////////////////////////////////
// TLK3131 is provided with 122.88MHz diff reference clock input.
// Data rate is 2.4576Gbps.
// TLK3131 should be configured in TBID Mode
// Parallel I/O Source Centered mode
// JADIS TX/RX set at Full Rate with 10x Multiplier for a Line Rate of 2.4576Gbps
// JADIS TX and RX gets Diff clock
// RCLK is RXBCLK AND RCLK IS 122.88 MHz
// Date: 03/12/2009
// Revision: 1.0
////////////////////////////////////

START      CLAUSE 22

//*****
//*****
//*****LEAD TLK3131*****
//*****
//*****

// Device Pin Settings
// CODE input pin is LOW
// PLOOP input pin is LOW
// SLOOP input pin is LOW
// SPEED[1:0] input pins are both HIGH (SW select)
// ENABLE input pin is HIGH
// PRBS_EN input pin is LOW
// PRTAD[4:0] = 5'b00000

//CONFIGURE LEAD TLK3131 (DUT WITH CRPAT GEN AND VERIFIER)
//Each TLK3131 has 2 channels but only 1 channel is used.
//2nd channel is powered down
//Assigning Port Address 0 for Channel 0
//Assigning Port Address 1 for Channel 1

SETPHYADD(00)
DISPLAY(Setting LEAD TLK3131)
// Software Reset
WRITE(00, 8000)
// Verify MDIO is functional
READ(11, 3590, FFFF)

// Power down the unusable channel 1 to save power
// RX1 Ch disable
WRITE(1E, 9004)
WRITE(1F, 0000)
// TX1 Ch disable
WRITE(1E, 900C)
WRITE(1F, 0000)
// Channel 1 powerdown
SETPHYADD(01)
WRITE(00, 0940)

// go back to channel 0
SETPHYADD(00)
// SERDES_PLL_CONFIG: use 10x MPY, same as default
WRITE(1E, 9000)
WRITE(1F, 1515)
// SERDES_RATE_CONFIG_TX_RX: use FULL rate, same as default
WRITE(1E, 9001)
WRITE(1F, 0000)
// Set the JADIS RX equalizer and AC Coupled RX Term
WRITE(1E, 9002)
WRITE(1F, 1005)
// Set the JADIS TX output swing to 1375mv,
// and set common mode bit
WRITE(1E, 900A)
WRITE(1F, 0F01)
// Issue HSTL Retrain
WRITE(1E, 9304)
WRITE(1F, 0088)
WRITE(1E, 9304)

```

```

WRITE(1F, 4088)
WRITE(1E, 9304)
WRITE(1F, 0088)
// Poll Serdes PLL Status for Locked State
WRITE(1E, 901B)
READ(1F)
READ(1F, 0011, 0011)
READ(1F, 0011, 0011)

// Set TBID mode and Enable Pattern Gen/Ver in LEAD TLK3131
// PHY_CH_CONTROL_2: Enable Encoder/Decoder. Set TBID mode.
WRITE(11, 3394)
// PHY_CH_CONTROL_1: perform datapath reset
WRITE(10, 0C00)
// PHY_CH_CONTROL_1: select CRPAT Long test pattern
WRITE(10, 0403)
// PHY_CH_CONTROL_1: enable CRPAT Long test pattern generation
WRITE(10, 0413)
// PHY_CRPAT_PATTERN_COUNTER_1: clear it
READ(17)
// PHY_CRPAT_PATTERN_COUNTER_2: clear it
READ(18)
// PHY_CH_CONTROL_1: enable CRPAT Long test pattern verification
WRITE(10, 041B)

// Devices are programmed. Test pattern should pass
DISPLAY(Pattern Verification in LEAD TLK3131)
SETPHYADD(00)

// PHY_TEST_PATTERN_SYNC_STATUS: CRPAT Sync
READ(15)
READ(15, 0001, 0001)
READ(15, 0001, 0001) // double check

// Now, test pattern generation and verification is in progress.
// Verify error-free operation.
//
// PHY_TEST_PATTERN_COUNTER
READ(17, 0000, FFFF)
READ(18, 0000, FFFF)
READ(17, 0000, FFFF)
READ(18, 0000, FFFF)

// Now, all done.
DISPLAY(CRPAT LONG TEST FINISHED)

//#####
//#####

// BELOW REGISTERS TO BE READ AFTER SOME TIME
// REGISTERS TO VERIFY TO MAKE SURE SET UP IS RUNNING ERROR FREE

// CONTROL REGS
//MULT
WRITE(1E, 9000)
READ(1F, 1515, FFFF)
//RATE
WRITE(1E, 9001)
READ(1F, 0000, FFFF)
// CH_CONTROL_1
READ(10, 041B, FFFF)
// CH_CONTROL_2
READ(11, 3394, FFFF)

// STATUS REGS
// PLL LOCK
WRITE(1E, 901B)
READ(1F, 0011, 0011)

// PHY_TEST_PATTERN_SYNC_STATUS: CRPAT Sync
READ(15, 0001, 0001)
// PHY_TEST_PATTERN_COUNTER
READ(17, 0000, FFFF)
READ(18, 0000, FFFF)

//#####
//#####

```

STOP

Appendix B Configuration Script for the Partner SerDes Devices

```

////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
// TLK3131_PARTNER_REF122_FULL_245G.txt
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
// TLK3131 is provided with 122.88MHz diff reference clock input.
// Data rate is 2.4576Gbps.
// TLK3131 should be configured in TBID Mode
// Parallel I/O Source Centered mode
// JADIS TX/RX set at Full Rate with 10x Multiplier for a Line Rate of 2.4576Gbps
// JADIS TX and RX gets Diff clock
// RCLK is RXCLK AND RCLK IS 122.88 MHz
// Date: 03/12/2009
// Revision: 1.0
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////

START      CLAUSE 22

//*****
//*****
//*****PARTNER TLK3131*****
//*****
//*****

// Device Pin Settings
// CODE input pin is LOW
// PLOOP input pin is LOW
// SLOOP input pin is HIGH
// SPEED[1:0] input pins are both HIGH (SW select)
// ENABLE input pin is HIGH
// PRBS_EN input pin is LOW
// PRTAD[4:0] = 5'b00000

//Each TLK3131 has 2 channels but only 1 channel is used.
//2nd channel is powered down
//Assigning Port Address 0 for Channel 0
//Assigning Port Address 1 for Channel 1

SETPHYADD(00)
DISPLAY(Setting PARTNER TLK3131)
// Software Reset
WRITE(00, 8000)
// Verify MDIO is functional
READ(11, 3590, FFFF)

// Power down the unusable channel 1 to save power
// RX1 Ch disable
WRITE(1E, 9004)
WRITE(1F, 0000)
// TX1 Ch disable
WRITE(1E, 900C)
WRITE(1F, 0000)
// Channel 1 powerdown
SETPHYADD(01)
WRITE(00, 0940)

// go back to channel 0
SETPHYADD(00)
// SERDES_PLL_CONFIG: use 10x MPY, same as default
WRITE(1E, 9000)
WRITE(1F, 1515)
// SERDES_RATE_CONFIG_TX_RX: use FULL rate, same as default
WRITE(1E, 9001)
WRITE(1F, 0000)
// Set the JADIS RX equalizer and AC Coupled RX Term
WRITE(1E, 9002)
WRITE(1F, 1005)
// Set the JADIS TX output swing to 1375mv,
// and set common mode bit
WRITE(1E, 900A)
WRITE(1F, 0F01)
// Issue HSTL Retrain
WRITE(1E, 9304)
WRITE(1F, 0088)
WRITE(1E, 9304)
WRITE(1F, 4088)

```

```

WRITE(1E, 9304)
WRITE(1F, 0088)
// Poll Serdes PLL Status for Locked State
WRITE(1E, 901B)
READ(1F)
READ(1F, 0011, 0011)
READ(1F, 0011, 0011)
// PHY_CH_CONTROL_2: Disable Encoder/Decoder. Set TBID mode.
WRITE(11, 3390)
// PHY_CH_CONTROL_1: perform datapath reset
WRITE(10, 0C00)
// Now, all done.
DISPLAY(PARTNER TLK3131 PROGRAMMING FINISHED)
//#####
//#####

// BELOW REGISTERS TO BE READ AFTER SOME TIME
// REGISTERS TO VERIFY TO MAKE SURE SET UP IS RUNNING ERROR FREE

// CONTROL REGS
//MULT
WRITE(1E, 9000)
READ(1F, 1515, FFFF)
//RATE
WRITE(1E, 9001)
READ(1F, 0000, FFFF)
// CH_CONTROL_1
READ(10, 0400, FFFF)
// CH_CONTROL_2
READ(11, 3390, FFFF)

// STATUS REGS
// PLL LOCK
WRITE(1E, 901B)
READ(1F, 0011, 0011)
//#####
//#####

STOP

```

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