

TAS3103 Errata

1 I²C Frame Sequence Error

1.1 Problem Description

An illegal I²C frame sequence (stop followed by a start) or a glitch on the SDA line can cause the TAS3103 to stop responding to I²C commands.

1.2 System Impact

The TAS3103 will stop responding to I²C commands. A device reset is needed to correct the issue.

1.3 Workaround

Avoid glitches on the I²C lines and illegal I²C frame sequences.

1.4 Comments

This issue has been corrected in the TAS3103A.

2 Volume Saturation

2.1 Problem Description

Volume saturation can occur when a clock error occurs during a volume ramp transition.

2.2 System Impact

Any channel where the volume is transitioning can saturate and require a device reset.

2.3 Workaround

If volume is busy during a clock error, reset the TAS3103.

2.4 Comments

This issue has been corrected in the TAS3103A.

3 Treble and Bass Filters

3.1 Problem Description

The TAS3103 has an intermittent problem when writing to the treble and bass filter set registers (0xF5 and 0xF7).

3.2 System Impact

Writing to these registers can cause the bass or treble filters to have an undetermined response.

3.3 Workaround

When writing to the registers (0xF5 or 0xF7), they should be written twice. The write commands should be separated by a minimum of TBLC (64 LRCLKs by default) + 2 LRCLKs.

3.4 Comments

This issue has been corrected in the TAS3103A.

4 Incorrect Operation Following a Reset or Power Down

4.1 Problem Description

Following a reset or power down, an internal voltage drop may occur due to inadequate power-supply and regulator decoupling. The internal voltage drop can cause the device to enter an indeterminate state.

4.2 System Impact

The TAS3103 may not operate correctly without adequate decoupling, as described in the following workaround.

4.3 Workaround

Two parallel capacitors should be connected from ground to the DVDD_BYPASS_CAP pin, pin 29, and located as close as possible to the pin: a 4.7- μ F ceramic capacitor ($\pm 20\%$ tolerance or better with low ESR) and a ceramic 0.01- μ F capacitor. Two parallel capacitors should be connected from ground to the VDDS power supply, pin 31, and should be placed within 1 inch (25 mm) of the device: a 47- μ F ($\pm 20\%$ tolerance) capacitor and a ceramic 0.1- μ F capacitor. A_VDDS (3.3 V) and AVDD_BYPASS_CAP should each have a 0.47- μ F, low-ESR decoupling capacitor to AVSS.

5 Impact of MCLK Frequency Change on PLL

5.1 Problem Description

A change of MCLK frequency can cause the PLL to lose lock and the device to enter an indeterminate state.

5.2 System Impact

The TAS3103 may not operate correctly.

5.3 Workaround

The TAS3103 should be placed in reset during or immediately following a change in MCLK frequency or when MCLK is stopped.

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