

TPS3899

Functional Safety FIT Rate, FMD and Pin FMA



Table of Contents

1 Overview.....	2
2 Functional Safety Failure In Time (FIT) Rates.....	3
3 Failure Mode Distribution (FMD).....	4
4 Pin Failure Mode Analysis (Pin FMA).....	5

Trademarks

All trademarks are the property of their respective owners.

1 Overview

This document contains information for TPS3899 (DSE package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

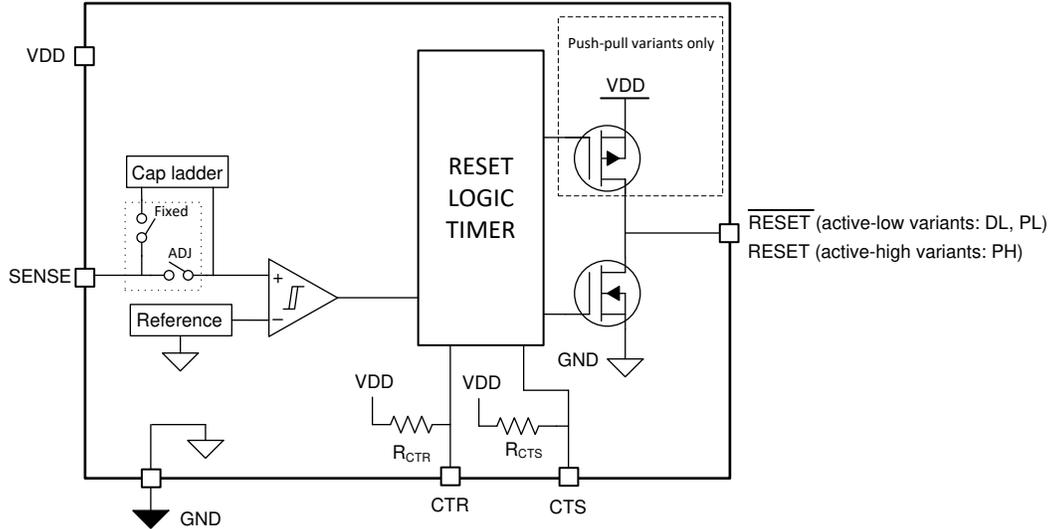


Figure 1-1. Functional Block Diagram

TPS3899 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS3899 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total Component FIT Rate	4
Die FIT Rate	2
Package FIT Rate	2

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 10 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

TABLE	CATEGORY	REFERENCE FIT RATE	REFERENCE VIRTUAL T _J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS3899 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

DIE FAILURE MODES	FAILURE MODE DISTRIBUTION (%)
RESET ($\overline{\text{RESET}}$) fails to trip	30%
RESET ($\overline{\text{RESET}}$) false trip	30%
RESET ($\overline{\text{RESET}}$) trip outside time specification	40%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS3899. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

CLASS	FAILURE EFFECTS
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

[Figure 4-1](#) shows the TPS3899 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS3899 data sheet.

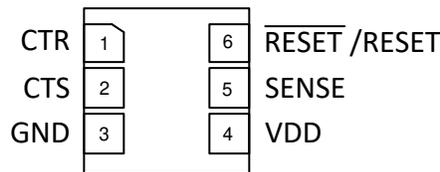


Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Unless otherwise specified, it is assumed that the voltages applied to all the pins are within the Recommended Operating Range specified in the data sheet
- Note that voltage maximum for some pins is referenced to VDD

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
CTR	1	No damage to device, can affect functionality. Forces RESET, RESET to be asserted.	B
CTS	2	No damage to device, can affect functionality. Forces RESET, RESET to be de-asserted.	B
GND	3	Normal operation.	D
VDD	4	No damage to device, can affect functionality. Shorts voltage supply to ground, increases system current.	C
SENSE	5	Defined operation, no damage to device. Forces RESET to be asserted.	C
RESET (open-drain)	6	No damage to device, can affect functionality. RESET stays asserted. Increased leakage current	B
RESET (push-pull)	6	May damage the device, can affect functionality. RESET stays asserted. Increased leakage current	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
CTR	1	Normal operation.	D
CTS	2	Normal operation.	D
GND	3	No damage to device, can affect functionality. Device is unpowered.	C
VDD	4	No damage to device, affects functionality. Device is unpowered.	B
SENSE	5	No damage to the device, sensed voltage indeterminate, output would be not as expected.	B
RESET (open-drain)	6	Reset functionality will be lost	B
RESET (push-pull)	6	Reset functionality will be lost	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

PIN NAME	PIN NO.	SHORTED TO	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
CTR	1	CTS	No damage to device, CTR, CTS delays not as expected.	C
CTS	2	GND	No damage to device, can affect functionality. Forces RESET, $\overline{\text{RESET}}$ to be de-asserted.	B
GND	3	VDD	No damage to device, can affect functionality. Shorts voltage supply to ground, increases current.	C
VDD	4	SENSE	No damage to device, can affect functionality. RESET, $\overline{\text{RESET}}$ does not pull low	B
SENSE	5	RESET (open-drain)	Potential damage to device and loss of functionality due to RESET pulling low fighting against SENSE.	A
SENSE	5	RESET (push-pull)	Potential damage to device and loss of functionality due to RESET pulling low and high fighting against SENSE.	A
$\overline{\text{RESET}}$ (open-drain)	6	CTR	No damage to device, can affect functionality. $\overline{\text{RESET}}$ does not pull high	C
RESET (push-pull)	6	CTR	No damage to device, can affect functionality. $\overline{\text{RESET}}$ does not pull high	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD Supply

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
CTR	1	No damage to device, can affect functionality. Forces RESET, $\overline{\text{RESET}}$ to be de-asserted.	B
CTS	2	No damage to device, can affect functionality. Forces RESET, $\overline{\text{RESET}}$ to be asserted.	B
GND	3	No damage to device, can affect functionality. Shorts voltage supply to ground, increases system current.	C
VDD	4	Normal operation.	D
SENSE	5	No damage to device, can affect functionality. RESET, $\overline{\text{RESET}}$ does not pull low	B
RESET (open-drain)	6	Might damage to device, can affect functionality. $\overline{\text{RESET}}$ stuck high. Increased leakage current.	A
RESET (push-pull)	6	Might damage the device, affects functionality. Increased leakage current	A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated