

# **Phase Noise Performance and Loop Bandwidth Optimization of CDCE62005**

Firoj Kabir

Clock and Timing Products

## **ABSTRACT**

This application note provides a guideline for using Texas Instruments CDCE62005 as a clock synthesizer or jitter cleaner to meet the requirements of different applications. Choosing the PLL loop bandwidth is critical for both clock generation (synthesizing) and jitter cleaning modes. Depending on the input clock phase noise, the PLL loop bandwidth can be optimized to ensure the best possible phase noise performance at the clock outputs.

## **Contents**

1	Background .....	2
2	Introduction .....	2
	2.1 Loop Filter Options .....	2
3	Measurements .....	2
	3.1 Input Clock Sources .....	3
	3.2 Free Running VCO Phase Noise Performance .....	6
	3.3 CDCE62005 Output Phase Noise Performance .....	8
4	Conclusions .....	15

## **List of Figures**

1	Phase Noise Plot of 100 MHz Generated from a Clean Clock Source (Wenzel Oscillator) .....	3
2	Phase noise Performance of a Typical Source (Agilent +HP8133) .....	4
3	Phase Noise Performance of a Noisy PLL .....	4
4	Phase Noise Performance of a Common Crystal and CDCE62005 Internal Oscillator .....	5
5	1000 MHz Free Running VCO Phase Noise Performance .....	6
6	100 MHz Free Running VCO Phase Noise Performance .....	7
7	PLL Loop Bandwidth Calculation at 520 kHz .....	8
8	Phase Noise Performance of 100 MHz Clock Output with 25 MHz Crystal and 520 kHz PLL Loop Bandwidth .....	9
9	Phase Noise Performance of 100 MHz Clock Output with 25 MHz Crystal and 105 kHz PLL Loop Bandwidth .....	9
10	PLL Phase Noise Performance with 100 MHz Clean Input Clock .....	10
11	PLL Phase Noise Performance with 100 MHz Input Clock (520 kHz PLL Loop Bandwidth) .....	11
12	PLL Phase Noise Performance with 100 MHz Input Clock (105 kHz PLL Loop Bandwidth) .....	12
13	PLL Phase Noise Performance With 100 MHz Noisy Input Clock (520 kHz PLL Loop Bandwidth) .....	13
14	PLL Phase Noise Performance With 100 MHz Noisy Input Clock (100 kHz PLL Loop Bandwidth) .....	14
15	PLL Phase Noise Performance With 100 MHz Noisy Input Clock (440 Hz PLL Loop Bandwidth) .....	15

## 1 Background

CDCE62005 is a programmable clock driver, so engineers can choose PLL loop bandwidth variables such as PFD (Phase Frequency Detector) frequency, charge pump current and external or internal RC components for the loop filter. CDCE62005 offers both internal loop and external loop filter options. The common concern is the PLL loop bandwidth settings for a particular application.

CDCE62005 employs an internal LC based oscillator which has high gain (70 MHz/V). The VCO has a good noise floor (> 5 MHz from the carrier), but noise performance at frequencies close to the carrier frequency may not always be attractive. Based on the VCO noise characteristics and incoming reference phase noise the PLL loop bandwidth can be optimized to produce lower phase noise at the output clocks.

In general, higher loop bandwidth is recommended if the input clock reference is clean. Crystals, oscillators and TCXOs are typically considered clean clock sources. A lower PLL loop bandwidth is typically recommended if the input clock is noisy and jitter cleaning is required. Clocks traveling through backplanes, clocks from low performance PLLs, or recovered clocks from SERDES or FPGAs may be considered noisy clocks and frequently require filtering to remove excessive noise. The PLL output directly depends on input clock phase noise and PLL in-band phase up to the loop bandwidth, after that VCO phase noise and buffer's noise floor dominate. Setting the loop bandwidth appropriately with respect to the input phase noise is always complicated. The phase noise of the VCO gets noisier close to carrier frequency. Selecting a lower loop bandwidth means that overall the PLL output is more dependent on VCO phase noise closer to the carrier frequency. Therefore, knowing the input clock phase noise performance is required to figure out the right loop settings.

Along with loop bandwidth value, Phase Margin is important for PLL stability. It is typically recommended to keep the phase margin value between 50 degrees to 80 degrees. Jitter peaking should also be considered. Too much peaking around the loop bandwidth will degrade the PLL performance.

## 2 Introduction

This application note will describe the impact of the performance at different loop bandwidth settings with various 100 MHz input clocks. The integrated loop bandwidth calculator provided with the CDCE62005 programming software is used to calculate the loop bandwidth and phase margin. The link for the software is: [SCAC105](#)

### 2.1 Loop Filter Options

The CDCE62005 offers both internal (completely integrated) and external loop filter options. In clock synthesizes mode using a higher PLL loop bandwidth yields better performance, therefore internal loop filter can be used and no external components are required. When the CDCE62005 is used as a jitter cleaner, a lower PLL loop bandwidth is recommended to clean low frequency and high frequency noise from the reference clock and the external loop filter option is typically recommended.

## 3 Measurements

All measurements were taken at nominal conditions (3.3V power supply and room temperature) using the CDCE62005 EVM. Outputs are configured in LVPECL mode. The CDCE62005 EVM is available for purchase in TI's eStore: <http://focus.ti.com/docs/toolsw/folders/print/cdce62005evm.html>

The integration bandwidth for RMS Jitter measurements of the 100 MHz clock is 10 kHz to 20 MHz; for 25 MHz clock measurements the bandwidth is 10 kHz to 5 MHz.

### 3.1 Input Clock Sources

Three different clock input sources were used to show the impact on PLL performance over different PLL loop bandwidth settings. A 25 MHz crystal was also used to show phase noise measurements at different loop bandwidth settings (crystal or oscillators are commonly used with CDCE62005 to generate higher frequencies).

#### 100 MHz Wenzel Oscillator – a clean clock source

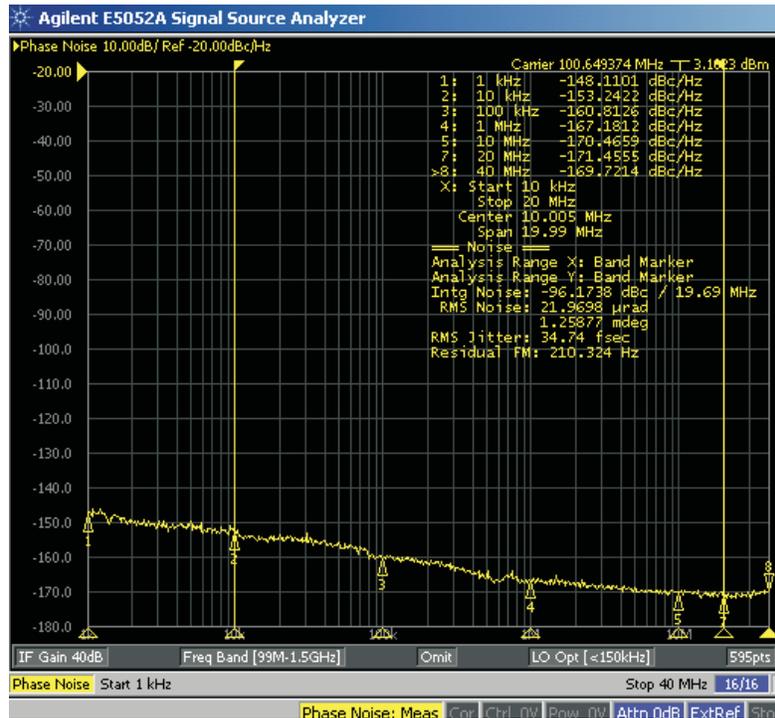


Figure 1. Phase Noise Plot of 100 MHz Generated from a Clean Clock Source (Wenzel Oscillator)

#### 100 MHz clock from Signal Generator – A typical clock source

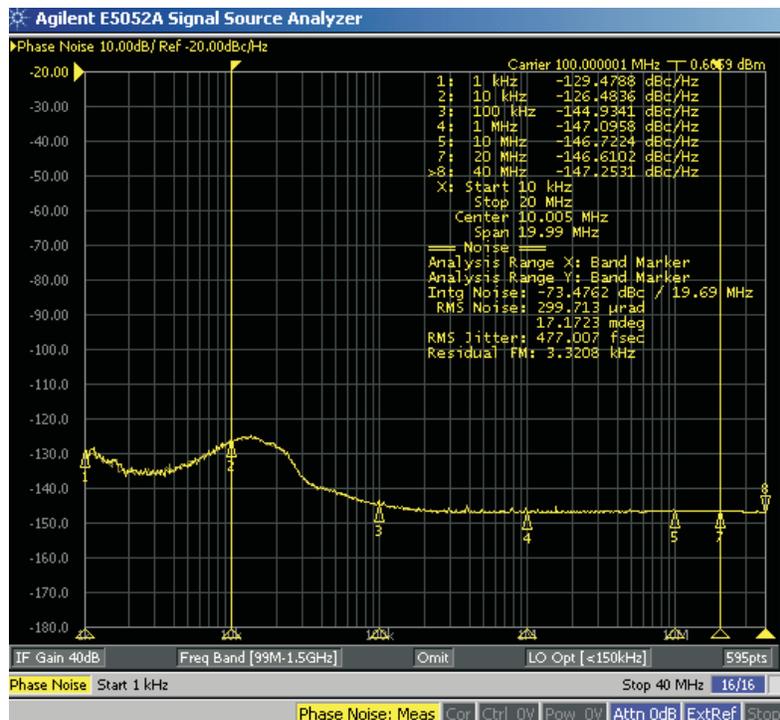


Figure 2. Phase noise Performance of a Typical Source (Agilent +HP8133)

100 MHz from a fractional PLL based clock driver – A noisy clock input



Figure 3. Phase Noise Performance of a Noisy PLL

25 MHz clock from Crystal and CDCE62005 SMARTMUX output

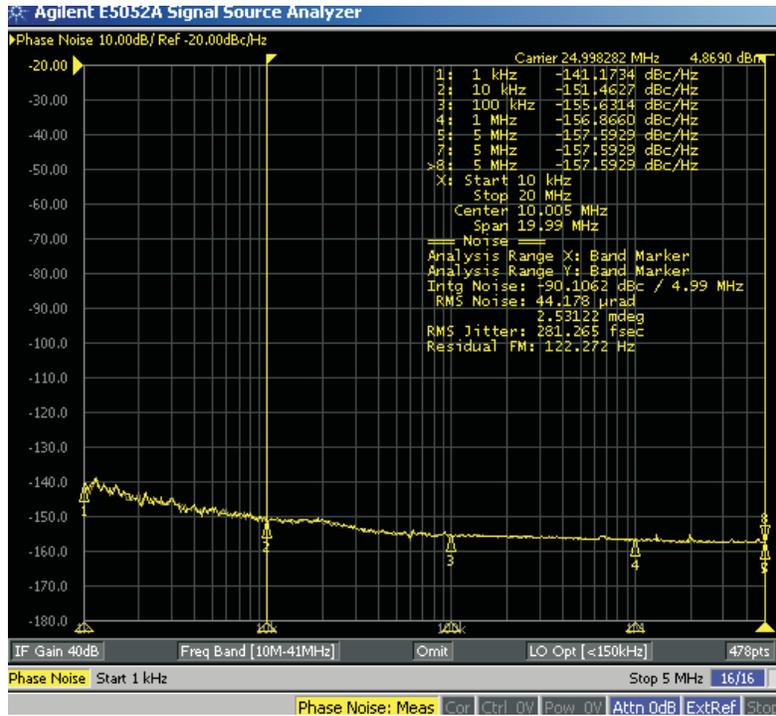


Figure 4. Phase Noise Performance of a Common Crystal and CDCE62005 Internal Oscillator

### 3.2 Free Running VCO Phase Noise Performance

The internal VCO of CDCE62005 was set to 2000 MHz and BUS frequency (directly after the pre-scalar) was 1000 MHz. The free running phase noise data can be helpful when configuring the PLL loop bandwidth. Below are two plots showing the phase noise performances of the free running VCO at 1000 MHz and a 100 MHz output.

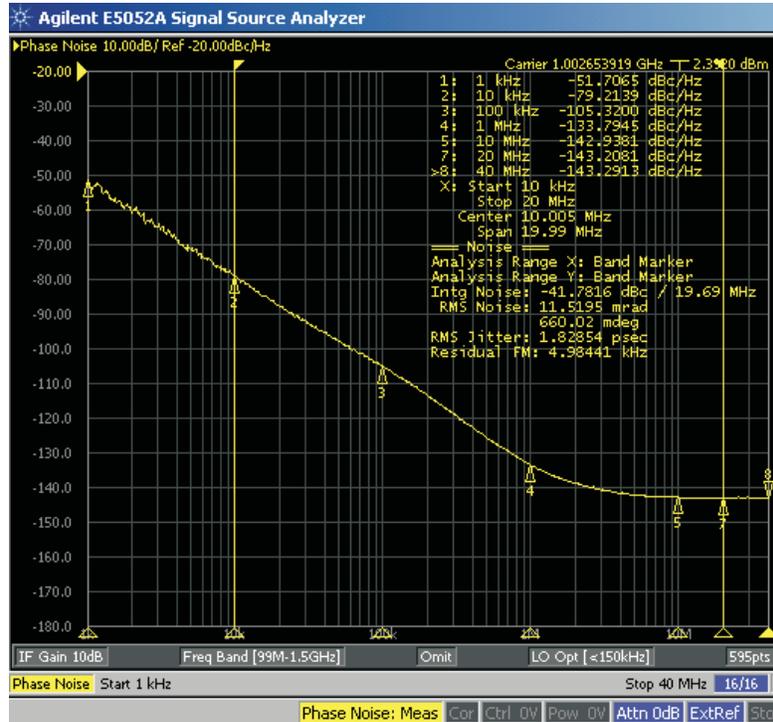


Figure 5. 1000 MHz Free Running VCO Phase Noise Performance

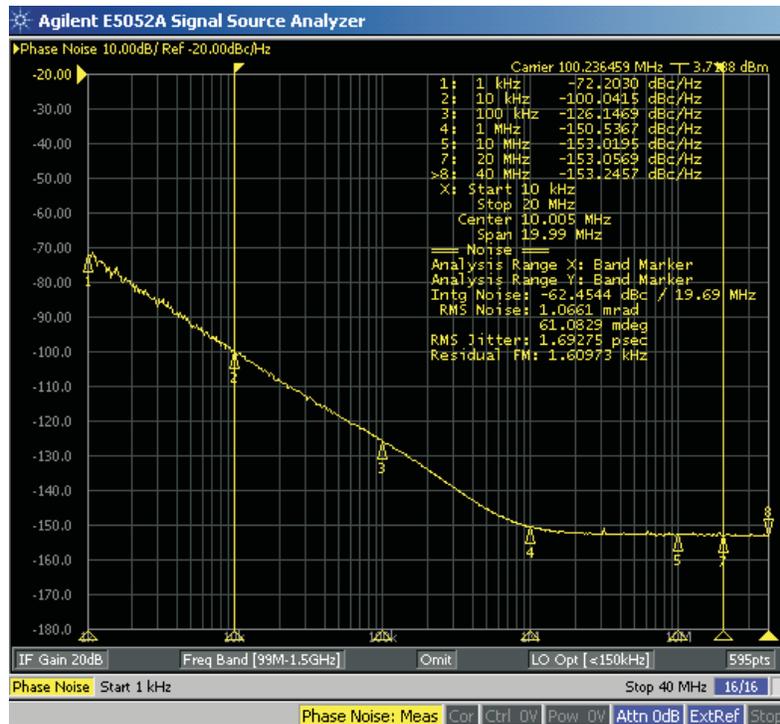


Figure 6. 100 MHz Free Running VCO Phase Noise Performance

The VCO phase noise data indicates that the 100 MHz VCO phase noise (> 5 MHz from the carrier) is around -153 dBc/Hz. The close to the carrier phase noise decreases about 25 dBc/ decade.

### 3.3 CDCE62005 Output Phase Noise Performance

As mentioned earlier, the overall phase noise performance depends on input clock phase noise, VCO phase noises, PLL in-band phase noise and PLL loop bandwidth settings. For the CDCE62005, VCO and in-band phase noise performances are fixed, so the data below indicates how input clock quality and loop bandwidth settings influence the PLL output phase noise performance.

#### 3.3.1 Phase Noise Measurements with 25 MHz Crystal

Figure 4 indicates using a crystal as a clock reference (connected to AUXIN pin) provides a clean clock reference for the PLL. In the synthesizer mode, CDCE62005 typically uses low frequency crystal or crystal oscillator to generate higher frequency clocks. A common PLL loop bandwidth setting is shown below (Figure 7):

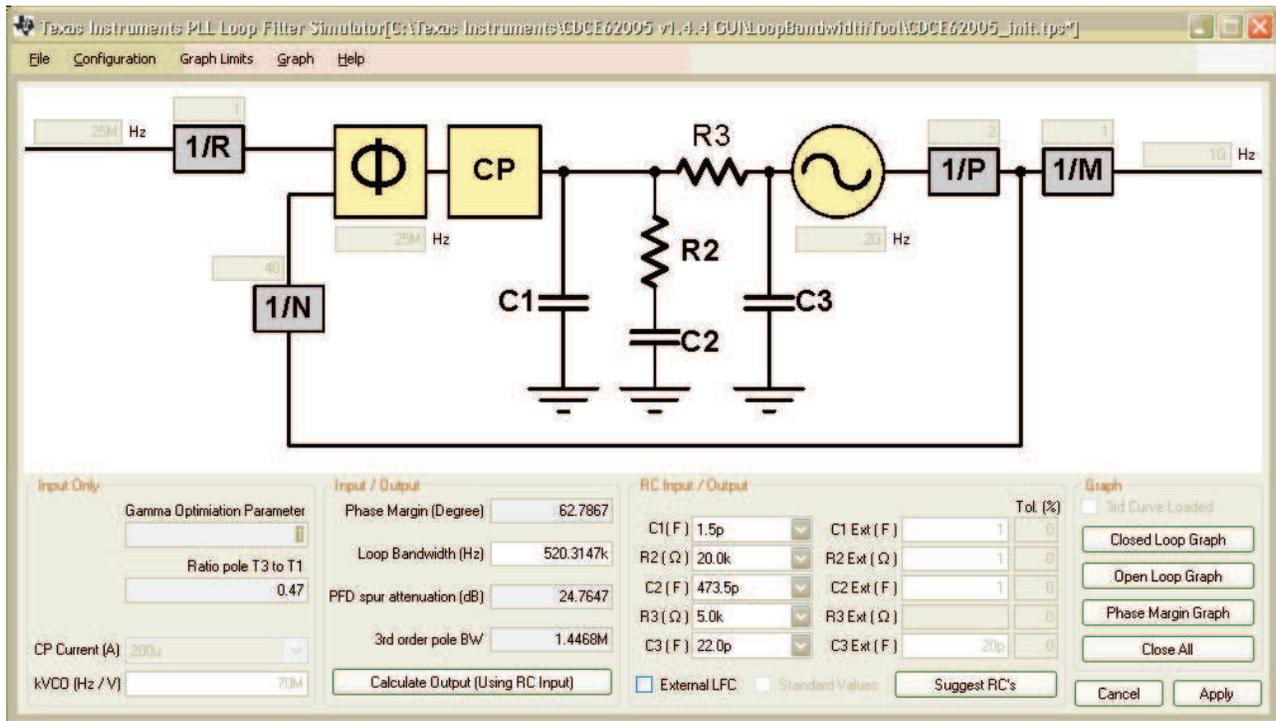


Figure 7. PLL Loop Bandwidth Calculation at 520 kHz

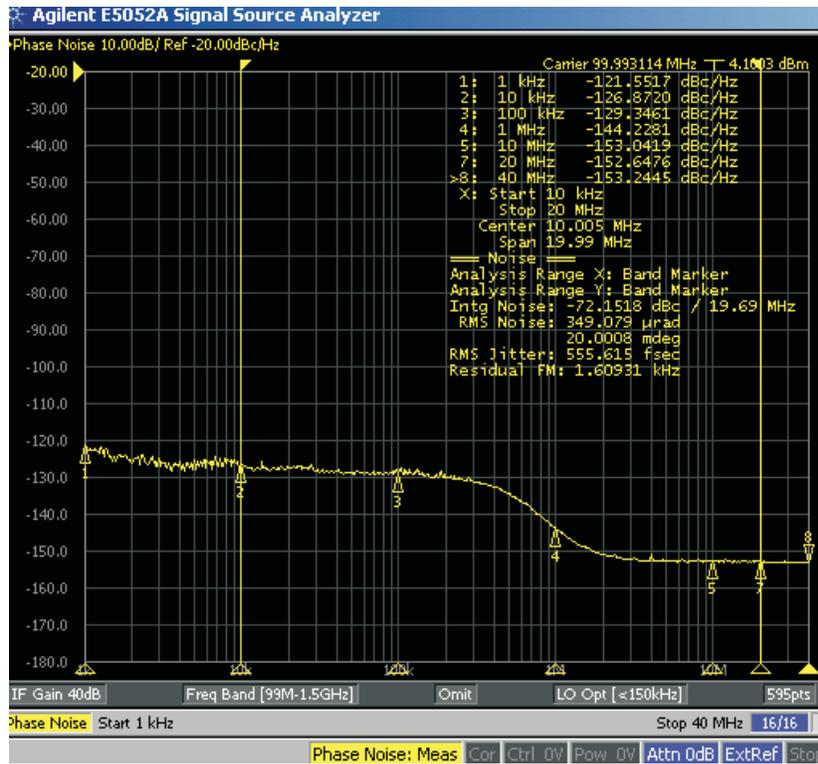


Figure 8. Phase Noise Performance of 100 MHz Clock Output with 25 MHz Crystal and 520 kHz PLL Loop Bandwidth

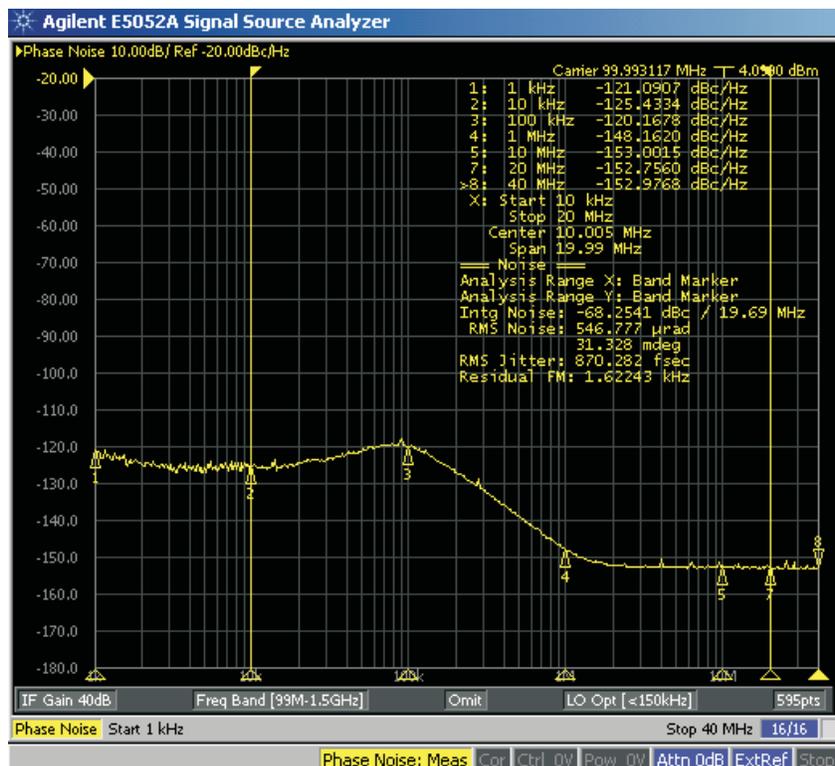


Figure 9. Phase Noise Performance of 100 MHz Clock Output with 25 MHz Crystal and 105 kHz PLL Loop Bandwidth

Using higher loop bandwidth settings (Figure 8) clearly indicates better phase noise performance compared to low loop bandwidth settings (Figure 9) with a crystal as the input clock reference. If the loop bandwidth is lower than 105 kHz in the above configuration, then the phase jitter will be higher as it will depend more on close to the carrier frequency VCO phase noise.

### 3.3.2 Phase Noise Measurements with 100 MHz Clean Clock

In this example, a Wenzel Oscillator (Figure 1) is used as a reference for the PLL. The same 520 kHz loop bandwidth is chosen as it provides the optimized phase noise performance.

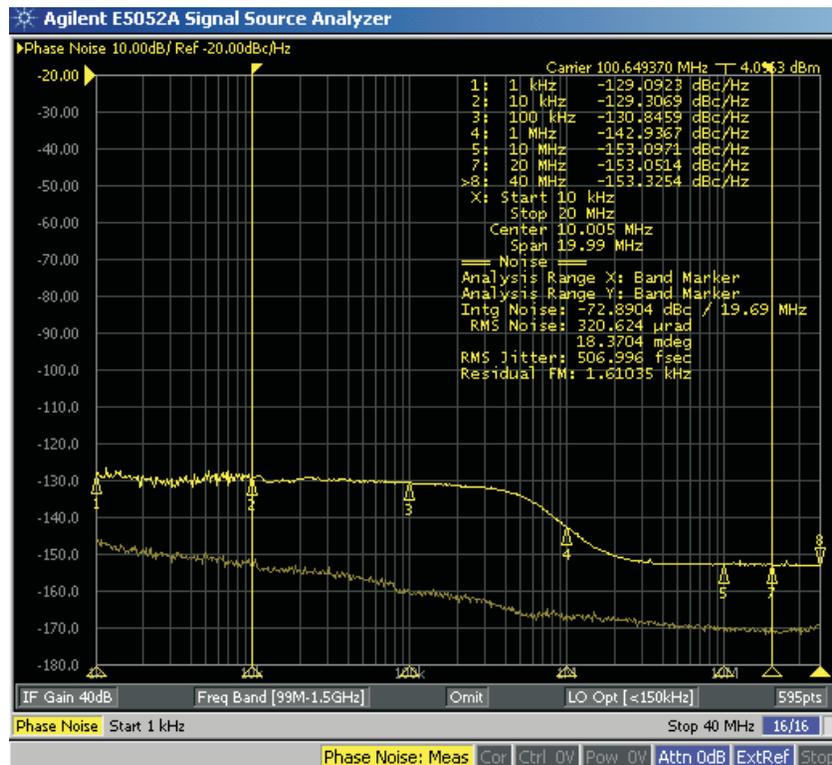


Figure 10. PLL Phase Noise Performance with 100 MHz Clean Input Clock

The shadow line in Figure 10 is the input clock phase noise performance. With a clean clock and 520 kHz loop bandwidth setting, around 0.5 ps rms jitter can be achieved. With higher loop bandwidths above 520 kHz, the rms jitter number can be decreased a few femto second (fs), but keeping the phase margin value within the limit is challenging just using the internal loop filter components.

The comparison of the phase noises of the input clock and the output is easier here as both the input clock and the output clock have the same frequencies. Figure 10 shows two important characteristics of the PLL. First the noise floor of the LVPECL buffer (at 100 MHz carrier frequency) is limited to  $-153$  dBc/Hz and secondly the PLL in-band phase noise (the contributions of the dividers and the phase detector) is limited to  $-130$  dBc/Hz.

### 3.3.3 Phase Noise Measurement with 100 MHz Clock from a Signal Generator

In Figure 2, a signal generator is used here to provide a clock reference which is similar to a crystal oscillator's output phase noise. The same 520 kHz loop bandwidth is used to show the PLL performance.

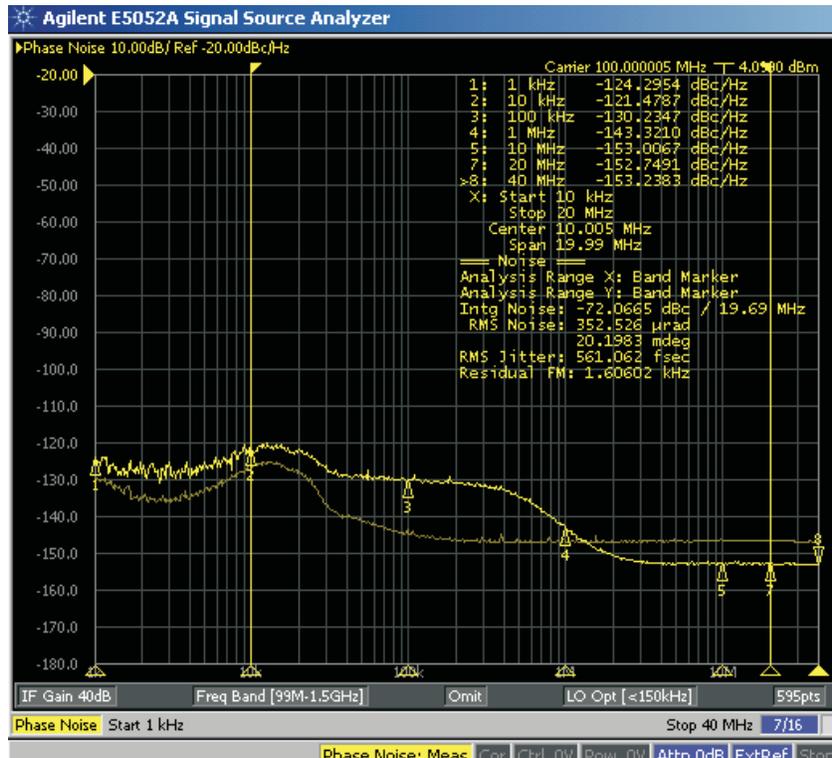


Figure 11. PLL Phase Noise Performance with 100 MHz Input Clock (520 kHz PLL Loop Bandwidth)

The phase noise performance (Figure 11) of the above combination is a perfect example how this PLL will behave with a crystal based clock source. Typically crystal based oscillators have good phase noise performance close to the carrier frequency and the VCO of this PLL offers a low noise floor (> 1 MHz from the carrier; Figure 6). So setting the right PLL loop bandwidth is critical. The PLL loop bandwidth should be set in such a way that the output phase noise can take advantage of the low phase noise of reference clock at close to carrier frequency and the low phase noise floor of the VCO. The in-band phase noise of the PLL contributes up to the loop bandwidth frequency.

If a lower PLL loop bandwidth is chosen, the output jitter will be higher as the phase noise performance of the VCO at lower frequencies is worse than the reference clock phase noise performance in that region. The plot shown below (Figure 11) is taken with 105 kHz loop bandwidth.

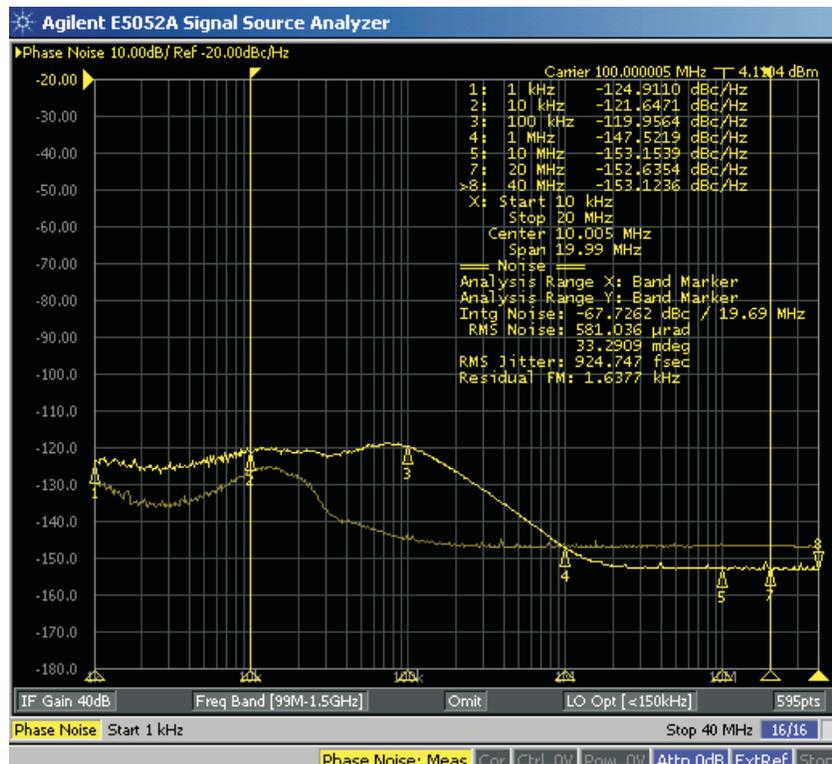


Figure 12. PLL Phase Noise Performance with 100 MHz Input Clock (105 kHz PLL Loop Bandwidth)

If a loop bandwidth higher than 600 kHz is chosen, the output jitter will be higher (compared to 520 kHz loop bandwidth setting) with this input clock as the phase noise performance of the reference clock is worse than VCO phase noise at > 600 kHz, and as a result the reference clock will contribute more noise to the PLL output clock.

### 3.3.4 Phase Noise Measurement with 100 MHz Noisy Clock

In Figure 3, a general purpose PLL is used here to provide a clock reference to CDCE62005. The same 520 kHz loop bandwidth is used to show the PLL performance

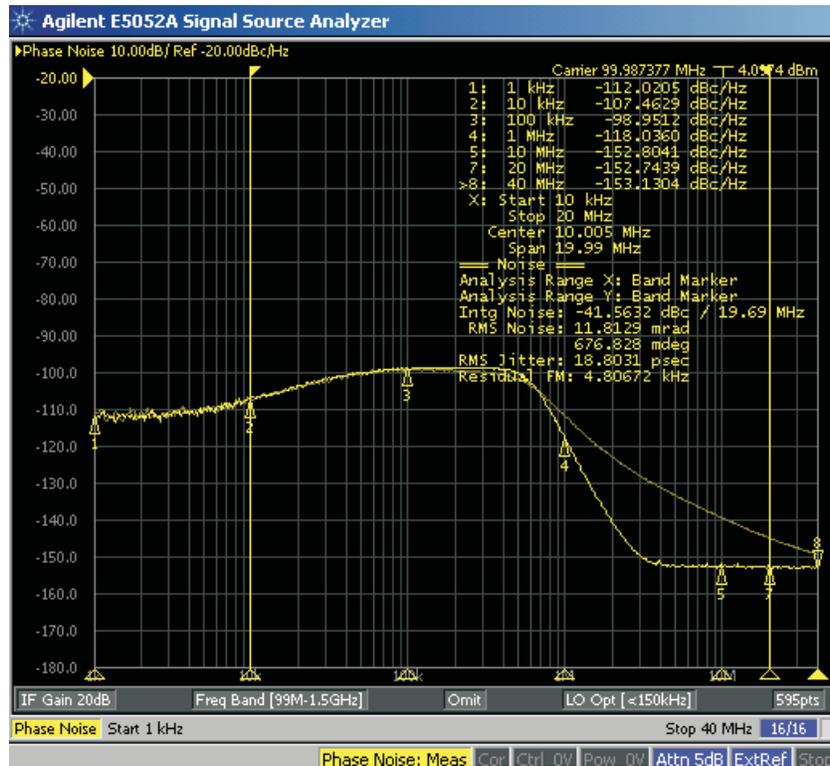


Figure 13. PLL Phase Noise Performance With 100 MHz Noisy Input Clock (520 kHz PLL Loop Bandwidth)

The phase noise performance (Figure 13) of the above combination is an example how this PLL will behave with a noisy clock source. Higher PLL loop bandwidth selection (520 kHz) yields higher jitter number (18 ps rms). As the phase noise of the input clock is higher than that of PLL in-band phase noise, the PLL output phase noise follows the input clock phase up to loop bandwidth and input phase noise is contributing to the PLL output significantly.

If a lower PLL loop bandwidth is chosen, the output jitter will be lower as the phase noise performance of the VCO is better than the reference clock phase noise performance in that region. The plot shown below (Figure 14) is taken with 100 kHz loop bandwidth.

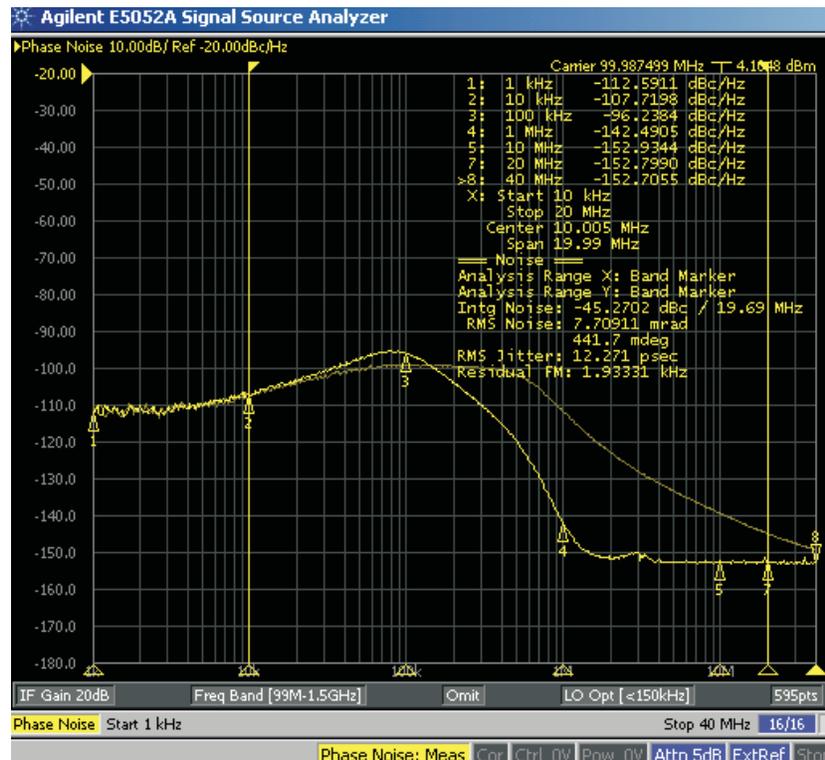


Figure 14. PLL Phase Noise Performance With 100 MHz Noisy Input Clock (100 kHz PLL Loop Bandwidth)

If the loop bandwidth is set low to 440 Hz, the output jitter will be reduced (Figure 15) dramatically even with the noisy input clock as the phase noise performance of the reference clock is worse than VCO phase noise close to carrier frequencies. The VCO phase noise contribution to the PLL output is dominant here.

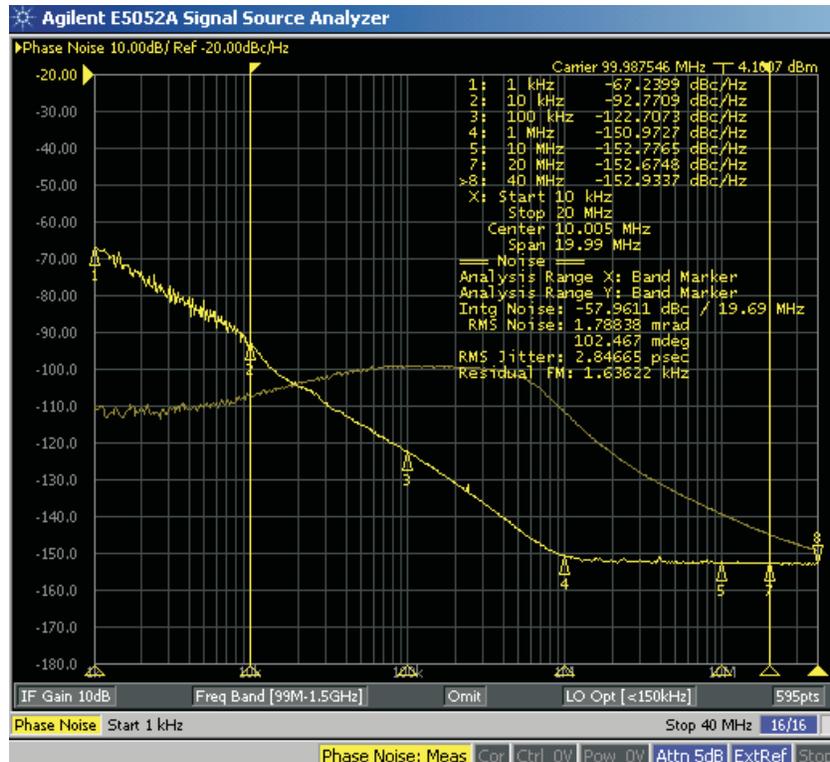


Figure 15. PLL Phase Noise Performance With 100 MHz Noisy Input Clock (440 Hz PLL Loop Bandwidth)

#### 4 Conclusions

The measured data indicates how the overall performance of the CDCE62005 depends on input clock quality and PLL loop bandwidth settings in different operating mode. The VCO phase noise performance of the PLL is fixed. Depending on input clock phase noise performance and the application, PLL loop bandwidth selection is critical to achieving the best possible performance from the PLL.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Transportation and Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>

TI E2E Community Home Page

[e2e.ti.com](http://e2e.ti.com)

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2011, Texas Instruments Incorporated