Design Guide: TIDA-010281

mmWave Radar Sensing Reference Design for Safer Robot Perception

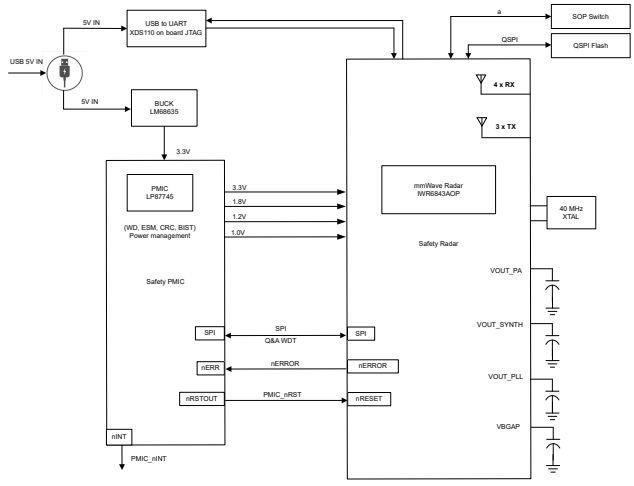
Description

This reference design features a safety millimeter-wave (mmWave) radar sensor (IWR6843AOP) and safety power management integrated circuit (PMIC) (LP87745) to enable safe perception in robotics and industrial automation applications. The design supports Q&A watchdog communication, level or PWM error signal monitoring (ESM), safety diagnostics, and radar reset functions for autonomous mobile robots (AMRs), automated guided vehicles (AGVs), humanoids, industrial robots, and collaborative robots.

Resources

TIDA-010281	Design Folder
IWR6843AOP	Product Folder
LP87745	Product Folder
LM68635-Q1	Product Folder

Ask our TI E2E™ support experts

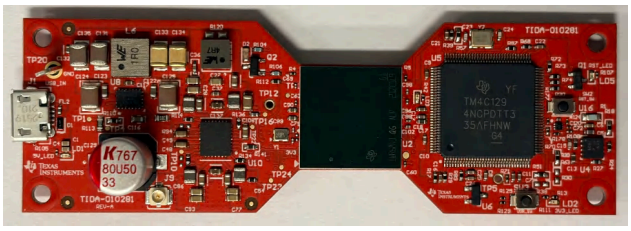


Features

- Functional safety compliant radar with hardware integrity level up to SIL-2 and systematic capability of SIL-3
- Functional safety compliant PMIC with hardware integrity level up to SIL-2 and systematic capability of SIL-3
- Software support for watchdog communication between PMIC and radar
- Provides test results for:
  - Radar performance with the safety PMIC
  - Q&A watchdog functionality from the PMIC
  - Level or PWM error signal monitoring (ESM)
  - Safety diagnostics and radar reset

Applications

- Mobile robot sensor
- Humanoid robot sensor module
- Robot sensor module
- Motion detector
- Occupancy detection (people tracking, people counting)



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1 System Description

This reference design provides a validated hardware foundation for deploying the IWR6843AOP single-chip 60GHz to 64GHz safety mmWave radar sensor in safety robotic systems. This design is a fully assembled performance-validated board paring the IWR6843AOP radar with the LP87745 safety power management IC (PMIC). The design explains Q&A watchdog communication between PMIC and radar, error signal monitoring, safety diagnostics, and radar reset using the hardware-side building blocks of a SIL 2 compliant robot perception module. The example test code used to test this design (detailed design guide with test software and test results can be accessed under NDA) also shows verified test results for Q&A watchdog communication with CRC, error signal monitoring, and radar reset. These results give developers a good starting point to build a safe radar-based robot perception sensing with SIL 2 compliant system targeting humanoids, AMRs, AGVs, and collaborative robots.

The IWR6843AOP integrates the antennas (Antennas-on-Package), RF front end, hardware accelerator, C674x DSP, and Arm Cortex-R4F in a single 15mm × 15mm package, so range-Doppler processing, CFAR detection, and point-cloud output run on-chip without an external host processor. This makes the design suitable for self-contained sensor nodes such as proximity detection around robots, safety-zone enforcement, obstacle detection and collision avoidance in humanoid robots and autonomous mobile robots (AMRs).

LP87745 is designed to meet the power management requirements of mmWave radar sensors. It generates all the supply rails of the IWR6843AOP from a single 3.3V input and is connected to the radar over SPI for Q&A watchdog communication, and through the radar NERROR_OUT signal for error signal monitoring. The PMIC reset output drives the radar reset input.

1.1 Key System Specifications

Table 1-1. Key System Specifications

Parameter	Specification
Board input supply	5V from USB connector (USB 2.0)
Intermediate supply	3.3V from LM68635-Q1 synchronous buck converter
Radar supply rails	1.2V, 1.0V (RF, internal LDO bypass), 1.8V, 3.3V (I/O)
Radar sensor	IWR6843AOP, 60GHz to 64GHz, 3TX / 4RX antennas on package
PMIC	LP87745, with 3 step-down DC/DC converters, a 5V boost converter and a 1.8V or 3.3V LDO
Radar-to-PMIC interface	SPI (radar SPIA port), radar is SPI controller
Fault and reset signals	NERROR_OUT (radar) to nERR (PMIC); nRSTOUT (PMIC) to NRESET (radar)
Functional safety	Radar and PMIC: hardware integrity up to SIL-2, systematic capability up to SIL-3
Boot	QSPI serial flash (autonomous boot) or JTAG
Clock	40MHz crystal
Debug and communication	On-board XDS110 (USB JTAG and USB-to-UART)

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2 System Overview

As demonstrated in the system block diagram. The USB 5V input supplies the on-board XDS110 debug probe and the LM68635-Q1 buck converter. The LM68635-Q1 generates 3.3V for the LP87745, which in turn generates the 3.3V, 1.8V, 1.2V, and 1.0V rails of the IWR6843AOP. The radar communicates with the PMIC over SPI, reports errors through NERROR_OUT, and is held in reset by the PMIC nRSTOUT output. The QSPI flash, the SOP (sense-on-power) boot-mode switches, and the 40MHz crystal complete the radar subsystem.

2.1 Block Diagram

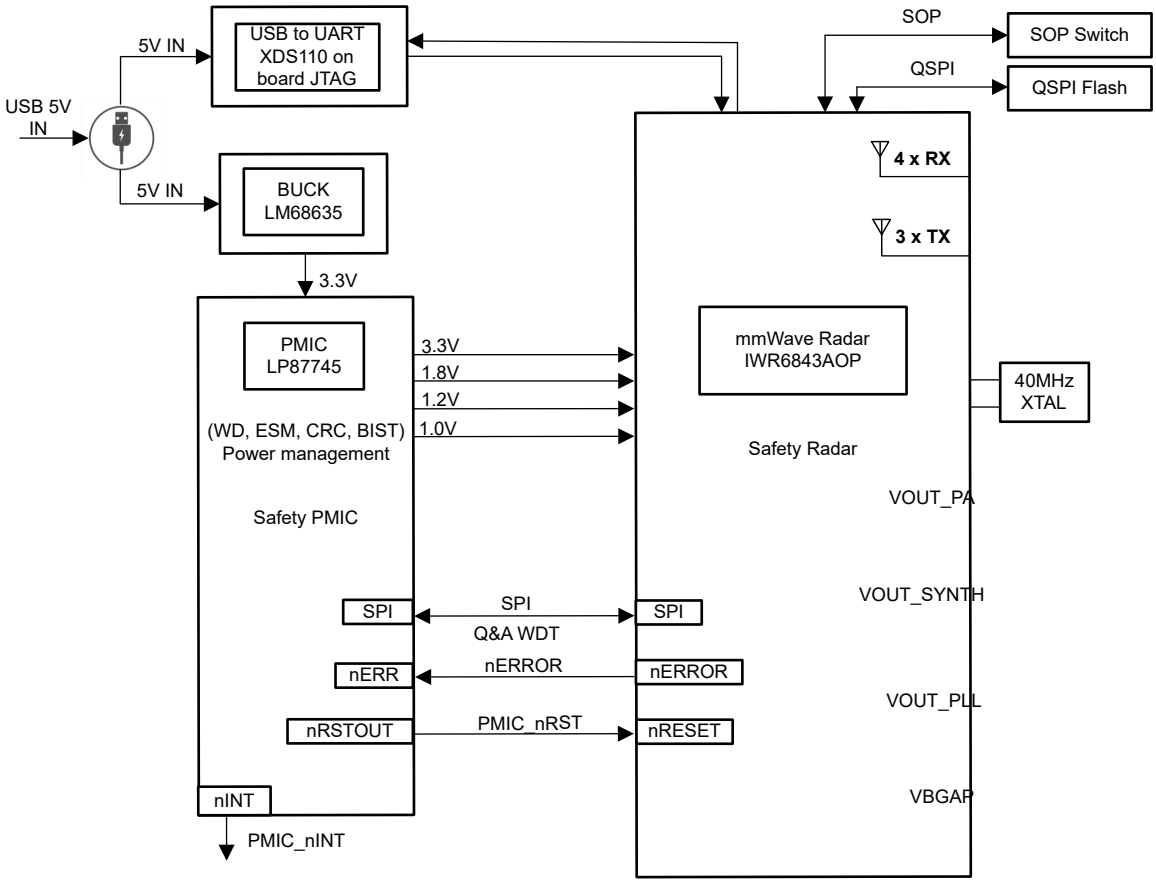


Figure 2-1. Block Diagram

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2.2 Design Considerations

Power Supply Architecture

The power tree has three stages:

1. USB 5V: supplies the LM68635-Q1 input and the XDS110 3.3V LDO (TPS79601).
2. LM68635-Q1: converts 5V to 3.3V (PMIC_INPUT3V3), which supplies the LP87745 PVIN and VCCA pins. The LP87745 ENABLE input is pulled up to this supply, so the PMIC starts its power-up sequence when the 3.3V input is present.
3. LP87745: generates the radar rails. The three buck converters generate the 1.2V (AR_1P2), 1.0V (AR_1P0_RF2), and 1.8V (AR_1V8) rails. The 5V boost output feeds the internal VIO LDO, which generates the 3.3V I/O rail (PMIC_3V3).

PMIC_3V3 supplies the radar VIOIN pins, the QSPI flash, and the board pull-ups. It is also used as a power-good signal: when it is present, it enables the XDS110 3.3V LDO and turns on a power-good LED.

Table 2-1. IWR6843AOP Supply Rails

Rail (net)	Source	IWR6843AOP Pins	Blocks Powered	Max Current (data sheet)
1.2V (AR_1P2)	LP87745 buck	VDDIN, VIN_SRAM, VNWA	Core digital and SRAMs	1000mA
1.0V (AR_1P0_RF2)	LP87745 buck	VIN_13RF1, VIN_13RF2, VOUT_PA	PA, LNA, mixers, LO distribution	2000mA (2 TX), 2500mA peak (3 TX)
1.8V (AR_1V8)	LP87745 buck	VIN_18BB, VIN_18VCO, VIN_18CLK, VIOIN_18, VIOIN_18DIFF	Synthesizer, APLL VCOs, oscillator, IF, ADC, LVDS	850mA
3.3V (PMIC_3V3)	LP87745 boost + VIO LDO	VIOIN	Digital I/Os	50mA

The RF rail is supplied at 1.0V in the IWR6843AOP internal LDO bypass mode. This is required for simultaneous three-transmitter operation, in which the 1V supply is also connected to the VOUT_PA pins. The high switching frequency and low noise of the LP87745 bucks enable an LDO-free power solution for the RF rails with minimal passive filtering. VOUT_14SYNTH, VOUT_14APLL, and VBGAP are internal regulator outputs of the radar and are only decoupled on the board.

Radar-to-PMIC SPI Interface

The IWR6843AOP communicates with the LP87745 through the SPI channel A (SPIA). The radar operates as SPI controller and PMIC as a SPI peripheral. Table 2-2 lists the connections.

Table 2-2. SPI Connections

IWR6843AOP Ball	IWR6843AOP Function	Board Net	LP87745 Pin
D2	SPIA_CLK	AR_SPICLK1	SCK_SPI (1)
F2	SPIA_MOSI	AR_MOSI1	SDI_SPI (8)
D1	SPIA_MISO	AR_MISO1	SDO_SPI (2)
C2	SPIA_CS_N pad, configured as GPIO_30	AR_CS1	CS_SPI/WD_DIS (4)

The chip select is driven by software through GPIO_30 (SPI 3-pin mode), so the chip select stays low for the whole multi-byte PMIC SPI frame. Table 2-3 lists the SPI settings on both sides.

Table 2-3. SPI Configuration

Setting	IWR6843AOP (controller)	LP87745 (peripheral)
Clock polarity	0 (SCLK idle low)	0 (SCK_SPI idle low)
Clock phase	mmWave SDK frameFormat = SPI_POL0_PHA1, which sets the MibSPI PHASE bit to 1: data is driven half a clock cycle before the first rising edge	Data sampled on the rising edge, changed on the falling edge

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Table 2-3. SPI Configuration (continued)

Setting	IWR6843AOP (controller)	LP87745 (peripheral)
Equivalent SPI mode	Mode 0 (CPOL = 0, CPHA = 0)	Mode 0 (CPOL = 0, CPHA = 0)
Bit order	MSB first	MSB first
Word size	8 bits	Byte-oriented frame
Clock rate	1MHz	—
Chip select	Software-controlled GPIO_30, active low	CS_SPI, active low

NOTE: The TI MibSPI PHASE bit uses the opposite convention to the common CPHA definition. In the mmWave SDK SPI driver, SPI_POL0_PHA1 corresponds to standard SPI mode 0. Selecting SPI_POL0_PHA0 shifts the data by half a clock cycle relative to what the PMIC expects.

Reset, Error, and Interrupt Signals

1. Reset: the PMIC nRSTOUT output (AR_NRST_PMIC) is combined with the XDS110 reset and the on-board reset push button through a three-input AND gate (SN74LVC1G11). The gate output (AR_NRST) drives the radar NRESET pin (ball U11), so the radar is held in reset whenever any of the three sources is low. An LED shows the reset state.
2. Error: the radar NERROR_OUT open-drain fail-safe output (ball U15, net AR_NERR_OUT, 10kΩ pull-up to PMIC_3V3) is connected to the LP87745 nERR/GPO2 pin, which is the system MCU error monitoring input.
3. Interrupt: the LP87745 nINT output is routed to a board net (PMIC_nINT) and is not connected to the radar.

Clocking and Boot Configuration

The radar uses a 40MHz crystal. The radar PMIC_CLKOUT pin (ball V10) is shared with SOP2, and the board provides an optional resistor path from PMIC_CLKOUT to the LP87745 SYNCCLKIN input for switching-frequency synchronization. The application firmware boots from the on-board QSPI flash (MX25R1635F). The SOP switches select the boot mode.

Table 2-4. SOP Configuration

Mode	SOP0 (S1.3)	SOP1 (S1.4)	SOP2 (S3)
Functional mode	OFF	OFF	OFF
Flash mode	OFF	OFF	ON
MMWAVEICEBOOST mode (DCA1000, JTAG)	OFF	ON	OFF

Debug and Communication

An on-board XDS110 debug probe (TM4C1294NCPDT) connects to the radar JTAG port and provides a USB-to-UART bridge for the radar UART, so a single USB cable provides power, debug, and the command-line interface. The board also includes a user LED, a user push button, and power and reset indicator LEDs.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

- TIDA-010281 board
- USB cable (5V supply, JTAG, and UART through the on-board XDS110)
- PC with a serial terminal program
- Logic analyzer or oscilloscope (optional, for SPI and signal measurements)

3.2 Software Requirements

- Code Composer Studio (CCS)
- mmWave SDK 3.6 LTS
- TIDA-010281 application software, based on the IWR6843AOP out-of-box demo (under NDA)

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3.3 Test Setup

1. Set the SOP switches for flash mode (Table 2-4) to program the QSPI flash, or for MMWAVEICEBOOST/ debug mode to load code through JTAG.
2. Connect the USB cable. The 5V LED, and then the 3.3V power-good LED, turn on.
3. Load or flash the application firmware, then set the SOP switches for functional mode and reset the board (details described in 3.4).
4. Open the XDS110 application UART in a terminal program to access the command-line interface.

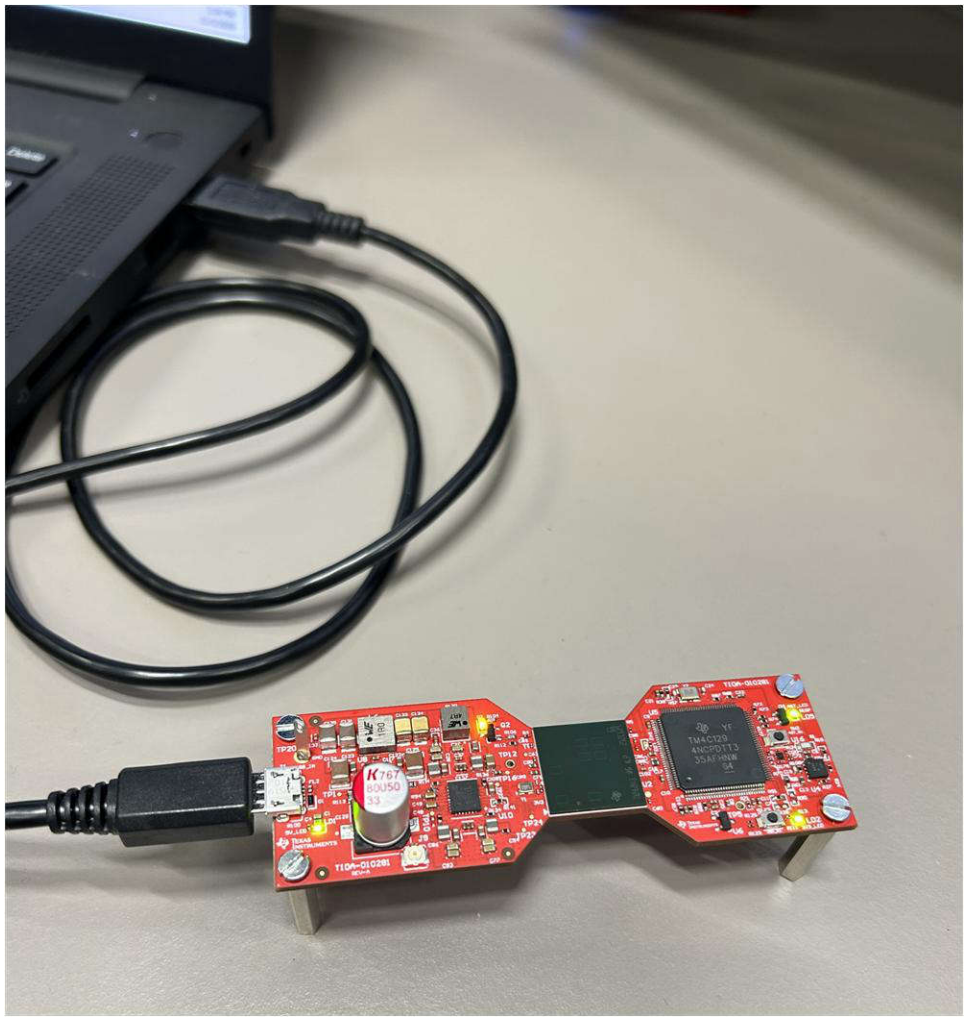


Figure 3-1. Test Set-Up image

Board Bring-Up and Firmware Flashing

Step 1: *XDS110 debug probe firmware update*

Before loading application firmware onto the IWR6843AOP, confirm the on-board XDS110 debug probe itself is on current firmware. Follow the manual update procedure (Updating the Firmware section of https://software-dl.ti.com/ccs/esd/documents/xdsdebugprobes/emu_xds110.html). Close CCS, open a command prompt, and run xdsdfu -e, xdsdfu -m, and xdsdfu -f firmware_<version>.bin -r from the uscif\xds110 directory, as described in the above link.

Step 2: *Verify the XDS110 COM ports in Device Manager*

1. After the firmware update and reconnecting the USB cable, open Windows Device Manager and confirm two XDS110 COM ports are enumerated under "Ports (COM & LPT)":

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2. XDS110 Class Application/User UART — the mmWave radar application/CLI UART (used for flashing and for the runtime CLI).
3. XDS110 Class Auxiliary Data Port — secondary debug data channel.

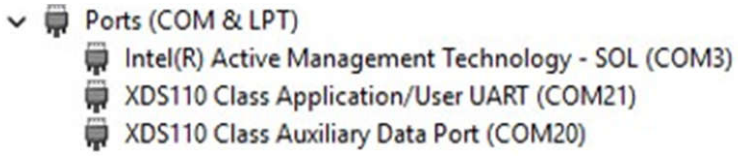


Figure 3-2. Device Manager: XDS110 COM

Note

1. Record the COM port number of the "XDS110 Class Application/User UART" (for example, COM21 in this test). This is the port UniFlash uses to flash the binary in Step 3.
2. Before flashing, set the SOP switches to Flash mode (SOP0 = OFF, SOP1 = OFF, SOP2 = ON, per Table 2-4). After every SOP switch change, press the NRST push button to reset the board into the new boot mode. The reset LED toggles when NRST is pressed — use this as visual confirmation that the board has registered the new SOP setting.

After flashing completes, set the SOP switches back to Functional mode (SOP0 = OFF, SOP1 = OFF, SOP2 = OFF) and press NRST again to boot the newly flashed application.

Step 3: *Flash the application binary with UniFlash*

1. Install TI UniFlash.
2. With the board in Flash mode (SOP switches set per the note above, followed by an NRST press), open UniFlash and select device IWR6843AOP, connection type Serial Connection.
3. Under "Program" → "Select and Load Images," browse to Meta Image 1 and select the application binary - C:\ti\mmwave_sdk_03_06_00_00 LTS\packages\ti\demo\xwr68xx\mmw\xwr68xx_mmw_demo.bin
4. Set COM Port to the "XDS110 Class Application/User UART" port identified in Step 2 (for example, COM21).

Click Load Image. UniFlash reports progress while downloading the image to the device (for example, "Downloading [META_IMAGE1] size [551044]...").

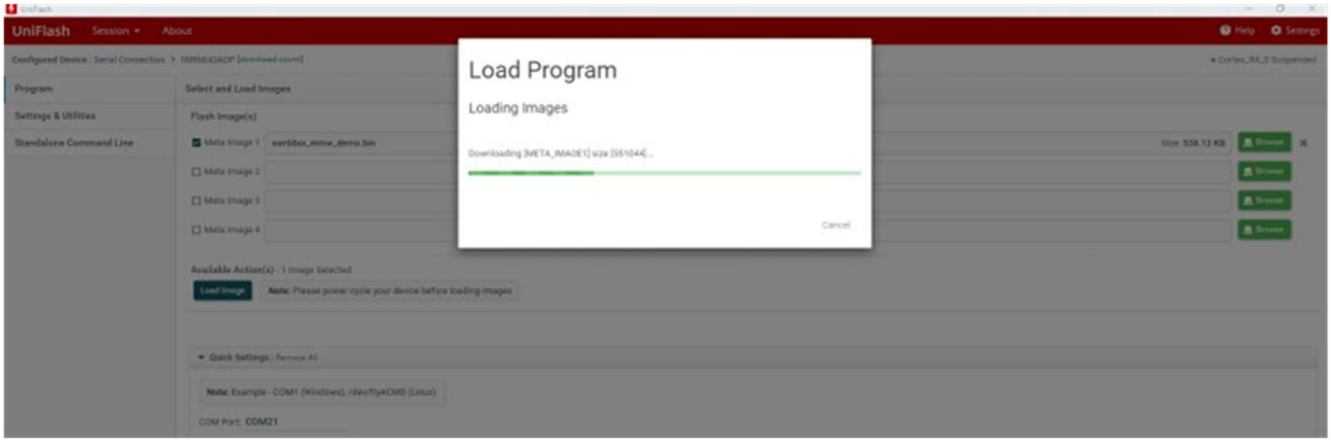


Figure 3-3. UniFlash: Load Program / Flashing xwr68xx_mmw_demo.bin

When flashing completes, set the SOP switches to Functional mode and press NRST (LED toggles) to boot the flashed application. Open a terminal on the Application/User UART COM port at 115200 baud, 8N1, and confirm the mmwDemo:/> CLI prompt appears.

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3.4 Test Results

The detailed design documentation, all the measurement results, relevant register map details, Q&A watchdog and error signal monitoring (ESM) application software needed to implement this design are available under a Non-Disclosure Agreement (NDA). To access these documents, please contact your TI representative.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2025) to Revision A (November 2026)	Page
• Updated publication for a full-length design guide	2

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