*Design Guide: TIDA-010954*

# *600W GaN-Based Single-Phase Cycloconverter Reference Design*

## Description

This reference design implements a 600W bidirectional single-stage DC-AC inverter based on cycloconverter (AC-DAB) topology and TI GaN power stages. The design supports up to 60V and ±16A on the DC side and on the single-phase, 230$V_{AC}$ and 2.6A. The inverter supports bidirectional power flow and can be used for various applications, such as a solar micro inverter or Battery Energy Storage System (BESS).

## Resources

| | |
|---|---|
| TIDA-010954 | Design Folder |
| LMG2104R022, LM5164, TLV61046 | Product Folder |
| TMS320F28P550SJ | Product Folder |
| AMC3302, TMCS1133, INA185, TLV9002 | Product Folder |
| UCC21550, UCC34141-Q1, ISOTMP35 | Product Folder |

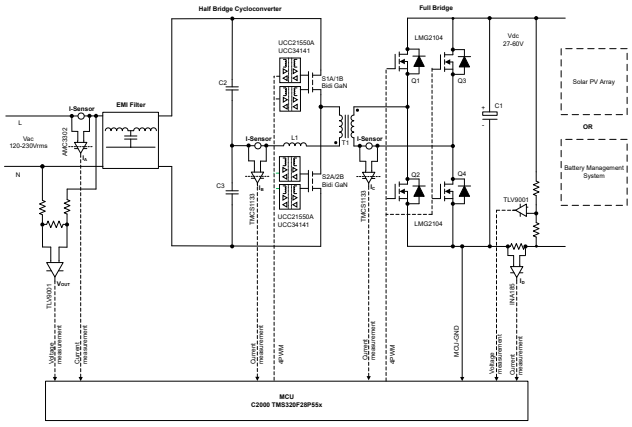
Ask the TI E2E™ support experts

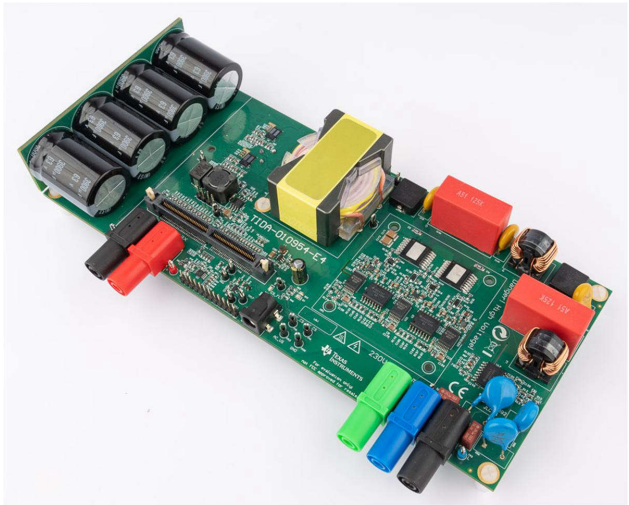
## Features

- Single stage DC-AC and AC-DC converter for photovoltaic (PV) or BESS application
- Bidirectional power flow and reactive power compensation capable
- Digital control implemented in a single controller: TMS320F28P55x
- Industrial temperature range (–40°C to +85°C)

## Applications

- Micro inverter
- Power conversion system (PCS)





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# 1 System Description

Energy sustainability and security are accelerating the demands for renewable energy like solar and energy storage systems. In residential use cases, micro inverters present a good trade-off in terms of cost and efficiency together with a simple end-user installation. Conversely, the energy storage system becomes a challenge in existing micro inverters due to the lack of a bidirectional converter in this end-equipment.

This reference design is intended to show an implementation of a single-stage bidirectional microinverter. The dimensions of the board are 235mm × 100mm × 32mm, thus leading to the calculated power density of 798 W/L.

## 1.1 Terminology

| | |
|---|---|
| **CCV** | Cycloconverter |
| **DAB** | Dual Active Bridge |
| **ZVS** | Zero Voltage Switching |
| **PV** | Photovoltaic |
| **MPPT** | Maximum Power Point Tracking |
| **THD** | Total harmonic Distortion |
| **PR** | Proportional-Resonant |
| **PLL** | Phase Locked Loop |
| **PWM** | Pulse Width Modulation |
| **PS** | Phase shift |
| **DT** | Dead time |

## 1.2 Key System Specifications

**Table 1-1. Key System Specifications**

| PARAMETER | VALUE |
|---|---|
| Input DC voltage range | 27V to 60V |
| Maximum input DC current | 16A |
| Switching frequency | 300kHz to 600kHz |
| Nominal Output AC voltage | $230V_{AC}$ |
| Nominal Output AC current | 2.6A |
| Nominal Output power | 600W |
| Peak Efficiency | 97.1% |
| Board dimensions | 235mm × 100mm × 32mm |



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# 2 System Overview

## 2.1 Block Diagram

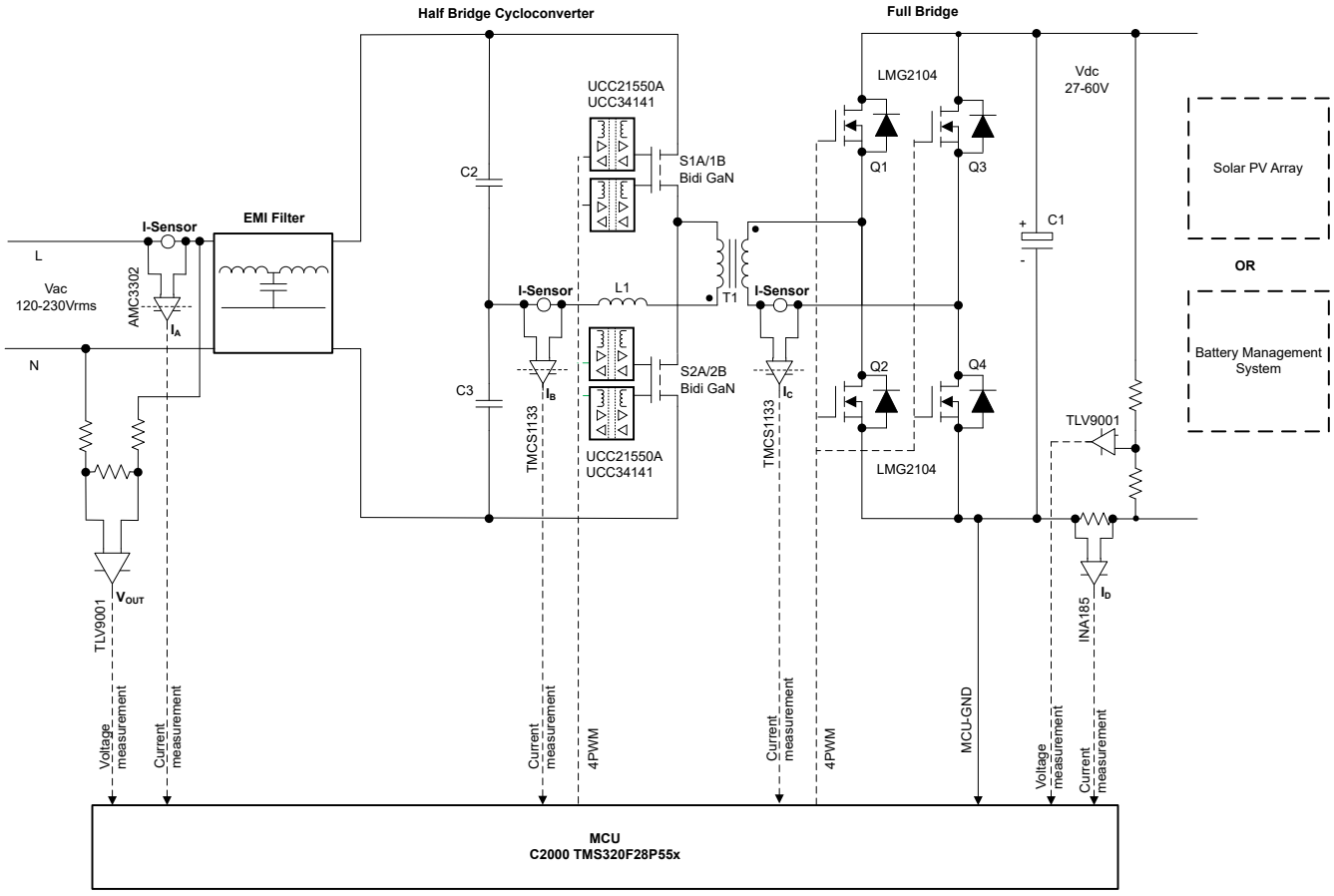



**Figure 2-1. TIDA-010954 Block Diagram**

## 2.2 Design Considerations

The design is composed of two parts: the DC side and the AC side.

The DC side has input voltage and current measurement circuits followed by a bank of electrolytic capacitors for handling the power ripple and full-bridge low-voltage primary side switches. The AC side has a half-bridge secondary side cycloconverter, filtering network, grid voltage, and current measurement.



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### 2.2.1 Input Capacitors Selection

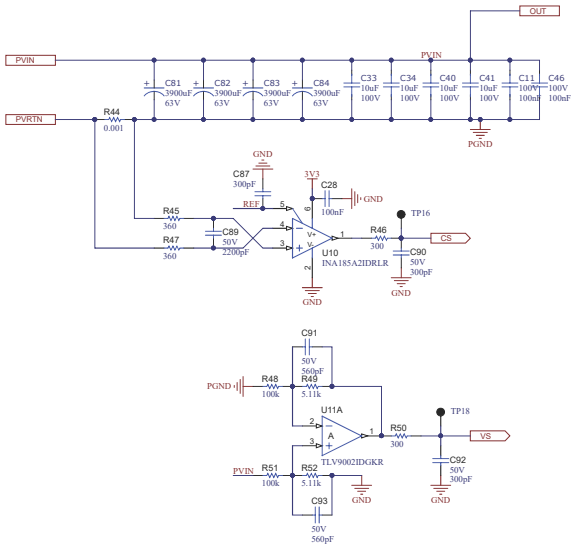



**Figure 2-2. DC Input and Current Measurements**

As Section 3.4 explained, in the design needs significant input capacitors to maintain power ripple and low input voltage variation.

In this design, the MPP deviation is defined as 1%, this means that > 99% of the maximum possible power is delivered to the inverter input. PV panels from several top manufacturers change output power for 1% from MPP if the voltage changed for ±4% from $V_{MPP}$. So input voltage ripple for input capacitors defined as 8%.

The MPP voltage for major 600W panels is more than 40V. This means the input capacitor needs to handle 600W, 100Hz power ripple with 8% voltage ripple.

Use Equation 16 to calculate the required capacitance.

About 15mF of capacitance is needed; therefore, 5 × capacitors, 3300µF, 63V, and 18mm in diameter are selected. The capacitors are installed horizontally to reduce the board height. Total capacitance is 16.5mF and the current ripple is about 2A which is lower than the maximum allowed current ripple for this type of capacitor – 2.6A.



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### 2.2.2 DC Side

Figure 2-2 shows the DC input side schematic. This image illustrates the shunt current sensing network based on INA185. The INA185 is a bidirectional, current-sense amplifier (also called a current-shunt monitor) that senses the voltage drop across a 1mΩ current-sense resistor. The INA185A2 version has a gain of 50V/V and a reference of 1.65V. These parameters result in the input current range of ±16.5A. The voltage sensing is based on the low-cost TLV9002 operational amplifier.

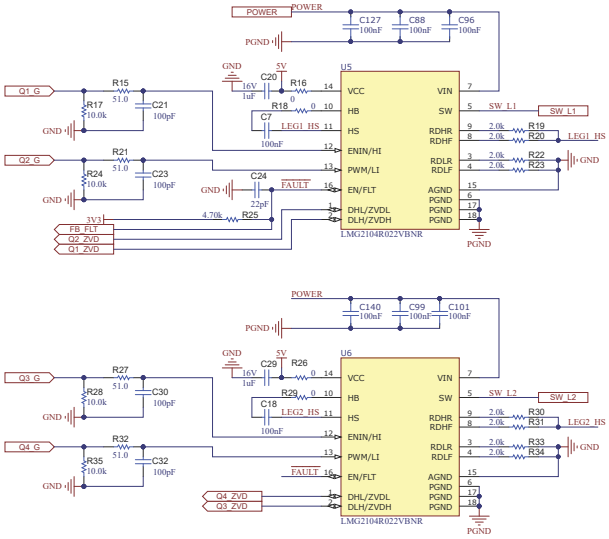



**Figure 2-3. Full-Bridge Converter**

Figure 2-3 shows the full-bridge converter is comprised of two LMG2104R022 power stages. The LMG2104R022 is half-bridge power stage with integrated gate-driver and enhancement-mode Gallium Nitride (GaN) FETs. GaN FETs provide significant advantages for power conversion because these FETs have zero reverse recovery and a very small output capacitance, $C_{OSS}$.



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### 2.2.3 AC Side

The AC side has a half-bridge cycloconverter developed with two AC switches. Figure 2-4 shows the AC switch schematic. Each AC switch is a monolithic bidirectional GaN (BDGaN) device (Q1, Q2). This configuration requires three isolated bias supplies (U19, U21, U23) that are referenced to line, neutral, and switching node via the Kelvin source pin. When UCC34141 is configured as a single-ended ouptut, D3, D15, D18, L11, L12, and L13 are DNP.

Note, the gate drive circuit is designed to have different turn off and turn off drive strengths. However, for many cases, the user can use 10R for both turn on and turn off gate resistors. This can be accomplish by DNP R129, R135, R145, and R150.

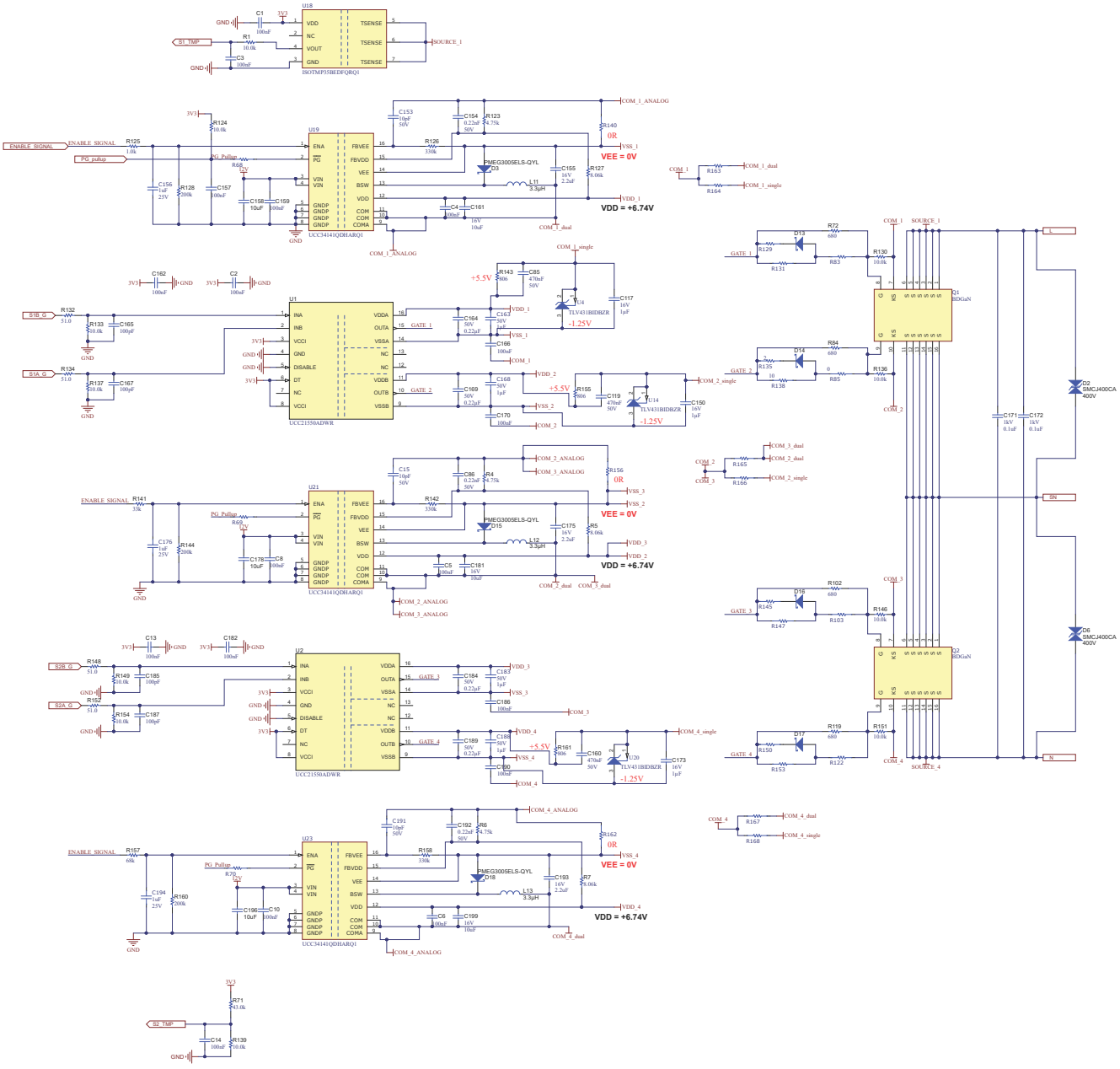



**Figure 2-4. High-Voltage AC Switch Schematic**

The isolated power supply for the gate driver is formed first by generating a 6.74V single-ended output from the 12-V rail via the UCC34141-Q1 module. This 6.74V is then converted to a split output of +5.5V and -1.25V via the TLV431 shunt reference and bias resistor.



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Note, typically the auxillary power input is provided from the J9 input jack (5V). However, the board is capable of using the input DC supply (J1) and step it down to 5V via the LM5164 buck converter. From there, the system power rails of 3.3V and 12V are generated. Jumper J7 needs to be used for this pathway to work.

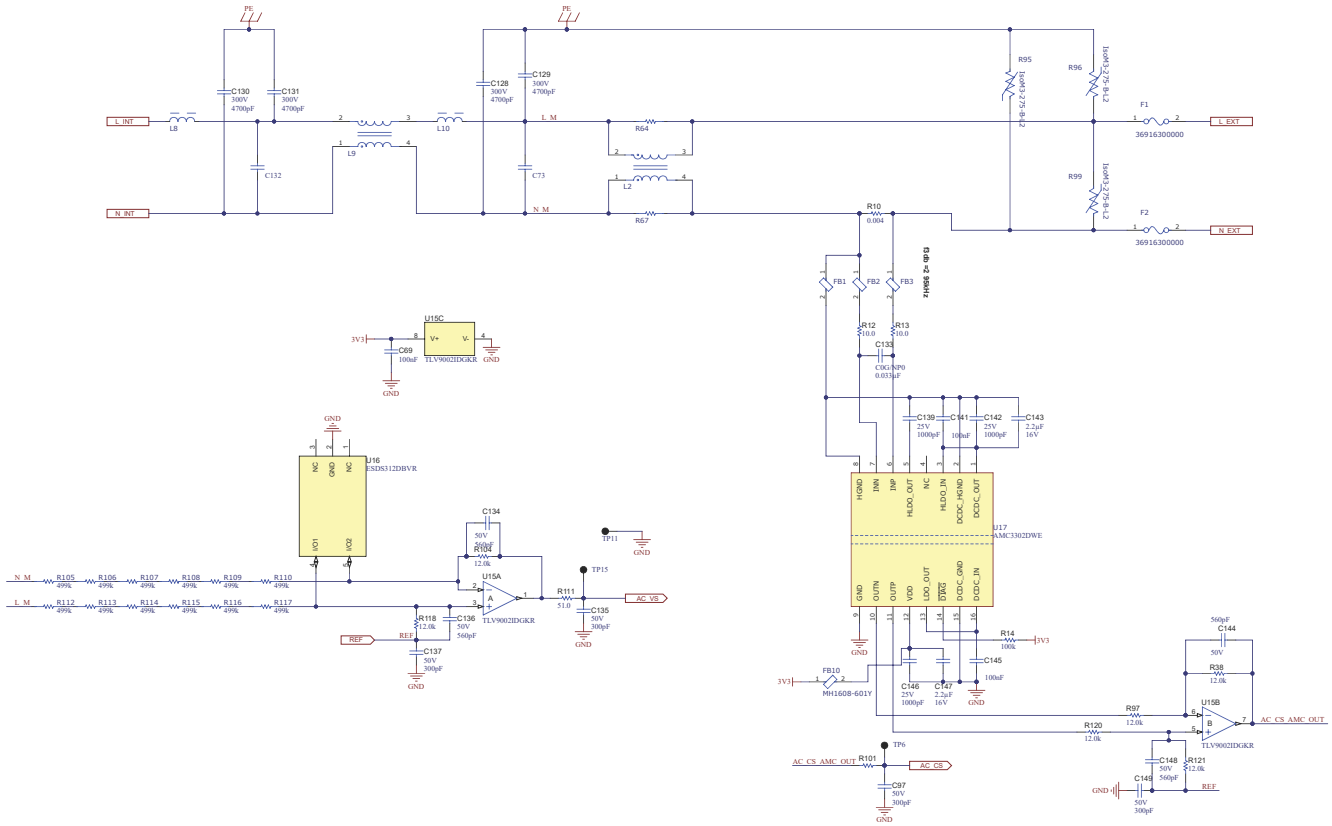



**Figure 2-5. AC Filtering and Measurement**

The AC side incorporates a shunt-based isolated current sensor AMC3302. Since the AMC3302 ouptput is differential, TLV9002 is used to convert it to single ended for the ADC input. Overall, the gain for the signal chain is 164 mV/A. For voltage measurement, a difference amplifier configuration is used with a voltage attentuation of 250:1. Figure 2-5 illustrates the AC filtering and measurement schematic.



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## 2.3 Highlighted Products

### *2.3.1 TMDSCNCD28P55X - controlCARD Evaluation Module*

TMDSCNCD28P55X is a low-cost evaluation and development board for TI's C2000™ MCU series of F28P55x devices. The device comes with a HSEC180 (180-pin high-speed edge connector) and, as a controlCARD, the device is an excellent choice for initial evaluation and prototyping. For evaluation of the TMDSCNCD28P55X, a 180-pin docking station TMDSHSECDOCK is required and can be purchased separately, or as a bundled kit.

#### 2.3.1.1 Hardware Features

The TMDSCNCD28P55X hardware features follow:

- Isolated onboard XDS110 USB-to-JTAG debug probe enables real-time in-system programming and debugging
- Standard 180-pin controlCARD HSEC interface
- Analog I/O, digital I/O, and JTAG signals at card interface
- Hardware files are in C2000Ware at `boards\controlCARDs\TMDSCNCD28P55X`

#### 2.3.1.2 Software Features

The TMDSCNCD28P55X software features include:

- TI Code Composer Studio IDE - integrated development environment for TI microcontrollers and embedded processors
- Software development kits (SDK)
- C2000Ware - low-level device drivers and examples
- MotorControl SDK - motor control system development for various three-phase motor control applications
- DigitalPower SDK - digital Power system development for various AC-DC, DC-DC and DC-AC power supply applications

### *2.3.2 LMG2104R022*

The LMG210xR0xx device is a family of 100V halfbridge power stages, with integrated gate-driver and enhancement-mode gallium nitride (GaN) FETs. The devices consist of a high-frequency GaN FET driver in a half-bridge configuration, that drives two 100V GaN FETs. GaN FETs provide significant advantages for power conversion as GaN FETs have zero reverse recovery and very small input capacitance (CISS) and output capacitance (COSS). All the devices are mounted on a completely bond-wire free package platform with minimized package parasitic elements, which can be easily mounted on PCBs.

### *2.3.3 AMC3302*

The AMC3302 is a precision, isolated amplifier optimized for shunt-based current measurements. The fully integrated, isolated DC/DC converter allows single-supply operation from the low-side of the device, which makes the device a unique solution for space-constrained applications. The reinforced capacitive isolation barrier is certified according to VDE V 0884-11 and UL1577 and supports a working voltage of up to 1.2kVRMS. The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-voltage side from hazardous voltages and damage. The input of the AMC3302 is optimized for direct connection to a low-impedance shunt resistor or another low-impedance voltage source with low signal levels. The excellent DC accuracy and low temperature drift supports accurate current measurements over the extended industrial temperature range from –40°C to +125°C. The integrated DC/DC converter fault-detection and diagnostic output pin of the AMC3302 simplify system-level design and diagnostics.

### *2.3.4 UCC21550A*

The UCC21550 is an isolated dual channel gate driver family with programmable dead time and wide temperature range. It is designed with 4A peak-source and 6A peak-sink current to drive power MOSFET, SiC, GaN, and IGBT transistors. The UCC21550 can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver. The input side is isolated from the two output drivers by a 5kVRMS isolation barrier, with a minimum of 125V/ns common-mode transient immunity (CMTI). Protection features include: resistor programmable dead time, disable feature to shut down both outputs simultaneously, and integrated de-glitch



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filter that rejects input transients shorter than 5ns. All supplies have UVLO protection. UCC21550A is selected for this design due to the UVLO requirement of BDGaN isolated bias supply.

### *2.3.5 TMCS1133 - Precision 1MHz Hall-Effect Current Sensor With Reinforced Isolation*

The TMCS1133 is a galvanically isolated Hall-effect current sensor with industry leading isolation and accuracy. An output voltage proportional to the input current is provided with excellent linearity and low drift at all sensitivity options. Precision signal conditioning circuitry with built-in drift compensation is capable of less than 1.4% maximum sensitivity error over temperature and lifetime with no system level calibration, or less than 0.9% maximum sensitivity error including both lifetime and temperature drift with a one-time calibration at room temperature. AC or DC input current flows through an internal conductor generating a magnetic field measured by integrated, on-chip, Hall-effect sensors. Coreless construction eliminates the need for magnetic concentrators. Differential Hall sensors reject interference from stray external magnetic fields. Low conductor resistance increases measurable current ranges up to ±96A while minimizing power loss and easing thermal dissipation requirements. Insulation capable of withstanding $5kV_{RMS}$, coupled with a minimum of 8mm creepage and clearance, provides high levels of reliable lifetime reinforced working voltage. Integrated shielding enables excellent common-mode rejection and transient immunity. Fixed sensitivity allows the device to operate from a single 3V to 5.5V power supply, eliminating ratiometry errors and improving supply noise rejection.

### *2.3.6 INA185 - 26V, 350kHz, Bidirectional, High-Precision Current Sense Amplifier*

The INA185 current sense amplifier is designed for use in cost-sensitive space-constrained applications. This device is a bidirectional, current-sense amplifier (also called a current-shunt monitor) that senses the voltage drop across a current-sense resistor at common-mode voltages from –0.2V to +26V, independent of the supply voltage. The INA185 integrates a matched resistor gain network in four, fixed-gain device options: 20V/V, 50V/V, 100V/V, or 200V/V. This matched gain resistor network minimizes gain error and reduces the temperature drift. The INA185 operates from a single 2.7V to 5.5V power supply. The device draws a maximum supply current of 260µA and features high slew rate and bandwidth making this device an excellent choice for many power-supply and motor-control applications. The INA185 is available in an industry standard SC70 package and low profile 6-pin, SOT-563 package. The SOT-563 package has a body size of size of only $2.56mm^2$ , including the device pins. All device options are specified over the extended operating temperature range of –40°C to +125°C.



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### 2.3.7 LM5164 – 100V Input, 1A Synchronous Buck DC-DC Converter With Ultra-Low $I_Q$

The LM5164 synchronous buck converter is designed to regulate over a wide input voltage range, minimizing the need for external surge suppression components. A minimum controllable on-time of 50ns facilitates large step-down conversion ratios, enabling the direct step-down from a 48V nominal input to low-voltage rails for reduced system complexity and design cost. The LM5164 operates during input voltage dips as low as 6V, at nearly 100% duty cycle if needed, making this device an excellent choice for wide input supply range industrial and high cell count battery pack applications. With integrated high-side and low-side power MOSFETs, the LM5164 delivers up to 1A of output current. A constant on-time (COT) control architecture provides nearly constant switching frequency with excellent load and line transient response. Additional features of the LM5164 include ultra-low $I_Q$ and diode emulation mode operation for high light-load efficiency, remarkable peak and valley overcurrent protection, integrated $V_{CC}$ bias supply and bootstrap diode, precision enable and input UVLO, and thermal shutdown protection with automatic recovery. An open-drain PGOOD indicator provides sequencing, fault reporting, and output voltage monitoring. The LM5164 is available in a thermally-enhanced, 8-pin SO PowerPAD™ integrated circuit package. The 1.27mm pin pitch provides adequate spacing for high-voltage applications.

### 2.3.8 UCC34141-Q1

UCC34141-Q1 is an automotive qualified , reinforced isolation, high working voltage, DC/DC power module designed to provide power to SiC and IGBT isolated gate drivers. TI's proprietary integrated transformer and advanced control architectures achieve high power density, low noise, and a low system bill of materials. This device is capable of delivering 1.5W typical output power at 85°C ambient temperature. The highly accurate dual-output voltages, easily set by resistor dividers, enables low on-resistance, fast and reliable switching for SiC/IGBT. The low-latency feedback control reduces the output capacitance for fast load transient and supports dynamic voltage programming. The wide input voltage and adjustable VIN UVLO supports both wide battery voltage of electric vehicles and regulated input rails. The device is operational from 5.5V to 20V VIN, and can withstand VIN overvoltage transients up to 28V.



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# 3 System Design Theory

## 3.1 Isolation for Solar Inverters

PV micro inverters require an isolation between PV panels and the AC grid because of a variety of reasons, such as the following:

- Electrical safety
- Mitigation of common-mode currents flowing between the panels and the grid
- High input-to-output voltage ratio

From a safety point of view, micro inverters combined with PV panels are commonly installed by the end-user, thus reinforced isolation between the panel and grid side is required to mitigate the electrical shock hazard from AC grid side.

The common-mode currents are a well-known challenge in PV applications due to PV surfaces exposed over grounded roofs or other surfaces in the proximity. This enormous quantity of surface leads to high parasitic capacitance between the panels and the ground (up to 200nF/kW). This parasitic capacitance can cause high common-mode current flowing into the system when common-mode voltage of the converters is not mitigated enough. A common strategy to significantly reduce the parasitic currents flowing in the system is using an isolation stage between the panels and the grid.

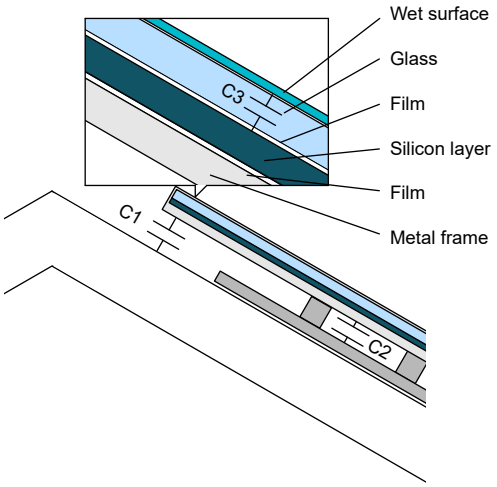



**Figure 3-1. PV Panel Parasitic Capacitance**

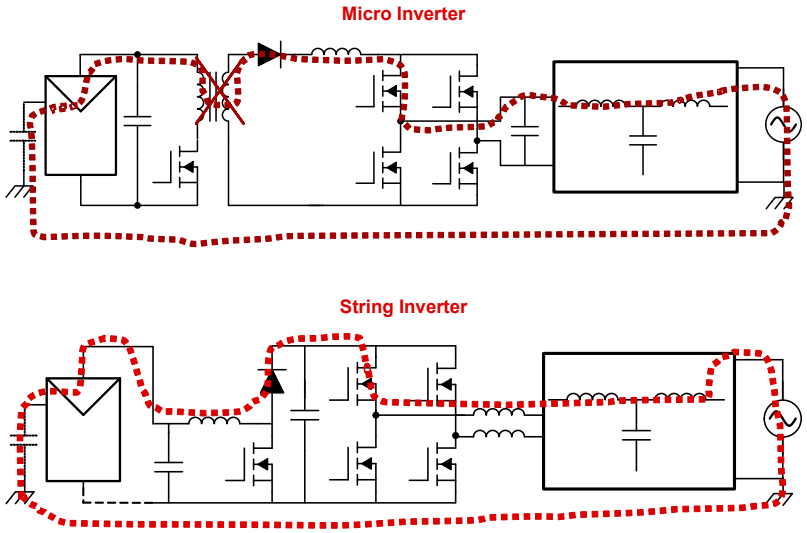



**Figure 3-2. Blocking Common-Mode Noise**



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## 3.2 Topology Overview

The cycloconverter is a topology that converts one high frequency AC waveform to another AC waveform with lower frequency. This approach eliminates the usage of an additional intermediate stage with the high-voltage DC-Link. This can increase efficiency, reduce size, and save cost. This converter can be implemented in multiple combination as DC-AC, AC-AC, 3ph AC-1ph AC and other combinations. This reference design is focused on the single-phase DC-AC operation. Figure 3-3 shows the block diagram.

The considered cycloconverter consists of:

- A full H-bridge on the DC side
- A half-bridge cycloconverter on the AC side
- A high-frequency transformer
- Transformer leakage inductance or an external inductor. This inductor determines the power transfer between the two bridges.

PWM (Pulse Width Modulation) is applied to all the power devices. On the AC side, two voltage levels are applied across the inductor. On the DC side, three voltage levels are applied. The power transfer is controlled by shifting the phase between the voltage waveforms on the primary and secondary sides.

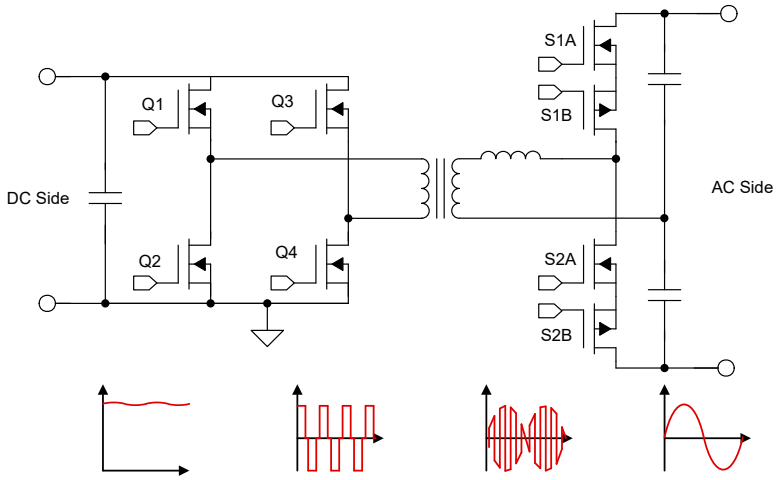



**Figure 3-3. Simplified Block Diagram**

Figure 3-3 shows that on the DC side, the cycloconverter consists of a traditional full H-bridge to generate a high-frequency rectangular AC waveform from the DC voltage source. This high-frequency AC voltage is applied to the high-frequency transformer. Due to the full-bridge structure, the DC side voltage has three levels: $+V_{DC}$, 0, and $–V_{DC}$. The formed AC waveform multiplied by the transformer ratio is applied to the left side of the inductor.

The AC side half-bridge is composed of two AC switches (S1 and S2). Each of the AC switches is composed of two unidirectional GaN power stages connected in common source. The common-source connection allows the AC switch to operate when the voltage of the grid is both positive and negative.

During the operation of the AC switch, one GaN device operates as rectifier and the second operates as a high-frequency switching device. The rectifier device is constantly turned-on for a half cycle of the grid voltage. The switching power stage operates on the same frequency as the DC-side forming high-frequency voltage across the inductor on the AC side. For example, when the AC voltage is positive, S1B and S2B are acting as rectifiers and are constantly turned on when S1A and S2A are switching. On grid zero crossing, the power stages exchange roles: when AC voltage is negative, S1A and S2A are constantly turned on and S1B and S2B are switching. To avoid shoot through, the switching devices have a dead time. During the dead time, both switching devices are turned off. Importantly, during this dead-time period, rectification devices provide a path for inductor current.

On the AC side, the voltage is following the grid and is always changing. The switching frequency for the inverter is significantly higher than the grid frequency. This allows consideration of the AC side voltage as constant voltage within each individual switching cycle.



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Due to the half-bridge structure, the AC side voltage generates two level voltage: $+V_{AC}/2$ and $-V_{AC}/2$, where $V_{AC}$ is the instantaneous grid voltage level. The half-bridge structure also means 2 × higher RMS current and higher conduction losses than full bridge. Nevertheless, for lower power converters, using the half-bridge topology can reduce system cost. For high-power designs, the full-bridge structure can provide a significant efficiency advantage. Full-bridge topology gives several benefits such as lower RMS current, higher voltage gain, and better EMI. One additional benefit for the full-bridge configuration is that this configuration has an ability to have three level voltage on the AC and increased range of ZVS switching.

The cycloconverter topology can be simplified and considered as a dual active bridge converter (DAB). As an example, for positive grid voltage, S1B and S2B operate as rectification switches and these switches are constantly turned on. Thus, S1B and S2B can be removed from the consideration; therefore, simplifying the DAB schematic with S1A and S2A operating as a half-bridge on the AC side. In comparison to regular DC-DAB, the considered AC-DAB has a few challenges:

- The voltage on the grid side changes and the voltage is not constant
- The AC side voltage has very wide voltage range, from 0 to $V_{AC_PEAK}$
- Need to achieve ZVS in wide voltages and load ranges
- The peak instantaneous power is twice the average power
- The 100Hz power ripple needs to be handled by the DC electrolytic capacitors

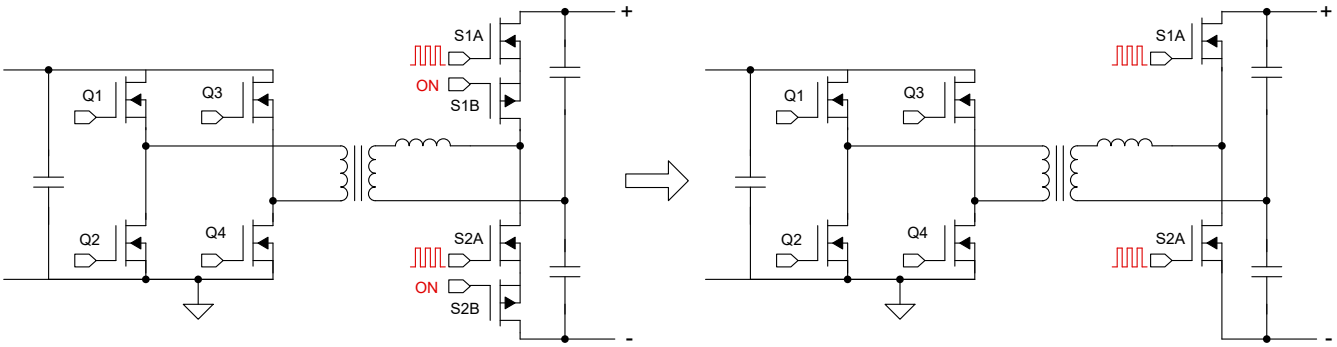



**Figure 3-4. Equivalent Circuit of the Cycloconverter in DAB When Grid Voltage is Positive**

## 3.3 Control Theory

The DAB converter consists of two voltage sources on the primary and secondary sides and a transformer with an inductor between the sides. The voltage sources and switch networks form high-frequency AC square waveforms across the inductor.

In the case of a full-bridge switching network, the AC square voltage generator can form $+V_{DC}$, 0, and $-V_{DC}$ voltage. In the case of a half-bridge switching network, the AC voltage generator can form only $+V_{AC}/2$ and $-V_{AC}/2$ voltage. In case of this reference design, the DC side has full-bridge and AC side has half-bridge configuration.

**Note**

From this point in the document to the end of the document, the DC side is called primary and the AC side is called the secondary side.

Each leg in the bridges has a 50% duty cycle and the power flow is controlled by changing the phase shift between legs. The phase shift between primary side leg is called internal phase shift. This phase shift determines the width of the voltage pulse applied to the inductor from the primary side. The secondary side does not have internal phase shift ability due to the half-bridge nature. Nevertheless, the controller has the ability to control the phase shift between centers of the primary and secondary side voltage pulses. This phase shift is commonly called external, or fundamental phase shift. The power transfer has much higher sensitivity to the external phase shift, so power transfer is commonly used for the output power regulation. The internal phase shift is commonly used for optimization purposes to decrease RMS current and extend ZVS range.



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### 3.3.1 Single and Extended Phase Shift Modulation Technique

The dual active bridge has a variation of different control methods with several degrees of freedom. Two popular methods are the Single Phase Shift (SPS) method and the Extended Phase Shift (EPS). The SPS uses only external phase shift to control output power while EPS uses both external and internal phase shift.

In SPS control, primary side legs are switching with fixed 180 degree internal phase shift and the voltage formed on the primary side is $+V_{DC}$ or $–V_{DC}$.

The single phase control is very simple and can be efficient for high load, but ZVS cannot be achieved on light loads and significant circulating currents across the inductor cause increased losses. The ZVS range can vary, depending on load and input/output voltage ratio.

To extend ZVS range and reduce circulating current, use the EPS control. The main difference for EPS is that the internal phase shift is not fixed to 180 degrees. By controlling the internal phase shift, the controller can apply three voltage levels: $+V_{DC}$, 0, and $–V_{DC}$, and manipulate the width of voltage pulses across the primary side of the inductor.

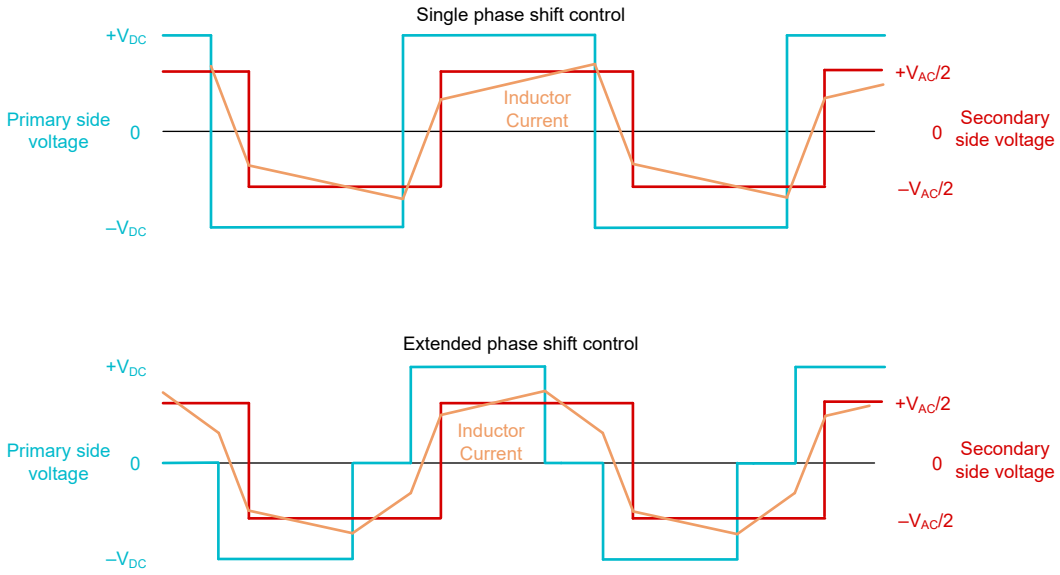



**Figure 3-5. SPS and EPS Control Waveforms**

This approach can increase ZVS range and decrease circulating power, but adds control complexity due to two degrees of freedom for the controller.

### 3.3.2 Zero Voltage Switching and Circulating Current

Zero Voltage Switching (ZVS) can significantly reduce switching losses and increase efficiency. To realize ZVS, the current flows from drain-to-source and discharge $C_{OSS}$ capacitance prior to turn on. In the DAB converter, the realization of ZVS plays a critical role because the switching frequency is high.

Consider a switching event for the Q1, Q2 leg of the DC side. Figure 3-6 shows that in the prior switching event, Q2 turned on and the current in the inductor flows. In the figure, parasitic $C_{OSS}$ and body diode is shown for Q1.

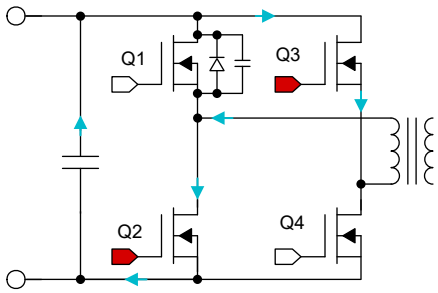



**Figure 3-6. Prior Switching**



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At the switching event, the controller turns off Q2 first and the dead time starts. The current flowing from transformer is almost constant because the current is driven by Lk on the secondary side. When Q2 is turned off, the current must go through Q1. This current starts to flow into the parasitic $C_{OSS}$ capacitance of Q1 and is discharged.

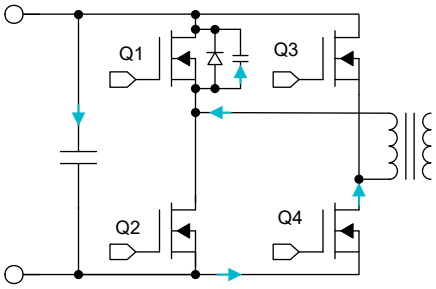



**Figure 3-7. $C_{OSS}$ Discharge**

When the $C_{OSS}$ is fully discharged, the body diode becomes forward biased and the diode starts to conduct. For GaN devices, this mode is commonly called third quadrant conduction. This mode can have significant losses due to high source-to-drain voltage in the third quadrant. TI recommends keeping the dead time reasonable so the losses remain low.

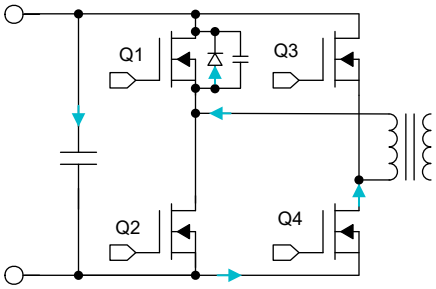



**Figure 3-8. Third Quadrant Conduction**

Finally, when the dead time is finished the controller turns Q1 on. The current starts to flow through the switch. This turn on is called a soft switch because there is almost no voltage loss, no current overlapping loss, and no $C_{OSS}$ losses.

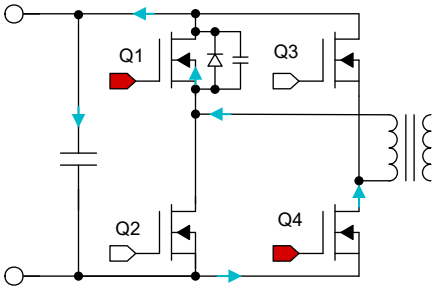



**Figure 3-9. Soft Switching**

There are three switching conditions:

- Full-ZVS
- Partial-ZVS
- Hard switch

If the current flowing from source-to-drain is able to fully discharge parasitic $C_{OSS}$ capacitance within the dead time, the ZVS condition is satisfied and this switching is called full soft switch.


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In case the current at the switching event is not enough to discharge $C_{OSS}$ within dead time - the switching is partial ZVS. The parasitic capacitor still has stored energy that is dissipated in the switch at the turn-on event. This decreases efficiency and increases switch temperature. The increase of the dead time and turn-off current helps to make the switching softer.

In case the current at the switching event flows in the opposite direction, the switching is fully hard. Full energy stored in the $C_{OSS}$ is dissipated in a switch. The increase of DT has no effect on switching behavior in this case. The controller needs to optimize the modulation parameters to achieve the correct direction of the current at the switching event. In many cases, phase shift angles or frequency can be optimized to increase range when ZVS is feasible. Nevertheless, in some conditions (for example, very light load) it is not possible to achieve ZVS for all legs.

Circulating current is very important for DAB. The circulating current is analogous with reactive current in grid systems. Like reactive current, the circulating current causes additional conduction losses. But unlike reactive current in a grid, the circulating current in DAB can be useful in some cases.

To illustrate the role of circulating current consider the SPS mode of DAB. The current transferred to the secondary side increases with the increase of the fundamental phase shift. Together with the active current increase, the circulating current is increased. When the primary- and secondary-side voltages have different polarities, the converter changes the direction of the current in the inductor (circulating time). During circulating time, DAB discharges the inductor current to zero and then recharges the inductor back with opposite polarity. This discharge and recharge does not contribute to the power transfer and has two negative effects. The first effect is basically conduction losses during the discharge and recharge process. The longer this process takes, the bigger the circulating losses are in the system. Second, the circulating time reduces active time in the power transfer cycle. This means that with shorter active time, the converter needs higher current amplitude to deliver the same average current to the output.

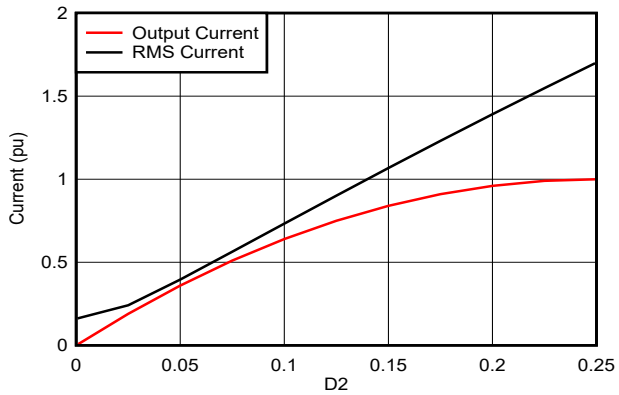



**Figure 3-10. Output Current and Circulating Current versus D2 Phase Shift**

The output current is increasing if the fundamental phase shift increases from 0 to 0.25 of the switching period. Nevertheless, the RMS current increases drastically if PS is higher than 0.125 while the active current increase is not so significant. So using fundamental phase shift higher than ±0.125 is not recommended in SPS mode.

Conversely, this circulating current provides the turn-off current for ZVS realization in DAB. Typically, the converter is designed to keep circulating current as small as needed to achieve ZVS. The internal phase shift in EPS method and frequency variation can be leveraged to control the amount of circulating current in the system.



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### 3.3.3 Optimized Control Method

In the case of the fixed frequency DAB converter with half-bridge, the designer has two values of control: internal and fundamental phase shift. The control algorithm needs to be designed to deliver reference current to the grid, thus fundamental phase shift is typically dependent on output current requirement and internal phase shift. The internal phase shift has some degree of freedom to optimize ZVS behavior. The optimized control method for this reference design is considered in [2].

In the optimized control method, the extended phase shift (EPS) is implemented with two modes of operation. In mode III, the positive pulse of $V_P$ is fully located inside the positive $V_S$ pulse. In mode II, the positive pulse of $V_P$ overlaps with both the positive and negative $V_S$ pulse. Mode I has a positive pulse for $V_P$, is fully located inside the negative $V_S$ pulse. Mode I has significant circulating current and is not considered.

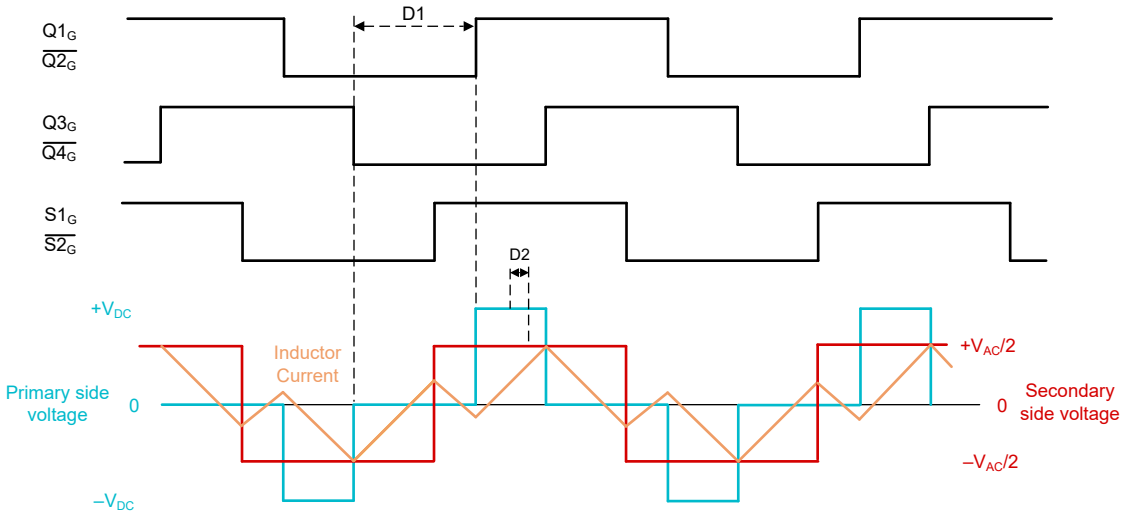



**Figure 3-11. Mode III of Operation**

Mode III has lower RMS current and is preferred for light loads, while mode II is used for high loads.

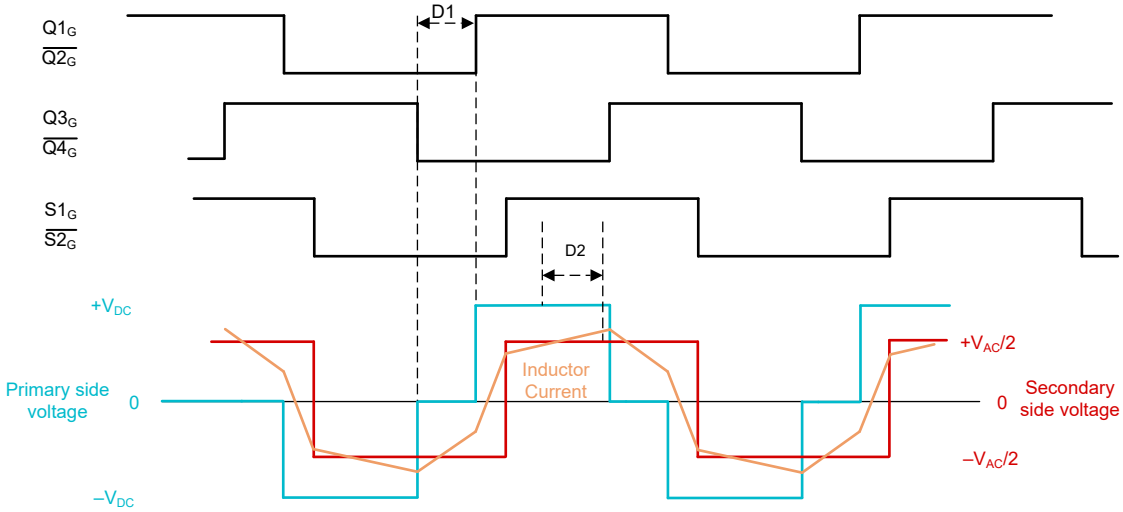



**Figure 3-12. Mode II of Operation**

The range of D1 is the internal phase shift with a range of 0 to 0.5 where 0 means the maximum primary side pulse width and 0.5 means minimum primary side pulse width. D2 is the fundamental phase shift with range –0.25 to +0.25, where positive values means power flow from the DC side to AC side.



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By definition of the operation modes, Equation 1 shows the only possible mode III operation.

$$D1 > 2 \times |D2| \tag{1}$$

Equation 2 defines the normalized output current.

$$I_N = \frac{N \times V_{DC}}{4 \times f_{sw} \times L_K} \tag{2}$$

where

- $V_{DC}$ is the DC side voltage
- N = transformer secondary to primary turns ratio
- Fs = switching frequency
- Lk = inductor value

The fundamental phase shift D2 is used to regulate output current, thus D2 is predefined by current reference and D1.

$$\begin{cases} D2_{II} = \frac{1 - \sqrt{1 - 4 \times M - 4 \times D1^2}}{4} \times \mathrm{sgn}\left(I_{REF}\right) \\ D2_{III} = \frac{M}{2 \times (1 - 2 \times D1)} \times \mathrm{sgn}\left(I_{REF}\right) \end{cases} \tag{3}$$

where

- M = | $I_{REF}/I_N$ | is the current transmission ratio

The internal phase shift is calculated with ZVS requirements. The control method defines ZVS requirements as zero current trajectories for the primary side lagging arm in Equation 4. The primary side leading arm can always realize ZVS, so the primary side is not considered.

$$\begin{cases} D1_{II,\ PRI} = \frac{(2-m) - \sqrt{(2+m)^2 - \left(2 \times m^2 - \left(2 \times m^2 + 4 \times m + 4\right) \times \left(1 + m^2 \times \left(M - 0.25\right)\right)\right)}}{2 \times m^2 + 4 \times m + 4} \\ D1_{III,\ PRI} = 0.25 - 0.5 \times \sqrt{\left|\frac{m \times M}{1 - 0.5 \times m}\right|} \end{cases} \tag{4}$$

where

- m = | $V_{AC}$ |/N × $V_{DC}$ is the voltage gain

If the requirement in Equation 5 is satisfied, the converter can operate in mode III to realize ZVS. In this case $D1_{III,PRI}$ is used as the primary side requirement. Otherwise, the converter needs to operate in mode II and $D1_{II,PRI}$ is used. If the control algorithm keeps D1 < $D1_{PRI}$ then primary side lagging arm can realize ZVS.

$$D1_{PRI} = \begin{cases} D1_{II,\ PRI}, M \geq D1_{III,\ PRI} \times \left(1 - 2 \times D1_{III,\ PRI}\right) \\ D1_{III,\ PRI}, \text{otherwise} \end{cases} \tag{5}$$



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Equation 6 defines the ZVS requirement for secondary-side switches.

$$\begin{cases} D1_{II,\,SEC} = \sqrt{\max\left\{0,\ 0.25 - M - \frac{m^2}{16}\right\}} \\ D1_{III,\ SEC} = \ 0.5 - 0.25 \times m \end{cases} \quad (6)$$

$$D1_{SEC} = \begin{cases} D1_{II,\ SEC},\ M\ \geq D1_{III,SEC} \times \left(1 - 2 \times D1_{III,\ SEC}\right) \\ D1_{III,\ SEC}, \text{otherwise} \end{cases} \quad (7)$$

Similarly, if the requirement in Equation 7 is satisfied the $D1_{III,SEC}$ value is used as secondary side requirement, otherwise the $D1_{II,SEC}$ value is used. If the control algorithm keeps D1 > $D1_{SEC}$, then the primary side lag arm can realize ZVS.

Figure 3-13 and Figure 3-14 show the calculated ZVS requirement curves within a grid cycle.

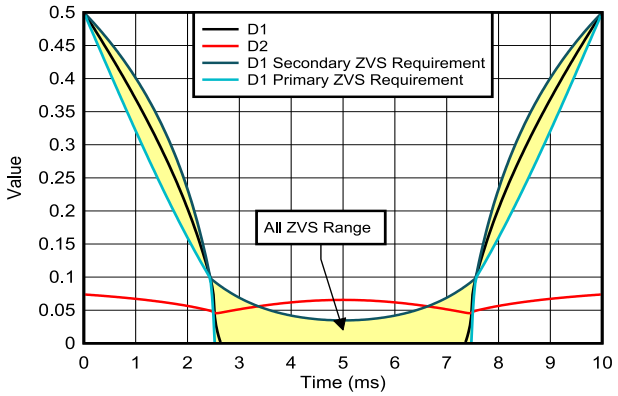



**Figure 3-13. ZVS Curves Over AC Half Wave at High Load**

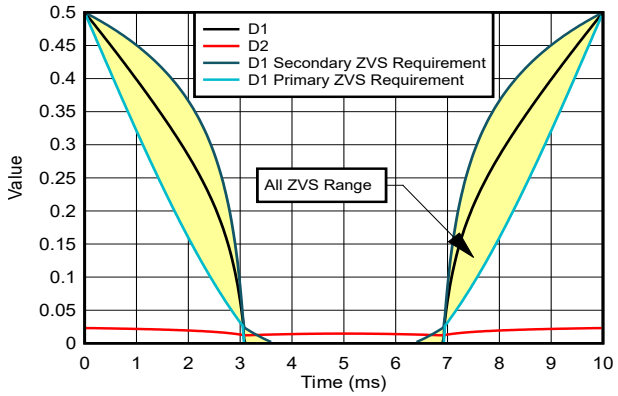



**Figure 3-14. ZVS Curves Over AC Half Wave at Medium Load**

As the trajectories illustrate, at the beginning of the grid sinusoid, the converter starts in mode III and then, due to increased voltage gain and load, transitions to mode II.

On light load, achieving Zero Voltage Switching (ZVS) for both primary and secondary side across zero crossing is easy, but achieving ZVS near to grid amplitude voltage is difficult. Conversely, at heavy load, the ZVS requirements for the distance between primary and secondary sides becomes narrower, making it hard to achieve ZVS across zero crossing. However, in this situation, achieving ZVS around grid amplitude voltage becomes easier.

There are two points where D1 and D2 are crossed – this is the mode transition point. There is no possibility of achieving ZVS for both primary lag and secondary sides because the turn-off current is very close to 0 at this point.

Equation 8 calculates how the controller uses a weighted sum from these two requirements to calculate the final value for D1.

$$D1 = \ \alpha \times D1_{PRI} + (1 - \ \alpha) \times D1_{SEC},\ \ \alpha \in (0,\ 1) \quad (8)$$

where

- α is the weighting coefficient

The weighted coefficient can be used to balance behavior of the primary and secondary sides. If the coefficient comes close to 1, the final D1 going closer to primary ZVS requirement giving less room for ZVS realization for the primary side, in the same time giving more room for ZVS on the secondary side. Typically the $C_{OSS}$ stored energy on the high-voltage switches is significantly higher and from the efficiency perspective, a balance with higher values for α gives slightly better results.



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### 3.3.4 Dead-Time Compensation

As previous sections in this design guide illustrate, the dead time plays an important role in ZVS realization. Unfortunately ZVS cannot be realized in the full range of voltage gains and loads, especially at the mode change point. When the converter loses ZVS for one of the legs, the effective phase shift changes causing distortion in the output current waveform.

The reason for the phase shift change is as follows: real applications employ switches with inherent dead time to prevent shoot-through and allow current to discharge in the switches. When Zero Voltage Switching (ZVS) is enabled, both the primary and secondary sides initiate the changes immediately upon the complementary switch being turned off. In cases of good ZVS, a new voltage is reached before the dead time expires.

A hard switch keeps the voltage unchanged until a turn-on event forces the voltage to a new level at the end of dead time.

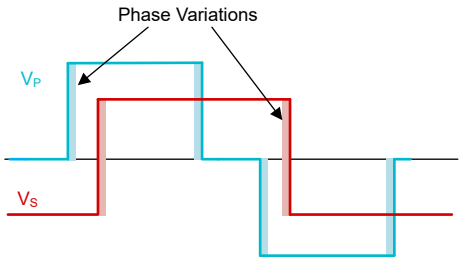



**Figure 3-15. Phase Shift Variations**

Dead-time effects alter the effective phase shift. Implementation of ZVS across different legs introduces varying changes in D1 and D2. Table 3-1 shows the compensation values for different legs.

**Table 3-1. Dead-Time Compensation Values**

| ZVS REALIZATION | COMPENSATION FOR D1 | COMPENSATION FOR D2 |
|---|---|---|
| Primary lead | $-DT_{DC}$ | $+DT_{DC}/2$ |
| Primary lag | $+DT_{DC}$ | $+DT_{DC}/2$ |
| Secondary | 0 | $-DT_{AC}$ |

To understand the ZVS realization, the controller calculates switch currents for all legs. Table 3-2 shows equations for turn-off current calculation.

**Table 3-2. Equations for Turn-Off Currents**

| | MODE II | MODE III |
|---|---|---|
| Primary lead | $\frac{N \times V_{DC} \times \left(D1 - \frac{1}{2}\right) + \lvert V_G \rvert \times \left(\frac{D1}{2} - D2 + 0.25\right)}{2 \times F_{SW} \times L_K}$ | $\frac{N \times V_{DC} \times \left(D1 - \frac{1}{2}\right) + \lvert V_G \rvert \times 0.25}{2 \times F_{SW} \times L_K}$ |
| Primary lag | $\frac{N \times V_{DC} \times \left(-D1 + \frac{1}{2}\right) + \lvert V_G \rvert \times \left(\frac{D1}{2} + D2 - 0.25\right)}{2 \times F_{SW} \times L_K}$ | $\frac{N \times V_{DC} \times \left(-D1 + \frac{1}{2}\right) + \lvert V_G \rvert \times \left(\frac{D1}{2} + D2 - 0.25\right)}{2 \times F_{SW} \times L_K}$ |
| Secondary | $\frac{N \times V_{DC} \times \left(2 \times D2 - \frac{1}{2}\right) + \lvert V_G \rvert \times 0.25}{2 \times F_{SW} \times L_K}$ | $\frac{N \times V_{DC} \times \left(D1 - \frac{1}{2}\right) + \lvert V_G \rvert \times \left(-\frac{D1}{2} + D2 + 0.25\right)}{2 \times F_{SW} \times L_K}$ |

If the calculated turn-off current is negative, then compensation can be applied with these switches. However, in real applications just positive current is not enough to realize ZVS, because the switches require some significant current to discharge $C_{OSS}$ within the dead time. If this current is not enough, there can be partial soft switching. So the compensation value in Table 3-1 needs to be linearized. In the linear compensation approach, additional linear coefficient $K_{COMP}$ is calculated in equation Equation 9 and applied to dead-time compensation values in Table 3-1.



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$$K_{COMP} = \min\left\{1, \frac{I_{ZVS} - I_S}{I_{ZVS}}\right\} \quad (9)$$

where

- $I_S$ is the switch current
- $I_{ZVS}$ is the desired current for full ZVS

The coefficient determines how hard the switching event is for this leg. Zeroing out the coefficient indicates that the turn-off current in this leg is sufficient to fully realize ZVS. However, when the coefficient is 1, the switching event is fully hard and the controller must apply full compensation effort to D1 and D2 values. The system designer chooses the desired $I_{ZVS}$ after characterizing the system. Notably, $I_{ZVS}$ can differ for primary and secondary sides because $C_{OSS}$ varies.

Deployment of the proposed compensation measures significantly reduces current spikes in the grid and improves THD for the converter.

### 3.3.5 Frequency Modulation

As the trajectories show, in Section 3.3.3, ZVS realization is different in different loads, voltages, and modes. At light load in mode III, the controller has wide room between primary and secondary ZVS requirements, this means that there is a lot of current circulating in the system. By changing the frequency, the distance between the primary and secondary ZVS requirements can be narrowed and reduce the circulating current.

In grid sine waves with high peaks, a low load causes a lack of primary side ZVS. The load coefficient M is defined as the ratio of $I_{REF}$ to $I_N$. $I_N$ is dependent on $L_K$ and the switching frequency. The controller can increase switching frequency at light loads to increase relative load M by decreasing $I_N$.

The best switching frequency is defined by the frequency that achieves the desired distance Δ between primary and secondary ZVS requirements. This Δ is selected by the system designer following a thorough characterization of the system.

Derive the equations for the best switching frequency from Equation 4 and Equation 6. Equation 10 and Equation 11 are the final equations.

$$F_{SW,\,III} = \frac{N \times V_{DC} \times \left(\frac{m}{2} - 2{*}\Delta\right)^2 \times \left(1 - \frac{m}{2}\right)}{4 \times L_K \times |I_{REF}| \times m} \quad (10)$$

$$F_{SW,\,II} = \frac{N \times V_{DC} \times \left(8 \times \Delta^2 \times m^2 + 16 \times \Delta^2 \times m + 16 \times \Delta^2 - 8 \times \Delta \times m - 16 \times \Delta - m^2 + 4\right)}{16 \times L_K \times |I_{REF}| \times m^2} \quad (11)$$

An increase of $F_{SW}$ is because of an increase in the relative load M of the converter. The increased load in mode III of operation reduced the distance between the primary and secondary ZVS requirements but at the same time reduced the RMS current. In mode II the increase of $F_{SW}$ helps to have the minimum load required by the primary lagging arm to keep the current positive at the positive voltage pulse, thus achieving ZVS.

The trajectories clearly show that with heavy loads, the calculated switching frequency is low, limited by the $F_{SW_MIN}$ requirement. Conversely, when working under light loads, the frequency rises to maximum ($F_{SW_MAX}$) saturation mark. With moderate loads, however, the frequency exhibits significant variability and achieves ZVS over a broad range while maintaining circulation current at a low level.

### 3.3.6 Controller Block Diagram

Figure 3-16 shows the block diagram of the controller. The controller contains an MPPT block that produces a reference current amplitude. The amplitude is then multiplied by the sine output of the Stationary-Frame Orthogonal Generalized Integrator (SOGI) PLL block facilitating utilization in the cycloconverter control. The cycloconverter control has a feedforward block, dead-time compensation, PI and PR controllers. The final D1 and D2 values are then calculated to come to the modulator that generates corresponding PWM signals.



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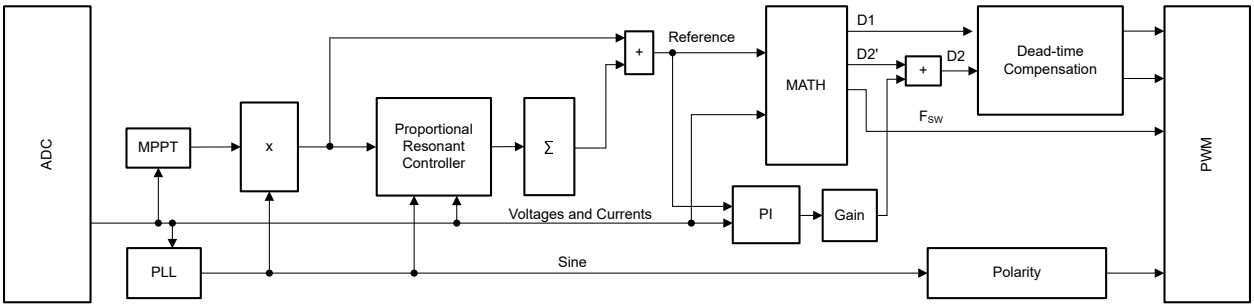



**Figure 3-16. Controller Block Diagram**

The modulator uses four ePWM channels in the C2000 MCU in up and down counting mode. Figure 3-17 shows the waveform generation timing diagram.

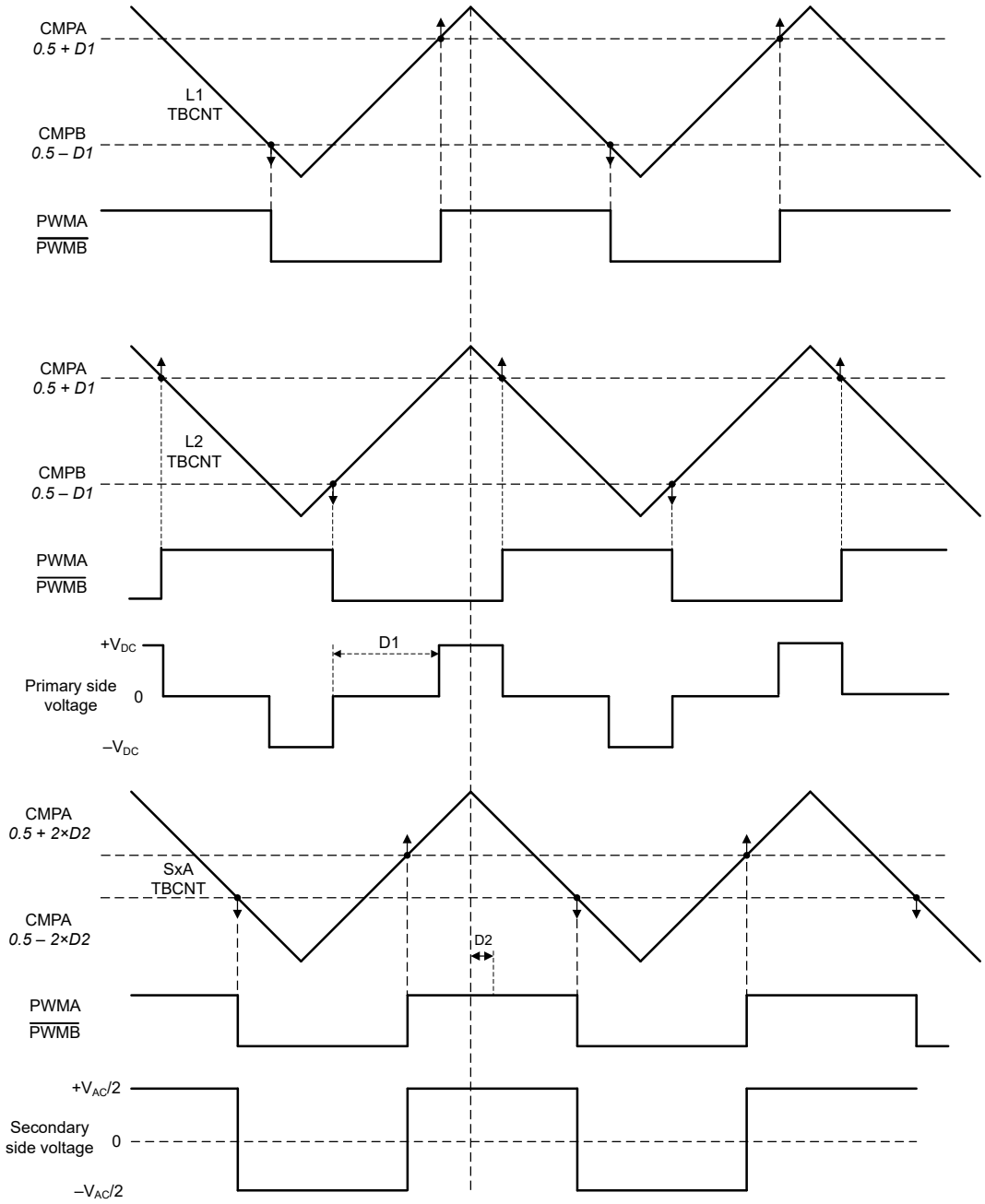



**Figure 3-17. PWM Timing Diagram**



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### 3.4 MPPT and Input Voltage Ripple

Single phase power applications have significant power ripple. The frequency of this ripple is twice the grid frequency

Equation 12 shows the average power transferred to grid.

$$P_{AVG} = V_{RMS} \times I_{RMS} \times \cos(\varphi) \quad (12)$$

Equation 13 calculates the voltage in the grid following the sine law.

$$V(t) = \sqrt{2} \times V_{RMS} \times \sin(\omega t) \quad (13)$$

When power factor equals 1, the current in the grid is following the sine wave too, see Equation 14.

$$I(t) = \sqrt{2} \times I_{RMS} \times \sin(\omega t) \quad (14)$$

Equation 15 is the equation for instantaneous power for a single-phase system.

$$P(t) = 2 \times V_{RMS} \times I_{RMS} \times \sin^2(\omega t) = V_{RMS} \times I_{RMS} \times (1 + \cos(2 \times \omega t)) \quad (15)$$

Equation 15 reveals that the instantaneous power consists of a constant part, which represents the average power, and an alternating part possessing twice the grid frequency, characterized as power ripple. This equation also shows that the instantaneous power exhibits variations ranging from zero up to double the average power.

In traditional two-stage inverter approaches, such as LLC plus totem pole configurations, the power ripple is typically managed by the DC-Link capacitors located within the high-voltage DC-AC stage. These DC-Link capacitors can effectively handle voltage ripples of 20% or higher. By contrast, the low-voltage to high-voltage LLC stage is generally designed with a focus on maximum average power capability.

In the single-stage approach, there is no DC-Link capacitor to handle the power ripple, so the converter must be designed to transfer both average power and power ripple to the AC side.

The input of the inverter comes from a PV panel that can be considered as a current source. The power output of this source depends on several factors, including irradiation received by the panel, panel voltage, panel temperature, and so forth.

This indicates that the input capacitors serve as intermediate energy storage elements within each grid cycle. As a result, the input voltage of the converter experiences some ripple, which is directly reflected onto the operating voltage of the PV panel.

Figure 3-18 illustrates the P-V curve of a typical solar panel, demonstrating the relationship between the output of the panel and various parameters. As conditions affecting the PV panel change throughout the day, the power output also varies continuously.

The input power to the inverter remains relatively constant around the Maximum Power Point (MPP), while the output power exhibits a ripple due to these changing conditions. This causes the input voltage of the converter to experience some ripple, which is directly reflected onto the operating voltage of the PV panel. The I-V curve, shown alongside the P-V curve, shows the relationship between the output current of the panel and the output voltage. The intermediate energy storage elements within each grid cycle, provided by the input capacitors, serve to mitigate this ripple effect on the operation of the converter.



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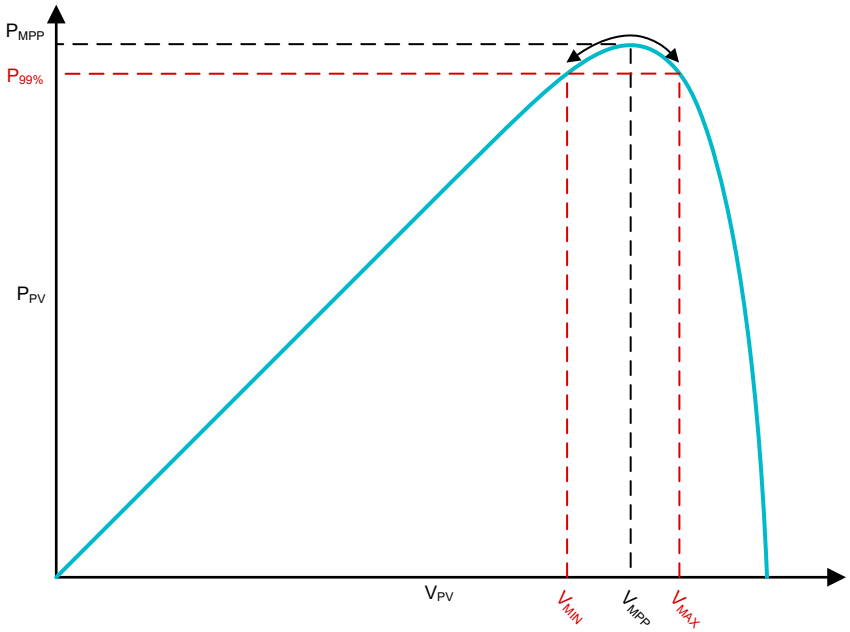



**Figure 3-18. Input Voltage Ripple on P-V Curve**

As Figure 3-18 shows, any change of the panel voltage from VMPP lowers the power delivered from the panel and lowers the overall output power. Fortunately, across the MPP voltage the variation of the output power is relatively low. To understand the required input capacitance, define the maximum deviation across the power point. This parameter needs to be properly selected, because a deviation that is too low can cause excessive size and cost for capacitors A deviation that is too high can cause the PV panel to operate at an unfavorable point. Typically, the designer selects 99% of the MPPT efficiency as a starting point.

The minimum required capacitance can be calculated with Equation 16.

$$C \geq \frac{P_{IN}}{2 \times \pi \times V_{IN} \times f_{AC} \times V_{RIPPLE}} \tag{16}$$

where

- $P_{IN}$ is the PV panel maximum power
- $V_{IN}$ is the PV panel voltage at MPP
- $f_{AC}$ is the line frequency
- $V_{RIPPLE}$ is the desired voltage ripple

The conclusion:

- The converter needs to be designed to handle instantaneous power two times higher than average
- The energy storage for this ripple is input capacitors
- The value of the input capacitor needs to be selected to handle maximum voltage ripple required by MPPT



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# 4 Hardware, Testing Requirements, and Test Results

## 4.1 Hardware Requirements

The hardware for this reference design is composed of the following:

- TIDA-010954
- TMDSCNCD28P55X control card
- USB Type-C® cable
- USB isolator
- Power adapter with 5V output
- Laptop
- Four-channel oscilloscope
- Current probe
- Rogowski coil
- Two high-voltage differential probes rated with a voltage higher than 400V

The following equipment is used to power and evaluate the DUT:

- DC power source Elektro-Automatik EA-PS 3080-20C
- AC power source Chroma 61611
- DC load Chroma 63208A
- AC load
- Power analyzer Tektronix PA-4000

## 4.2 Software Requirements

- Download and install *DigitalPower_SDK_5_03_00_00* from ti.com. This is the tested version but the latest version should work as well. C:\ti\c2000\C2000Ware_DigitalPower_SDK_5_03_00_00
- Download the latest TIDA-010954 FW from ti.com and then copy and paste the project folder into the SDK path under the *solutions* folder

  C:\ti\c2000\C2000Ware_DigitalPower_SDK_5_03_00_00\solutions\tida_010954
- Install CCS Version: 12.8.1.00005 if not already. Compiler version tested is TI v22.6.3.LTS. Version 22.6.2 (not validated yet but is recommended by the C2K team to fix some of the compiler warnings from v22.6.3). Check compiler version by right click on project then properties->general menu. If needed install the right compiler and have it discoverable by CCS
- From CCS import the project into workspace

Make sure that the following #define are used in *cyclo_settings.h* for proper scaling

```
#define I_PRI_SCALE ((float32_t)(ADC_V_SCALE / 0.025f))    //  25mV/A
#define I_SEC_SCALE ((float32_t)(ADC_V_SCALE / 0.075f))    //  75mV/A
#define I_AC_SCALE  ((float32_t)(0.5f * ADC_V_SCALE / 0.164f))    // 150mV/A -> 164mV/A (per 1A you
have 4mV*41V/V = 164mV/A)
#define I_DC_SCALE  ((float32_t)(0.5f * ADC_V_SCALE / 0.05f))          // 1mOhm * 50 times = 20 A/V
or 50mV/A
#define V_DC_SCALE  ((float32_t)(ADC_V_SCALE * 105.11f / 5.11f) * 0.95f) // Divider 100 / 5.11 kOhm
and 0.3 / 30KOhm
#define V_AC_SCALE  ((float32_t)(ADC_V_SCALE * 3006u / 12u / 2u)) // Divider 2994 / 12 kOhm

#define cyclo_N ((float32_t)3.5f)
#define cyclo_LK_DEF ((float32_t)4.0e-6f)
```

Depending on which lab you're testing, set the lab number in cyclo_settings.h. For example if I'm testing lab 1:

```
#define CYCLO_LAB (1)
```

Make the following edit to *cyclo_board_revision_init* in *cyclo_dcac.c*:

```
float32_t cyclo_Lk = cyclo_LK_DEF;

void cyclo_board_revision_init() { // }
```


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Right-click on the project name and click *Rebuild Project*. Confirm that the project builds successfully. To load the project, first make sure in the Project Explorer the correct target configuration file is *set as Active under targetConfigs (*.ccxml file).*

Then, click *Run* → *Debug* to launch a debugging session. The project will then load on the device and the CCS debug view will become active. The code will halt at the start of the main routine. Click *Run* → Resume to run the program.

To populate this window with the correct variables, click View → Expressions. Then right click on the Expressions tab on CCS and select Remove All. This will clear the Expressions window. Now right click again on the cleared Expressions window and select Import. Then browse to the project folder (solutions --> tida-010954 --> source --> debug) and select lab1.txt. This will populate the watch window with the appropriate variables needed to debug the system. Enable Continuous Refresh button on the watch window to enable continuous update of values from the control. Repeat this process each lab number. For more information, scroll down to the Test Setup section.

### 4.3 Test Setup

The recommended sequence of tests follow:

- Test of the board switches and measurement functionality (Lab 1 and 2)
- Test of DC/DC operation with low voltage and open loop (Lab 3 and 4)
- Test of DC/DC operation with low voltage and closed loop (Lab 5)
- Test of DC/DC operation with high voltage and closed loop (Lab 5)
- Test of DC/AC operation with low voltage (Lab 6, 7, 8)
- Test of DC/AC operation with high voltage (Lab 6, 7, 8)
- Test of AC/DC reverse charge operation with high voltage (lab 8)
- Test of PV to AC operation with high voltage (Lab 8, 9)
- Test of DC/AC offgrid mode operation with high voltage (lab 10)



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### 4.3.1 Board Check

Figure 4-1 shows the board connections.

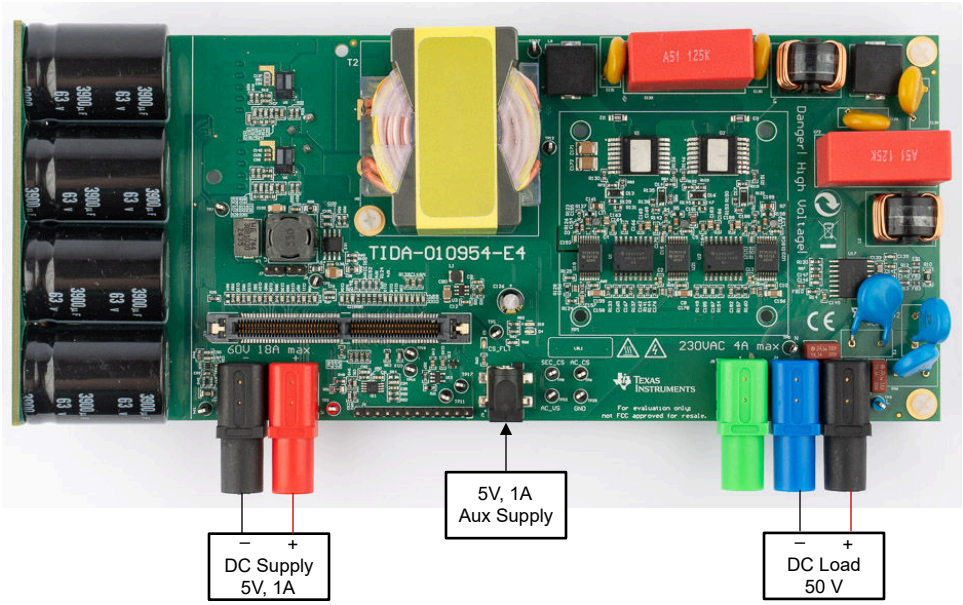



**Figure 4-1. Board Connections for Low-Voltage Tests**

The test sequence follows:

1. Connect the negative terminal of the differential probe to TP13 and the positive terminal to TP10. Connect the second differential probe to TP27 and TP12, respectively. Connect the Rogowski coil around transformer T1 secondary side wire
2. Set `CYCLO_LAB` define in `cinv_settings.h` to 1
3. Build and download firmware to the controller and run
4. Import the `<DPSDK>\solutions\tida_010954\source\debug\lab1.txt` file to the expressions view
5. Set following variables `cyclo_iref_g` = 0.0, `cyclo_d1` = 0.47, `cyclo_d2` = 0.0
6. Set `cyclo_run` = 1, observe that `cyclo_started` become 1
7. Observe the oscilloscope waveforms. The primary side needs to have clean, 3 level waveforms with narrow positive and negative pulses. The secondary side needs to have 2 level waveforms, the current needs to have triangular waveforms


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### 4.3.2 DC-DC Tests

Figure 4-2 shows the board connections.

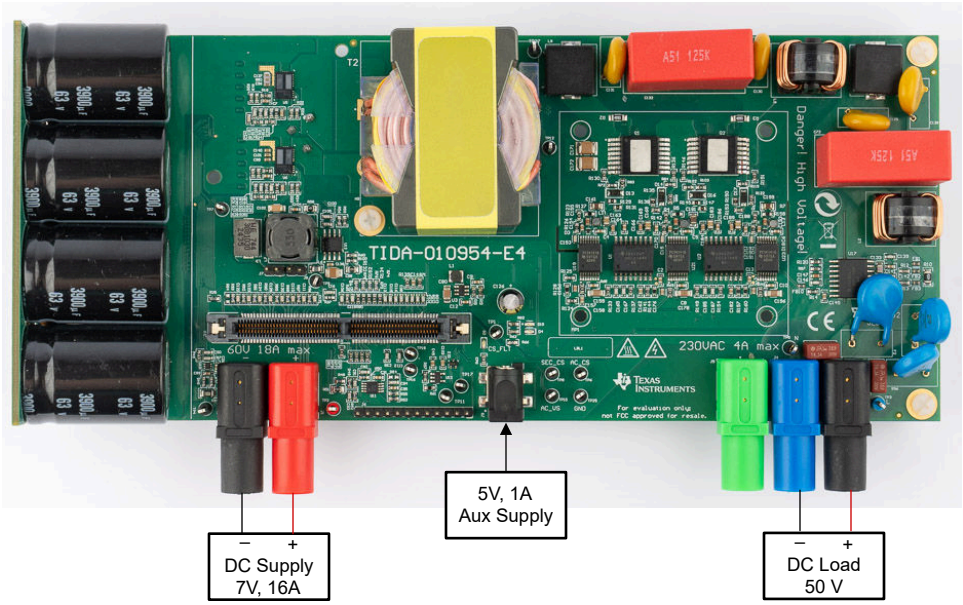



**Figure 4-2. Board Connections for DC-DC Tests**

The test sequence for lab 3 follows:

1. Connect the negative terminal of the differential probe to TP13 and the positive terminal to TP10.
2. Connect the second differential probe to TP27 and TP12, respectively.
3. Connect the Rogowski coil around the transformer T1 secondary side wire.
4. Connect the current probe to the wire going to DC load.
5. Set `CYCLO_LAB` define in `cinv_settings.h` to 3.
6. Configure the DC source to 7V with 10A limit, and DC load to 50V in constant voltage mode
7. Build and download firmware to the controller and run.
8. Import `<DPSDK>\solutions\tida_010954\source\debug\lab3.txt` file to expressions view.
9. Set the following variables `cyclo_iref_g` = 0.0, `cyclo_polarity` = 1, `cyclo_d1` = 0.47, `cyclo_d2` = 0.0.
10. Set `cyclo_run` = 1, observe that `cyclo_started` becomes 1.
11. In 0.05 steps, decrease `cyclo_d1` to 0.25, observe that the primary side voltage pulse becomes wider.
12. Make sure the DC power source current limit still has enough margin before applying change.
13. In 0.02 steps, change `cyclo_d2` to 0.1, observe that the center primary side pulse becomes the leading secondary pulse center. The output current increased. The input current increased too.
14. Observe measurements in variables `cyclo_v_dc_V`, `cyclo_v_ac_V`, `cyclo_i_dc_A`, and `cyclo_i_ac_A`

The test sequence for lab 4 follows:

1. Connect the negative terminal of differential probe to TP13 and the positive terminal to TP10.
2. Connect the second differential probe to TP27 and TP12, respectively.
3. Connect the Rogowski coil around transformer T1 secondary side wire.
4. Connect current probe to wire going to DC load.
5. Set `CYCLO_LAB` define in `cinv_settings.h` to 4.
6. Configure DC source to 7V with 10A limit, and DC load to 50V in constant voltage mode.
7. Build and download firmware to the controller and run.
8. Import the `<DPSDK>\solutions\tida_010954\source\debug\lab4.txt` file to expressions view.
9. Set the following variables `cyclo_iref_g` = 0.0, `cyclo_polarity` = 1.
10. Set `cyclo_run` = 1, observe that `cyclo_started` becomes 1.
11. Change `cyclo_iref_g` = 0.0 to 0.5A with 0.1 steps.
12. Observe that the output current changed corresponding to the reference setting with some calculation error.



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The test sequence for lab 5 follows:

1. Connect the negative terminal of the differential probe to TP13 and the positive terminal to TP10.
2. Connect the second differential probe to TP27 and TP12, respectively.
3. Connect the Rogowski coil around transformer T1 secondary side wire.
4. Connect the current probe to the wire going to DC load.
5. Set `CYCLO_LAB` define in `cinv_settings.h` to 5.
6. Configure the DC source to 7V with 10A limit, and the DC load to 50V in constant voltage mode.
7. Build and download firmware to the controller and run.
8. Import the `<DPSDK>\solutions\tida_010954\source\debug\lab5.txt` file to expressions view.
9. Set the following variables `cyclo_iref_g` = 0.0, `cyclo_polarity` = 1, `cyclo_pi_enabled` = 1.
10. Set `cyclo_run` = 1, observe that `cyclo_started` becomes 1.
11. Change `cyclo_iref_g` = 0.0 to 0.5A with 0.1 steps.
12. Observe that the output current changed corresponding to the setting with error compensation with the PI controller.

Check the DC-DC negative polarity operation by swapping polarity on the AC side (eload polarity swap) and repeating all the steps with `cyclo_polarity` = –1 and positive `cyclo_iref_g`. This is still pushing power from primary side to secondary side. An easier test load would be a power resistor since it is an AC load and there is no need to switch the connection polarity.

Check the DC-DC operation with backward current flow by connecting the DC load (7V) on the DC side and the DC source (50V) on the AC side and doing negative `cyclo_d2` or negative `cyclo_iref_g`. For this test, TI recommends setting `cyclo_polarity` = –1 and use `cyclo_d2` or negative `cyclo_iref_g` to push power in reverse while keeping the power supply and eload polarity the same.

Check high-voltage operation by slowly increasing the voltage on the DC side up to 40V and the secondary side voltage up to 325V.

**Note**

For DC to AC labs, the user does not need to manually set `cyclo_polarity`the for either forward or reverse power flow. The user will only need to set the `cyclo_iref_g` +/- sign and magnitude value.

### *4.3.3 DC-AC Tests*

Figure 4-3 shows the board connections for DC-AC tests. If the AC source does not allow backward current flow, connect power resistors in parallel to AC lines.


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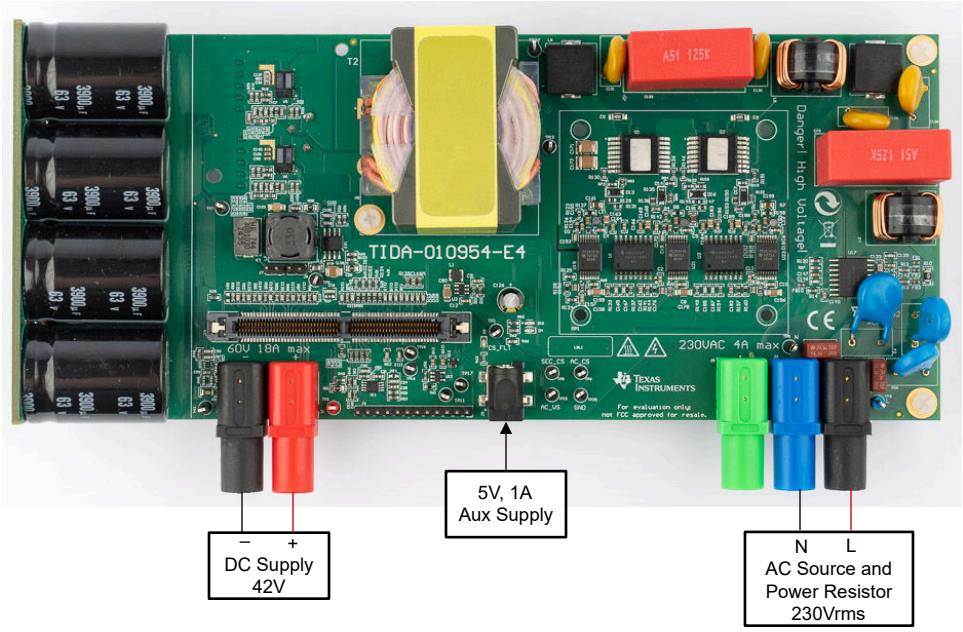



**Figure 4-3. Board Connections for DC-AC Tests**

The test sequence for lab 6 follows:

1. Connect the differential probe to AC connectors, J4 and J2.
2. Connect the second differential probe to TP27 and TP12, respectively.
3. Connect the Rogowski coil around transformer T1 secondary side wire.
4. Connect the current probe to the wire going to the AC line.
5. Set `CYCLO_LAB` define in `cinv_settings.h` to 6.
6. Configure the DC source to 40V with 16A limit in parallel with the DC load settled to 42V in constant voltage mode (DC load only needed if testing in reverse power flow).
7. Configure the AC source to $25V_{AC}$ with 5A limit.
8. Connect the resistors in parallel, if needed.
9. Build and download firmware to controller and run.
10. Import `<DPSDK>\solutions\tida_010954\source\debug\lab6.txt` file to expressions view.
11. Set the following variables `cyclo_iref_g` = 0.2.
12. Set `cyclo_run` = 1, observe that `cyclo_started` becomes 1, `cyclo_polarity` is changing the sign.
13. Change `cyclo_iref_g` = 0.5A with 0.1 steps.
14. Observe the AC voltage and current waveforms. On high output voltage, current spikes can be observed due to the mode change.

The test sequence for lab 7 follows:

1. Connect the differential probe to AC connectors J4 and J2.
2. Connect the second differential probe to TP27 and TP12, respectively.
3. Connect the Rogowski coil around transformer T1 secondary side wire.
4. Connect the current probe to the wire going to the AC line.
5. Set `CYCLO_LAB` define in `cinv_settings.h` to 7.
6. Configure the DC source to 40V with a 16A limit in parallel with the DC load settled to 42V in constant voltage mode.
7. Configure the AC source to $25V_{AC}$ with 5A limit.
8. Connect the resistors in parallel, if needed.
9. Build and download the firmware to the controller and run.
10. Import the `<DPSDK>\solutions\tida_010954\source\debug\lab7.txt` file to expressions view.
11. Set the following variables `cyclo_iref_g` = 0.2, `cyclo_pi_enabled` = 1, `cyclo_dt_comp_enabled` = 1
12. Set `cyclo_run` = 1, observe that `cyclo_started` becomes 1, `cyclo_polarity` is changing the sign.
13. Change `cyclo_iref_g` to 3.6A with 0.1 steps.



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14. Observe the AC voltage and current waveforms. On high output voltage, current spikes is significantly lower, but THD is still high.

The test sequence for lab 8 follows:

1. Connect the differential probe to the AC connectors, J4 and J2.
2. Connect the second differential probe to TP27 and TP12, respectively.
3. Connect the Rogowski coil around the transformer T1 secondary side wire.
4. Connect the current probe to the wire going to the AC line.
5. Set `CYCLO_LAB` define in `cinv_settings.h` to 8.
6. Configure the DC source to 40V with a 16A limit in parallel with the DC load settled to 42V in the constant voltage mode.
7. Configure the AC source to $25V_{AC}$ with a 5A limit.
8. Connect the resistors in parallel, if needed.
9. Build and download the firmware to the controller and run.
10. Import the `<DPSDK>\solutions\tida_010954\source\debug\lab8.txt` file to the expressions view.
11. Set the following variables `cyclo_iref_g` = 0.2, `cyclo_pi_enabled` = 1, `cyclo_dt_comp_enabled` = 1, `cyclo_pr_enabled` = 1.
12. Set `cyclo_run` = 1, observe that `cyclo_started` becomes 1, `cyclo_polarity` is changing the sign.
13. Change `cyclo_iref_g` = 3.6A with 0.1 steps.
14. Observe AC voltage and current waveforms. THD is significantly reduced.

### *4.3.4 AC-DC Tests*

Figure 4-3 shows the board connections for AC-DC tests. Make sure the eload is in constant voltage mode and is turned on with enough current sink before pushing power from the AC grid to the DC side.

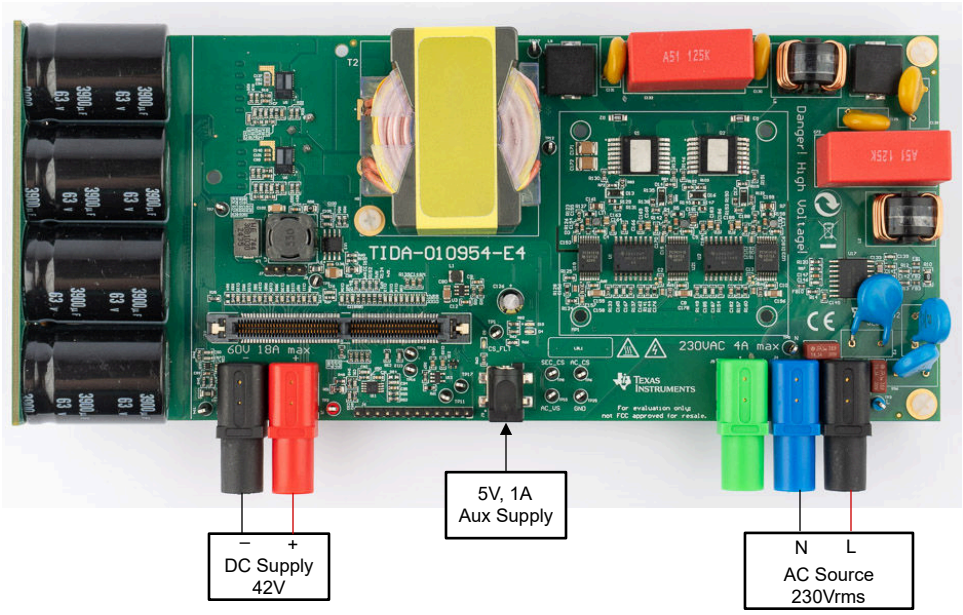



**Figure 4-4. Board Connections for DC-AC Tests**

The test sequence for lab 8 follows:

1. Connect the differential probe to the AC connectors, J4 and J2.
2. Connect the second differential probe to TP27 and TP12, respectively.
3. Connect the Rogowski coil around the transformer T1 secondary side wire.
4. Connect the current probe to the wire going to the AC line.
5. Set `CYCLO_LAB` define in `cinv_settings.h` to 8.
6. Configure the DC load to 42V in the constant voltage mode with max currrent sink around 16A.
7. Configure the AC source to $230V_{AC}$ with a 5A limit.
8. Build and download the firmware to the controller and run.


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9. Import the <DPSDK>\solutions\tida_010954\source\debug\lab8.txt file to the expressions view.
10. Set the following variables cyclo_iref_g = -0.2, cyclo_pi_enabled = 1, cyclo_dt_comp_enabled = 1, cyclo_pr_enabled = 1.
11. Set cyclo_run = 1, observe that cyclo_started becomes 1, cyclo_polarity is changing the sign.
12. Change cyclo_iref_g = -3.6A with -0.1 steps from the initial -0.2A.
13. Observe AC voltage and current waveforms.

### 4.3.5 DC-AC Offgrid Tests

Figure 4-3 shows the board connections for DC-AC offgrid tests. The power load must be able to handle AC current. Do not use a DC eload for this test.

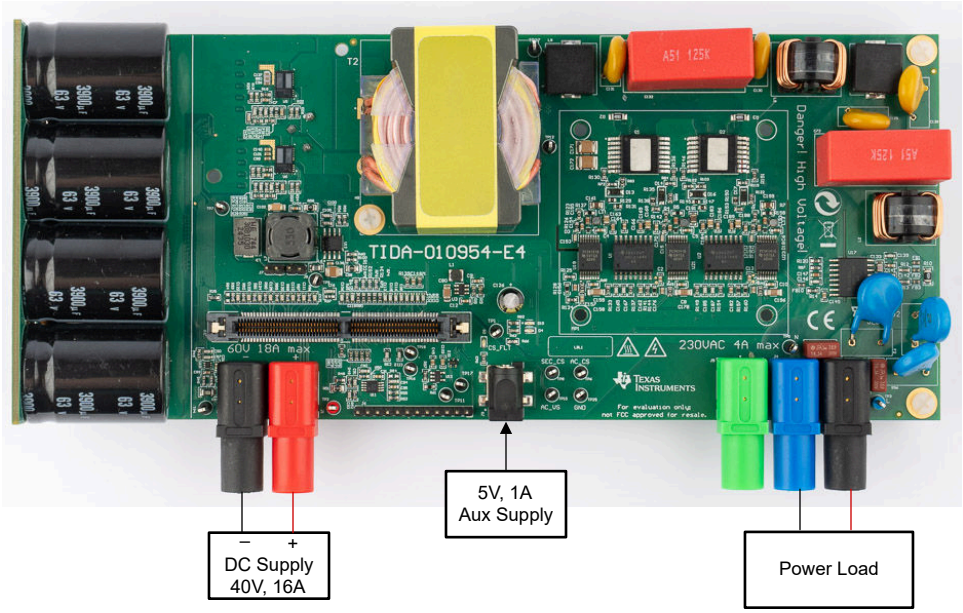



**Figure 4-5. Board Connections for DC-AC Offgrid Tests**

The test sequence for lab 10 follows:

1. Connect the differential probe to the AC connectors, J4 and J2.
2. Connect the second differential probe to TP27 and TP12, respectively.
3. Connect the Rogowski coil around the transformer T1 secondary side wire.
4. Connect the current probe to the wire going to the AC line.
5. Set CYCLO_LAB define in cinv_settings.h to 10.
6. Configure the DC supply to 40V with current limit.
7. Build and download the offgrid firmware to the controller and run.
8. Import the <DPSDK>\solutions\tida_010954\source\debug\lab8.txt file to the expressions view.
9. Set the following variables cyclo_vref_g = 35, cyclo_pi_enabled = 1, cyclo_dt_comp_enabled = 1, cyclo_pr_enabled = 1.
10. Set cyclo_run = 1, observe that cyclo_started becomes 1, cyclo_polarity is changing the sign.
11. Change cyclo_vref_g = 325V with 50V steps from the initial 35V.
12. Observe AC voltage and current waveforms.



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## 4.4 Test Results

### *4.4.1 Efficiency and iTHD*

The following section highlights the both the efficiency and iTHD (current total harmonic distortion) performance for both ongrid and offgrid operations. For ongrid, the converter operates in both DC to AC and AC to DC modes. For offgrid, the converter operates in DC to AC mode. Note that the x-axis shows the load percentage of fullscale (FS) output power. For lower input VDC voltages, such as 33V, the FS output power is lowered from 600W to 400W.

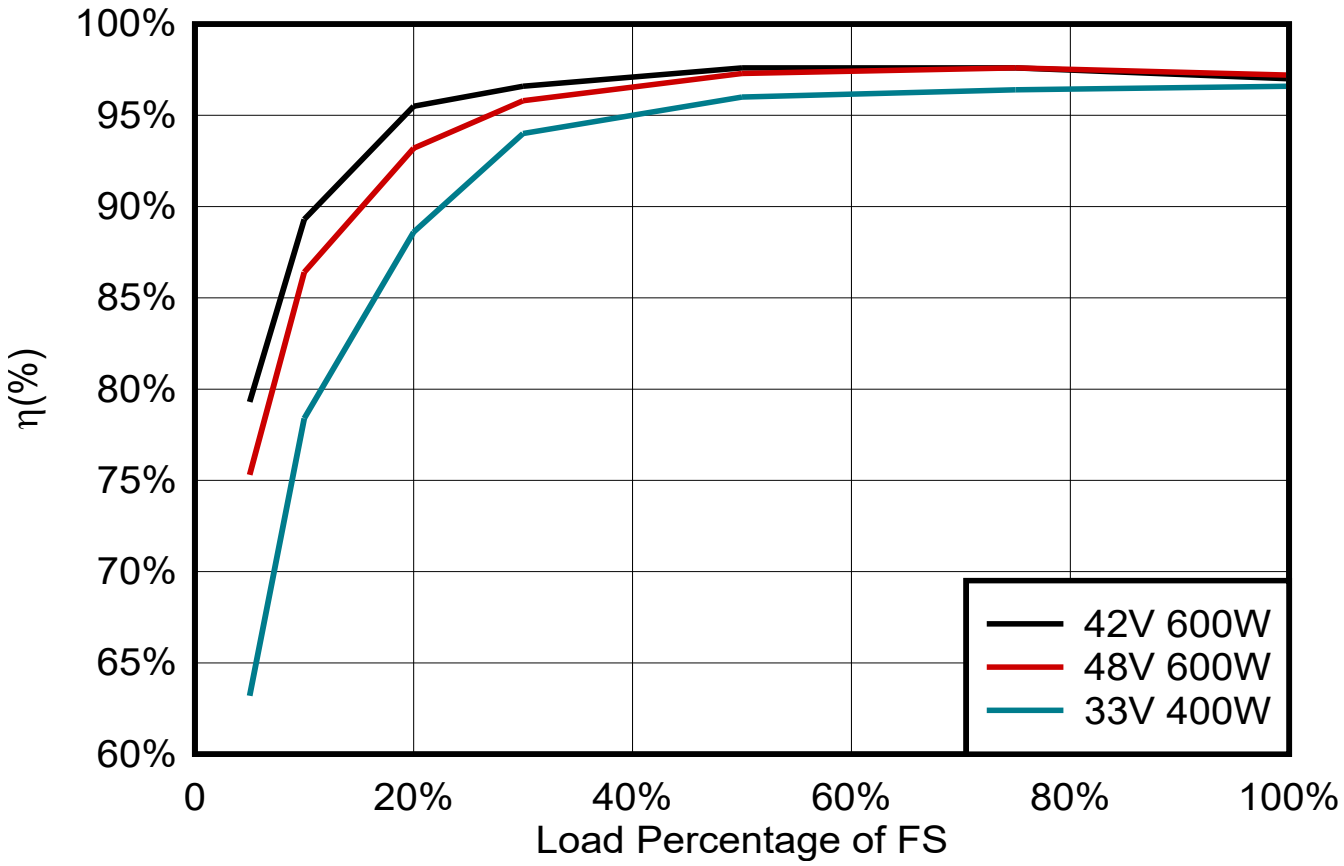



**Figure 4-6. DC-AC Ongrid Efficiency**

**Table 4-1. DC-AC Ongrid Efficiency**

| Power, % FS | 42V 600W | 48V 600W | 33V 400W |
|---|---|---|---|
| 5% | 79.3% | 75.3% | 63.2% |
| 10% | 89.3% | 86.4% | 78.4% |
| 20% | 95.5% | 93.2% | 88.6% |
| 30% | 96.6% | 95.8% | 94.0% |
| 50% | 97.6% | 97.3% | 96.0% |
| 75% | 97.6% | 97.6% | 96.4% |
| 100.0% | 97.0% | 97.2% | 96.6% |
| **Euro Eff** | 96.1% | 95.3% | 92.9% |
| **CEC Eff** | 97.0% | 96.6% | 94.9% |


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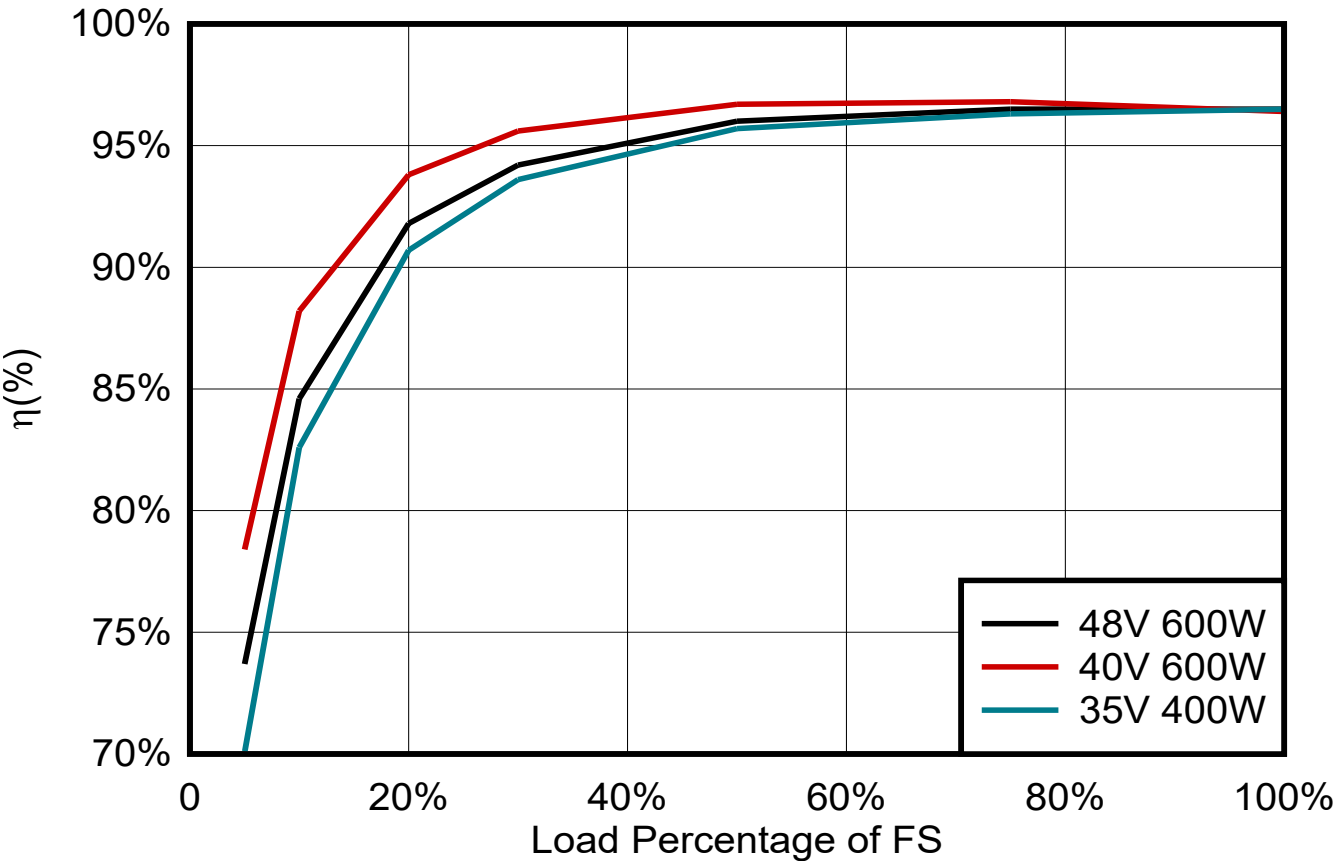



**Figure 4-7. AC-DC Ongrid Efficiency**

**Table 4-2. AC-DC Ongrid Efficiency**

| Power, % FS | 48V 600W | 40V 600W | 35V 400W |
|---|---|---|---|
| 5% | 73.7% | 78.4% | 70.1% |
| 10% | 84.6% | 88.2% | 82.6% |
| 20% | 91.8% | 93.8% | 90.7% |
| 30% | 94.2% | 95.6% | 93.6% |
| 50% | 96.0% | 96.7% | 95.7% |
| 75% | 96.5% | 96.8% | 96.3% |
| 100.0% | 96.5% | 96.4% | 96.5% |
| **Euro Eff** | 94.0% | 95.1% | 93.4% |
| **CEC Eff** | 95.4% | 96.1% | 95.0% |



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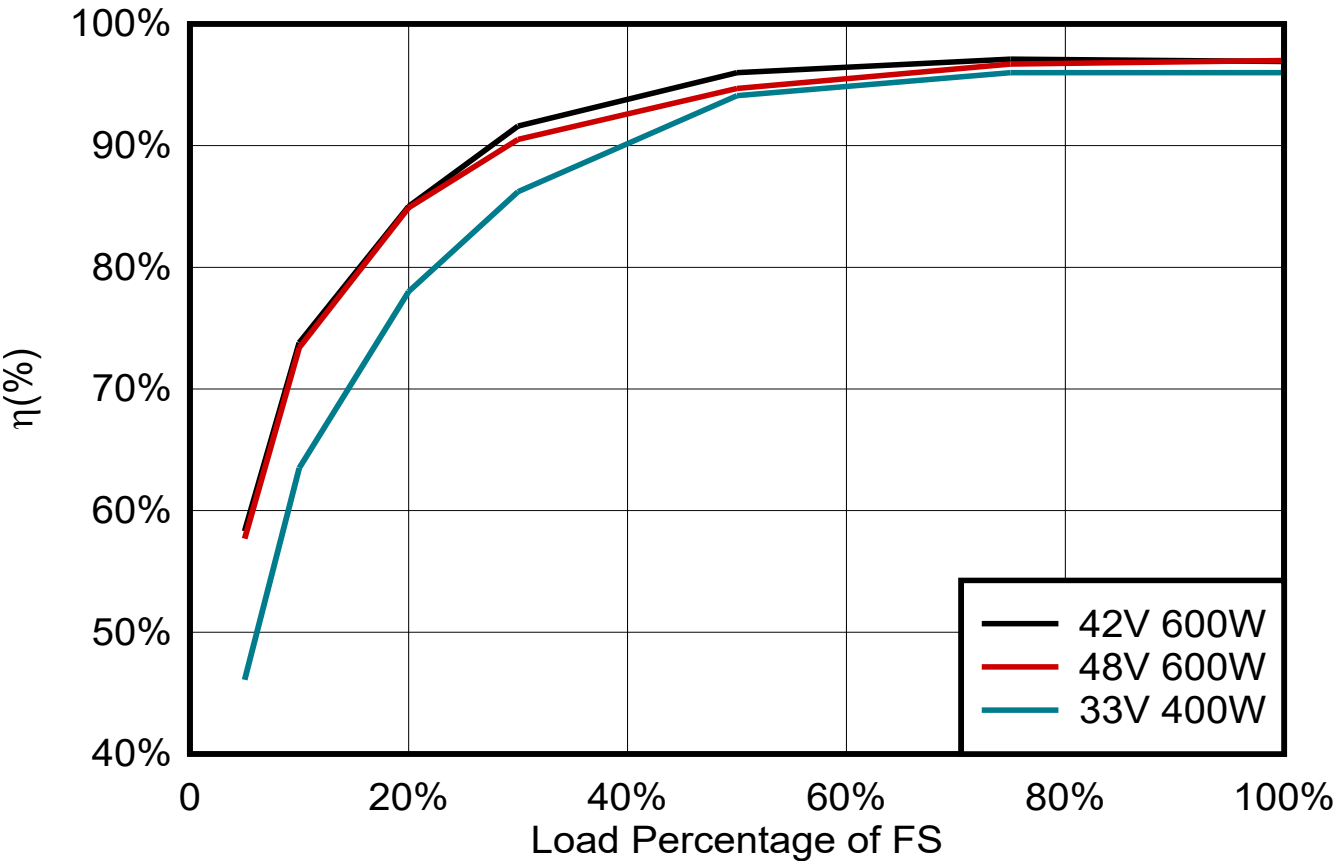



**Figure 4-8. DC-AC Offgrid Efficiency**

**Table 4-3. DC-AC Offgrid Efficiency**

| Power, % FS | 42V 600W | 48V 600W | 33V 400W |
|---|---|---|---|
| 5% | 58.3% | 57.7% | 46.1% |
| 10% | 73.8% | 73.4% | 63.5% |
| 20% | 85.0% | 84.9% | 78.0% |
| 30% | 91.6% | 90.5% | 86.2% |
| 50% | 96.0% | 94.7% | 94.1% |
| 75% | 97.1% | 96.7% | 96.0% |
| 100.0% | 96.9% | 97.0% | 96.0% |
| **Euro Eff** | 91.8% | 91.1% | 88.3% |
| **CEC Eff** | 94.7% | 94.0% | 92.2% |


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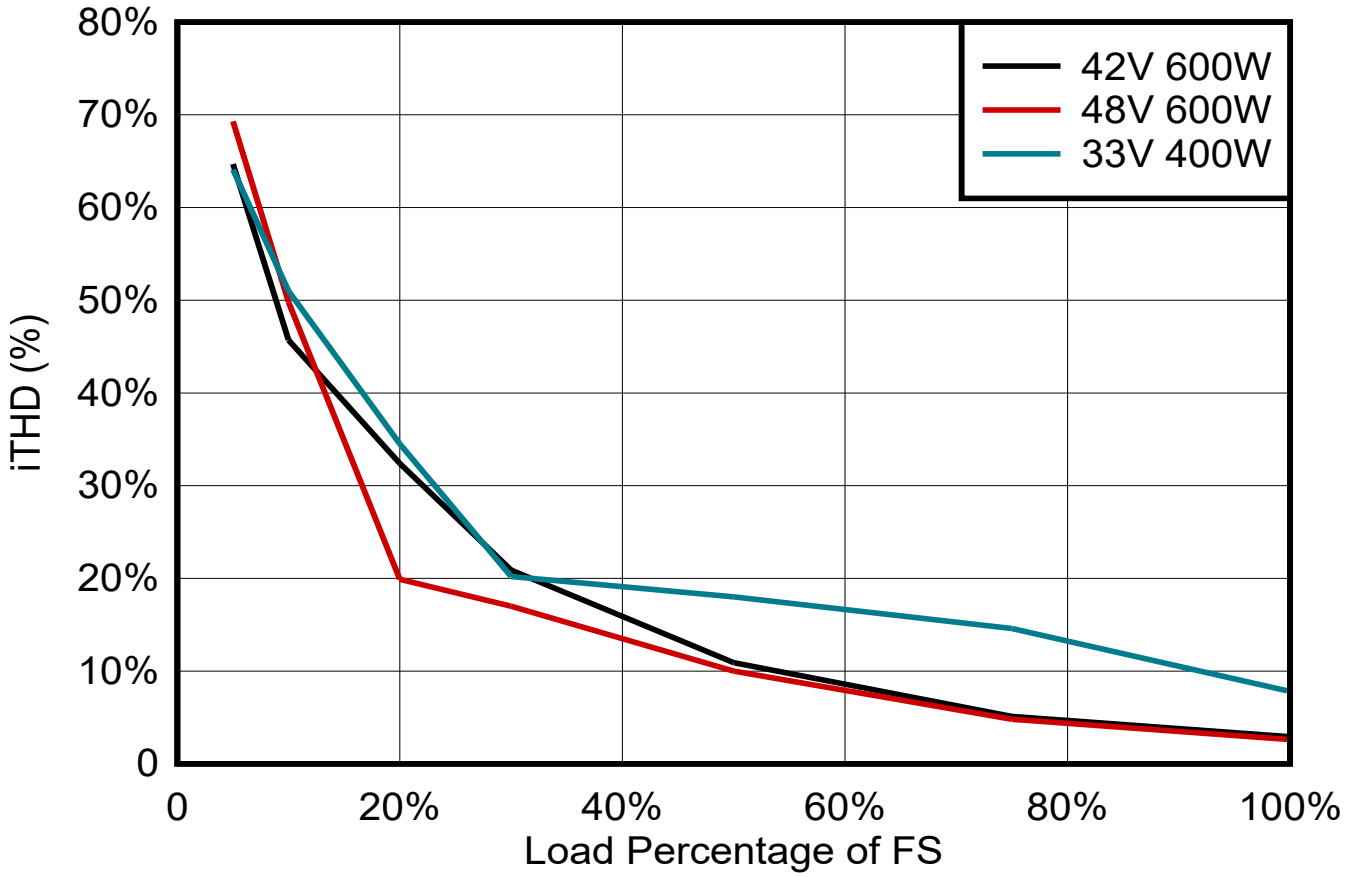



**Figure 4-9. DC-AC Ongrid iTHD**

**Table 4-4. DC-AC Ongrid iTHD**

| Power, % FS | 42V 600W | 48V 600W | 33V 400W |
|---|---|---|---|
| 5% | 64.7% | 69.3% | 64.1% |
| 10% | 45.7% | 49.8% | 51.0% |
| 20% | 32.4% | 19.9% | 34.5% |
| 30% | 20.9% | 17.0% | 20.2% |
| 50% | 10.9% | 10.0% | 18.0% |
| 75% | 5.1% | 4.8% | 14.6% |
| 100.0% | 2.9% | 2.6% | 7.8% |



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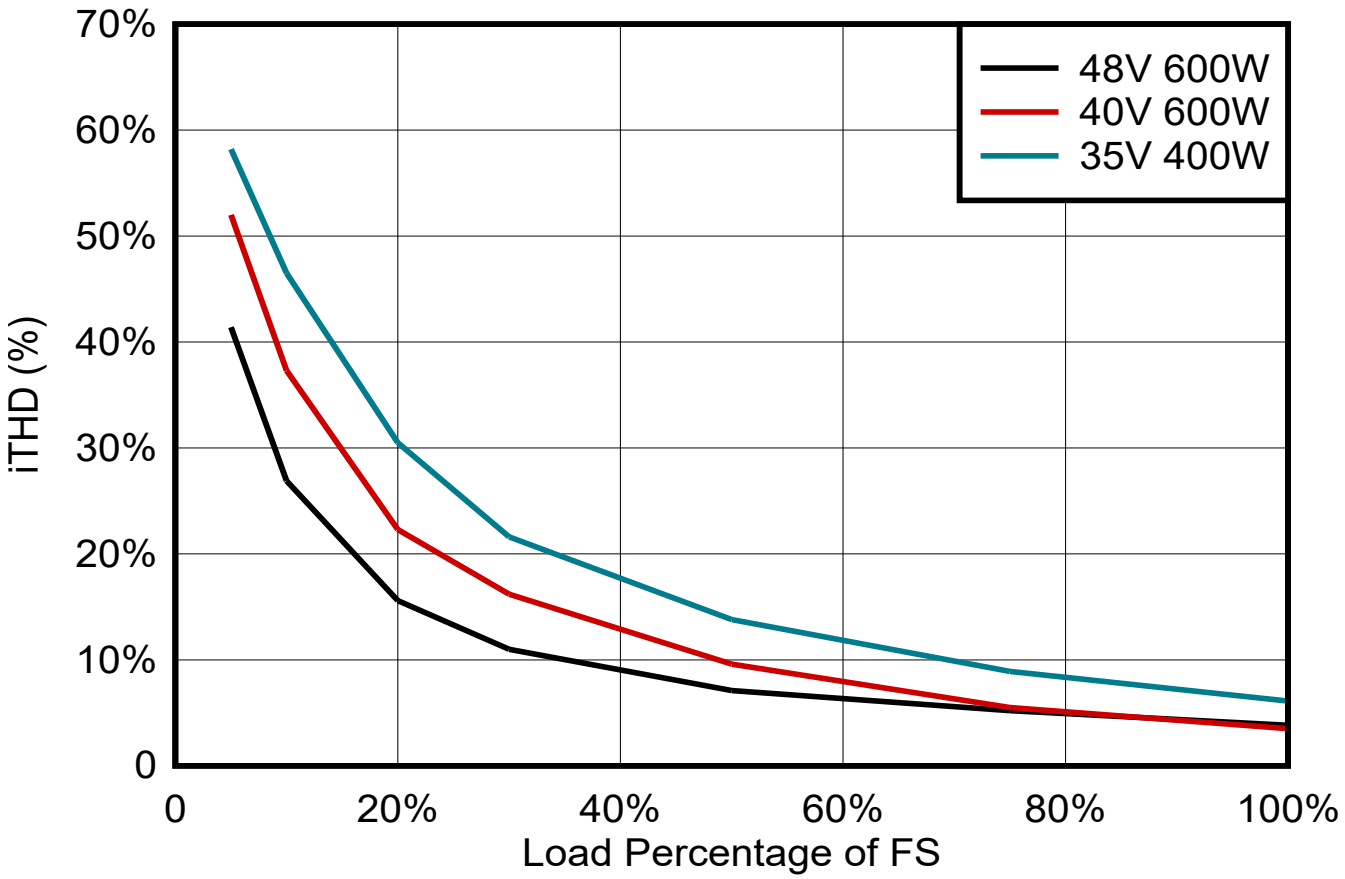



**Figure 4-10. AC-DC Ongrid iTHD**

**Table 4-5. AC-DC Ongrid iTHD**

| Power, % FS | 48V 600W | 40V 600W | 35V 400W |
|---|---|---|---|
| 5% | 41.4% | 52.0% | 58.2% |
| 10% | 26.9% | 37.3% | 46.5% |
| 20% | 15.6% | 22.3% | 30.5% |
| 30% | 11.0% | 16.2% | 21.6% |
| 50% | 7.1% | 9.6% | 13.8% |
| 75% | 5.2% | 5.5% | 8.9% |
| 100.0% | 3.8% | 3.5% | 6.1% |


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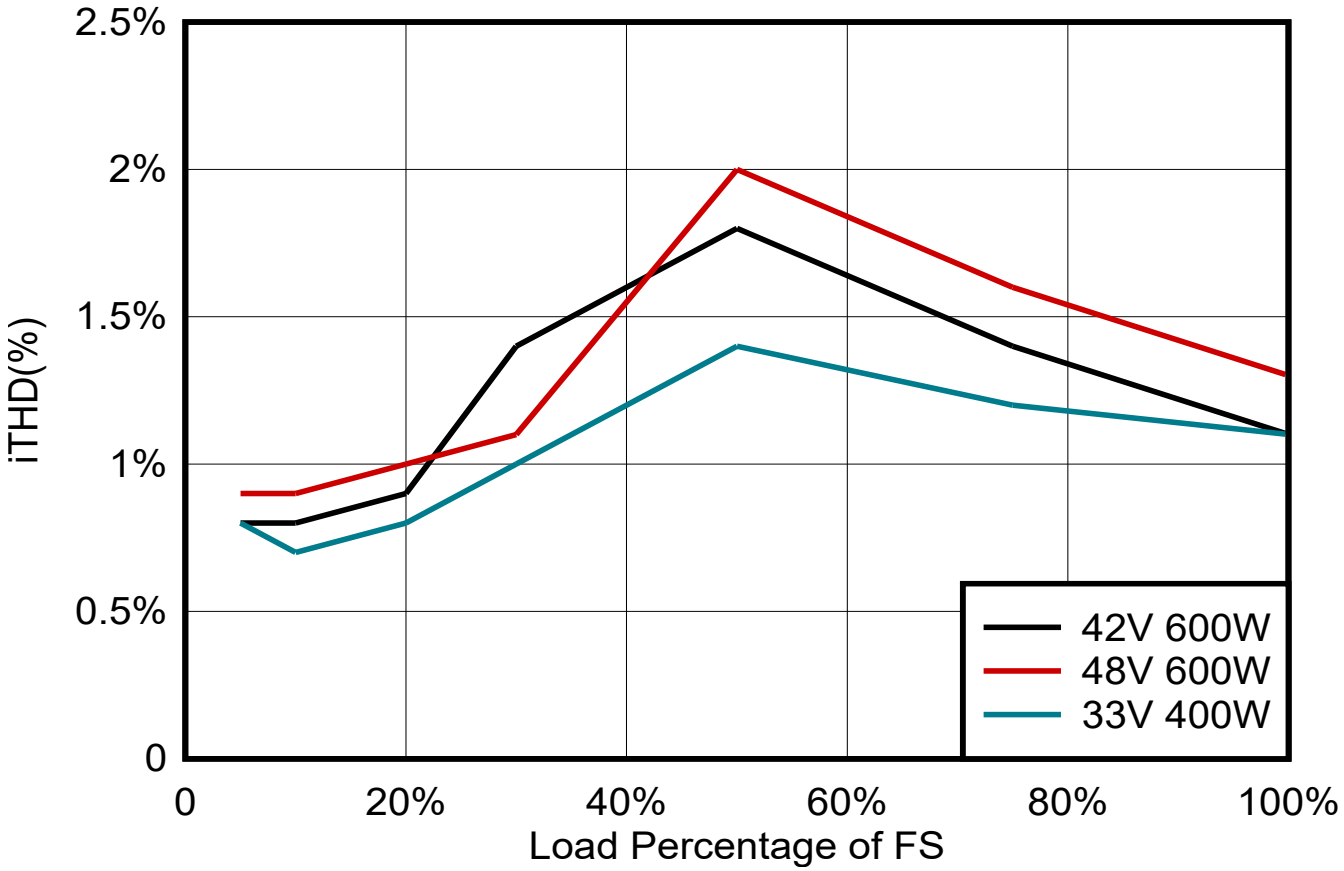



**Figure 4-11. DC-AC Offgrid iTHD**

**Table 4-6. DC-AC Offgrid iTHD**

| Power, % FS | 42V 600W | 48V 600W | 33V 400W |
|---|---|---|---|
| 5% | 0.8% | 0.9% | 0.8% |
| 10% | 0.8% | 0.9% | 0.7% |
| 20% | 0.9% | 1.0% | 0.8% |
| 30% | 1.4% | 1.1% | 1.0% |
| 50% | 1.8% | 2.0% | 1.4% |
| 75% | 1.4% | 1.6% | 1.2% |
| 100.0% | 1.1% | 1.3% | 1.1% |

### *4.4.2 Operating Waveforms for Various Loads*

Figure 4-12 through Figure 4-16 show examples of the converter operating in both DC-AC and AC-DC ongrid modes. In these two examples, the converter is pushing the maximum rated output power of 600W.



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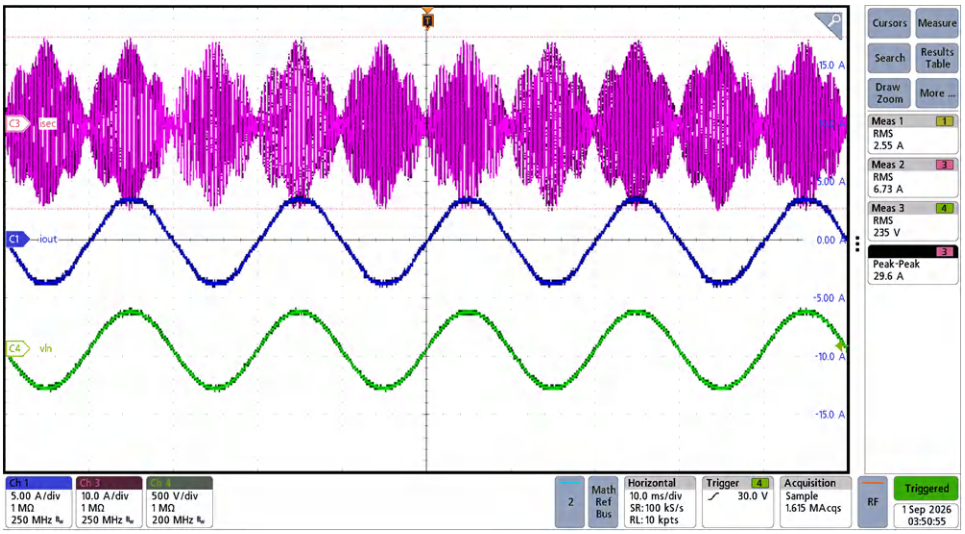



**Figure 4-12. DC-AC 42VDC to 230Vrms Ongrid 600W**

**Note**

Channel 1 - AC side output current Iout (blue). 2.55 Arms.

Channel 4 - AC output phase voltage Vln (green). 235 Vrms.

Channel 3 - Transformer secondary side current Isec (red). 6.73 Arms.

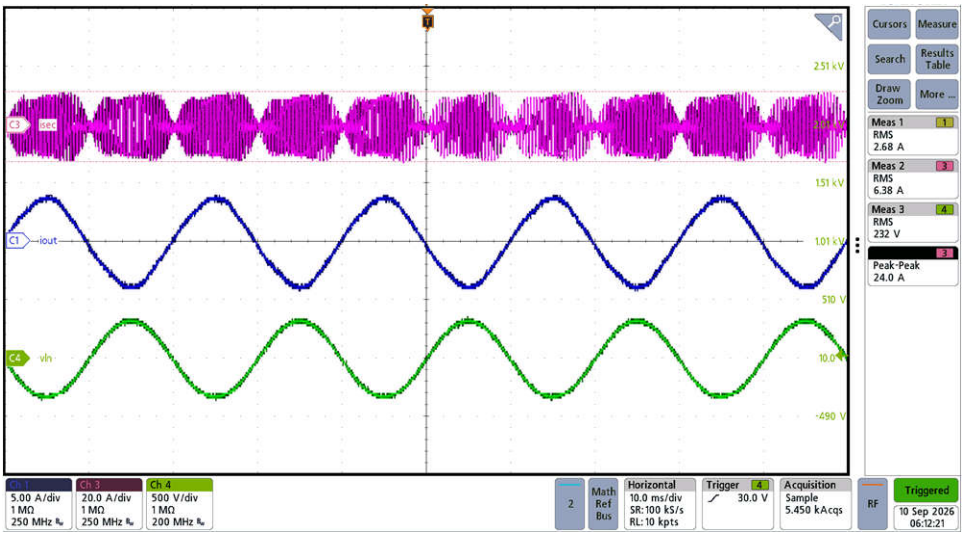



**Figure 4-13. AC-DC 230Vrms to 48VDC Reverse Charge 600W**

**Note**

Channel 1 - AC side output current Iout (blue). 2.68 Arms.

Channel 4 - AC output phase voltage Vln (green). 232 Vrms.

Channel 3 - Transformer secondary side current Isec (red). 6.38 Arms.

The three figures below show examples of the converter operating in **offgrid DC-AC mode** for various resistive, capacitive, and inductive loads.


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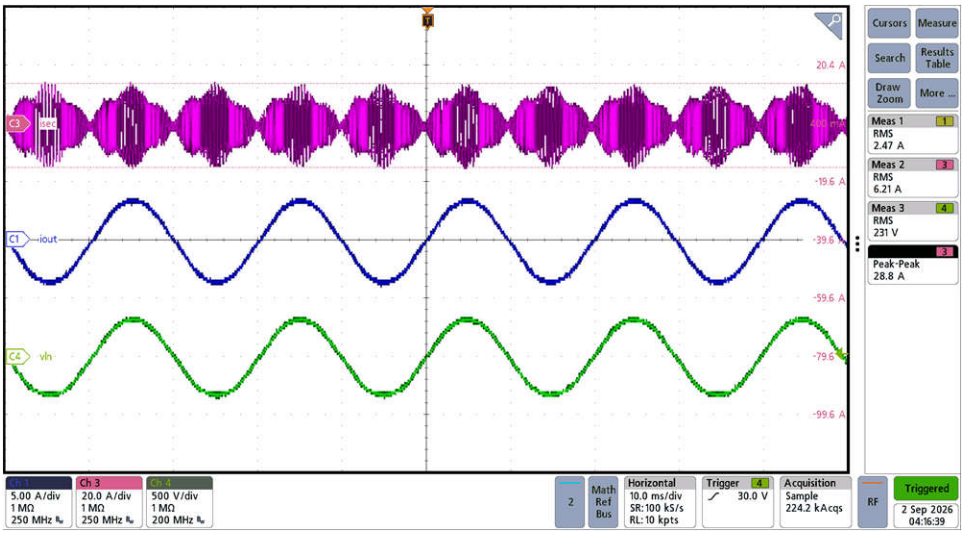



**Figure 4-14. DC-AC 42VDC to 230Vrms Offgrid Resistive Load (90R)**

**Note**

Channel 1 - AC side output current Iout (blue). 2.47 Arms.

Channel 4 - AC output phase voltage Vln (green). 231 Vrms.

Channel 3 - Transformer secondary side current Isec (red). 6.21 Arms.

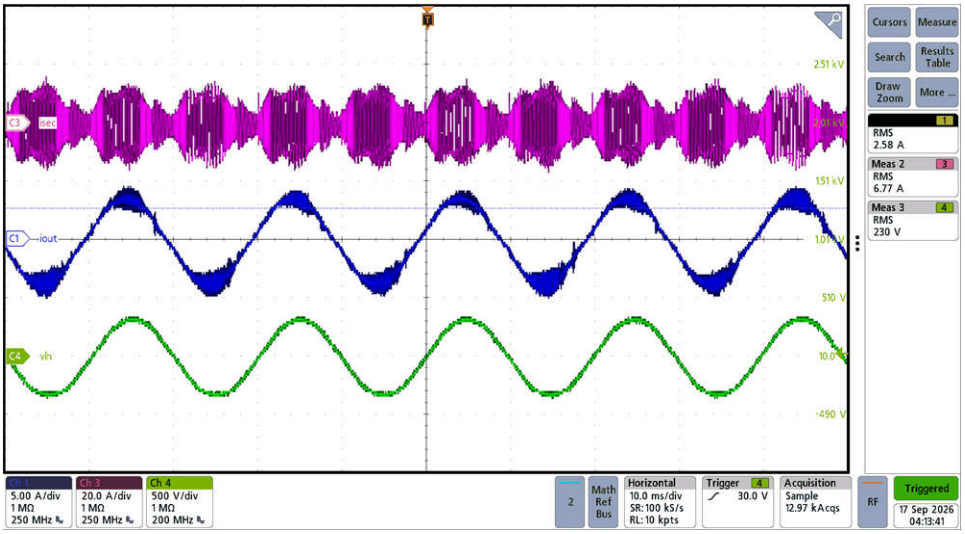



**Figure 4-15. DC-AC 42VDC to 230Vrms Offgrid Capacitive Load (90R||10uF)**

**Note**

Channel 1 - AC side output current Iout (blue). 2.58 Arms.

Channel 4 - AC output phase voltage Vln (green). 230 Vrms.

Channel 3 - Transformer secondary side current Isec (red). 6.77 Arms.



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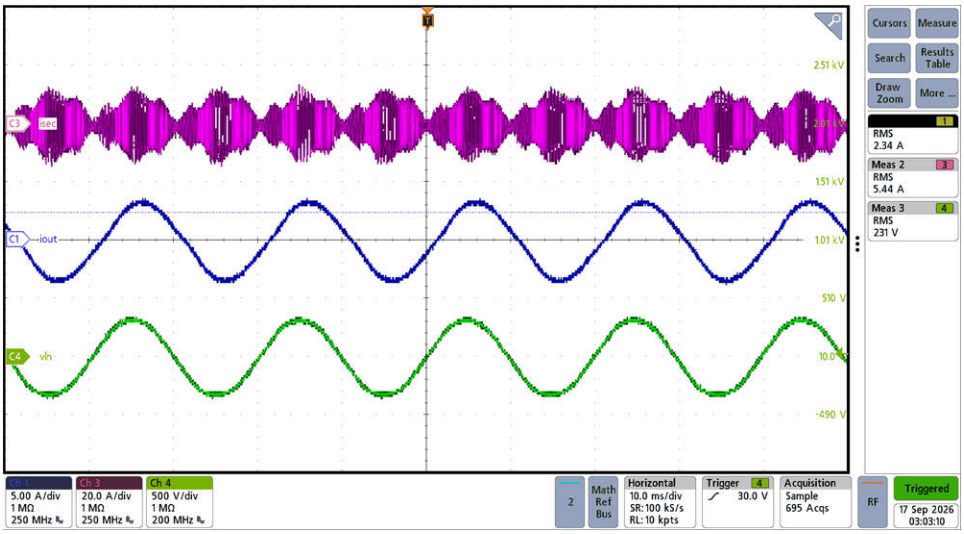



**Figure 4-16. DC-AC 42VDC to 230Vrms Offgrid Inductive Load (82R+70mH)**

**Note**

Channel 1 - AC side output current Iout (blue). 2.34 Arms.

Channel 4 - AC output phase voltage Vln (green). 231 Vrms.

Channel 3 - Transformer secondary side current Isec (red). 5.44 Arms.


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# 5 Design and Documentation Support

## 5.1 Design Files

### 5.1.1 Schematics

To download the schematics, see the design files at TIDA-010954.

### 5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010954.

## 5.2 Tools and Software

**Tools**

| | |
|---|---|
| TMDSCNCD28P55X | TMDSCNCD28P55X controlCARD evaluation module |

**Software**

| | |
|---|---|
| Code Composer Studio™ | Integrated development environment (IDE) |
| C2000WARE-DIGITALPOWER-SDK | DigitalPower software development kit (SDK) for C2000™ MCUs |

## 5.3 Documentation Support

1. Texas Instruments, *400-W GaN-Based MPPT Charge Controller and Power Optimizer Reference Design Guide*
2. Yang, Q., Yang, J., and Li, R. (April 2023). *Analysis of Grid Current Distortion and Waveform Improvement Methods of Dual-Active-Bridge Microinverter*. IEEE Transactions on Power Electronics, vol. 38, no. 4, pp. 4345-4359. Retrieved from https://ieeexplore.ieee.org/document/9969945

## 5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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# 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.



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| **Changes from Revision * (May 2025) to Revision A (October 2026)** | **Page** |
|---|---|
| • Updated schematic and layout for E4 version with bidirectional GaN | 2 |
| • Updated electrical performance specifications | 2 |
| • Updated test setup and results | 25 |


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