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Load Switches for Power MUXing and Reverse Current Blocking Design Guide

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Design Resources

TIDA-00514	Tool Folder Containing Design Files
TPS22959	Product Folder
CSD13381F4	Product Folder
TPS22959EVM-079	Product Folder

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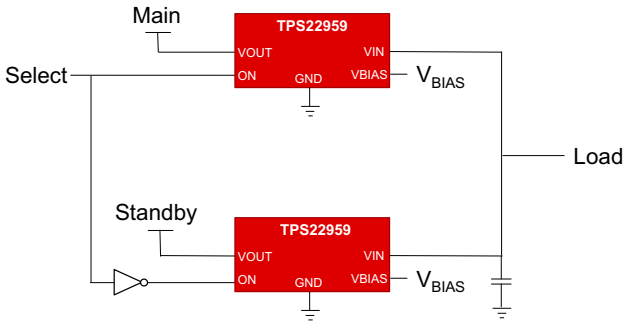
WEBENCH® Calculator Tools

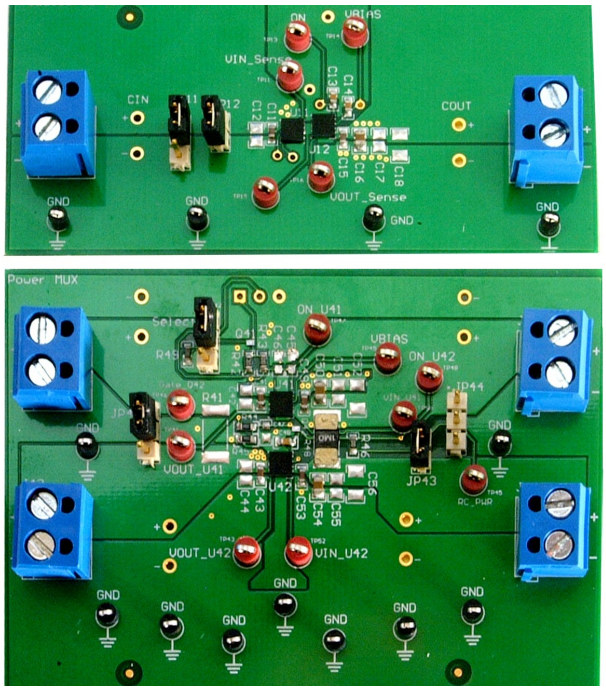
Design Features

- Control Power Multiplexing (MUX) With A Single GPIO Control Signal
- Optimized RC Circuit Ensures Make-Before-Break Logic For A Seamless Switch Over
- Configure Single-Switch Direction For Various Levels Of Reverse Current Blocking
- Includes Back-to-Back Switch Configuration For Bi-Directional Current Blocking

Featured Applications

- Servers
- Enterprise Computing
- Medical
- Telecom Systems
- Industrial Systems
- High Current Voltage Rails





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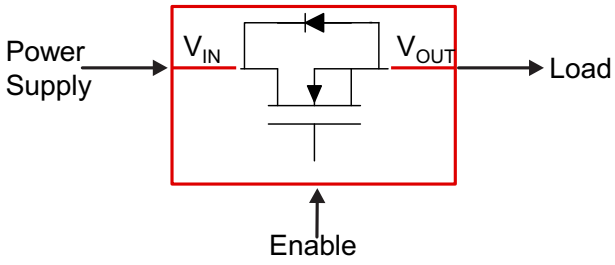
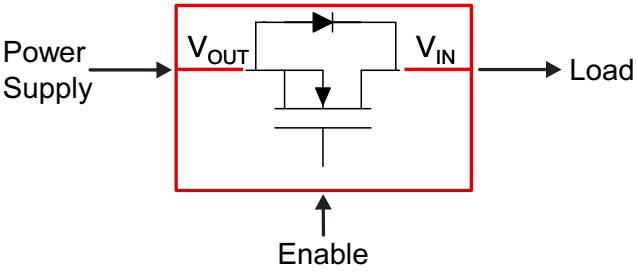
1 System Description

The functionality of existing load switches can be expanded by using them in the reverse configuration to block reverse current. This TI design demonstrates two examples of using load switches in the reverse configuration.

1.1 Forward vs. Reverse Switch Configuration

Typically, a load switch is used to control current only in the forward direction from a power supply to a load. This is because a single MOSFET can only block current in one direction due to the intrinsic body diode. However, some applications require blocking current in the reverse direction. In this case, a load switch can be used in the reverse direction for an ideal diode function. Table 1 summarizes the differences between the forward and reverse configuration.

Table 1. Forward versus Reverse Switch Configuration

FORWARD CONFIGURATION (TYPICAL)	REVERSE CONFIGURATION
	
Features: • Blocks forward current when disabled • Very low ON resistance when enabled • Does not block reverse current	**Features**: • Blocks reverse current when disabled • Very low ON resistance when enabled • Does not block forward current
Applications: • Shutdown load for power savings • Power sequencing • Inrush current control	**Applications**: • Reverse current blocking • Power MUXing

NOTE: Two load switches in a series with opposite configurations (back-to-back) can be used in applications that require features from both forward and reverse configurations.

The separate VBIAS pin allows for the load switch to receive power from any source instead of just the switch input (VIN). A V_{BIAS} supply must be present for the load switches to be enabled and have low ON Resistance.

1.2 Make-Before-Break 2:1 Power Multiplexer (MUX)

The first circuit featured in this design is a make-before-break 2:1 power MUX using two TPS22959 in the reverse configuration. The make-before-break logic ensures a seamless transition between the two power supplies by turning on the second switch before the first switch is turned off. This configuration can only be used in applications where the main and standby voltages are the same in order to prevent reverse current flow when both switches are on.

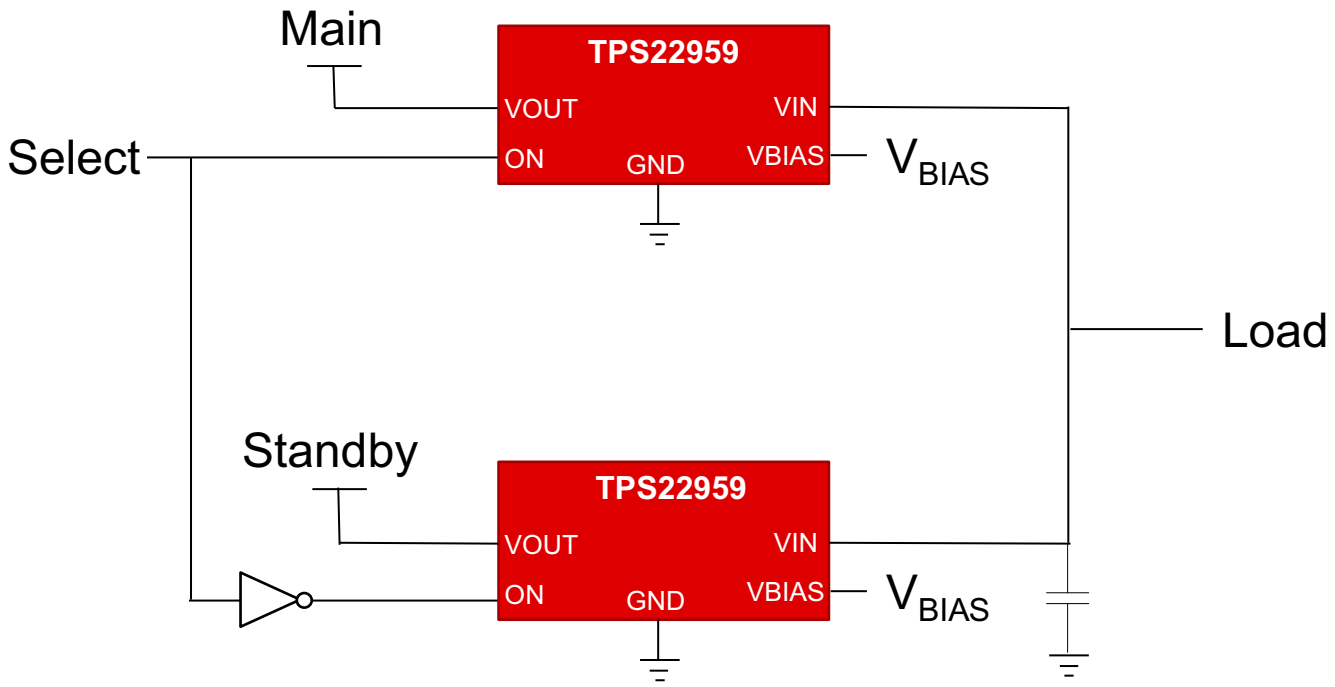


Figure 1. Make-Before-Break 2:1 Power MUX Block Diagram

1.2.1 Key Specifications

Table 2. Key Specifications

PARAMETER	SPECIFICATION	DETAILS
Maximum continuous output current	15 A	Maximum continuous current rating of TPS22959
Typical ON resistance	4.4 mΩ	See Section 4.2
Switch over time	<20 ms	See Section 7.1 and Section 7.2

1.2.2 Alternate Configurations

Resistors R41, R47, and R48 can configure the main and standby switches into the forward or reverse direction. Each resistor represents a different case, and only one should be installed at a time. time. None of these resistors are needed in the final design, and the chosen resistor can be replaced by a wide PCB trace to further reduce power dissipation and voltage drop. This design guide highlights the case where both switches are in the reverse configuration (R48 installed) for reverse current blocking on both power supplies. In cases where one supply is always available or reverse current is not a concern, the forward configuration may be preferred.

Table 3. Alternate Power MUX Switch Configurations

INSTALL RESISTOR[1]	MAIN POWER SWITCH (U41)	STANDBY POWER SWITCH (U42)	LOAD CONNECTION
R48	Reverse Configuration Input Connector J41	Reverse Configuration Input Connector J43	Connectors J42 and J44
R47	Reverse Configuration Input Connector J41	Forward Configuration Input Connector J44	Connectors J42 and J43
R41	Forward Configuration Input Connector J42	Forward Configuration Input Connector J44	Connectors J41 and J43

[1]Refer to Section 9.1 for resistor placement.

All configurations can make use of the make-before-break circuitry by using jumper J41 or J44 to connect power to this circuit from an available power supply. Using jumper J41 or J44 provides an identical control scheme regardless of configuration, but the RC delay is dependent upon input voltage.

1.3 Back-to-Back Configuration for Bi-Directional Current Blocking

The second circuit uses two TPS22959 in a back-to-back configuration for bi-directional current blocking up to 15 A.

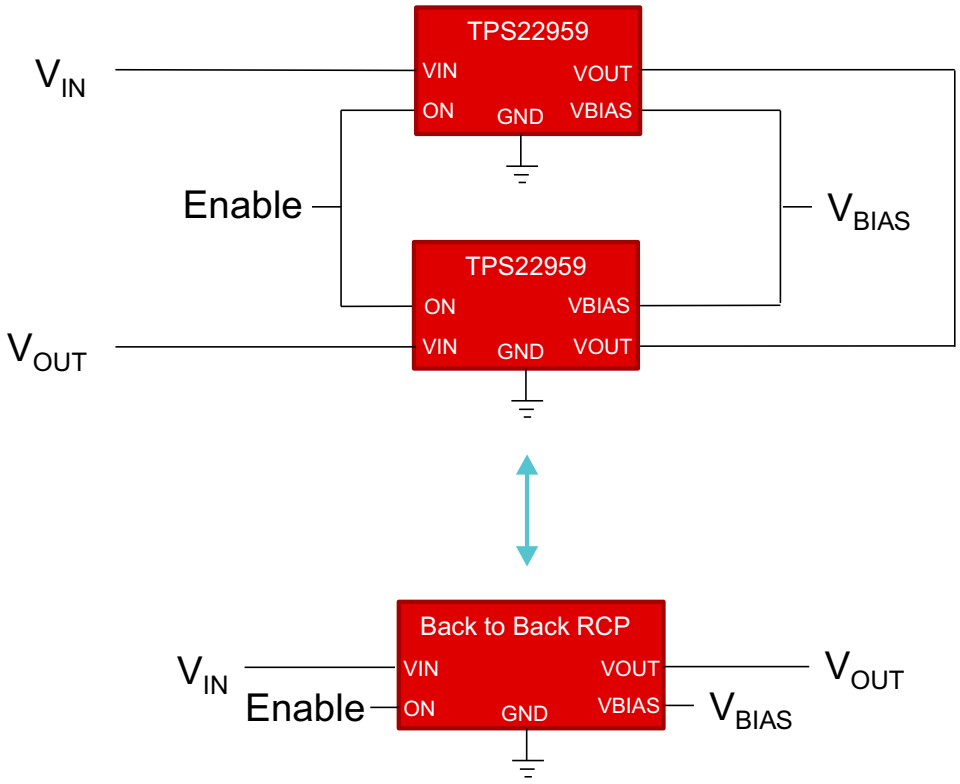


Figure 2. Back-to-Back Configuration for Bi-Directional Current Blocking

1.3.1 Key Specifications

Table 4. Key Specifications

PARAMETER	SPECIFICATION	DETAILS
Maximum continuous output current	15 A	Maximum continuous current rating of TPS22959
Typical ON resistance	8.8 mΩ	See Section 4.2 and Section 8.2
Maximum reverse leakage current	0.5 µA	See Section 8.1

2 Block Diagram

The block diagram for the TPS22959 load switch in these designs is shown in Figure 3.

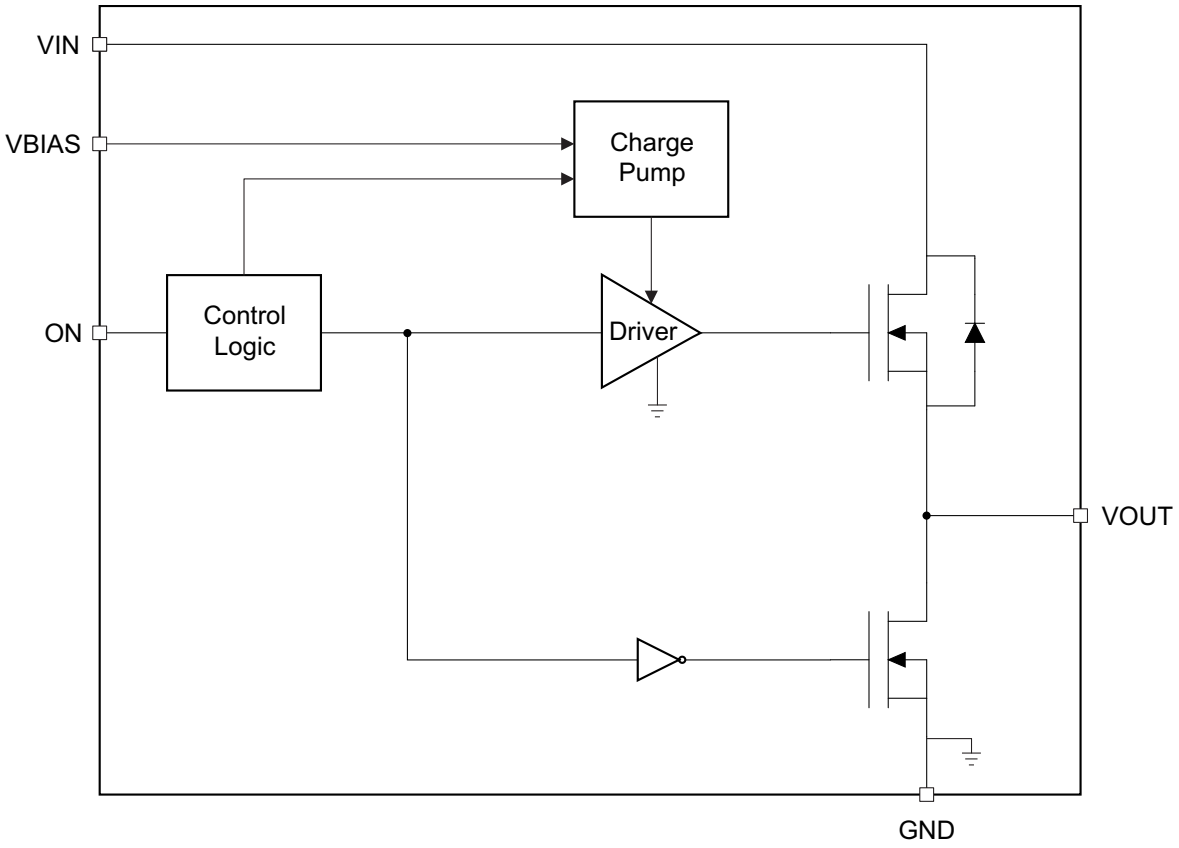


Figure 3. TPS22959 Functional Block Diagram

3 Highlighted Products

3.1 TPS22959

- Integrated Single Channel Load Switch
- V_{BIAS} Voltage Range: 2.5 V to 5.5 V
- VIN Voltage Range: 0.8 V to 5.5 V
- Ultra Low R_{ON} Resistance
  - R_{ON} = 4.4 mΩ at V_{IN} = 5 V (V_{BIAS} = 5 V)
- 15-A Maximum Continuous Switch Current
- Low Quiescent Current (20 µA for V_{BIAS} = 5 V)
- Low Shutdown Current (1 µA for V_{BIAS} = 5 V)
- Low Control Input Threshold Enables Use of 1.2 V or Higher GPIO
- Controlled and Fixed Slew Rate Across V_{BIAS} and V_{IN}
  - t_R = 2663 µs at V_{IN} = 5 V (V_{BIAS} = 5 V)
- Quick Output Discharge (QOD)
- SON 8-Terminal Package with Thermal Pad
- Pin-to-pin with TPS22962 (10-A Maximum Continuous Switch Current)
- Pin-to-pin with TPS22969 (6-A Maximum Continuous Switch Current)

3.2 CSD13381F4

- Low On-Resistance
- Low Q_g and Q_{gd}
- Low Threshold Voltage
- Ultra-Small Footprint (0402 Case Size)
  - 1.0 mm × 0.6 mm
- Ultra-Low Profile
  - 0.35 mm Height

4 System Design Theory

The functionality of existing load switches can be expanded by using them in the reverse configuration to block reverse current. This section will discuss the key features of the reverse configuration.

4.1 Reverse Current Blocking

When a load switch is placed in the reverse configuration, the intrinsic body diode will face towards the load. If the load voltage is higher than the input voltage, the body diode will remain reverse biased and will not allow reverse current to flow.

4.2 Total ON-Resistance (R_{ON})

Placing two switches in the series back-to-back configuration will double the total ON Resistance. Using a single switch in the reverse configuration to block current will minimize the total ON resistance and V = IR voltage drop.

4.3 Make-Before-Break Timing Circuit

Figure 4 shows the timing circuit to implement make-before-break logic when switching both from main to standby and from standby to main.

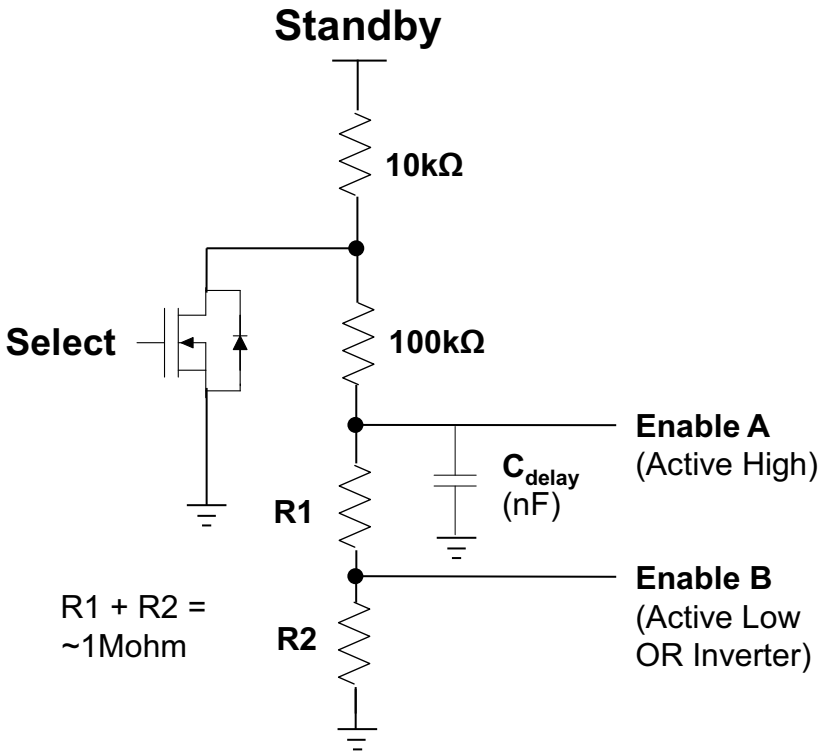


Figure 4. Make-Before-Break RC Timing Circuit

When Select goes low, Enable A is slowly charged up to the standby voltage (5 V in this case). Enable B follows Enable A through a resistor divider. The RC delay and resistor divider offset allow for Switch A to be enabled before Switch B is disabled.

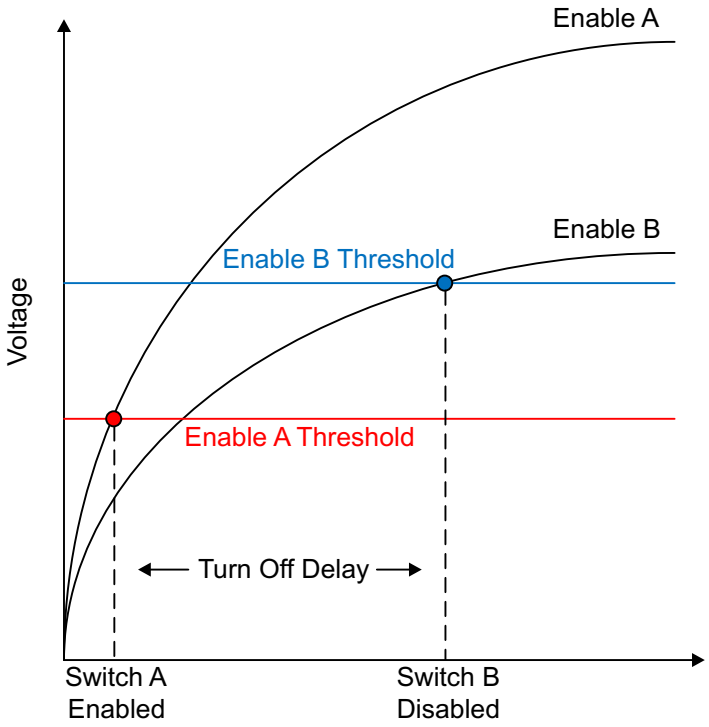


Figure 5. RC Timing Circuit Charging

The following equations can be used the find the voltages at each of the enables during charging.

$$\text{Enable A}(t) = V_{stby} \times \frac{R1 + R2 + 100k\Omega}{R1 + R2 + 100k\Omega + 10k\Omega} \times \left(1 - e^{\left(\frac{-t}{(10k\Omega + 100k\Omega) \times C_{delay}}\right)}\right) \quad (1)$$

$$\text{Enable B}(t) = \frac{R2}{R1 + R2} \times \text{Enable A}(t) \quad (2)$$

When Select goes high, Enable A is slowly discharged down to GND. Enable B follows Enable A through a resistor divider. The RC delay and resistor divider offset allow for Switch B to be enabled before Switch A is disabled.

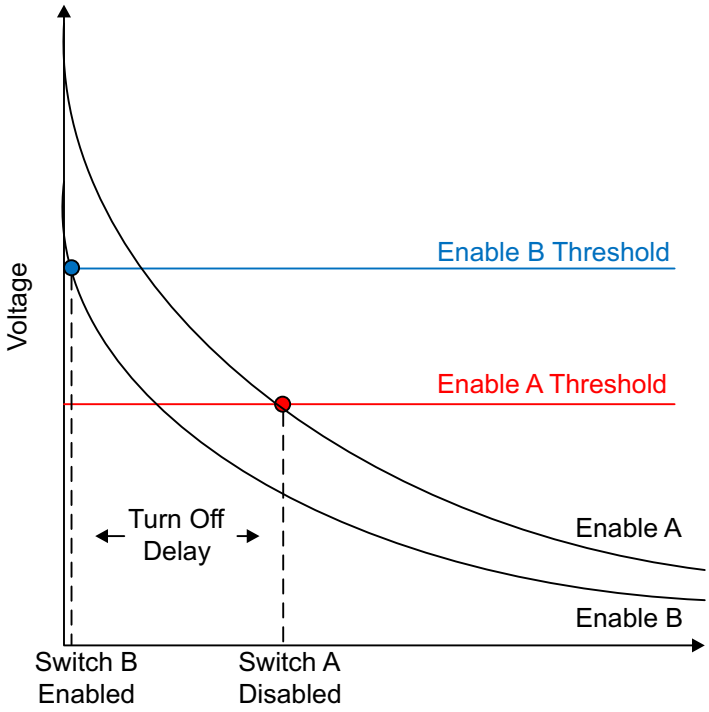


Figure 6. RC Timing Circuit Discharging

The following equations can be used the find the voltages at each of the enables during discharge.

$$\text{Enable A}(t) = V_{stby} \times \frac{R1 + R2 + 100k\Omega}{R1 + R2 + 100k\Omega + 10k\Omega} \times e^{(-t/((\frac{1}{100k\Omega} + \frac{1}{R1+R2})^{-1} \times C_{delay}))} \quad (3)$$

$$\text{Enable B}(t) = \frac{R2}{R1 + R2} \times \text{Enable A}(t) \quad (4)$$

The discharge time will always be less than the charge time because less resistance occurs in a series with the C_{delay} capacitor. Because of this, it is recommended that R1 + R2 ≥ 1 MΩ to minimize the time difference between charging and discharging cycles. Furthermore, the shorter discharge time should be used to set the C_{delay} value. The turn-off delay in Figure 6 should be greater than the turn-on delay of the load switch.

The R1 / R2 resistor ratio should be set so that Enable B will always surpass the threshold when charging. A lower threshold will allow a higher resistor-divider ratio and minimize the required switch-over delay. The CSD13381F4 FemtoFET™ was specifically chosen for this design because of its small size and low threshold voltage.

Note that in this design, Enable A is controlling the Main Power Supply Switch, and Enable B is controlling the Standby Power Supply Switch. When Select is Low, the main supply will power the load. When Select is High, the standby supply will power the load. The Select logic can be reversed simply by swapping the Main- and Standby-Power Supply connections. Just be sure the make-before-break timing circuit and V_{BIAS} supplies have power.

5 Getting Started Hardware

5.1 Make-Before-Break 2:1 Power MUX Connections and Test Points

The connections and test points for the make-before-break power MUX (with R48 installed) are summarized in Table 5:

Table 5. Power MUX Circuit Connections and Test Points

CONNECTION	NAME	DESCRIPTION
J41	Main power input	DC Input to main power switch
J42, J44	V_{load}	Load connection
J43	Standby power input	DC Input to standby power switch
JP41, JP44	make-before-break circuit power rail selection	Connects make-before-break circuit power to one of the four power connectors J41, J42, J43, or J44
JP42	Switch control	Power supply connection
JP43	V_{BIAS} power	Option V_{BIAS} connection to make-before-break circuit power rail
TP41	Main power sense	Sense connection to main power switch
TP52	V_{load} sense	Sense connection to the switches' output
TP43	Standby power sense	Sense connection to standby power switch
TP45	make-before-break circuit power rail	Connection for external power to make-before-break circuit power rail
TP47	V_{ON_Main}	Sense connection for main switch enable
TP48	$V_{ON\_Standby}$	Sense connection for standby switch enable
TP45	Make-before-break circuit power rail	Connection for external power to make-before-break circuit power rail
TP46	Inverter input	Sense connection for input to NMOS inverter
TP49	V_{BIAS} power	Connection for external power to V_{BIAS}
TP32, TP36, TP37, TP38	GND	Connection to board ground

5.2 Back-to-Back Circuit Connections and Test Points

The connections and test points for the back-to-back TPS22959 circuit are summarized in Table 6:

Table 6. Back-to-Back Circuit Connections and Test Points

CONNECTION	NAME	DESCRIPTION
J11	V_{IN}	DC Input to V_{IN}
J12	V_{OUT}	Load connection for V_{OUT}
JP12	V_{BIAS} power	Connects V_{BIAS} to V_{IN}
JP11	ON control	Connects ON pin to V_{IN} or GND
TP11	V_{IN} sense	Sense connection to V_{IN}
TP16	V_{OUT} sense	Sense connection to V_{OUT}
TP14	V_{BIAS}	V_{BIAS} connection
TP13	ON	Enable connection
TP12, TP17, TP18, TP19	GND	Connection to board ground

6 Test Setup

This section shows the test setup for both the make-before-break 2:1 Power MUX circuit as well as the back-to-back TPS22959 circuit.

6.1 Make-Before-Break 2:1 Power MUX Test Setup

Figure 7 shows the test points for the power MUX waveform collection:

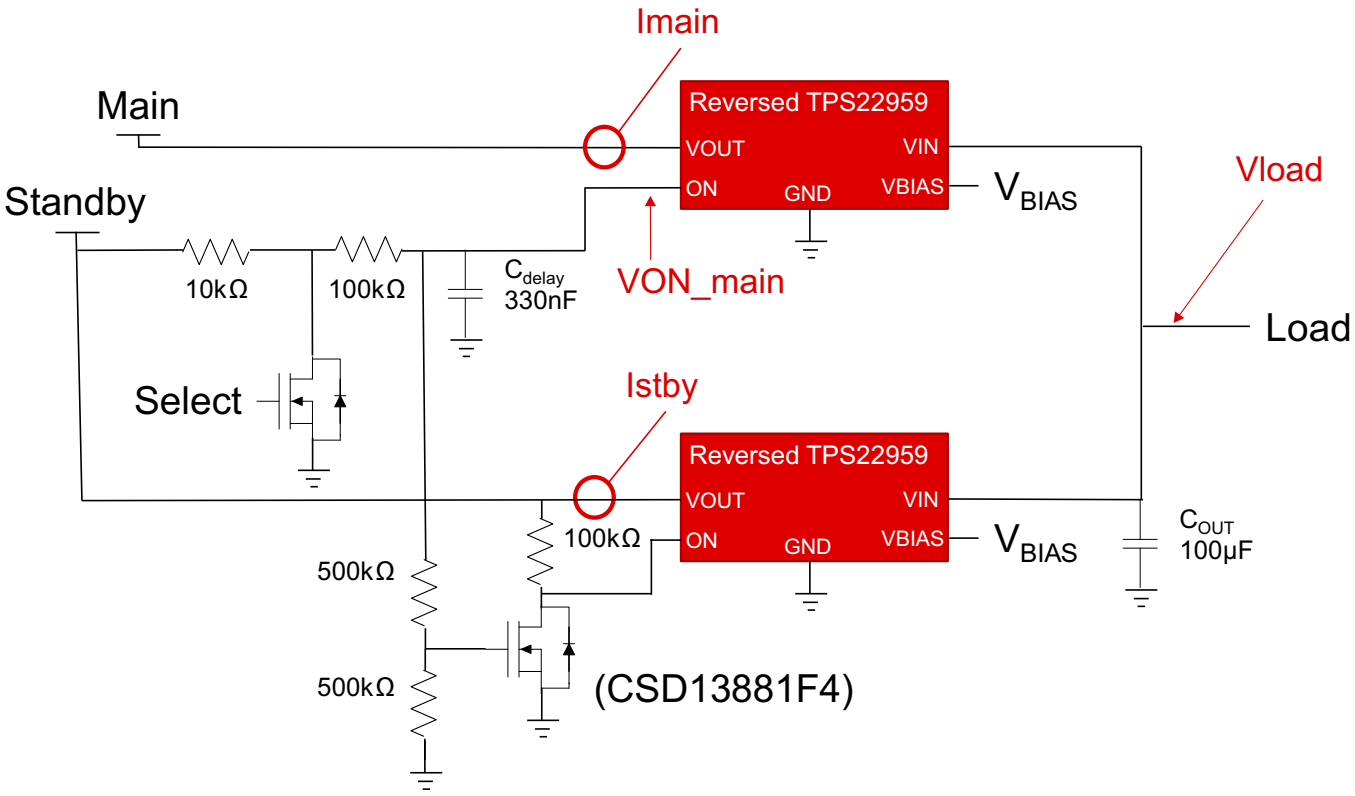


Figure 7. Power MUX Waveform Setup

6.2 Back-to-Back Circuit Reverse Current Blocking Test Setup

Figure 8 shows the proper test setup for measuring the reverse leakage current through the back-to-back load switches when they are disabled:

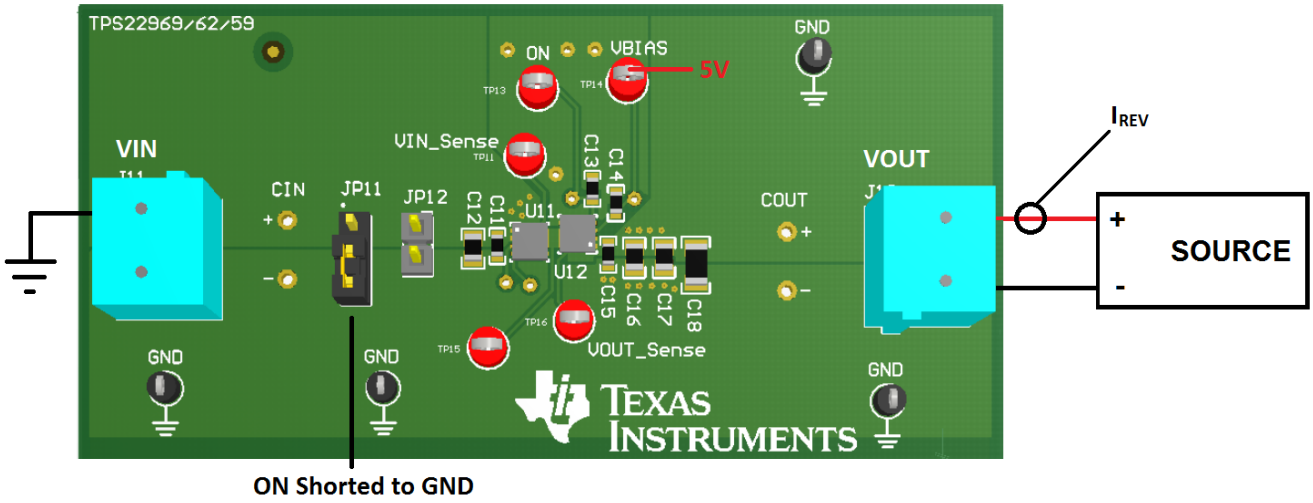


Figure 8. Back-to-Back Reverse Current Blocking Test Setup

6.3 Back-to-Back Circuit ON Resistance Test Setup

Figure 9 shows the proper test setup for measuring the ON resistance of the back-to-back TPS22959 circuit:

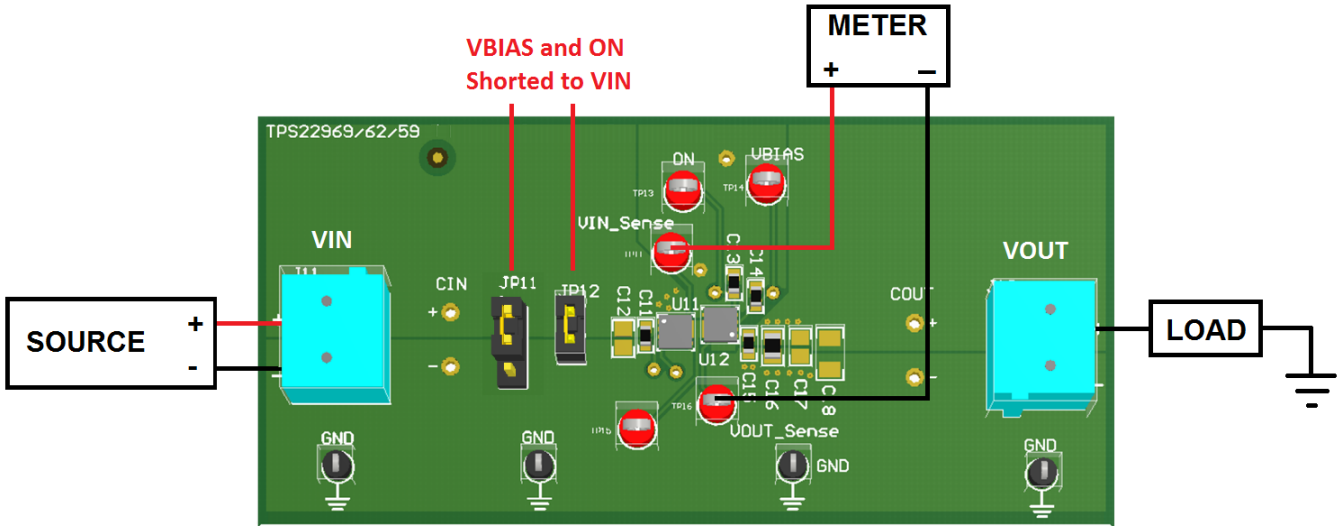


Figure 9. Back-to-Back Circuit ON Resistance Test Setup

7 Make-Before-Break 2:1 Power MUX Test Data

This section will cover the test data from the power MUX circuit.

7.1 Switching Waveforms (5 V)

The following waveforms show the switch-over waveforms when both main and standby are at 5 V. During switching, the make-before-break logic allows the current to be temporarily shared between the two supplies to ensure a seamless switch over.

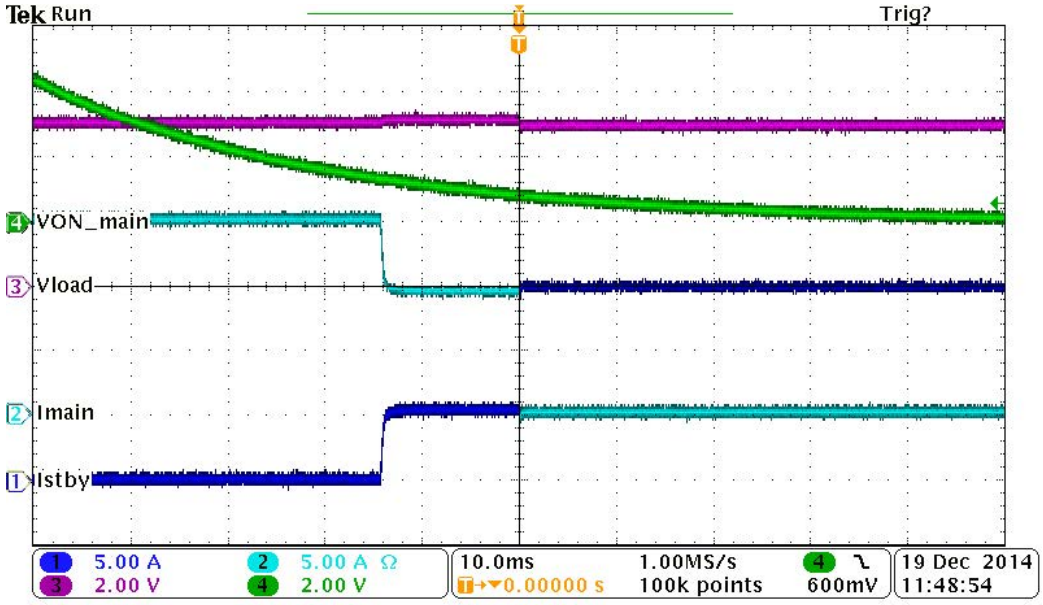


Figure 10. Switching from Main to Standby (5 V)

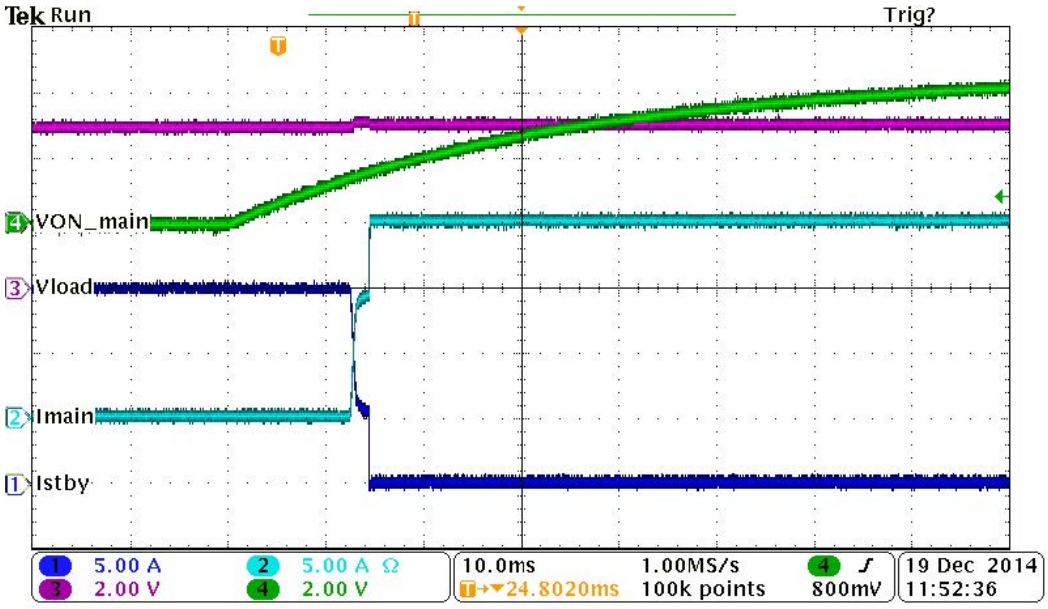


Figure 11. Switching from Standby to Main (5 V)

Because very little overlap occurs when switching from standby to main, the C_{delay} capacitor should not be reduced from 330 nF to prevent a dip in the load voltage when switching.

7.2 Switching Waveforms (3.3 V)

The following waveforms show the switch-over waveforms when both main and standby are at 3.3 V. During switching, the make-before-break logic allows the current to be temporarily shared between the two supplies to ensure a seamless switch over.

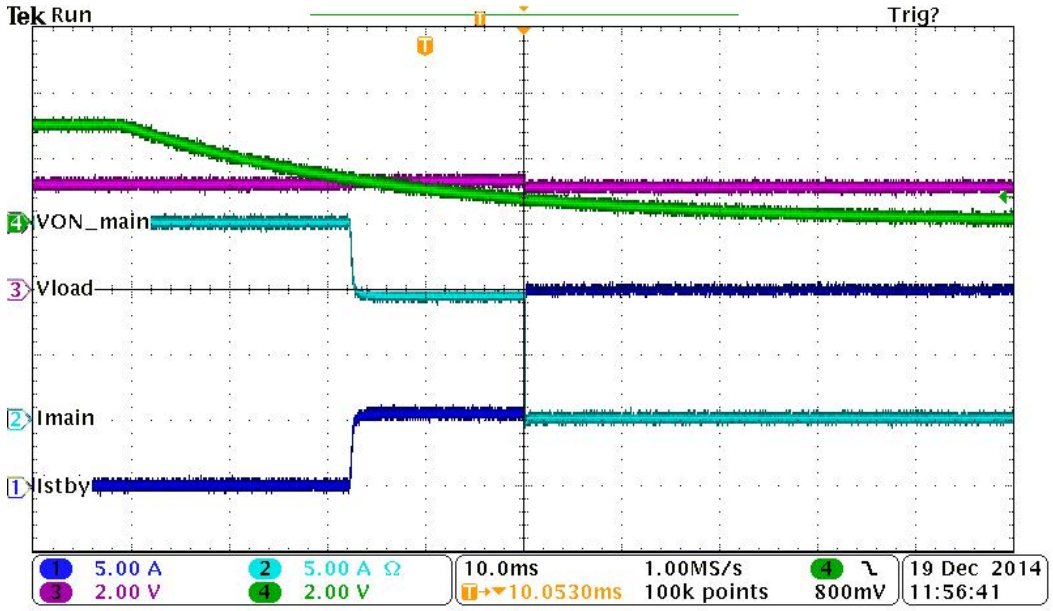


Figure 12. Switching from Main to Standby (3.3 V)

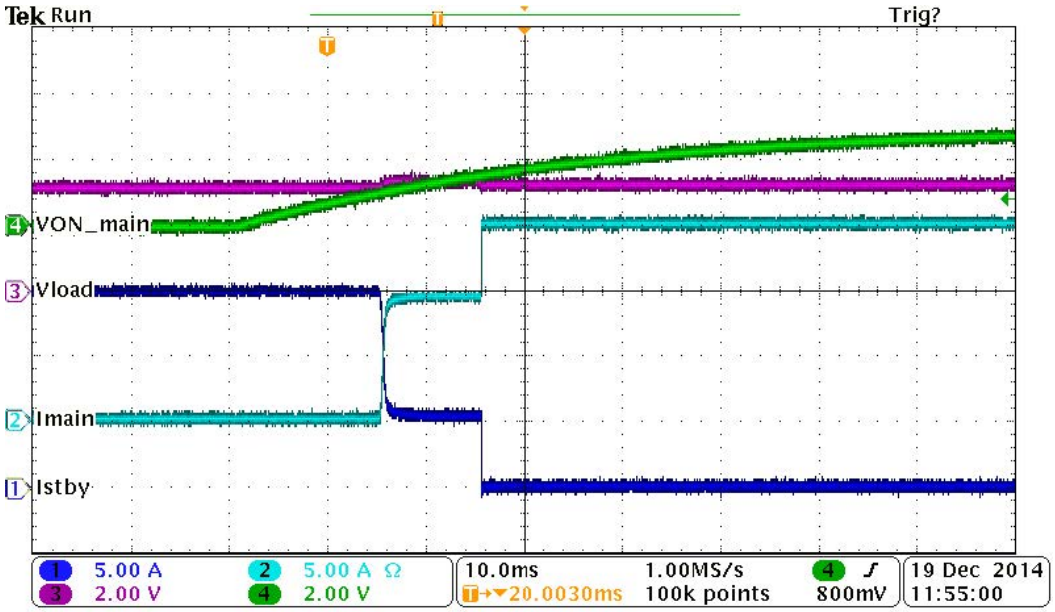


Figure 13. Switching from Standby to Main (3.3 V)

Because at least 10 ms of overlap occurs when switching from main to standby and from standby to main, the C_{delay} capacitor could be reduced from 330 nF for a faster switchover. This reduction would not be possible in the 5-V case because very little overlap occurs when switching from standby to main.

8 Back-to-Back Circuit Test Data

This section will cover the test data from the back-to-back TPS22959 circuit.

8.1 Reverse Leakage Current

Figure 14 shows the reverse leakage current through the back-to-back load switches when they are disabled.

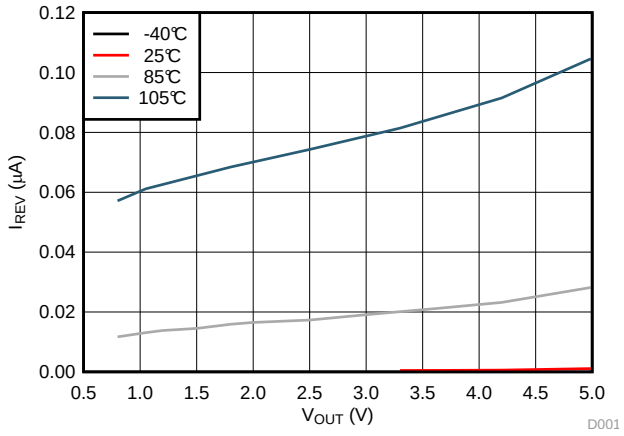


Figure 14. Back-to-Back Circuit Reverse Leakage Current

8.2 ON Resistance versus Load Current

Figure 15 summarizes the ON resistance measured at various loads:

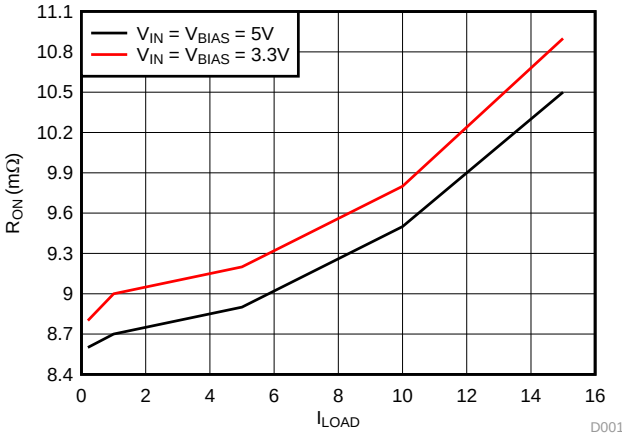


Figure 15. Back-to-Back Circuit ON Resistance versus Load Current

9 Design Files

9.1 Schematics

To download the Schematics, see the design files at TIDA-00514.

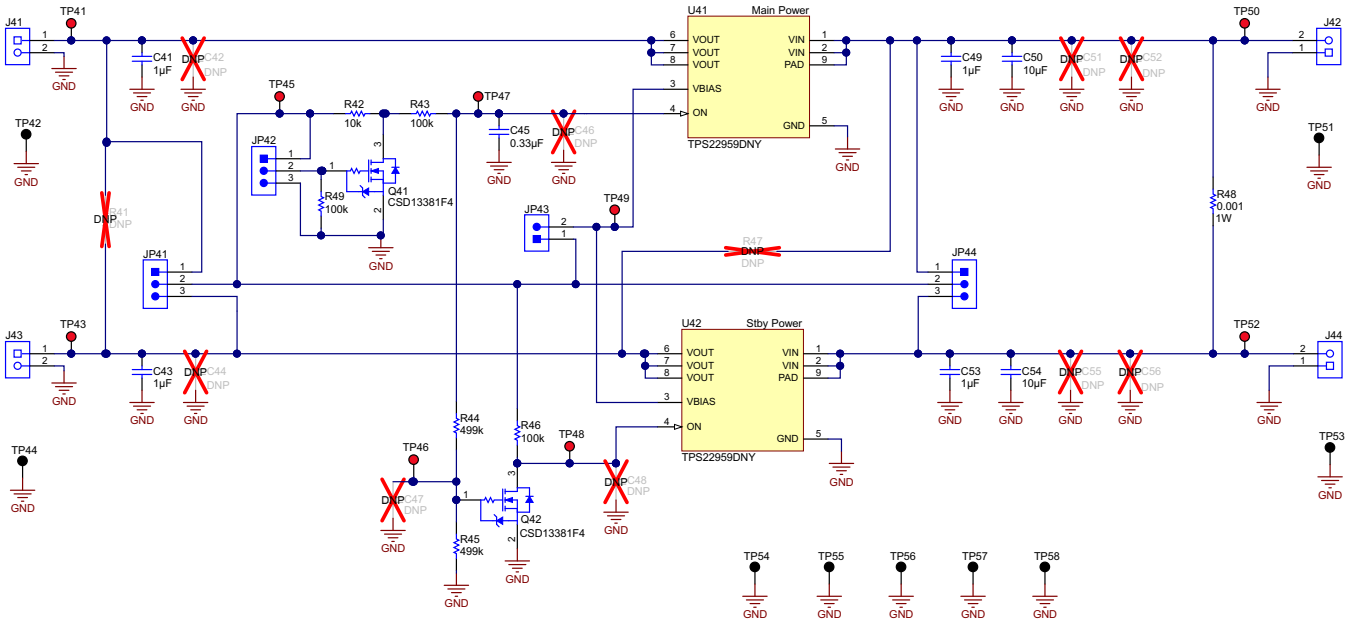


Figure 16. Make-Before-Break 2:1 Power MUX Schematic

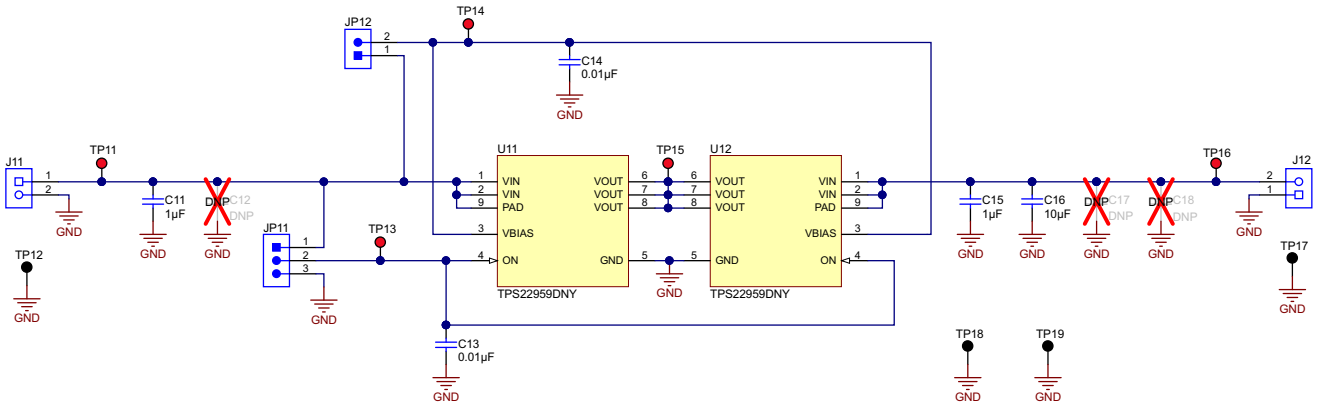


Figure 17. Back-to-Back TPS22959 Schematic

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00514.

9.3 PCB Layout Recommendations

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

9.4 Layout Prints

To download the layout prints, see the design files at TIDA-00514.

9.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00514.

9.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00514.

10 References

1. *Load Switch Thermal Considerations App Report* (SLVUA74)

11 About the Author

ADAM HOOVER is a Systems Engineer at Texas Instruments, where he is responsible for developing Load Switch and Power MUX solutions. Adam earned his Bachelors of Science in Electronics Engineering Technology (EET) from Texas A&M University in College Station, TX.

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