Test Report: PMP31190

PFC Flyback and Charger Reference Design

Description

This reference design consists of an AC/DC battery-backup charger with system and battery outputs. A 4-switch bidirectional buck-boost charges the battery and supplies system load. The optional LaunchPad™ disables main power sections, reducing stand-by power while collecting parameters for telemetry.

Resources

PMP31190	Design Folder
BQ25751 UCC28810	Product Folder
UCC24612-1 TL431	Product Folder
AMC1311 TLV6001	Product Folder
TLV704 TPS560430	Product Folder
SN6501	Product Folder

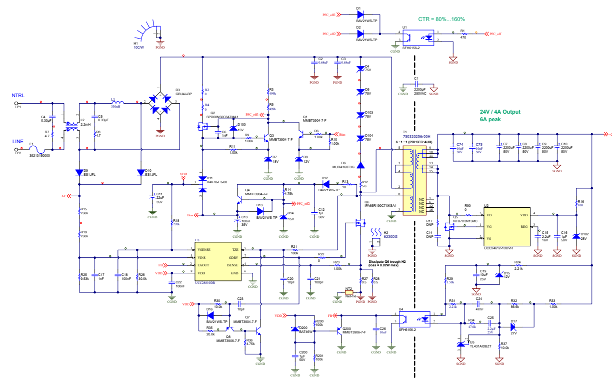
Features

- Based on 4-SW buck-boost bi-directional charger BQ25751
- Automatic switch from primary (AC) to secondary (DC) power
- Direct power path management

Applications

- Fire alarm control panel (FACP)

Top of Board



Schematic of PFC

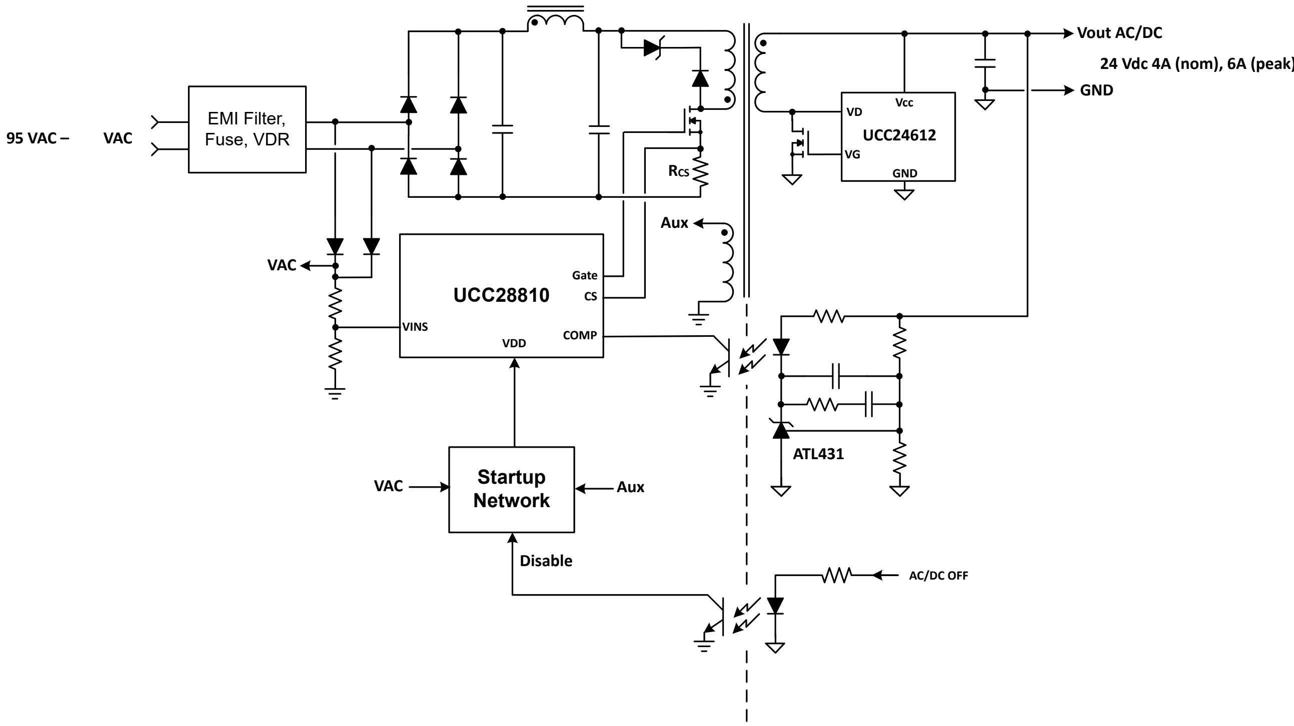


Figure 1-1. AC/DC Flyback

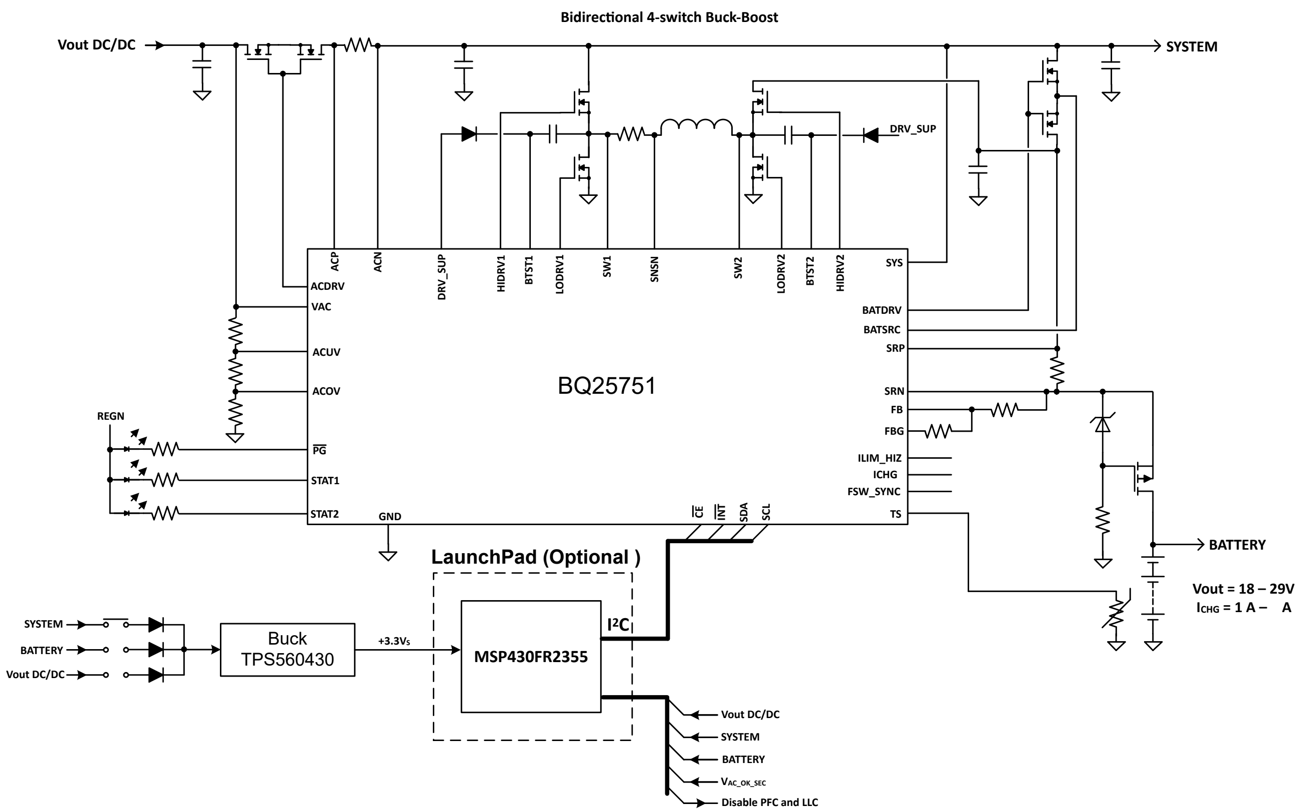


Figure 1-2. Battery Charger

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	95V to 132V (AC)
Output Voltage (Flyback)	24V
Maximum Output Current (Flyback)	4A (6A peak)
Output Voltage (Charger)	22.8V to 28.8V (DC)
Charging Current	0A - 1A

1.2 Required Equipment

- 0…250V_{AC}, AC constant voltage generator (VS1)
- Electronic load, (constant current range 0… 6A minimum)
- Two elements of Lead-Acid batteries with 12V nominal voltage (5 – 10Ah)
- Oscilloscope (minimum 100MHz bandwidth)
- Current probe (minimum 100kHz bandwidth)
- EV2400 (HPA500) interface to BQ-Studio software

1.3 Safety Considerations

Always follow TI's set-up and application instructions, including use of all interface components within the recommended electrical rated voltage and power limits. Always use electrical safety precautions to help verify your personal safety and those working around you. Contact TI's Product Information Center http://ti.com/customer support for further information.

WARNING

Failure to follow warnings and instructions can result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits*. Any other *use and/or application are strictly prohibited by Texas Instruments*. If you are not suitably qualified, then immediately stop from further use of the HV EVM.

1. Work Area Safety:
   a. Keep work area clean and orderly.
   b. Qualified observers must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and the interface electronics are energized, indicating operation of accessible high voltages can be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.

e. Use stable and non-conductive work surface.
f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.

1. Electrical Safety:
   a. As a precautionary measure, a good engineering practice is to assume that the entire EVM has fully accessible and active high voltages.
   b. De-energize the TI HV EVM and all the inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely deenergized.
   c. c. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   d. d. Once EVM readiness is complete, energize the EVM as intended.

   WARNING

   While the EVM is energized, never touch the EVM or the electrical circuits, as the circuits can be at high voltages capable of causing electrical shock hazard.
2. Personal Safety
   a. Wear personal protective equipment for example, latex gloves or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

1.4 Dimensions

The size of the four-layer board is 165.1mm × 83.8mm. The copper thickness of the outer layers is 70µm and the copper thickness of both inner layers is 35µm.

1.5 Test Setup

1. Connect the source VS1 to TP1 and TP3
2. Connect the load to terminals 3 (positive) and terminal 1 (negative) of output system voltage (J1)
3. Connect two elements of batteries (in series each other) to terminals 1 (positive) and terminal 3 (negative). Use the temperature sensing terminal 3 (TS) to provide temperature information. Connect a resistor to ground if not used.
4. Turn on VS1 (accepted range: $95V_{AC}$ - $132V_{AC}$).
5. BQ-Studio software can be used to set the internal parameters of the BQ25751.
6. Increase the load on the system output and measure the battery charging / discharging current.

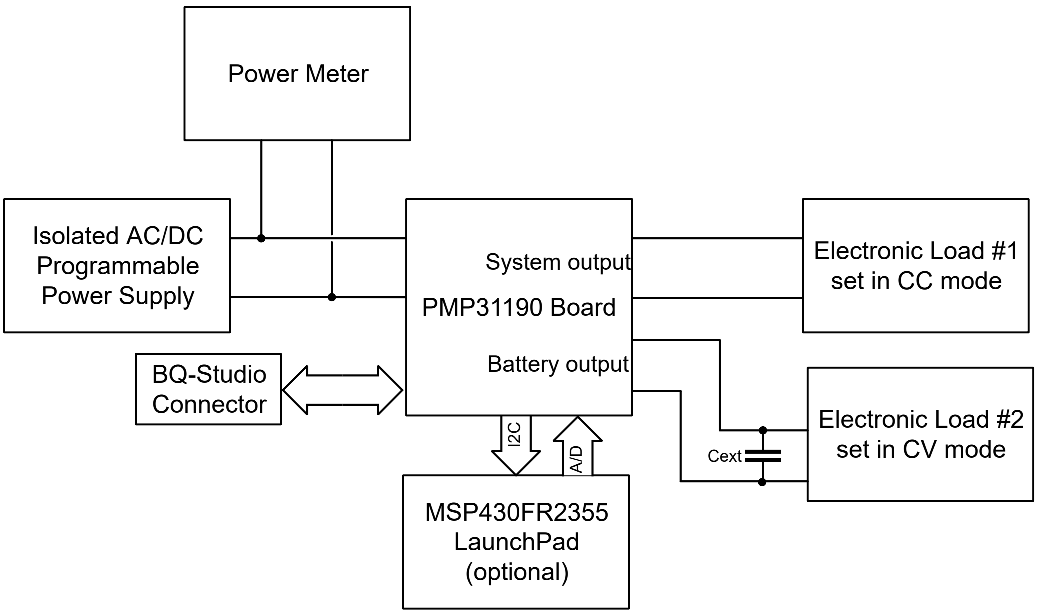


Figure 1-1. Test Setup

2 Testing and Results

2.1 Efficiency Graphs

Efficiency is shown in Figure 2-1.

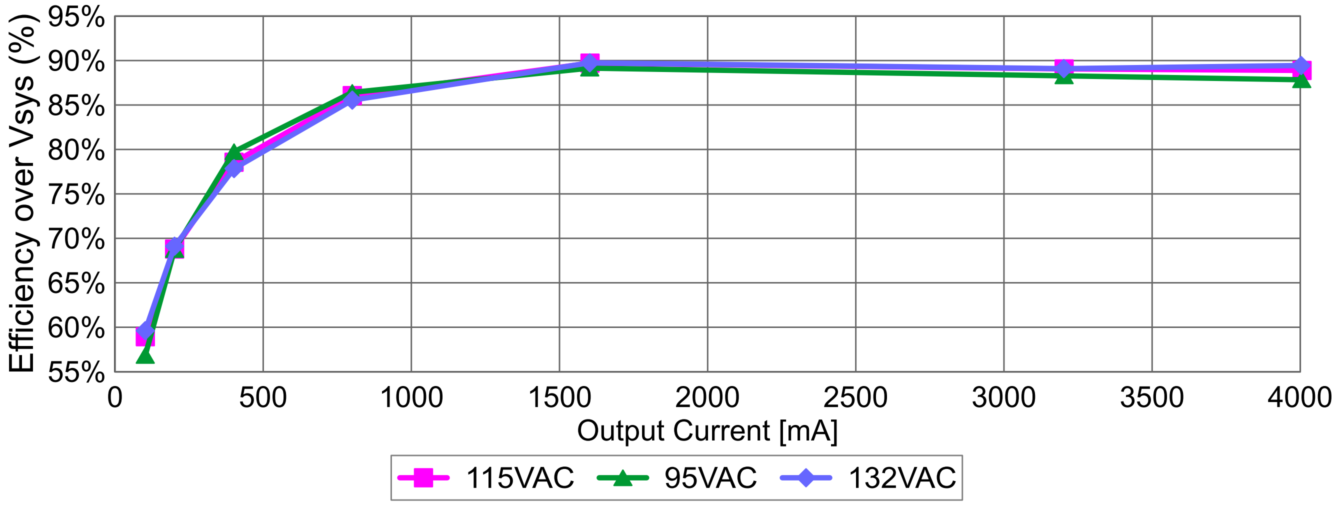


Figure 2-1. Efficiency over V_{sys} (%) versus Output Current

2.2 Efficiency Data

2.2.1 115V_{AC} Input Voltage

Table 2-1. Efficiency Data for 115V_{AC}, 60Hz Input Voltage

P_{IN} (W)	PF (%)	THDi (%)	V_24V (V)	V_sys (V)	I_sys (mA)	P_{OUT} (W)	Efficiency (%)
1.15	0	0.00	24.18	24.15	0.0	0.00	0.00%
4.19	60.11	56.72	24.18	24.15	102.2	2.47	58.93%
7.06	70.10	45.10	24.18	24.15	201.0	4.85	68.79%
12.34	81.22	25.24	24.18	24.14	401.6	9.69	78.56%
22.45	91.16	13.41	24.18	24.13	800.7	19.32	86.06%
43.08	96.58	9.55	24.18	24.11	1603	38.65	89.71%
86.53	98.40	12.04	24.16	24.06	3203	77.06	89.06%
108.30	98.61	13.09	24.16	24.03	4006	96.26	88.89%

2.2.2 95V_{AC} Input Voltage

Table 2-2. Efficiency Data for 95V_{AC}, 60Hz Input Voltage

P_{IN} (W)	PF (%)	THDi (%)	V_24V (V)	V_sys (V)	I_sys (mA)	P_{OUT} (W)	Efficiency (%)
1.04	0	0.00	24.18	24.15	0.0	0.00	0.00%
4.34	69.37	47.09	24.17	24.15	102.1	2.47	56.83%
7.06	79.18	31.41	24.18	24.14	200.9	4.85	68.74%
12.15	88.48	15.86	24.18	24.14	401.5	9.69	79.75%
22.35	95.30	9.87	24.17	24.13	800.5	19.32	86.42%
43.31	98.07	9.46	24.17	24.10	1602	38.61	89.14%
87.26	98.77	13.29	24.15	24.05	3203	77.03	88.28%
109.52	98.79	14.36	24.14	24.02	4005	96.20	87.84%

2.2.3 132V_{AC} Input Voltage

Table 2-3. Efficiency Data for 132V_{AC}, 60Hz Input Voltage

P_{IN} (W)	PF (%)	THDi (%)	V_24V (V)	V_sys (V)	I_sys (mA)	P_{OUT} (W)	Efficiency (%)
1.18	0	0.00	24.18	24.15	0.0	0.00	0.00%
4.14	52.60	57.40	24.18	24.15	102.1	2.47	59.62%
7.02	63.39	52.89	24.18	24.15	200.9	4.85	69.11%
12.45	75.07	33.15	24.18	24.14	401.6	9.69	77.85%
22.58	86.51	16.69	24.18	24.13	800.5	19.32	85.55%
43.04	94.56	10.61	24.18	24.11	1602	38.62	89.75%
86.47	97.88	10.94	24.17	24.06	3202	77.04	89.09%
107.59	98.22	12.24	24.16	24.04	4003	96.23	89.44%

2.3 Power Factor Graph

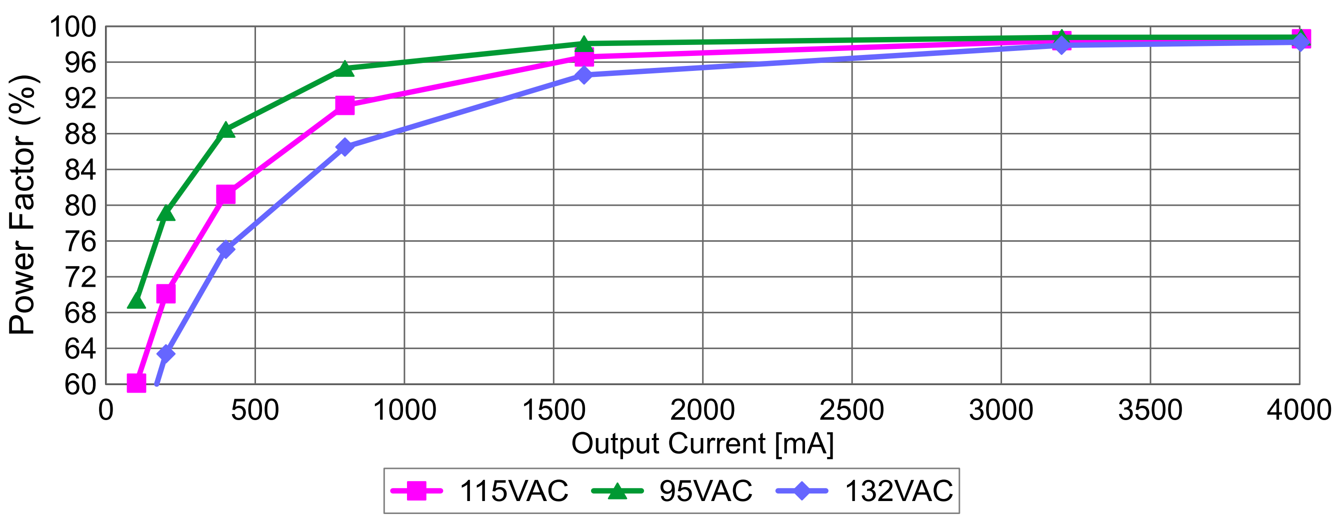


Figure 2-2. Power Factor versus Output Current

2.4 Load Regulation

2.4.1 Output Voltage V_24V

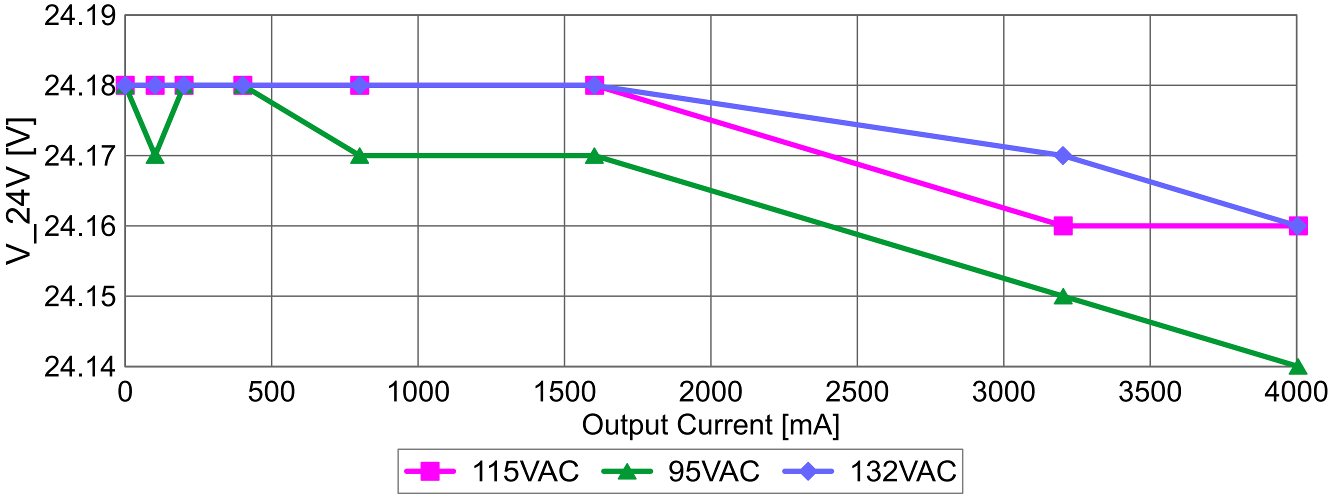


Figure 2-3. Output Voltage V_24V versus Output Current

2.4.2 Output Voltage V_sys

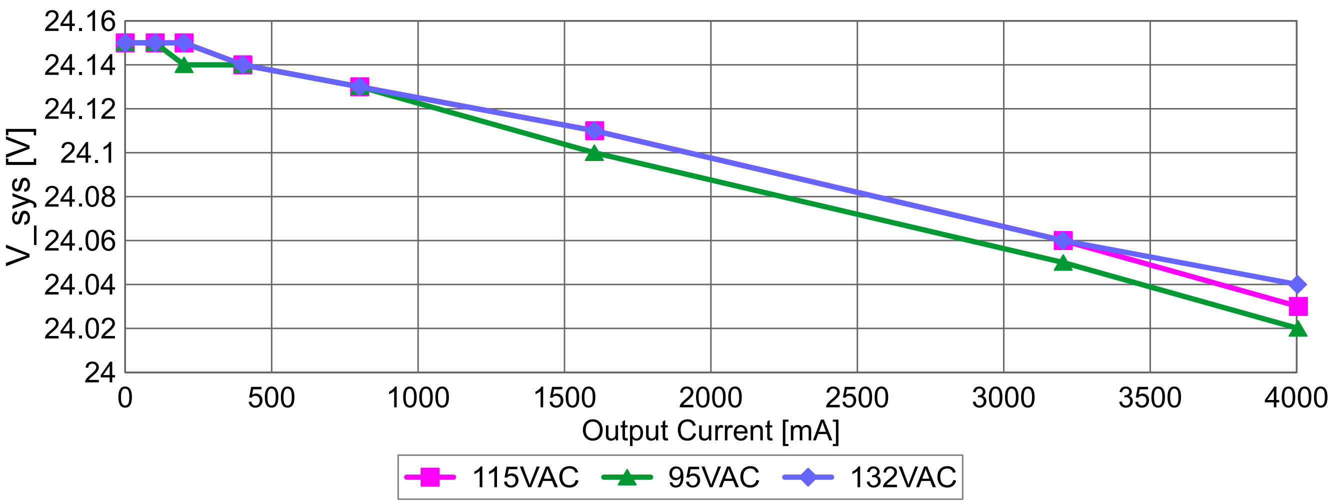


Figure 2-4. Output Voltage V_sys versus Output Current

2.5 AC Current Total Harmonic Distortion (THD)

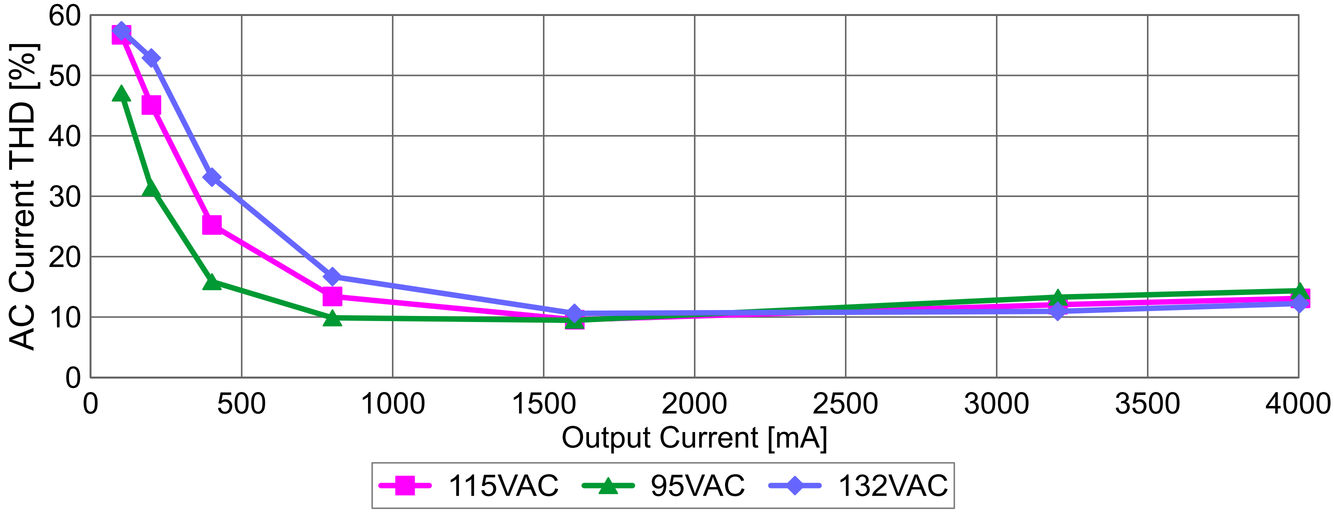


Figure 2-5. AC Current THD versus Output Current

2.6 V_{AC_U} Readout Chart

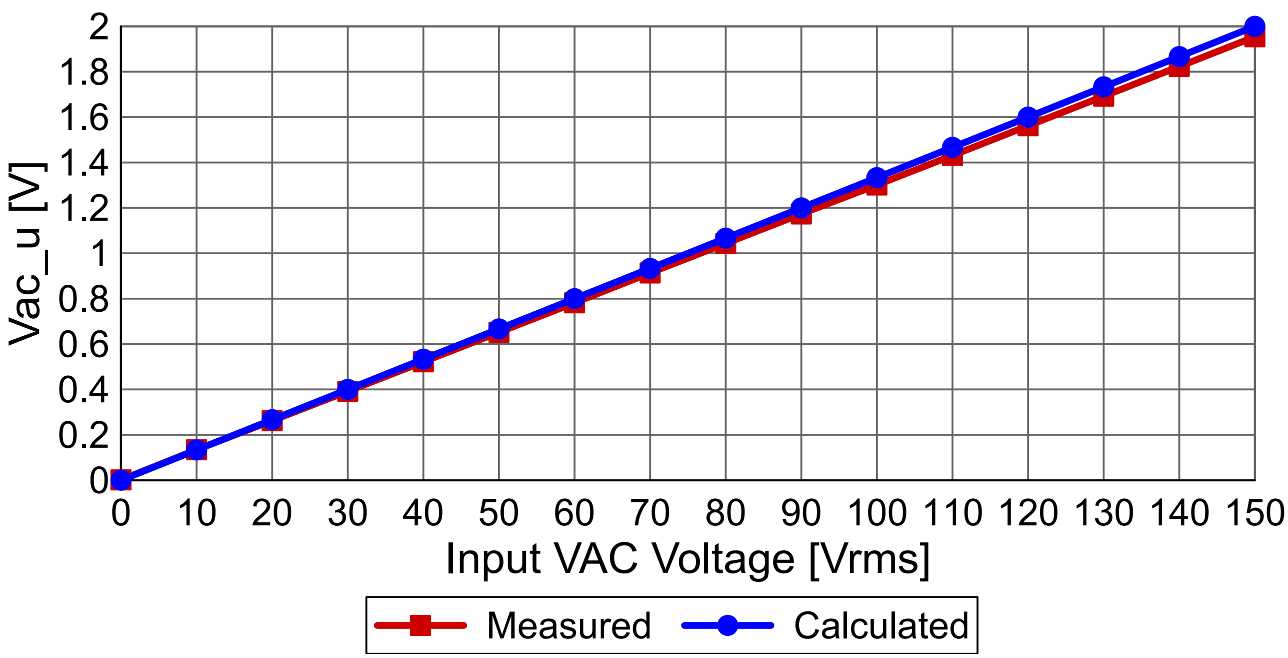


Figure 2-6. V_{AC_U} Readout versus Input V_{AC} Voltage; this voltage is Proportional to AC Input, and Fed to the Microcontroller Through the LaunchPad Interface

2.7 V_{AC_U} Readout Data

Table 2-4. V_{AC_U} Readout Data

V_{AC_U} Readout, 60Hz		
V_{AC} (Vrms)	V_{AC_U} (Vdc)	V_{AC_U} calc
0	0.001	0.000
10	0.135	0.133
20	0.262	0.267
30	0.392	0.400
40	0.522	0.533
50	0.652	0.667
60	0.782	0.800
70	0.913	0.933
80	1.043	1.067
90	1.173	1.200
100	1.301	1.333
110	1.431	1.467
120	1.562	1.600
130	1.692	1.733
140	1.823	1.867
150	1.954	2.000

2.8 Thermal Images

Thermal image is shown in Figure 2-7.

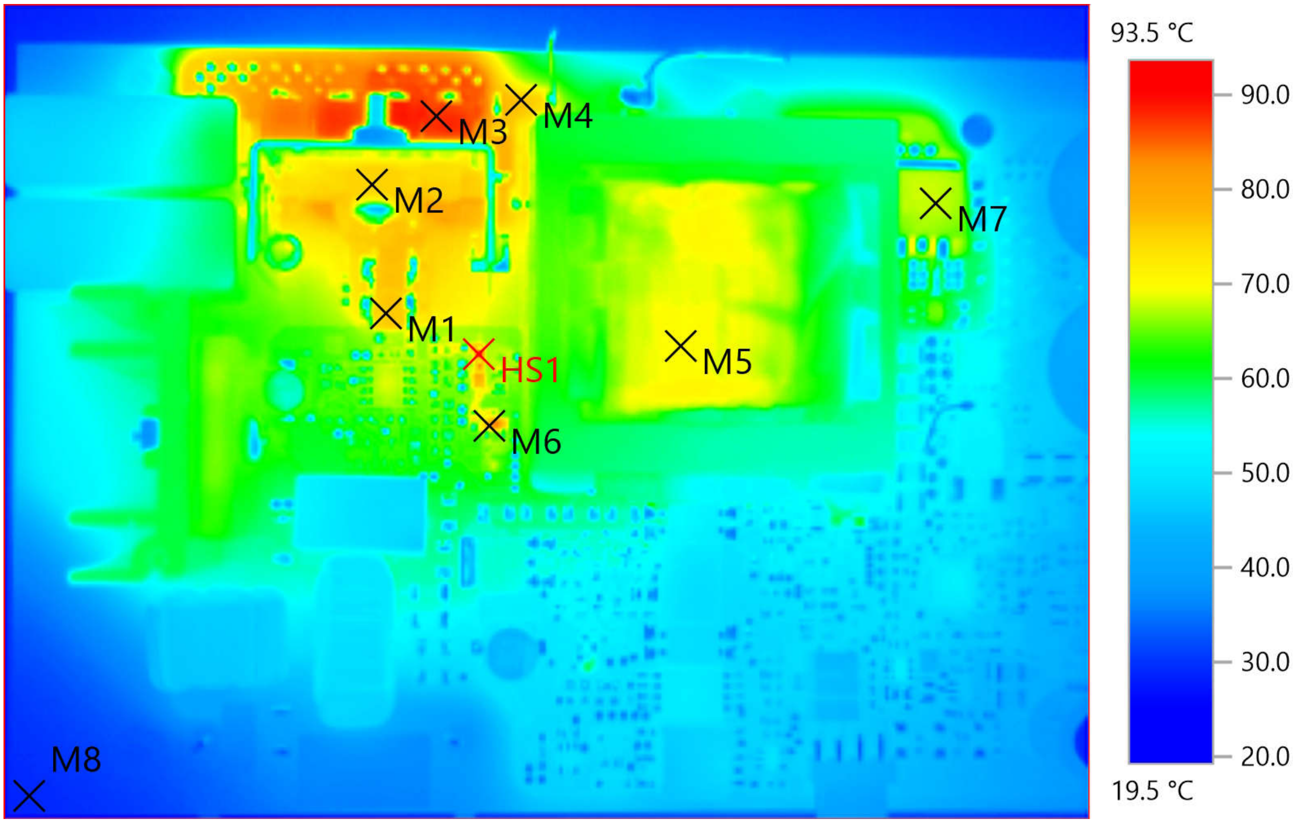


Figure 2-7. Thermal Image

Table 2-5. Thermal Data

Name	Temp. [°C]
Board temperature	26.2
D104	86.1
Q4	74.1
Q5	62.9
Q6	70.0
R12	72.1
R13	93.5
R28	70.6
T1	65.0

2.9 Bode Plots

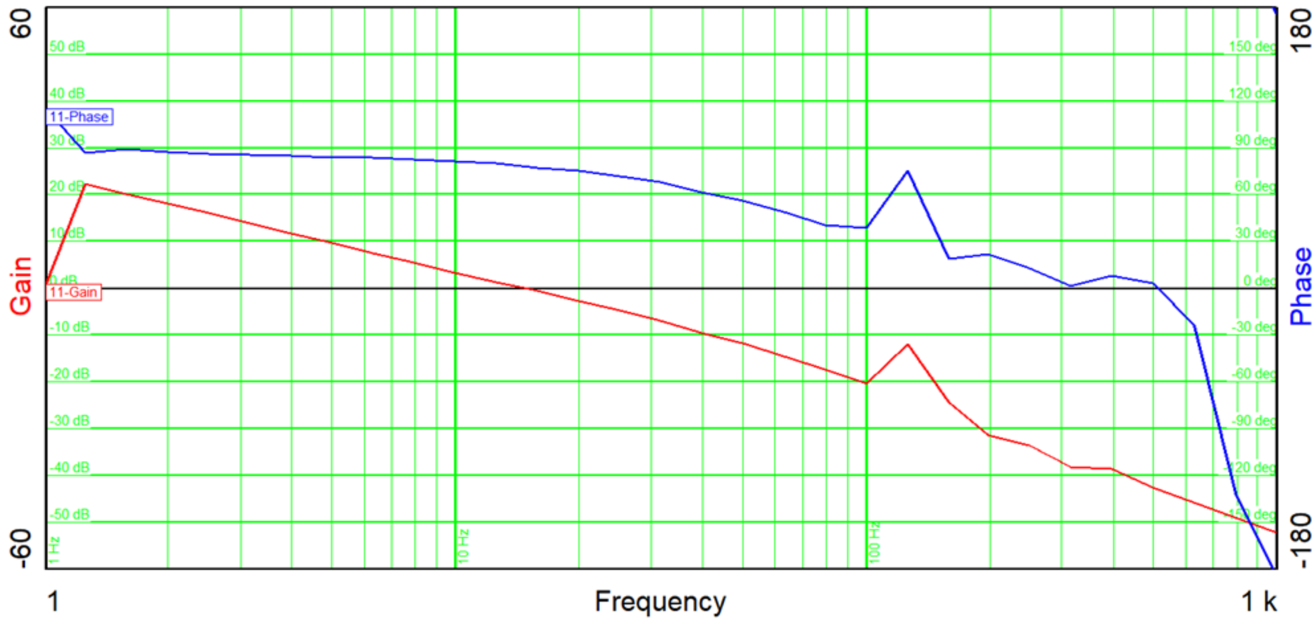


Figure 2-8. Bode Plot for 115V_{AC} Input Voltage

Table 2-6. Bode Plot Results

	115V_{IN}
Loop bandwidth (Hz)	17.7
Phase margin	78°
Slope (20dB/decade)	-0.96
Gain margin (dB)	-43
Slope (20dB/decade)	-1.59
Roll off freq (Hz)	513

3 Waveforms

3.1 Switching

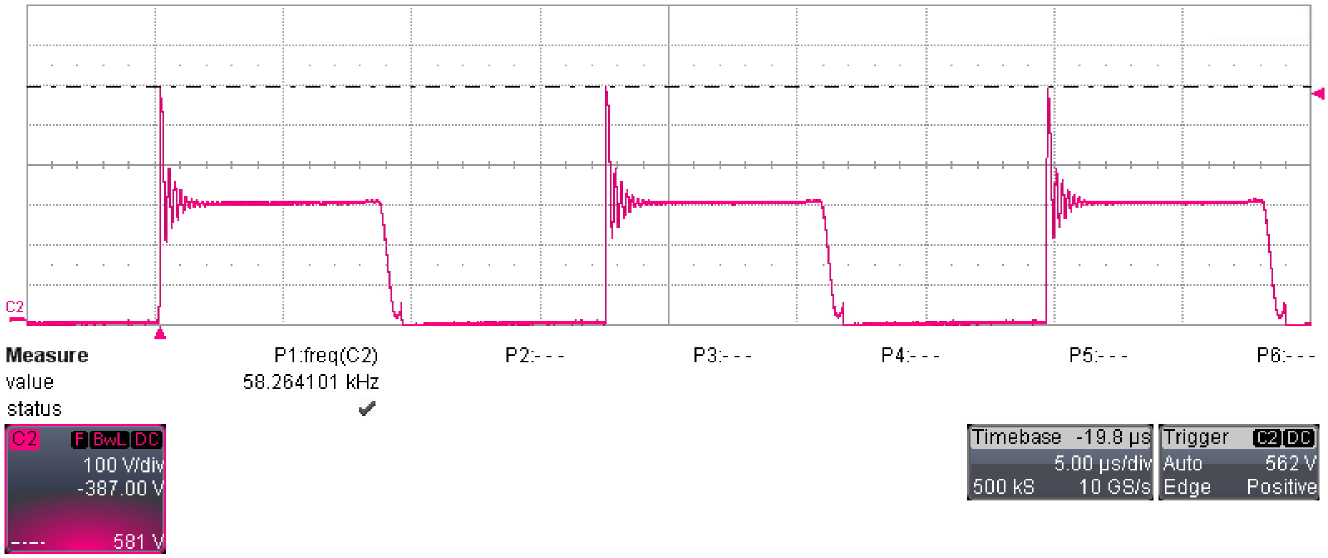


Figure 3-1. SW Node (Drain of Q6 Referred to PGND)

- 100V / div
- 5µs / div

3.2 Output Voltage Ripple

3.2.1 V_{AC_U}

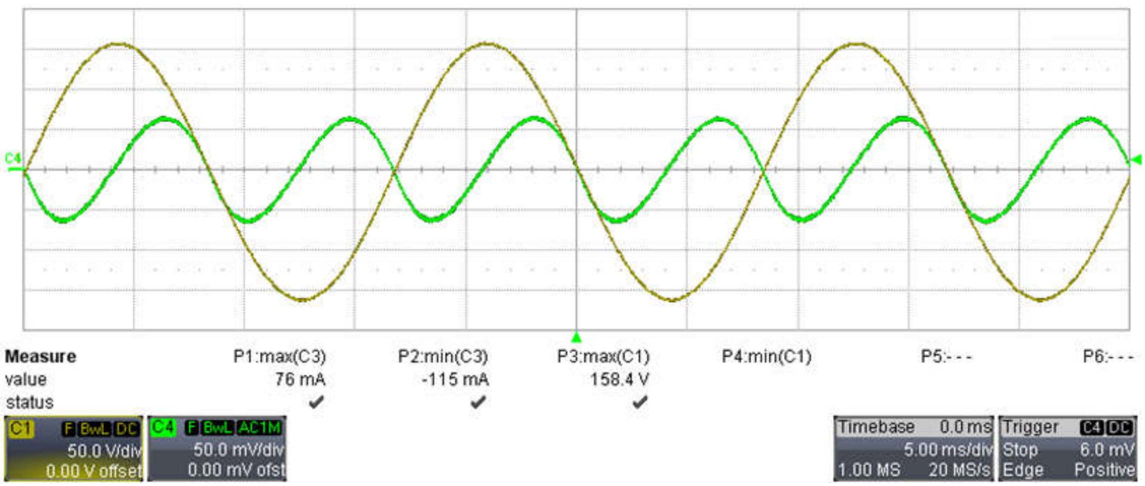


Figure 3-2. Output Voltage Ripple V_{AC_U} at $115V_{IN}$ and PFC off

C1
Input Voltage
50V / div

C4
V_{AC_U}
50mV / div

5ms / div

3.2.2 V_{SYS}

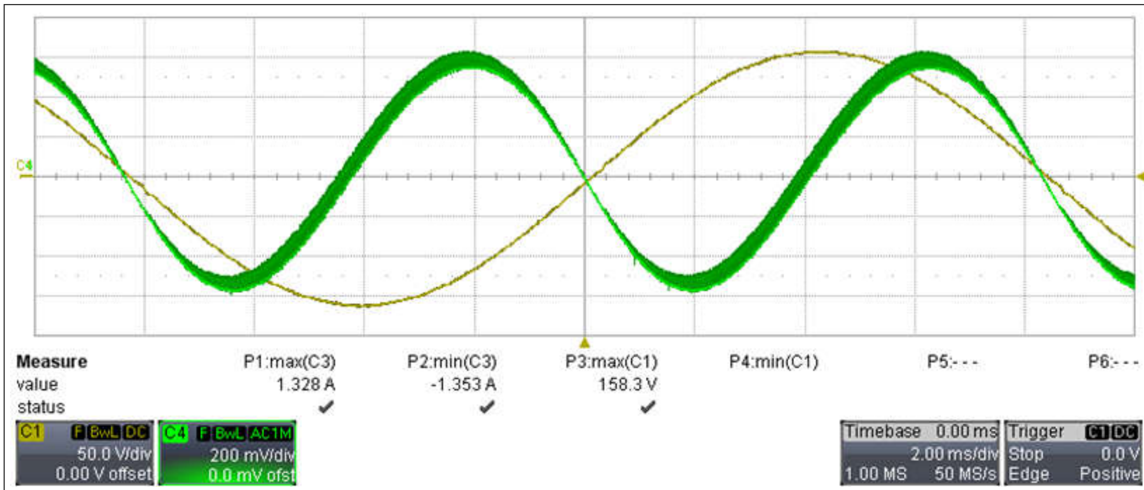


Figure 3-3. Output Voltage Ripple V_{SYS} at $115V_{IN}$ and PFC Off

C1
Input Voltage
50V / div

C4
V_{sys}
200mV / div

2ms / div

3.3 Input Voltage Ripple

3.3.1 95V_{AC} Input Voltage

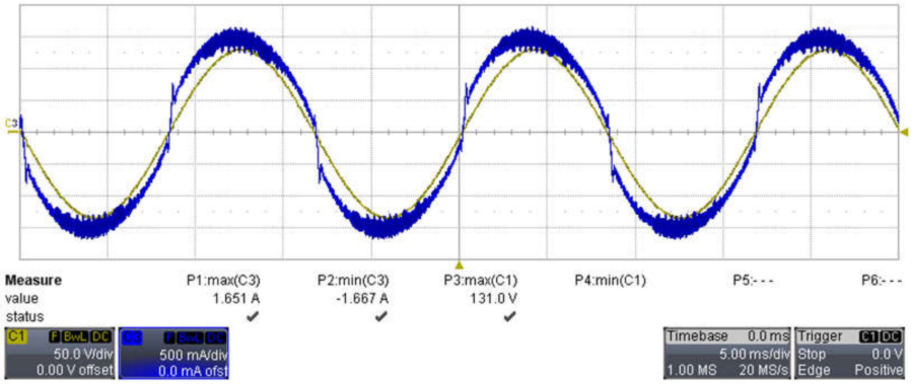


Figure 3-4. Waveform of 95V $_{AC}$ Input Voltage and Current

C1
Input Voltage
50V / div

C3
Input Current
500mA / div

5ms / div

3.3.2 115V_{AC} Input Voltage

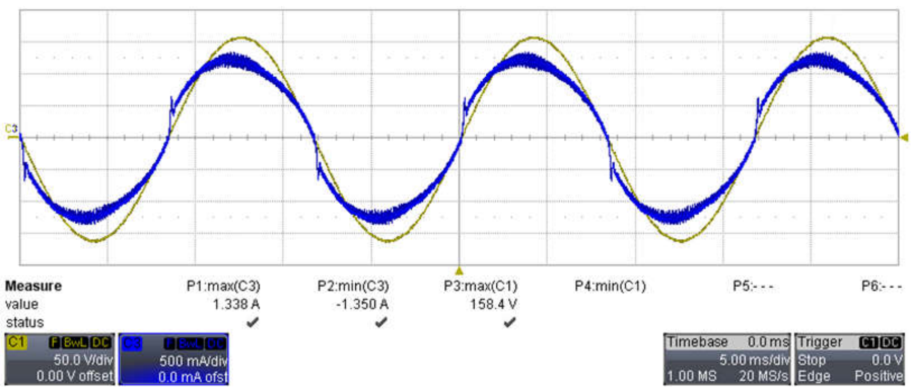


Figure 3-5. Waveform of 115V $_{AC}$ Input Voltage and Current

C1
Input Voltage
50V / div

C3
Input Current
500mA / div

5ms / div

3.3.3 132V_{AC} Input Voltage

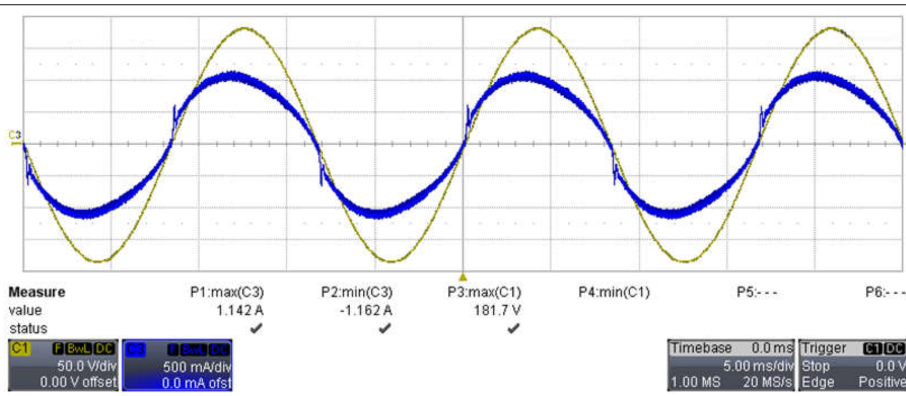


Figure 3-6. Waveform of 132V $_{AC}$ Input Voltage and Current

C1
Input Voltage
50V / div

C3
Input Current
500mA / div

5ms / div

3.4 Load Transients

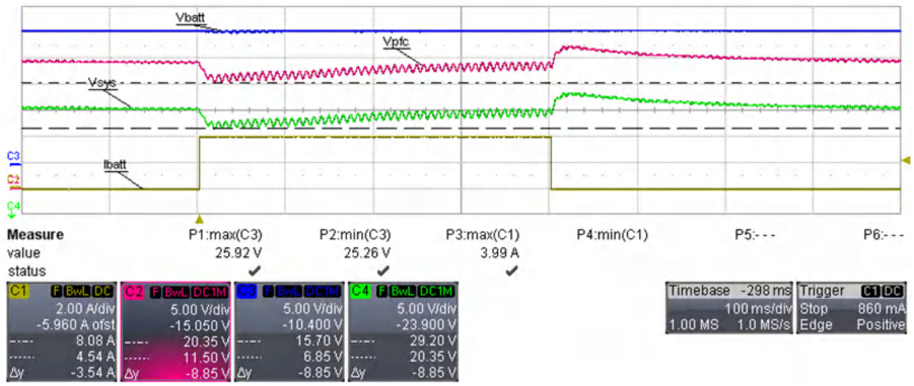


Figure 3-7. 0A to 4A Transient at $115V_{AC}$-Input Voltage

C3
V_{BATT}
5V / div

C2
V_{PFC}
5V / div

C4
V_{SYS}
5V / div

C1
I_{BATT}
2A / div

100ms / div

3.5 Start-up Sequence

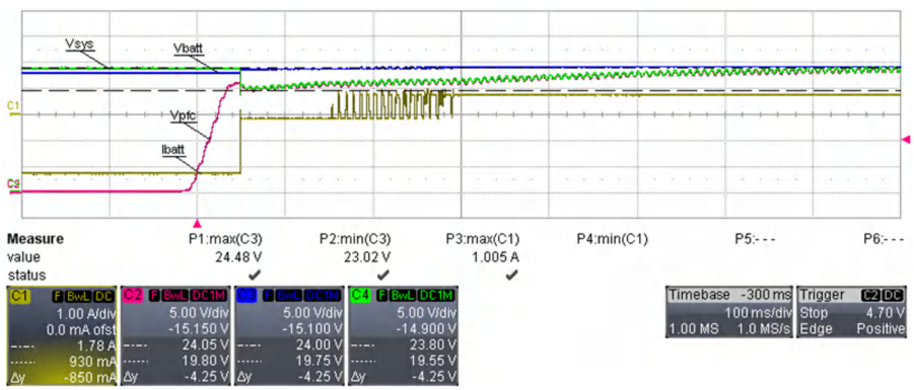


Figure 3-8. Start-up Sequence for $115V_{AC}$ Input Voltage

C3
V_{BATT}
5V / div

C2
V_{PFC}
5V / div

C4
V_{SYS}
5V / div

C1
I_{BATT}
1A / div

100ms / div

Figure 3-9 displays the same waveform as in Figure 3-8 with a different time base.

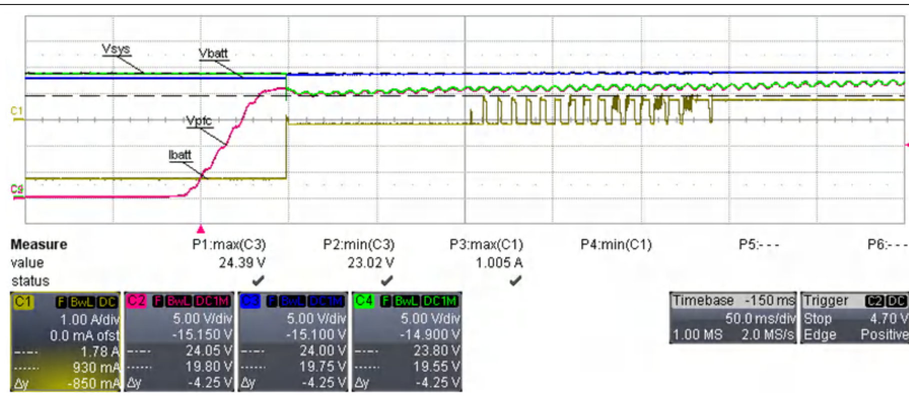


Figure 3-9. Start-up Sequence for $115V_{AC}$ Input Voltage

C3
V_{BATT}
5V / div

C2
V_{PFC}
5V / div

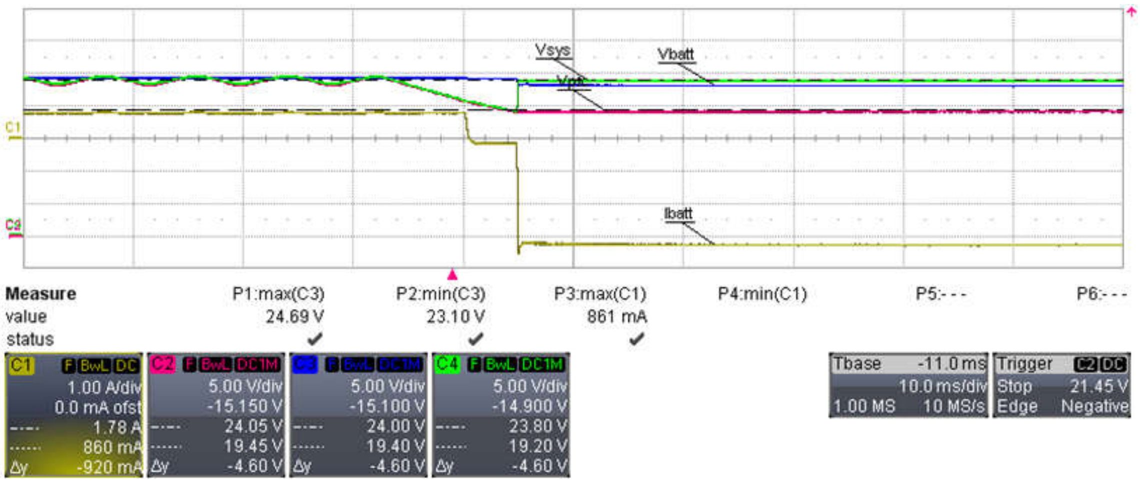
C4
V_{SYS}
5V / div

C1
I_{BATT}
1A / div

50ms / div

3.6 Mains Fail 115V_{AC} Input Voltage

3.6.1 3A system Current



C4
V_{SYS}
5V / div

C3
V_{BATT}
5V / div

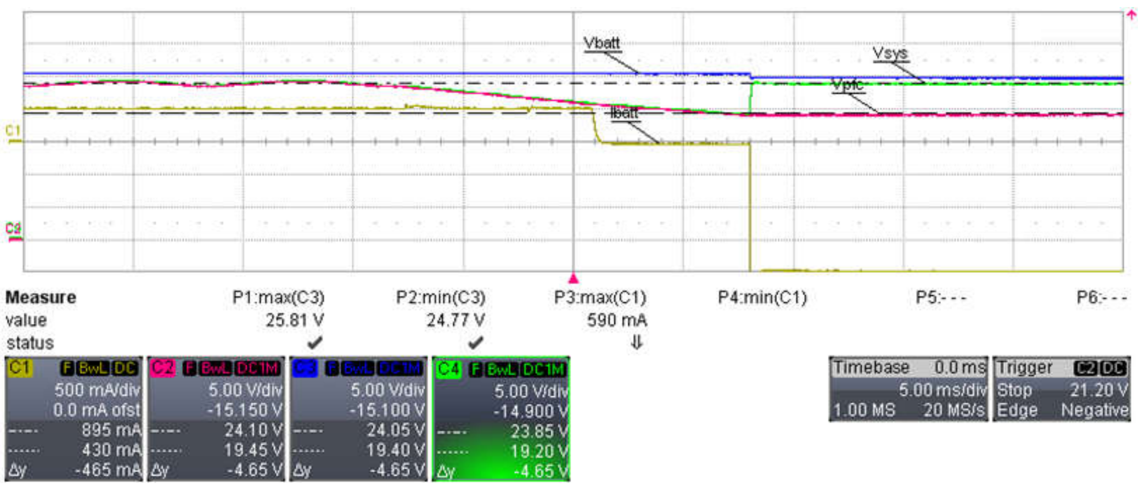
C1
I_{BATT}
1A / div

C2
V_{PFC}
5V / div

10ms / div

Figure 3-10. Mains Fail at 3A System Current

3.6.2 2A System Current



C4
V_{SYS}
5V / div

C3
V_{BATT}
5V / div

C1
I_{BATT}
500mA / div

C2
V_{PFC}
5V / div

5ms / div

Figure 3-11. Mains Fail at 2A System Current