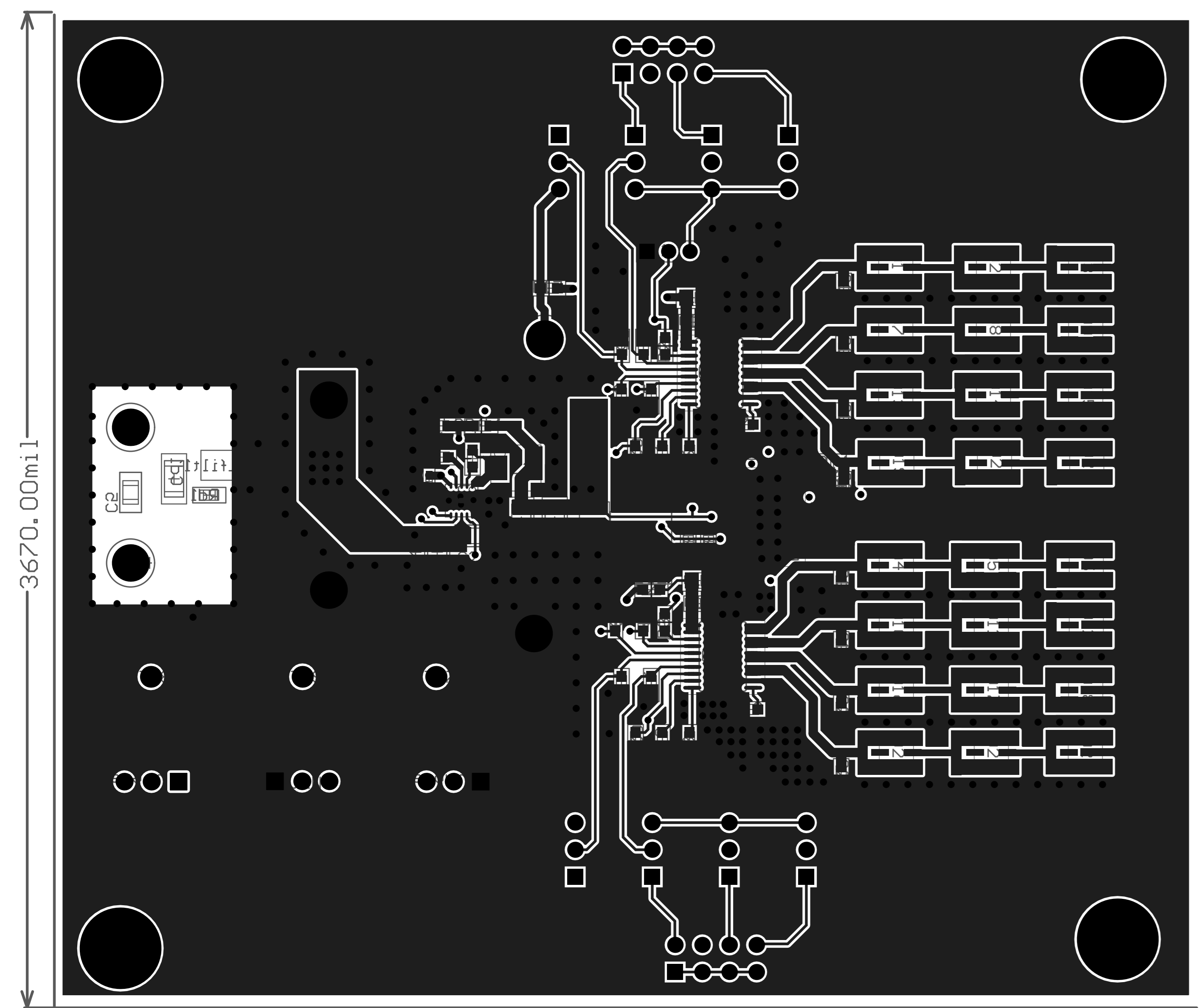


Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



3670.00mil

4220.00mil

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
REFERENCE: AS SHOWN NC_DRILL FILES
PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
SILKSCREEN: TOP BOTTOM
SILKSCREEN COLOR: WHITE OTHER _____
SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEUM/01LAEUM

DESIGNED FOR: Public Release

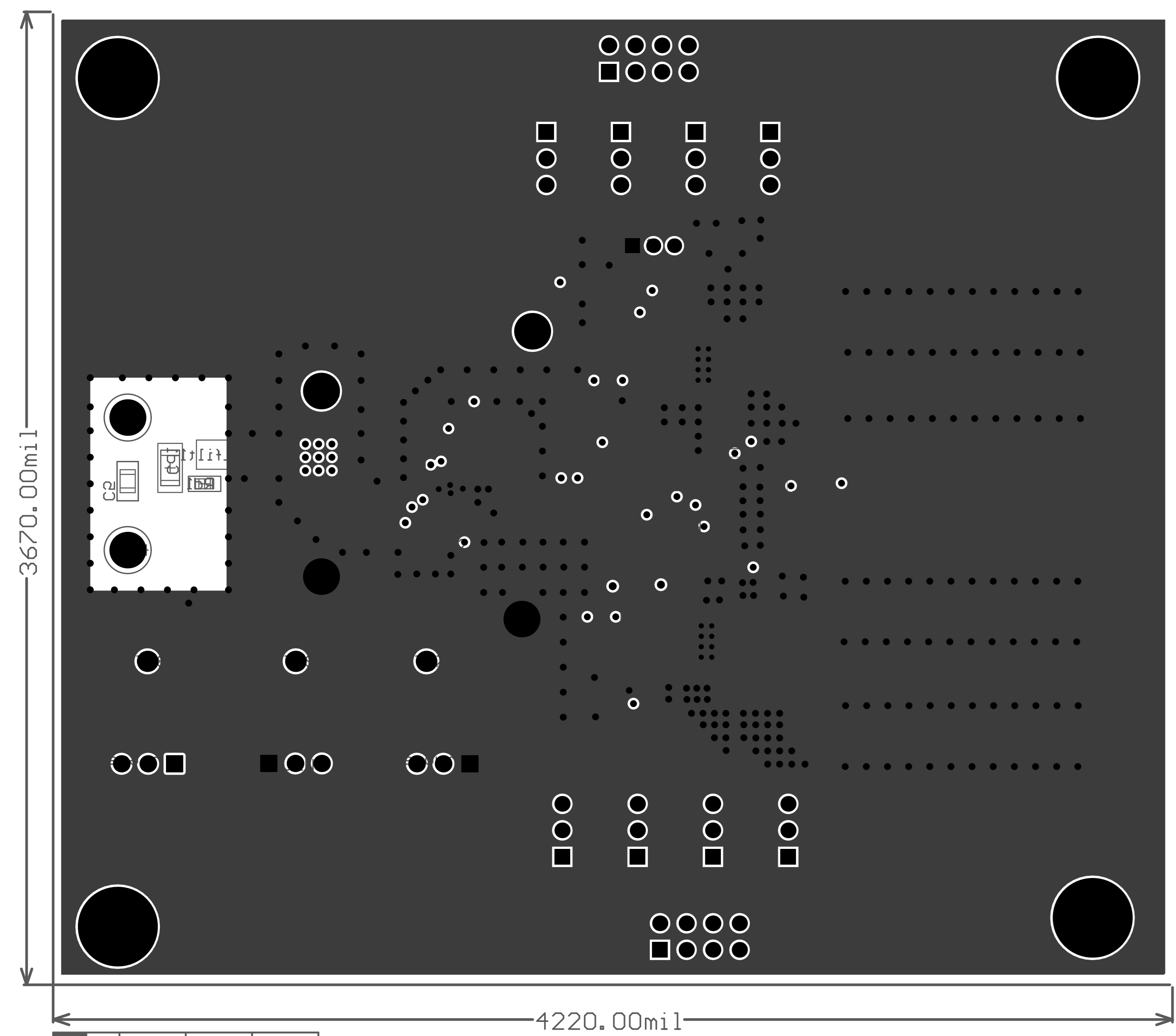
FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Component Side	GENERATED : 9/26/2016 3:37:38 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner	LAYOUT BY: Robert Blattner
SCALE: 1.00	ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	TID #: TIDA-01348			
PLOT NAME = MidLayer1	GENERATED : 9/26/2016 3:37:40 PM	TEXAS INSTRUMENTS		

TEXAS INSTRUMENTS

PROJECT TITLE: LM53600NAEVM/01LAEVM

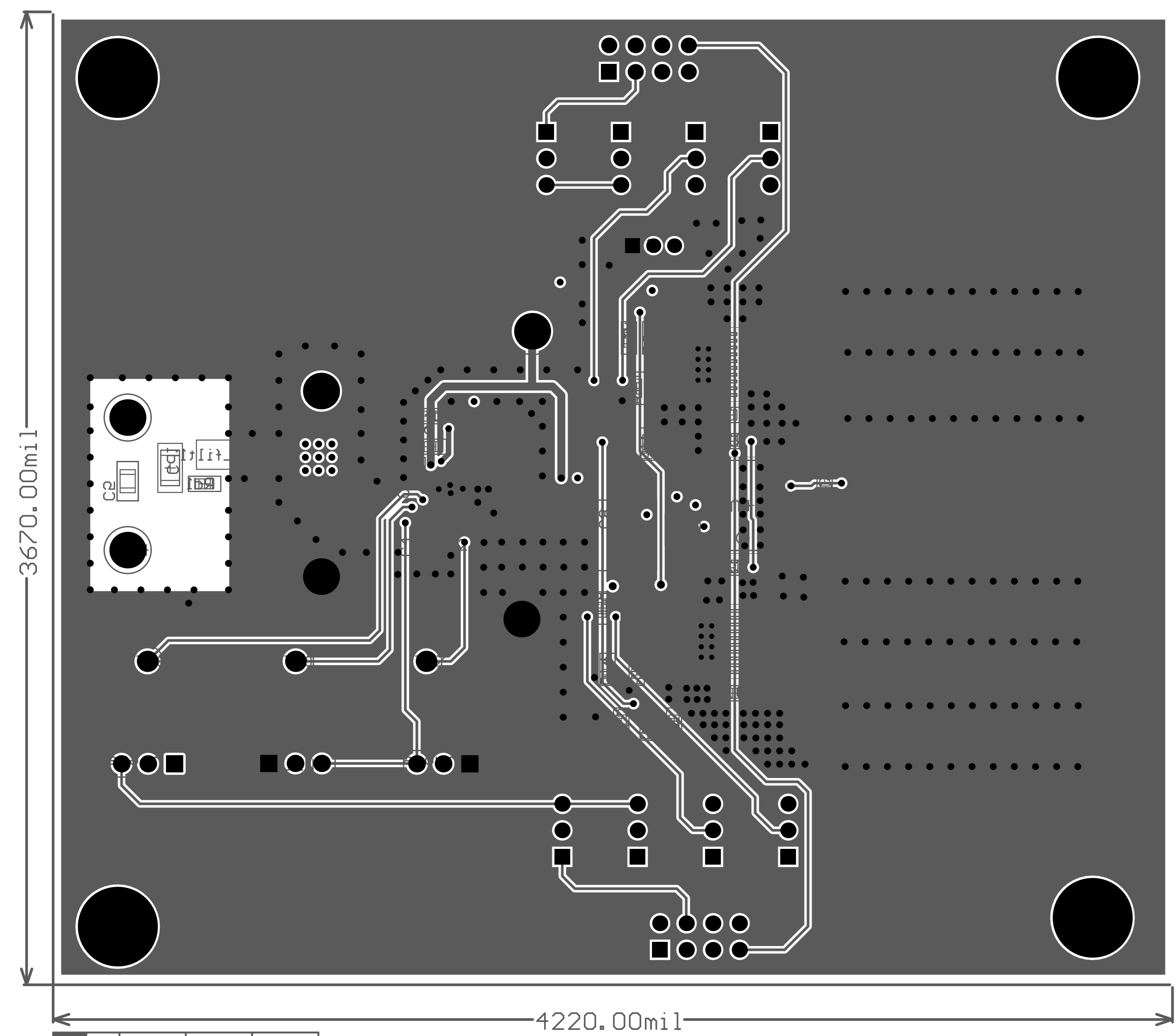
DESIGNED FOR: Public Release

FILE NAME: TIDA01348.PcbDoc

ENGINEER: Robert Blattner LAYOUT BY: Robert Blattner

SCALE: 1.00 ALTUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.
LAYER NAME =	TID #: TIDA-01348			
PLOT NAME = Mid-Layer 2	GENERATED : 9/26/2016 3:37:45 PM	TEXAS INSTRUMENTS		

TEXAS INSTRUMENTS

PROJECT TITLE: LM53600NAEVM/01LAEVM

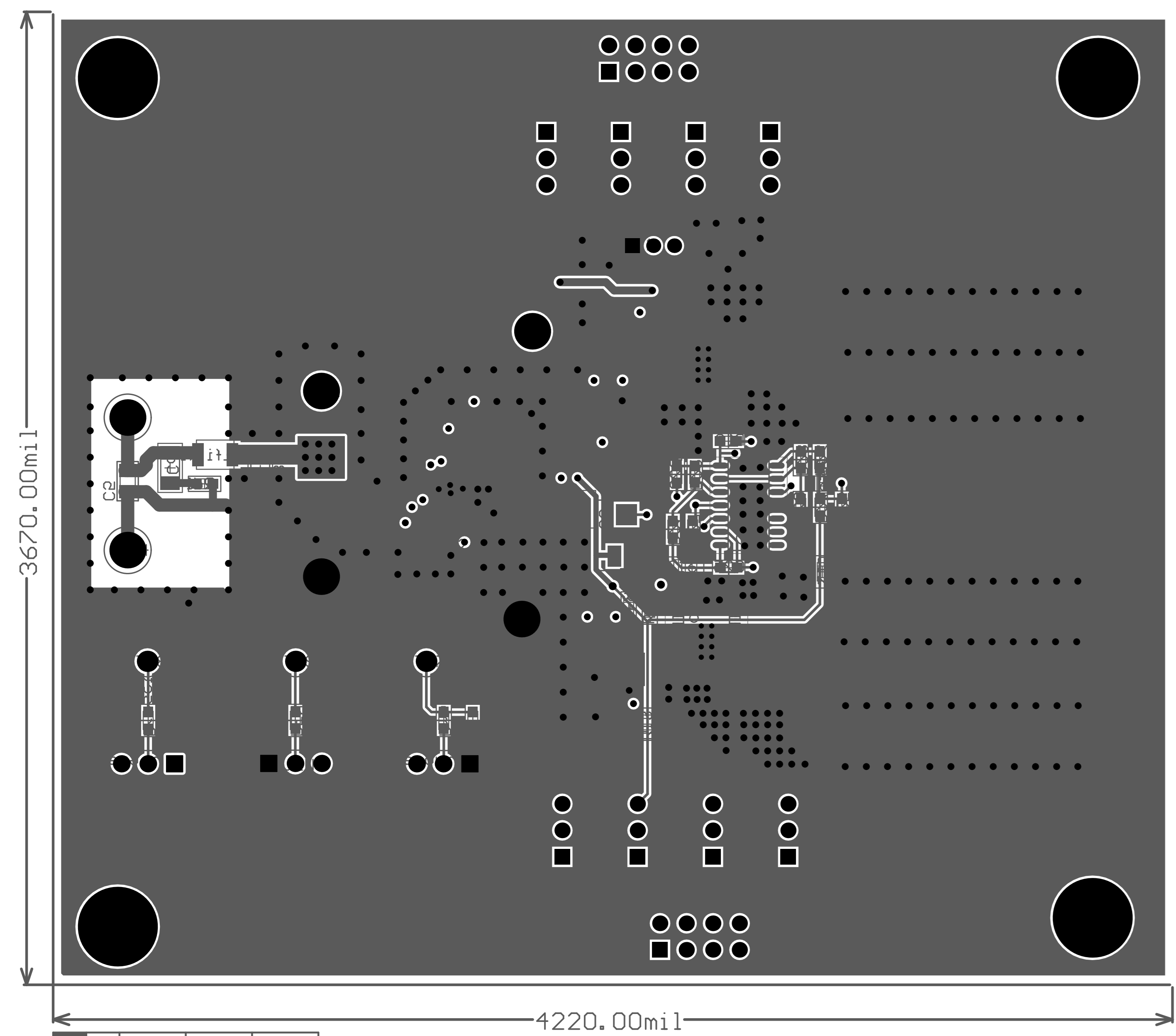
DESIGNED FOR: Public Release

FILE NAME: TIDA01348.PcbDoc

ENGINEER: Robert Blattner LAYOUT BY: Robert Blattner

SCALE: 1.00 ALTUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK



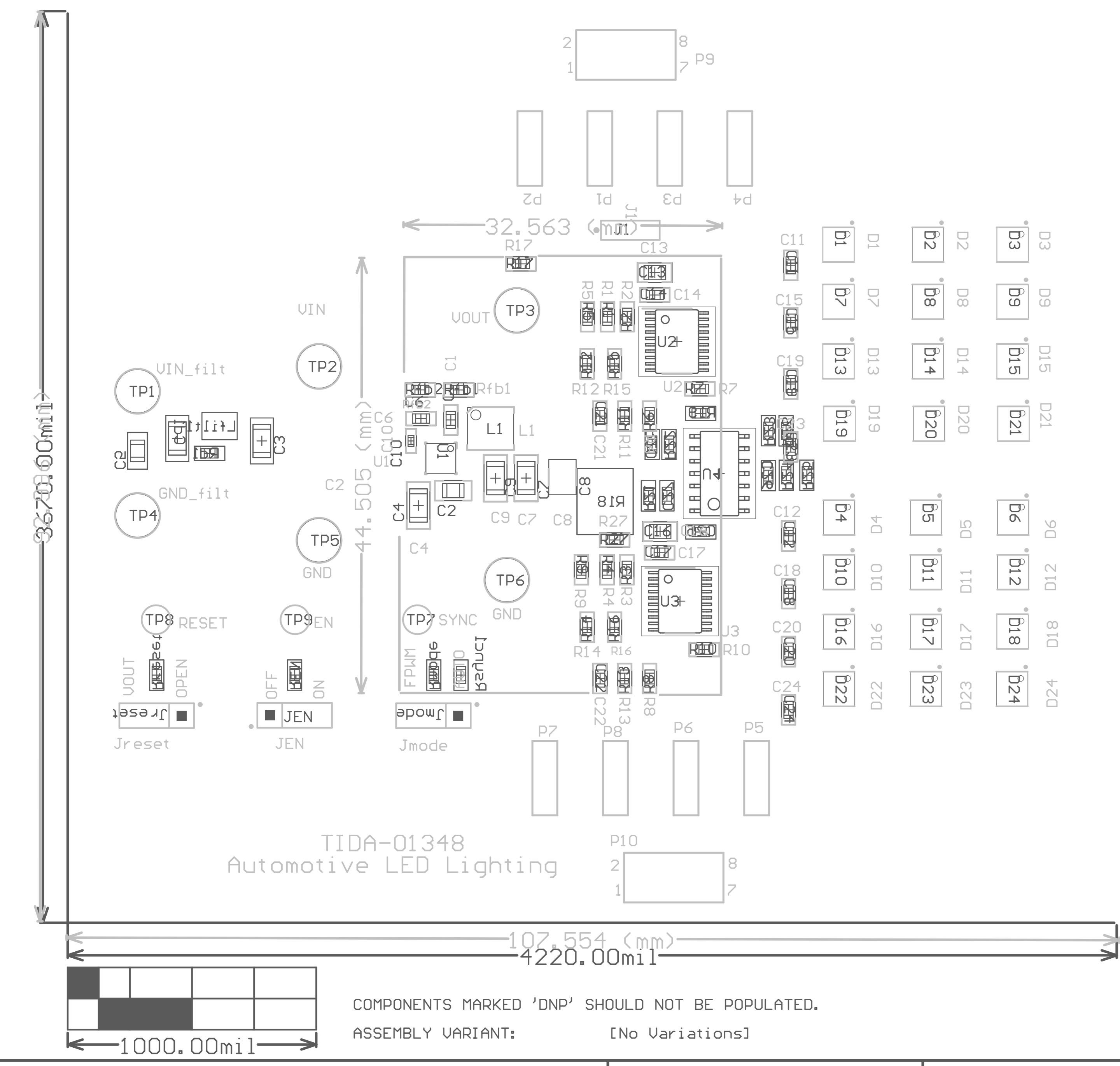
PROJECT TITLE: LM53600NAEUM/01LAEUM
 DESIGNED FOR: Public Release
 FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Solder Side	GENERATED : 9/26/2016 3:37:48 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
 LAYOUT BY: Robert Blattner
 SCALE: 1.00
 ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM
 DESIGNED FOR: Public Release
 FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Top Silkscreen Overlay	GENERATED : 9/26/2016 3:37:58 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
 LAYOUT BY: Robert Blattner
 SCALE: 1.00
 ALTUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
REFERENCE: AS SHOWN NC_DRILL FILES
PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
SILKSCREEN: TOP BOTTOM
SILKSCREEN COLOR: WHITE OTHER _____
SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM

DESIGNED FOR: Public Release

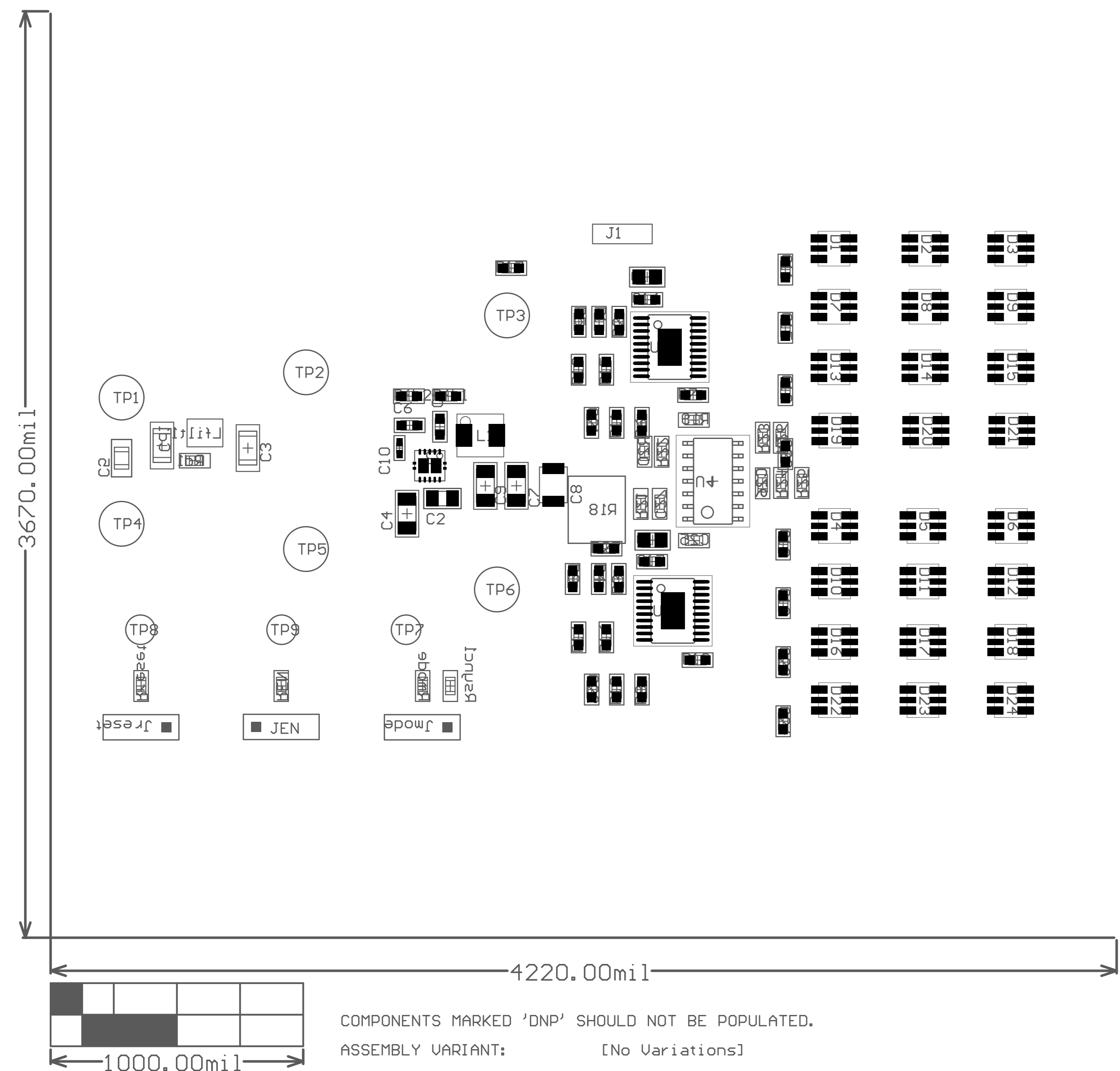
FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Bottom Silkscreen Overlay	GENERATED : 9/26/2016 3:37:56 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner	LAYOUT BY: Robert Blattner
SCALE: 1.00	ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
THICKNESS: 62 ML (1.6mm) +/-10% OTHER _____
TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
REFERENCE: AS SHOWN NC_DRILL FILES
PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
SILKSCREEN: TOP BOTTOM
SILKSCREEN COLOR: WHITE OTHER _____
SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL SILK



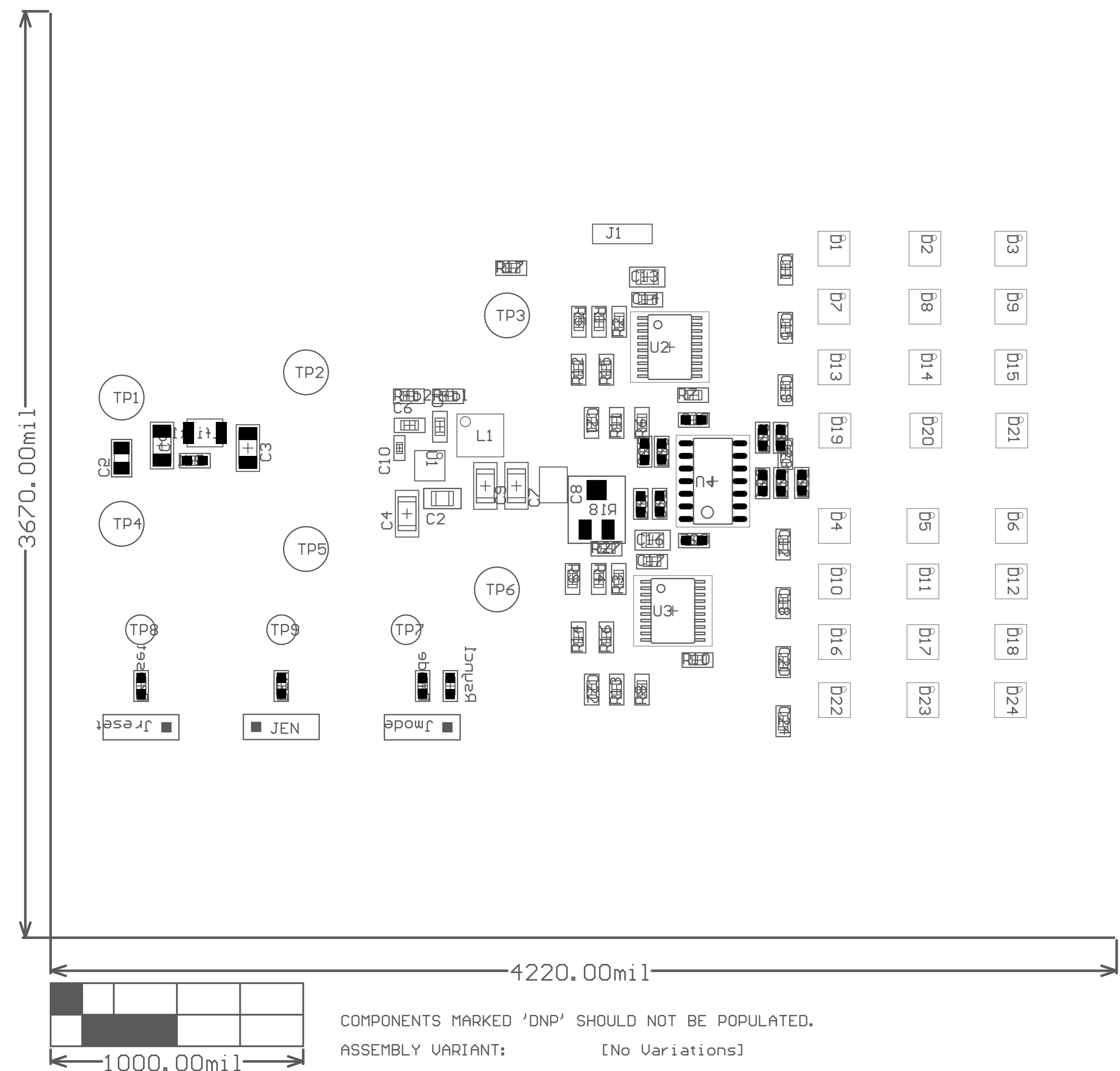
PROJECT TITLE: LM53600NAEVM/01LAEVM
DESIGNED FOR: Public Release
FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Top Paste Mask Print	GENERATED : 9/26/2016 3:38:00 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
LAYOUT BY: Robert Blattner
SCALE: 1.00
ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
THICKNESS: 62 ML (1.6mm) +/-10% OTHER _____
TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
REFERENCE: AS SHOWN NC_DRILL FILES
PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
SILKSCREEN: TOP BOTTOM
SILKSCREEN COLOR: WHITE OTHER _____
SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL SILK

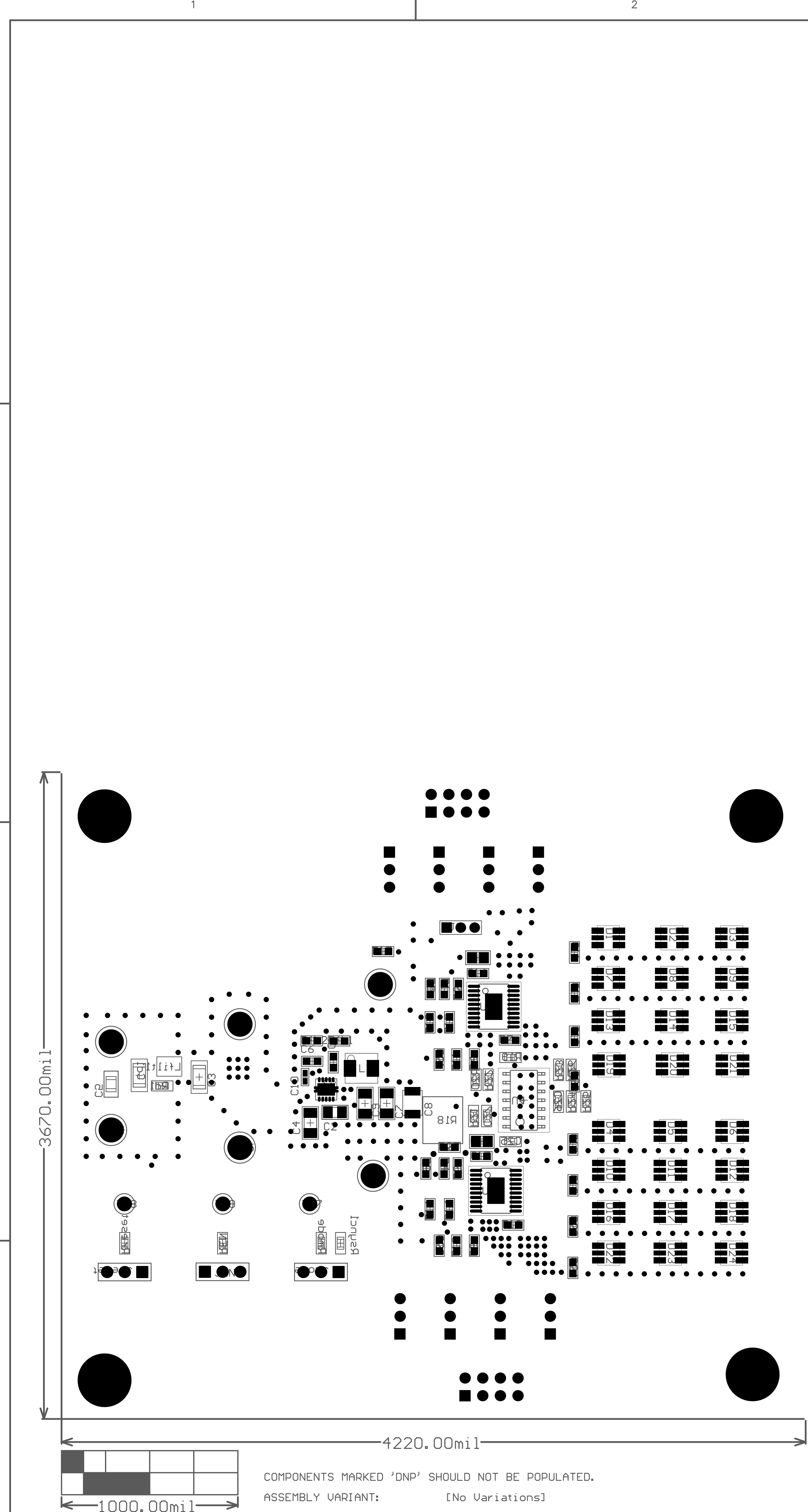


PROJECT TITLE: LM53600NAEVM/01LAEVM
DESIGNED FOR: Public Release
FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Bottom Paste Mask Print	GENERATED : 9/26/2016 3:38:02 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
LAYOUT BY: Robert Blattner
SCALE: 1.00
ALTIUM DESIGNER VERSION: 16.0.9.368



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK

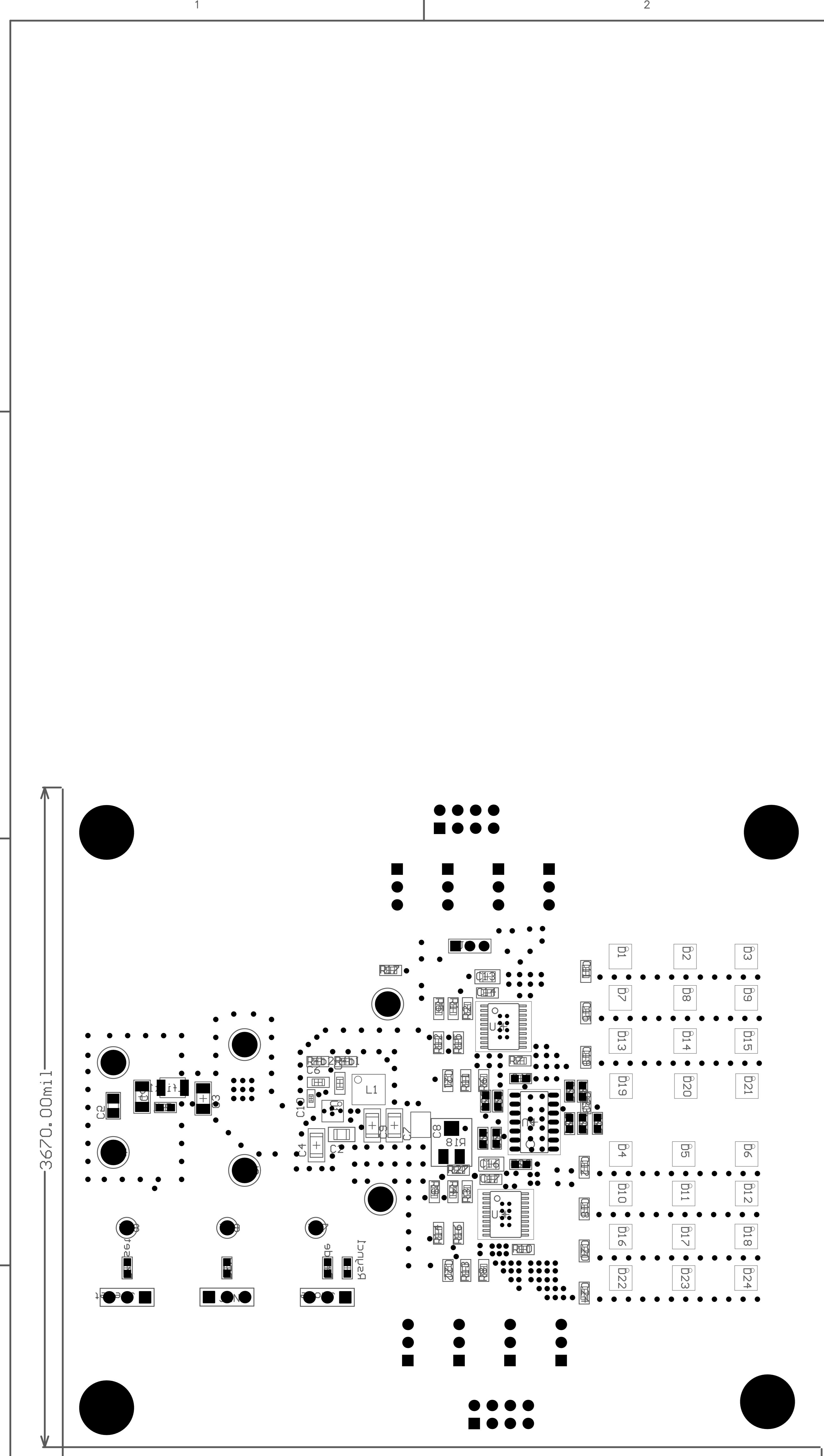


PROJECT TITLE: LM53600NAEVM/01LAEVM
 DESIGNED FOR: Public Release
 FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Top Solder Mask Print	GENERATED : 9/26/2016 3:38:08 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
 LAYOUT BY: Robert Blattner
 SCALE: 1.00
 ALTUM DESIGNER VERSION: 16.0.9.368



3670.00mil

4220.00mil

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____

THICKNESS: 62 ML (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM

DESIGNED FOR: Public Release

FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Bottom Solder Mask Print	GENERATED : 9/26/2016 3:38:10 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner

LAYOUT BY: Robert Blattner

SCALE: 1.00

ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM
 DESIGNED FOR: Public Release
 FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Mechanical 1	GENERATED : 9/26/2016 3:38:13 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
 LAYOUT BY: Robert Blattner
 SCALE: 1.00
 ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
REFERENCE: AS SHOWN NC_DRILL FILES
PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
SILKSCREEN: TOP BOTTOM
SILKSCREEN COLOR: WHITE OTHER _____
SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM
DESIGNED FOR: Public Release
FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Mechanical 2	GENERATED : 9/26/2016 3:38:18 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
LAYOUT BY: Robert Blattner
SCALE: 1.00
ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
REFERENCE: AS SHOWN NC_DRILL FILES
PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
SILKSCREEN: TOP BOTTOM
SILKSCREEN COLOR: WHITE OTHER _____
SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM

DESIGNED FOR: Public Release

FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Mechanical 3	GENERATED : 9/26/2016 3:38:20 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner

LAYOUT BY: Robert Blattner

SCALE: 1.00

ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM
 DESIGNED FOR: Public Release
 FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Mechanical 4	GENERATED : 9/26/2016 3:38:29 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
 LAYOUT BY: Robert Blattner
 SCALE: 1.00
 ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM
 DESIGNED FOR: Public Release
 FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Mechanical 5	GENERATED : 9/26/2016 3:38:29 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
 LAYOUT BY: Robert Blattner
 SCALE: 1.00
 ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
REFERENCE: AS SHOWN NC_DRILL FILES
PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
SILKSCREEN: TOP BOTTOM
SILKSCREEN COLOR: WHITE OTHER _____
SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM

DESIGNED FOR: Public Release

FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Mechanical 6	GENERATED : 9/26/2016 3:38:30 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner

LAYOUT BY: Robert Blattner

SCALE: 1.00

ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
THICKNESS: 62 ML (1.6mm) +/-10% OTHER _____
TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
REFERENCE: AS SHOWN NC_DRILL FILES
PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
SILKSCREEN: TOP BOTTOM
SILKSCREEN COLOR: WHITE OTHER _____
SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM
DESIGNED FOR: Public Release
FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Mechanical 9	GENERATED : 9/26/2016 3:38:35 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
LAYOUT BY: Robert Blattner
SCALE: 1.00
ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
THICKNESS: 62 ML (1.6mm) +/-10% OTHER _____
TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
REFERENCE: AS SHOWN NC_DRILL FILES
PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
SILKSCREEN: TOP BOTTOM
SILKSCREEN COLOR: WHITE OTHER _____
SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM
DESIGNED FOR: Public Release
FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Mechanical 10	GENERATED : 9/26/2016 3:38:38 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
LAYOUT BY: Robert Blattner
SCALE: 1.00
ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM
 DESIGNED FOR: Public Release
 FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Mechanical 11	GENERATED : 9/26/2016 3:38:48 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
 LAYOUT BY: Robert Blattner
 SCALE: 1.00
 ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
REFERENCE: AS SHOWN NC_DRILL FILES
PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
SILKSCREEN: TOP BOTTOM
SILKSCREEN COLOR: WHITE OTHER _____
SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM
DESIGNED FOR: Public Release
FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Mechanical 12	GENERATED : 9/26/2016 3:38:45 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
LAYOUT BY: Robert Blattner
SCALE: 1.00
ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
REFERENCE: AS SHOWN NC_DRILL FILES
PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
SILKSCREEN: TOP BOTTOM
SILKSCREEN COLOR: WHITE OTHER _____
SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM

DESIGNED FOR: Public Release

FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Mechanical 13	GENERATED : 9/26/2016 3:38:48 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner

LAYOUT BY: Robert Blattner

SCALE: 1.00

ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
REFERENCE: AS SHOWN NC_DRILL FILES
PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
SILKSCREEN: TOP BOTTOM
SILKSCREEN COLOR: WHITE OTHER _____
SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM
DESIGNED FOR: Public Release
FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Mechanical 14	GENERATED : 9/26/2016 3:38:52 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
LAYOUT BY: Robert Blattner
SCALE: 1.00
ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
REFERENCE: AS SHOWN NC_DRILL FILES
PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
SILKSCREEN: TOP BOTTOM
SILKSCREEN COLOR: WHITE OTHER _____
SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL SILK



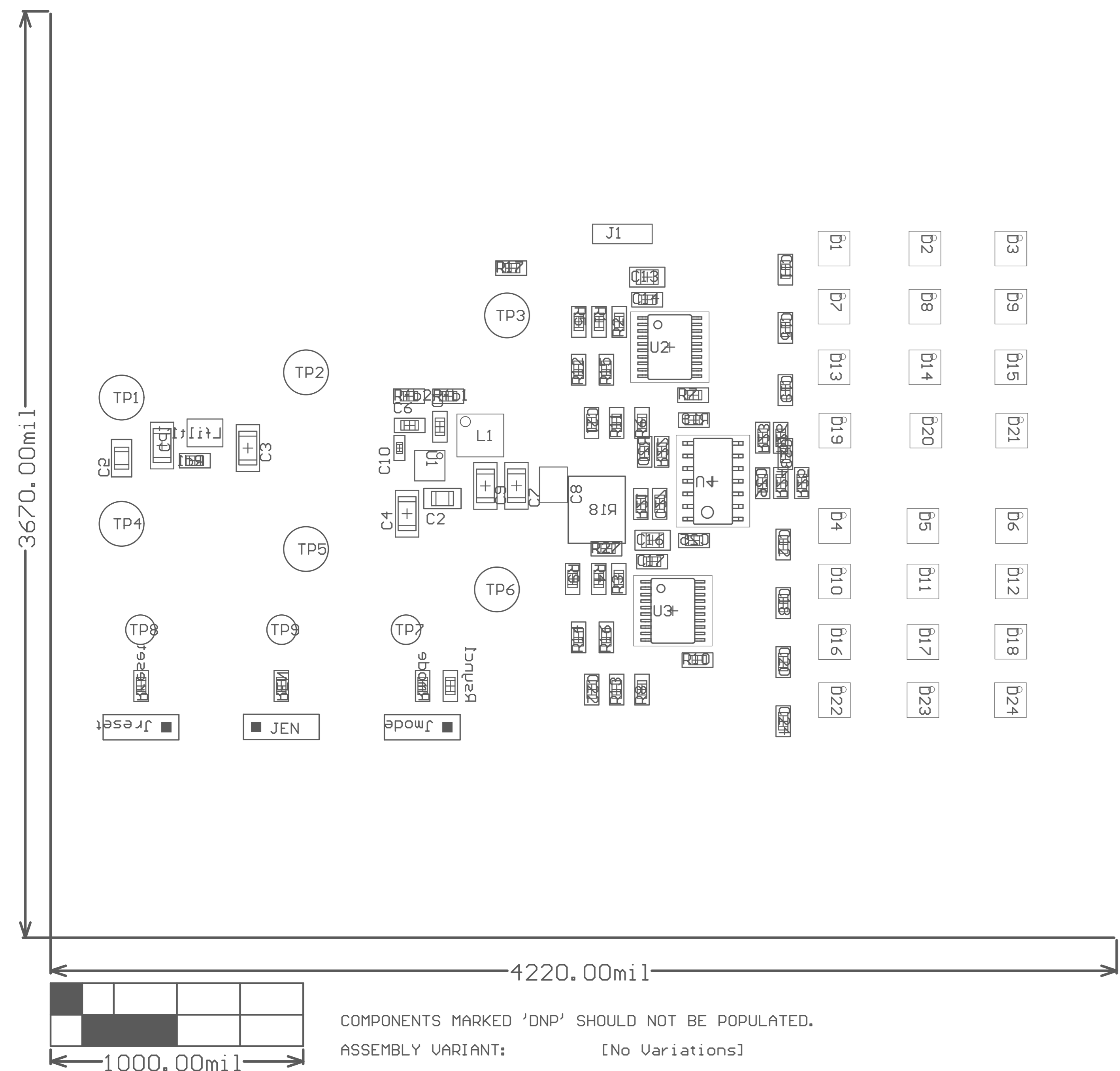
PROJECT TITLE: LM53600NAEVM/01LAEVM
DESIGNED FOR: Public Release
FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Mechanical 15	GENERATED : 9/26/2016 3:38:55 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
LAYOUT BY: Robert Blattner
SCALE: 1.00
ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
REFERENCE: AS SHOWN NC_DRILL FILES
PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
SILKSCREEN: TOP BOTTOM
SILKSCREEN COLOR: WHITE OTHER _____
SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM

DESIGNED FOR: Public Release

FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Mechanical 16	GENERATED : 9/26/2016 3:38:58 PM	TEXAS INSTRUMENTS	

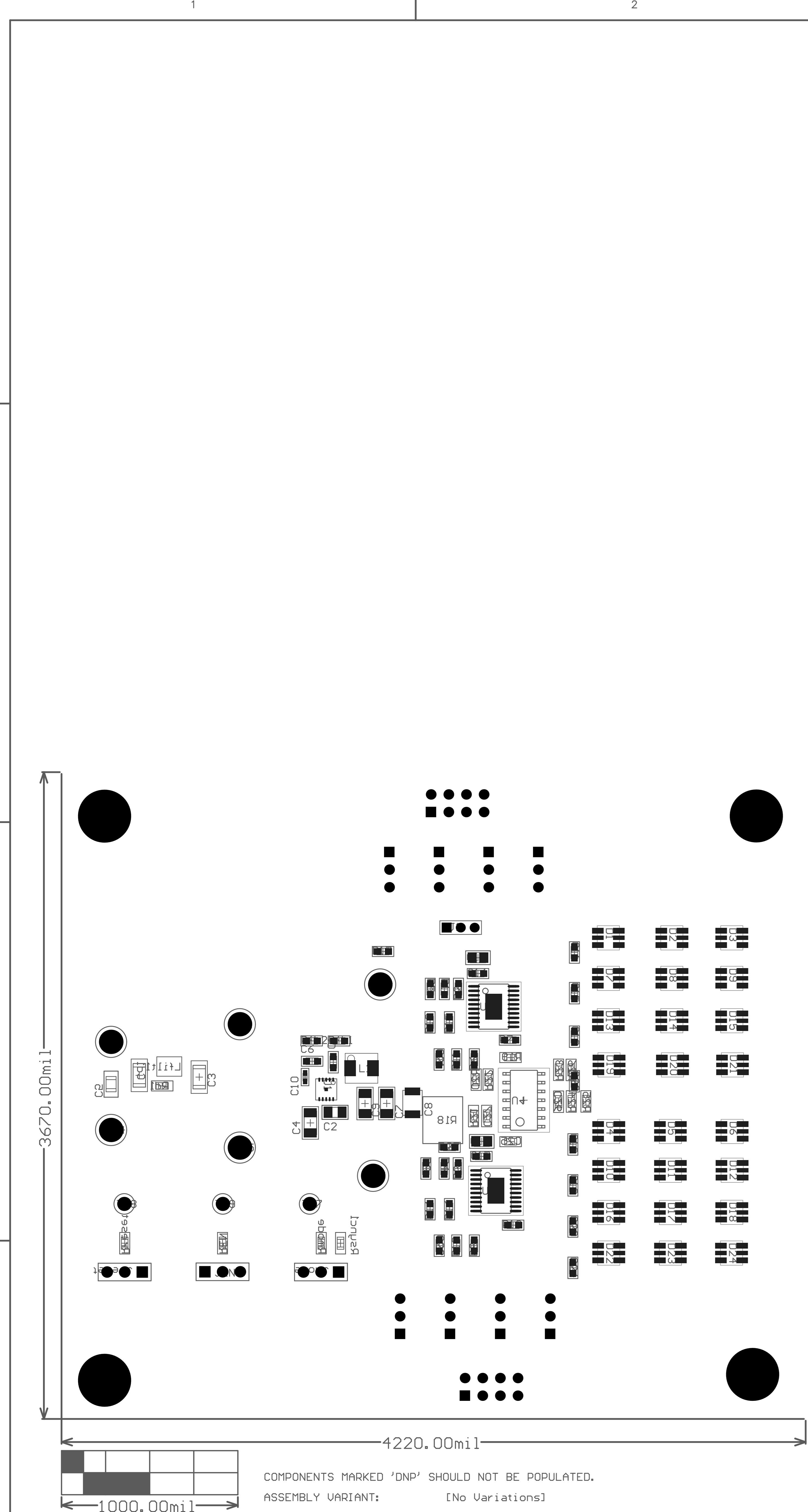
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ENGINEER: Robert Blattner

LAYOUT BY: Robert Blattner

SCALE: 1.00

ALTIUM DESIGNER VERSION: 16.0.9.368



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
 ASSEMBLY VARIANT: [No Variations]

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____

THICKNESS: 62 ML (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK

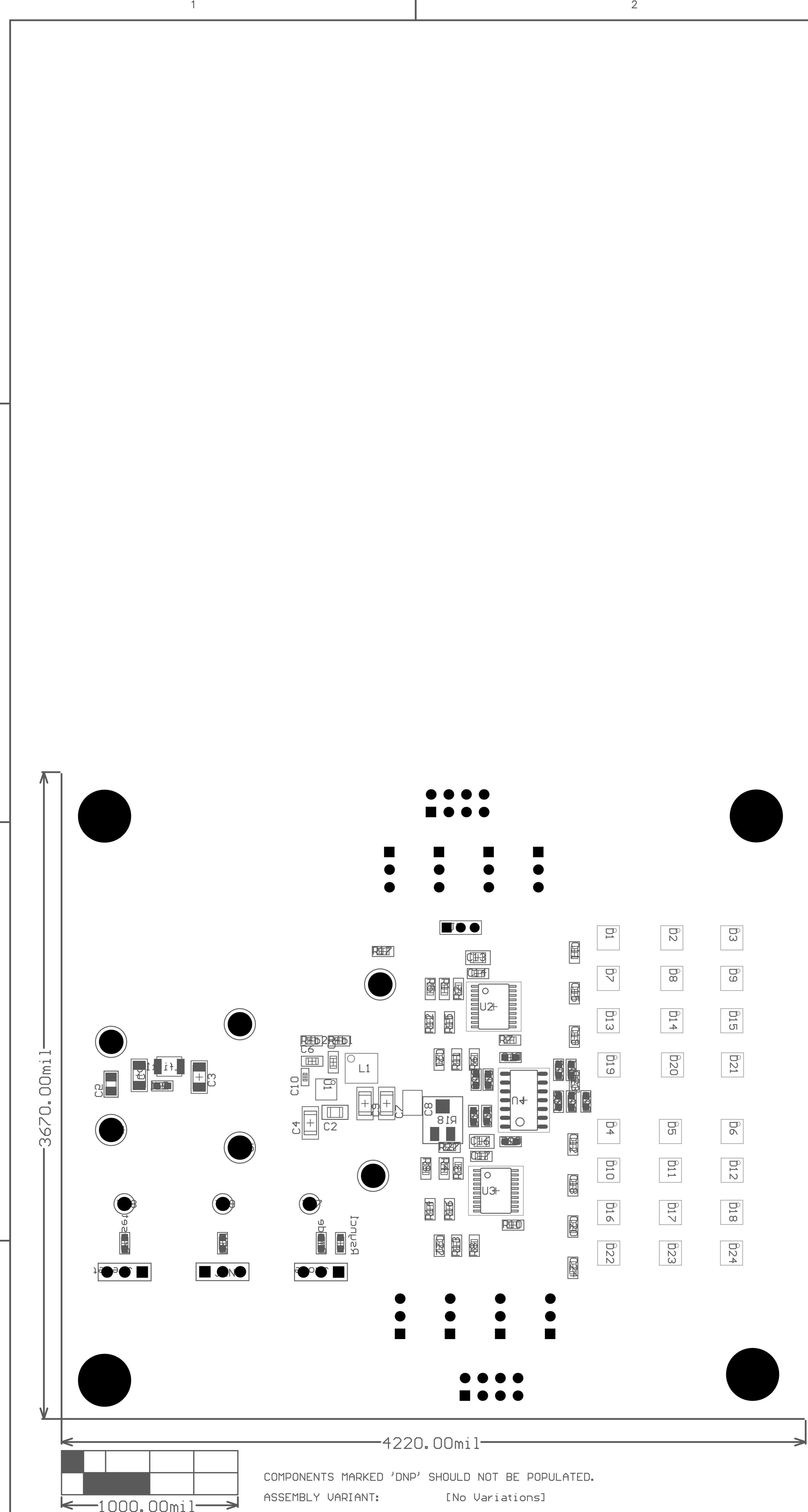


PROJECT TITLE: LM53600NAEVM/01LAEVM
 DESIGNED FOR: Public Release
 FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Top Pad Master	GENERATED : 9/26/2016 3:39:02 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
 LAYOUT BY: Robert Blattner
 SCALE: 1.00
 ALTUM DESIGNER VERSION: 16.0.9.368



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM

DESIGNED FOR: Public Release

FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Bottom Pad Master	GENERATED : 9/26/2016 3:39:05 PM	TEXAS INSTRUMENTS	

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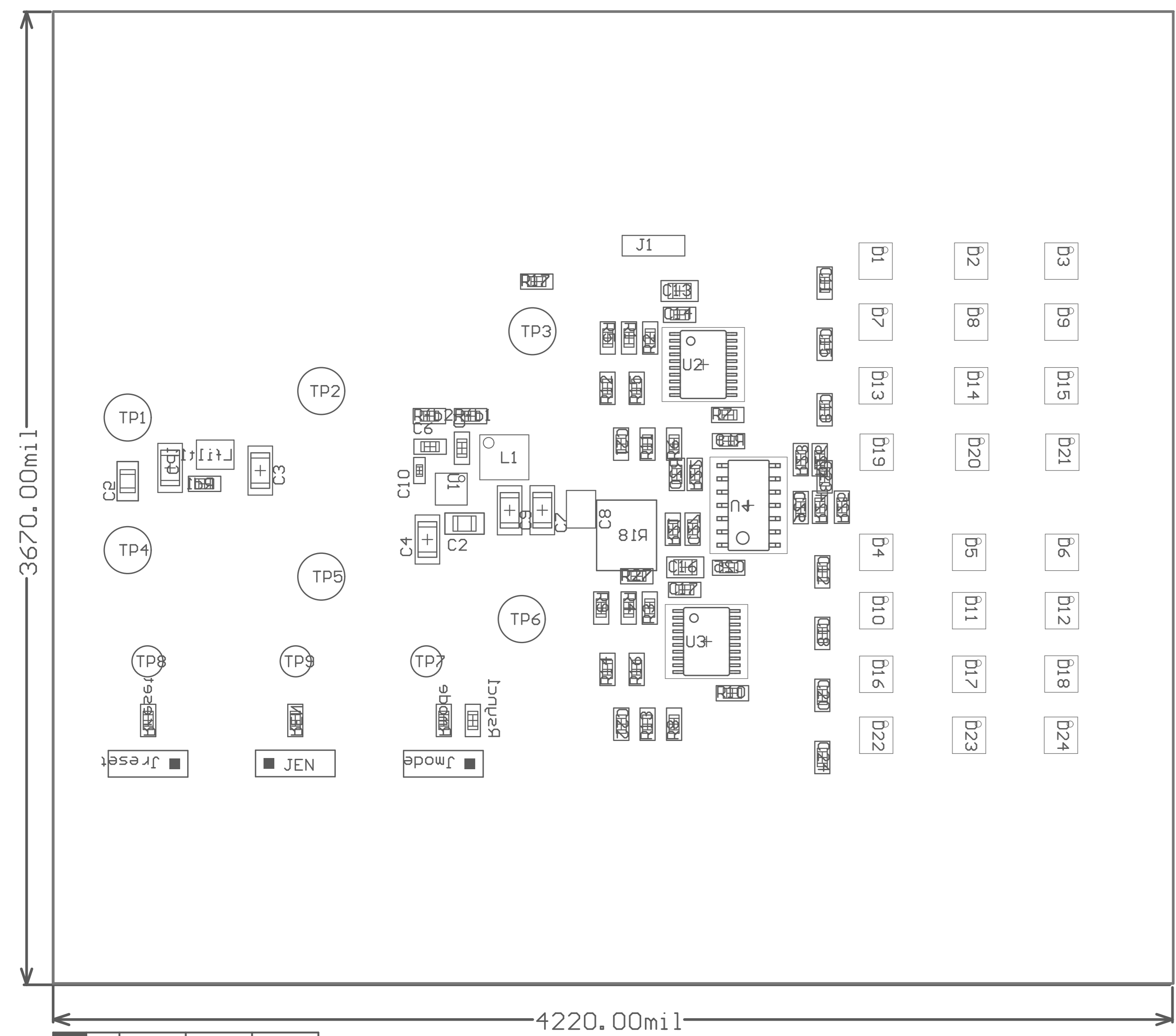
ENGINEER: Robert Blattner

LAYOUT BY: Robert Blattner

SCALE: 1.00

ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
THICKNESS: 62 ML (1.6mm) +/-10% OTHER _____
TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
REFERENCE: AS SHOWN NC_DRILL FILES
PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
SILKSCREEN: TOP BOTTOM
SILKSCREEN COLOR: WHITE OTHER _____
SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL SILK



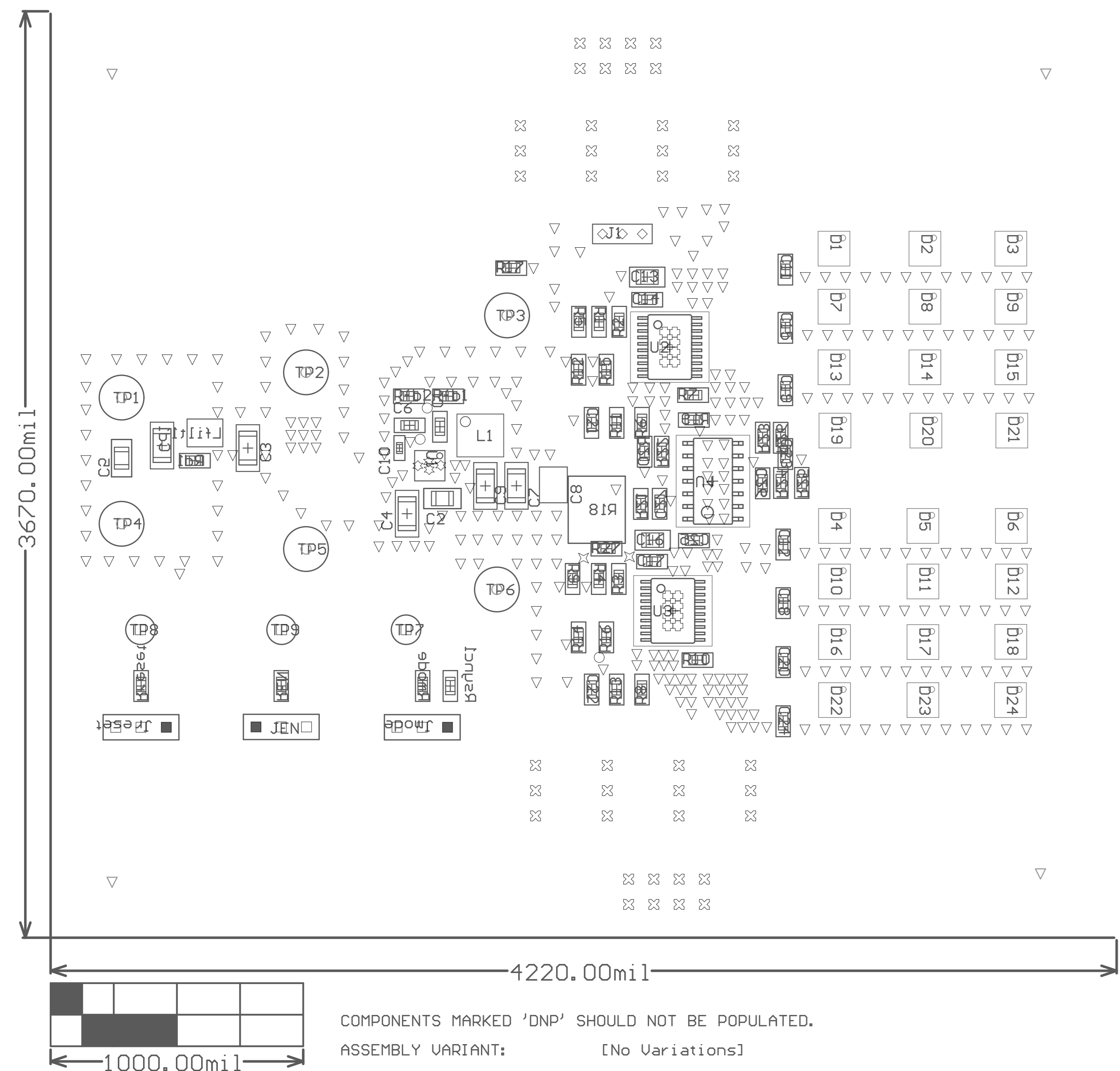
PROJECT TITLE: LM53600NAEVM/01LAEVM
DESIGNED FOR: Public Release
FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Keep Out Layer	GENERATED : 9/26/2016 3:39:08 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
LAYOUT BY: Robert Blattner
SCALE: 1.00
ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



Symbol	Quantity	Finished Hole Size	Plated	Hole Type
○	4	7.87mil (0.200mm)	PTH	Round
✱	165	12.00mil (0.305mm)	PTH	Round
▽	12	40.00mil (1.016mm)	PTH	Round
☆	6	96.43mil (2.500mm)	PTH	Round
□	4	125.98mil (3.200mm)	PTH	Round
	191 Total			

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING: 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK



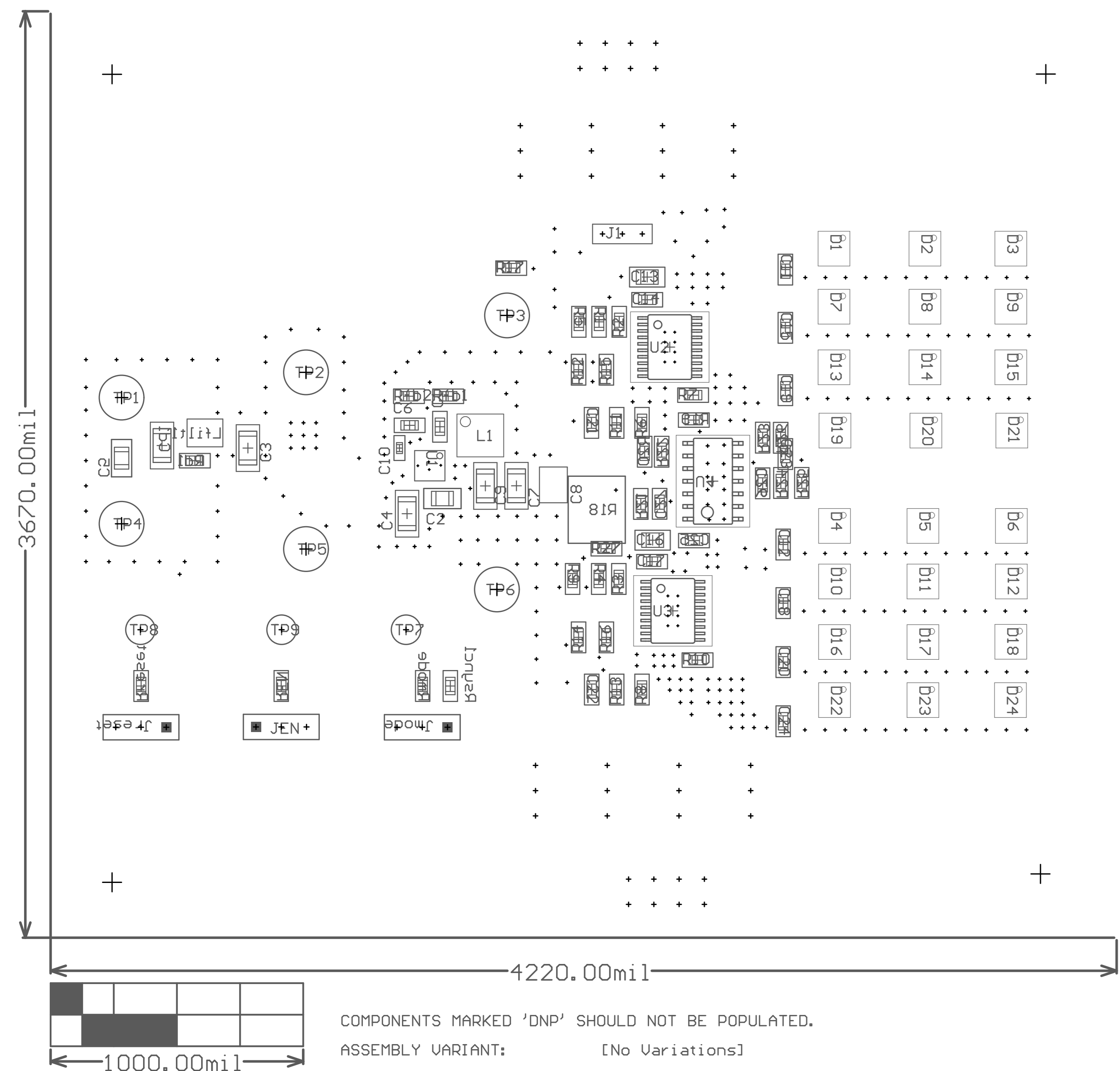
PROJECT TITLE: LM53600NAEUM/01LAEUM
 DESIGNED FOR: Public Release
 FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Drill Drawing For (Solder Side,Component Side)	GENERATED : 9/26/2016 3:39:12 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner
 LAYOUT BY: Robert Blattner
 SCALE: 1.00
 ALTUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Component Side	Copper	1.42mil		
4	Dielectric 1	FR-4	12.00mil	4.2	
5	Ground Plane	Copper	1.42mil		
6	Dielectric 3	FR-4	32.00mil	4.2	
7	Signal Layer 1	Copper	1.42mil		
8	Dielectric 4	FR-4	12.00mil	4.2	
9	Solder Side	Copper	1.42mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS --> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE: LM53600NAEVM/01LAEVM

DESIGNED FOR: Public Release

FILE NAME: TIDA01348.PcbDoc

PCB VIEWED FROM TOP SIDE	BOARD #: TIDA-01348	REV: A	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01348		
PLOT NAME = Drill Guide For (Solder Side,Component Side)	GENERATED : 9/26/2016 3:39:18 PM	TEXAS INSTRUMENTS	

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ENGINEER: Robert Blattner

LAYOUT BY: Robert Blattner

SCALE: 1.00

ALTIUM DESIGNER VERSION: 16.0.9.368

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