Design Guide: TIDA-050026-23882

24-Port (2 Pair) Power Sourcing Equipment Reference Design for Multiport Applications

Description

This reference design features an evaluation module for the 24-port (2 pair) PSE system which contains a hardware kit, a system firmware image, and a system firmware GUI. The hardware kit consists of a mother board (PSEMTHR24EVM-081), MSP430 daughtercard (PSEMCUDAUEVM-082) or MSPM0 daughtercard (PSEM0MCUDAUEVM-018), and a PSE daughter card (TPS23882EVM-084 and TPS23882B1EVM-035). To evaluate the system (both hardware and software), USB2ANY and MSP-FET/ XDS110 adapters are also needed. This guide has been revised to reflect hardware design using the new MSPM0G1107 MCU for multiport PoE systems.

Resources

TIDA-050026-23882	Design Folder
TPS23882EVM-084 TPS23882B1EVM-035	Tool Folder
PSEMTHR24EVM-081 PSEMCUDAUEVM-082	Tool Folder
TPS23882, TPS23882B	Product Folder
MSP430F5234 MSPM0G1107	Product Folder
CSD19538Q3A	Product Folder

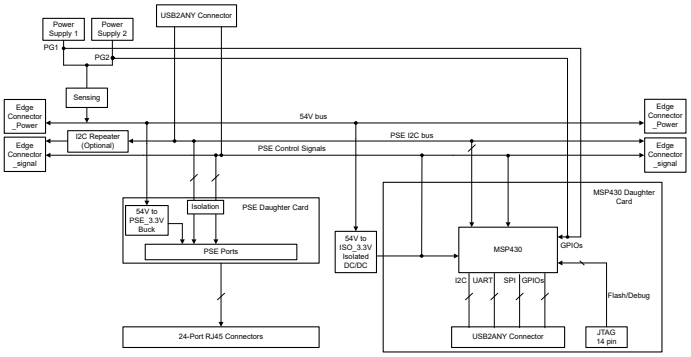
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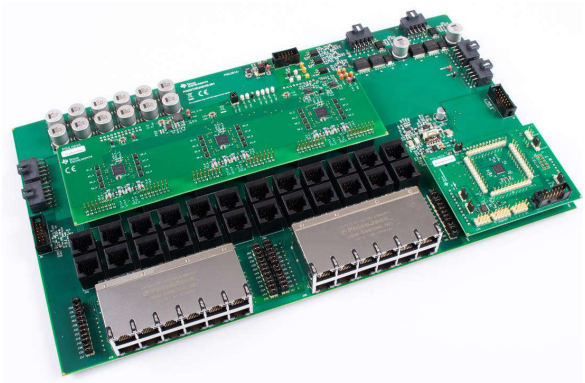
Features

- Onboard power monitoring
- 24 (2 pair) port system, and expandable to 48 port system
- Highly flexible system with configurable GUI and selectable host interface (I^2C or UART)
- Multiport power management
- Multiple power supplies
- Supports legacy powered devices (PDs)

Applications

- Campus and branch switches
- Video recorder
- Edge router





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1 System Description

This reference design provides a competitive and alternative design.

In a multiport PSE system, the system-level software is the biggest challenge. The software handles complicated situations and addresses the following challenges:

- The power supply is typically not able to support all ports with a full load due to size and cost constraints. The system software manages the port power with priority to keep the total power consumption below the power budget.
- There are multiple power supplies in the system. These power supplies can be in sharing mode or backup mode. The system software shuts down low-priority ports fast enough to keep the total power consumption below the remaining power budget.
- There are some legacy PD devices that do not present the standard PoE PD signature. The system software finds a way to supply power to these devices.
- System software limits the port power based on the PD class levels or host configuration.
- When there are load-step changes on multiple ports, the system software acts quickly enough to keep the power consumption below the power budget.

1.1 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage	44V – 57V	
Port power limit	2W – 60W	> 30W is considered as nonstandard power
Compliance	IEEE 802.3bt Type 3	
PD class level supported	Class 0 to class 4	
Number of power supply supported	1 – 2	In sharing mode and redundant mode
Max port number supported	48	Referred to RJ45 ports

1.2 Description

This reference design features the TPS23882/TPS23882B daughtercard, the octal channel, the TPS23882/TPS23882B device, and the IEEE802.3bt ready PoE PSE controller. When paired with the PSE motherboard PSEMTHR24-081 (sold separately) and MCU daughtercard PSEMCUDAUEVM-082/PSEM0MCUDAUEVM-018 (sold separately), users can evaluate the TPS23882/TPS23882B device and PSE system firmware solution.

The full PoE evaluation ecosystem includes the following:

- PSEMTHR24EVM-081: motherboard for 24-port PoE PSE applications (sold separately)
- PSEMCUDAUEVM-082: MSP430 daughtercard for 24-port PoE PSE applications (sold separately)
- PSEM0MCUDAUEVM-018: MSPM0 daughtercard for 24-port PoE PSE applications (sold separately)
- TPS23882EVM-084: TPS23882 daughtercard for 24 port Type 3 (2 pair) PSE PoE PSE applications (sold separately)
- TPS23882B1EVM-035: TPS23882B daughtercard for 24 port Type 3 (2 pair) PSE PoE PSE applications (sold separately)
- USB2ANY interface adapter: used with PSE system firmware GUI for I^2C/UART interaction with the PSEMCUDAU-082 daughtercard (sold separately)
- XDS110 Debugger: Used with UniFlash GUI for programming the MSPM0
- MSP-FET programmer: used with Uniflash GUI for programming the MSP430 device
- PSE system firmware code image (request access to the code image through TIDA-050026-23882 folder or PSEMCUDAUEVM-082 tool folder)
- PSE system firmware GUI (request access to the code image through TIDA-050026-23882 folder or PSEMCUDAUEVM-082 tool folder)

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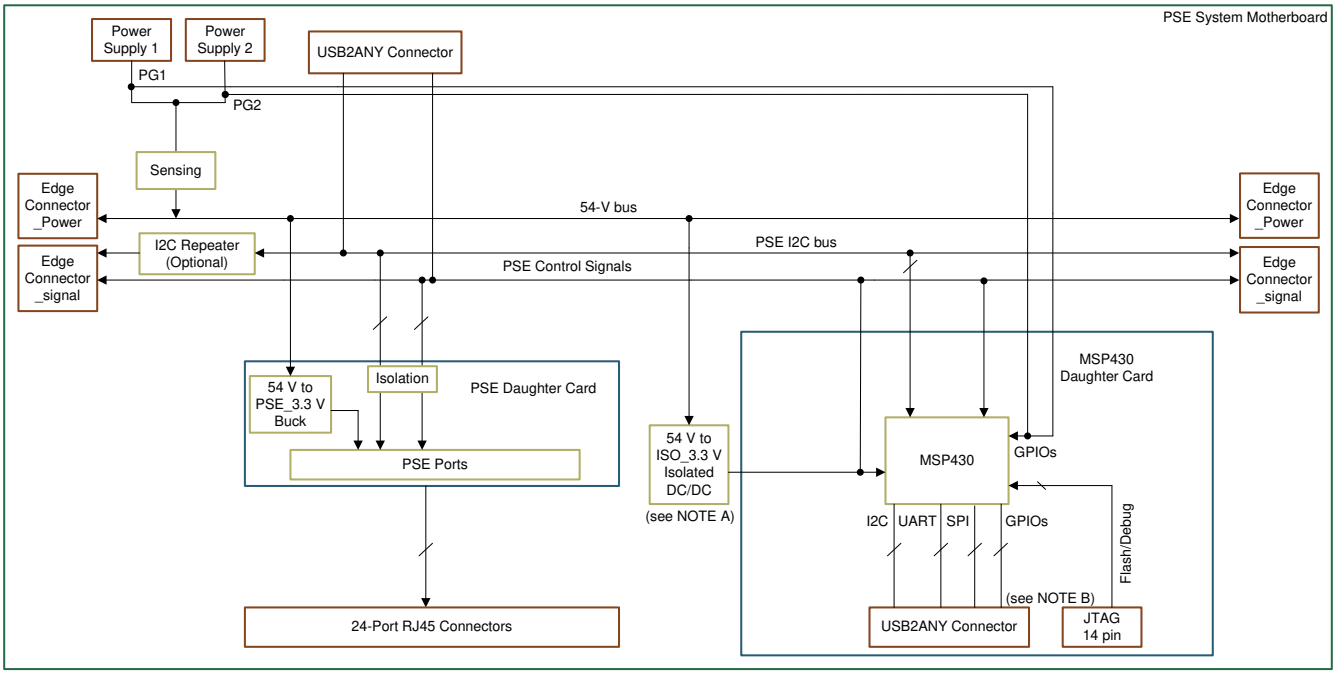
Note

The MSP430F5234 on PSEMCUDAUEVM-082 is programmed with pre-production firmware for EVM testing purposes. Follow the instructions in this user's guide to flash the latest firmware from the TIDA-050026-23882 folder or the PSEMCUDAUEVM-082 tool folder before evaluation. Similarly, latest firmware for the MSPM0G1107 on PSEM0MCUDAUEVM-018 can be found from the TIDA-050026-23882 folder.

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2 System Overview

2.1 Block Diagram



A. The 54V to 3.3V isolated DC/DC is for demonstration purposes only and is not needed in a real system.

B. Only connect a USB2ANY connector or JTAG to avoid GND loops.

Figure 2-1. TIDA-050026-23882 Block Diagram

2.2 Design Considerations

2.2.1 Input Power

2.2.1.1 Vpwr

DC input voltage is provided through J1 and J3. This board supports a dual power source in sharing mode and redundant mode. If the power supplies are in redundant mode, make sure the main power supply is connected to J1 and a backup power supply is connected to the J3 connector.

The minimum PSE port voltage is 44VDC for Type 1, 50V for Type 2 and Type 3, and 52V for Type 4. The maximum DC voltage at VPWR is 57V for all types. During evaluation, choose the appropriate DC power supply for the different type environment.

2.2.1.2 3.3V

A local 3.3V for local devices (labeled as 3.3V) is provided by the onboard LM5017 buck converter. The LM5017 device provides a basic power-on sequence and provides a well-controlled and consistent startup to prevent erratic operation. In addition to 44V to 57V, the TPS238x requires 3.3V for the digital circuitry and each TPS2388x device consumes 6mA typical and 12mA maximum.

2.2.1.3 3.3V_ISO

The reference design kit provides galvanic isolation between PoE power side and host side using digital isolators. The host side power is provided by 3.3V_ISO.

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2.2.2 Communication Interface

2.2.2.1 PSE I²C Communication

The board provides two I²C interfaces communicating to PSE:

1. J10 on the motherboard (PSEMTHR24EVM-081) provides I²C access to all PSE devices directly. The TPS2388x GUI can communicate to PSE devices with the USB2ANY interface adapter.
2. J11 and J12 on the motherboard (PSEMTHR24EVM-081) provides I²C access and system control signal to the MSP430 daughtercard.

2.2.2.2 MCU - Host Communication

The MSP430 daughtercard provides I2C/UART communication port to host through J12 to J14 on MSP430 daughtercard (PSEMCUDAUEVM-082). The MSPM0 daughtercard (PSEM0MCUDAUEVM-018) provides I2C communication to host through J12, J13, and J16. The PSE system GUI provides host configurations to the PSE system

The host interface user's guide can be accessed from TIDA-050026-23882 folder or PSEMCUDAUEVM-082 tool folder.

2.2.3 MSP430F523x and MSPM0G1107x Hardware Design

Table 2-1. MSP430 GPIO Pin Assignment

PIN NUMBER MSP430F5234 (48RGZ)	TERMINAL	FUNCTION	COMMENT
COMMUNICATION			
22	P3.0	I²C SDA USCI_B0	I²C to PSEs
23	P3.1	I²C SCL USCI_B0	I²C to PSEs
30	P4.1	I²C SDA USCI_B1	I²C to host
31	P4.2	I²C SCL USCI_B1	I²C to host
33	P4.4	UART TX USCI_A1	UART to host (debug only)
34	P4.5	UART RX USCI_A1	UART to host (debug only)
21	P2.7	SPI CLK USCI_A0	SPI to host (reserved)
24	P3.2	SPI peripheral TX enable, USCI_A0	SPI to host (reserved)
25	P3.3	UART TX,USCI_A0 or SPI peripheral in, controller out	UART to host TX or SPI to host (reserved)
26	P3.4	UART RX, USCI_A0 or SPI peripheral out, controller in	UART to host RX or SPI to host (reserved)
HARDWARE INTERRUPT			
13	P1.0	PSE INT	Connect to PSE INT pin
16	P1.3	OC Alert	Connect to external current sensing circuit if not used, connect to 3.3V
18	P1.5	Power supply 1	Connect to power supply 1 power good signal. In RPS mode, P1.5 must be connected to main power supply. **If there is only one power supply, the power good signal must be connected to P1.5.**
19	P1.6	Power supply 2	Connect to power supply 2 power good signal, if not used, connect to GND. In RPS mode, P1.6 must be connected to backup power supply
20	P1.7	Disable all ports	This is for hardware disable ports(Reserved)
GENERAL I/O			
4	P5.0	RESET	PSE RESET Connect to PSE RESET pin
17	P1.4	OSS	PSE OSS Connect to PSE OSS pin
46	P6.0	Interrupt pin to host	
35	P4.6	BSL mode indication to host	MCU configures as output. If MCU is in BSL mode, output high. If in normal operation mode, output low.

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Table 2-1. MSP430 GPIO Pin Assignment (continued)

PIN NUMBER MSP430F5234 (48RGZ)	TERMINAL	FUNCTION	COMMENT
48	P6.2	Guard-band indication	Need an external LED
47	P6.1	Selection between I^2C and SPI/ UART	(Need to pullup or pulldown)
PROGRAM DOWNLOAD AND DEBUG			
44	PJ.3	TCK	JTAG clock input
43	PJ.2	TMS	JTAG state control
42	PJ.1	TDI/TCLK	JTAG data input, TCLK input
41	PJ.0	TDO	JTAG data output
40		TEST/SBWTCK	Enable JTAG pins
45		RSTDVCC/SBWTDIO	External reset
EXTERNAL CRYSTAL			
7	P5.4	XTIN	External low frequency clock (use if needed)
8	P5.5	XTOUT	External low frequency clock (use if needed)

Pre-configure the host interface protocol through hardware as shown in Table 2-2.

Table 2-2. Host Interface Protocol (MSP430)

	P6.1	CS(P3.2)
I^2C	high	Don't care
UART	low	low
SPI (Reserved)	low	high

Table 2-3 shows the MSPM0 GPIO pin assignments:

Table 2-3. MSPM0 GPIO Pin Assignments

PIN NUMBER MSPM0G1107 (48RGZ)	TERMINAL	FUNCTION	COMMENT
COMMUNICATION			
31	PA16	I2C SDA controller	I2C1_SDA
30	PA15	I2C SCL controller	I2C1_SCL
1	PA0	I2C SDA peripheral	I2C0_SDA
2	PA1	I2C SCL peripheral	I2C0_SCL
18	PA10	UART TX (Comm and BSL)	UART0 transmit to host (reserved), Bootstrap loader
19	PA11	UART RX (Comm and BSL)	UART0 receive to host (reserved), Bootstrap loader
29	PA14	UART TX (Debug)	UART3 TX Debug
28	PA13	UART RX (Debug)	UART3 RX Debug
23	PB9	SPI CLK	SPI1 clock signal I/O
20	PB6	SPI peripheral TX enable	SPI1 chip-select 0
24	PB14	SPI peripheral in/controller out	SPI1 POCI
25	PB15	SPI peripheral out/controller in	SPI1 PICO
HARDWARE INTERRUPT			
13	PA7	PSE INT	Connect to PSE INT pin
16	PA18	OC Alert	Connect to external current sensing circuit if not used, connect to 3.3V

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Table 2-3. MSPM0 GPIO Pin Assignments (continued)

PIN NUMBER MSPM0G1107 (48RGZ)	TERMINAL	FUNCTION	COMMENT
21	PB7	Power supply 1	Connect to power supply 1 power good signal. In RPS mode, PB7 must be connected to main power supply. **If there is only one power supply, the power good signal must be connected to PB7.**
22	PB8	Power supply 2	Connect to power supply 2 power good signal, if not used, connect to GND. In RPS mode, PB8 must be connected to backup power supply
17	PA9	Disable all ports	This is for hardware disable ports (reserved)
32	PA17	I2C Reset	Connect to host GPIO pin to reset I2C module when host I2C fails.
GENERAL I/O			
14	PB2	RESET	PSE RESET Connect to PSE RESET pin
15	PB3	OSS	PSE OSS Connect to PSE OSS pin
46	PA26	Interrupt pin to host	
36	PB17	BSL mode indication to host	MCU configures as output. If MCU is in BSL mode, output high. If in normal operation mode, output low.
33	PA18	BSL Invoke	Input pin used to invoke bootloader
45	P6A25	Guard-band indication	Need an external LED
47	PA27	Selection between I2C and SPI, UART	Need to pullup or pulldown
PROGRAM DOWNLOAD AND DEBUG			
35	PA20	SWCLK	Serial wire debug input clock
34	PA19	SWDIO	Serial wire debug I/O
EXTERNAL CRYSTAL AND POWER			
9	PA3	XTIN	External low frequency clock (use if needed)
10	PA4	XTOUT	External low frequency clock (use if needed)
11	PA5	HFXIN	Extra high frequency clock
12	PA6	HFXOUT	Extra high frequency clock
8		ROSC	Output for high frequency HFXT
7	VSS	M0+ Ground Supply	Refer to MSPM0 datasheet for schematic requirements
6	VDD	M0+ Power Supply	Refer to MSPM0 datasheet for schematic requirements
48	VCORE	M0+ Regulated core power supply output	Refer to MSPM0 datasheet for schematic requirements

Pre-configure the host interface protocol through hardware as shown in Table 2-4.

Table 2-4. Host Interface Protocol (MSPM0)

	PA27	CS (PB6)
I2C	high	Don't care
UART	low	low
SPI (CS ActiveLow)	low	high

2.3 Highlighted Products

2.3.1 TPS23882 and TPS23882B

The TPS2388x device is the main IC to handle PoE functions to deliver power to PDs through Ethernet cable.

The TPS23882/TPS23882B is an 8-channel power sourcing equipment (PSE) controller engineered to insert power onto Ethernet cables in accordance with the IEEE 802.3bt standard. The PSE controller can detect powered devices (PDs) that have a valid signature, determine the power requirements of the devices according to their classification, and apply power. The TPS23882 and the TPS23882B improves on the TPS2388 with

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reduced current sense resistors, selectable autonomous operation, SRAM programmability, programmable power limiting, capacitance measurement, and compatibility with TI's FirmPSE system firmware (see Device Comparison Table). Dedicated per-port ADCs provide continuous port current monitoring and the ability to perform parallel classification measurements for faster port turn on times. A 1.25A port current limit and adjustable power limiting allows for the support of non-standard applications above 60W sourced. The 200 mΩ current sense resistor and external FET architecture allow designs to balance size, efficiency, thermal, and solution cost requirements. Port remapping and pin-to-pin compatibility with the TPS2388/80/81 devices eases migration from previous generation PSE designs and enables interchangeable 2-layer PCB designs to accommodate different system PoE power configurations.

2.3.2 MSPM0G1107x and MSP430F523x

The TI MSPM0G1107 family of ultra-low-power microcontrollers consists of devices featuring a range of peripherals targeted for various applications, including industrial, medical, and consumer electronics. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 32-bit Arm Cortex-M0+ CPU, up to 128KB of flash memory, and up to 32KB of SRAM. The device also includes a range of peripherals, such as two 12-bit ADCs, two I2C interfaces, two SPIs, four UART interfaces, and a real-time clock (RTC) module with alarm capabilities. The MSPM0G1107 family also includes a range of low-power modes, including sleep, stop, and standby modes, which can be used to minimize power consumption. The device is an excellent choice for a range of applications, including industrial control, medical devices, and consumer electronics.

The TI MSP family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in 3.5µs (typical). The MSP430F524x series are microcontroller configurations with four 16-bit timers, a high-performance 10-bit ADC, two USCIs, a hardware multiplier, DMA, a comparator, and an RTC module with alarm capabilities. The MSP430F523x series microcontrollers include all of the peripherals of the MSP430F524x series except for the ADC.

MSP430F523x and MSPM0G1107x are the main controllers to control PSE devices (TPS2388x) through the I2C bus and also communicate to host CPU through I2C or UART to receive configurations and report system status.

2.3.3 ISO7741

The ISO7741 isolator is used to isolate I^2C signals between PSE devices and the MCU.

The ISO774x devices are high-performance, quadchannel digital isolators with 5000 VRMS (DW package) and 3000 VRMS (DBQ package) isolation ratings per UL 1577. This family of devices has reinforced insulation ratings according to VDE, CSA, TUV and CQC. The ISO774x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO2) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-controller driving applications and to reduce power consumption. The ISO7740 device has all four channels in the same direction, the ISO7741 device has three forward and one reverse-direction channels, and the ISO7742 device has two forward and two reverse-direction channels. If the input power or signal is lost, default output is high for devices without suffix F and low for devices with suffix F.

2.3.4 ISO7731

The ISO7731 digital isolator is used to isolate control signals (OSS, RESET, INT) between MCU and PSE devices.

The ISO773x devices are high-performance, triple channel digital isolators with 5000 VRMS (DW package) and 3000 VRMS (DBQ package) isolation ratings per UL 1577.

This family of devices has reinforced insulation ratings according to VDE, CSA, TUV, and CQC.

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The ISO773x family of devices provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO2) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-controller driving applications and to reduce power consumption. The ISO7730 device has all three channels in the same direction and the ISO7731 device has two forward and one reverse-direction channel. If the input power or signal is lost, the default output is high for devices without suffix F and low for devices with suffix F. See the device *Functional Modes* section for further details.

Used in conjunction with isolated power supplies, this device helps prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through remarkable chip design and layout techniques, electromagnetic compatibility of the ISO773x device has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance.

2.3.5 CSD19538

This 100V, 49mΩ, SON 3.3mm × 3.3mm NexFET™ power MOSFET is designed to minimize conduction losses and reduce the board footprint in PoE applications.

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2.3.6 LM5017

The LM5017 device is used to generate 3.3V to supply PSE devices.

The LM5017 is a 100V, 600mA synchronous step-down regulator with integrated high-side and low-side MOSFETs. The constant on-time (COT) control scheme employed in the LM5017 device requires no loop compensation, provides excellent transient response, and enables very high step-down ratios. The on-time varies inversely with the input voltage resulting in nearly constant frequency over the input voltage range. A high-voltage startup regulator provides bias power for internal operation of the IC and for integrated gate drivers. A peak current limit circuit protects against overload conditions. The undervoltage lockout (UVLO) circuit allows the input undervoltage threshold and hysteresis to be independently programmed. Other protection features include thermal shutdown and bias supply undervoltage lockout (VCC UVLO).

2.3.7 LM5020

The LM5020 device is used to generate isolated LM5020 to supply MCU and isolators.

The LM5020 high-voltage pulse-width modulation (PWM) controller contains all of the features needed to implement single-ended primary power converter topologies. Output voltage regulation is based on current-mode control, which eases the design of loop compensation while providing inherent line feed-forward. The LM5020 device includes a high-voltage start-up regulator that operates over a wide-input range up to 100V. The PWM controller is designed for high-speed capability including an oscillator frequency range to 1MHz and total propagation delays less than 100ns. Additional features include an error amplifier, precision reference, line undervoltage lockout, cycle-by-cycle current limit, slope compensation, soft start, oscillator synchronization capability, and thermal shutdown.

2.3.8 LM5050

The LM5050 device is used to support two power supplies in the system to work in backup mode.

The LM5050-1 and LM5050-1-Q1 high-side ORing FET controller operates in conjunction with an external MOSFET as an ideal diode rectifier when connected in series with a power source. This ORing controller allows MOSFETs to replace diode rectifiers in power distribution networks, thus reducing both power loss and voltage drops.

The LM5050-1 and LM5050-1-Q1 controllers provide charge pump MOSFET gate drive for an external N-channel MOSFET and a fast response comparator to turn off the FET when current flows in the reverse direction. The LM5050-1 and LM5050-1-Q1 can connect power supplies ranging from 5V to 75V and can withstand transients up to 100V.

2.3.9 INA240

The INA240 amplifier is used to measure the total current from the input to support fast shutdown in an event of load step change.

The INA240 device is a voltage-output, current-sense amplifier with enhanced PWM rejection that can sense drops across shunt resistors over a wide common-mode voltage range from –4V to 80V, independent of the supply voltage. The negative common-mode voltage allows the device to operate below ground, accommodating the flyback period of typical solenoid applications. Enhanced PWM rejection provides high levels of suppression for large common-mode transients ($\Delta V / \Delta t$) in systems that use PWM signals (such as motor drives and solenoid control systems). This feature allows for accurate current measurements without large transients and associated recovery ripple on the output voltage. This device operates from a single 2.7V to 5.5V power supply, drawing a maximum of 2.4mA of supply current. Four fixed gains are available: 20V/V, 50V/V, 100V/V, and 200V/V. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10mV full-scale.

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2.3.10 REF3425

The REF3425 device is used to provide a threshold to output the INA240 and generate a signal to MCU for overcurrent alert.

The REF34xx device is a low temperature drift (6ppm/℃), low-power, high-precision CMOS voltage reference, featuring ±0.05% initial accuracy, low operating current with power consumption less than 95µA. This device also offers very low output noise of 3.8µVp-p /V, which enables its ability to maintain high signal integrity with high-resolution data converters in noise critical systems. With a small SOT-23 package, the REF34xx offers enhanced specifications and pin-to-pin replacement for MAX607x and ADR34xx. The REF34xx family is compatible to most of the ADC and DAC such as the ADS1287, ADUCM360, and ADS1112 devices. Stability and system reliability are further improved by the low output-voltage hysteresis of the device and low long-term output voltage drift. Furthermore, the small size and low operating current of the devices (95µA) can benefit portable and battery-powered applications.

2.3.11 TPS3890

The TPS3890 device is used to monitor the existence of the power supply and generate power good signal to MCU. The MCU can adjust the total power budget of the system.

The TPS3890 device is a precision voltage supervisor with low-quiescent current that monitors system voltages as low as 1.15V, asserting an open-drain RESET signal when the SENSE voltage drops below a preset threshold or when the manual reset (MR) pin drops to a logic low. The RESET output remains low for the user-adjustable delay time after the SENSE voltage and manual reset (MR) return above the respective thresholds. The TPS3890 family uses a precision reference to achieve 1% threshold accuracy. The reset delay time can be user-adjusted between 40µs and 30s by connecting the CT pin to an external capacitor. The TPS3890 device has a very low quiescent current of 2.1µA and is available in a small 1.5mm × 1.5mm package, making the device well-suited for battery-powered and space-constrained applications.

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3 Hardware, Software, Testing Requirement and Test Result

3.1 Required Hardware and Software

3.1.1 Hardware

The following hardware is required to get started with the reference design:

- PSEMTHR24EVM-081: motherboard for 24 port PoE PSE applications (sold separately)
- PSEMCUDAUEVM-082: MSP430 daughtercard for 24 Port PoE PSE applications (sold separately)
- PSEM0MCUDAUEVM-018: MSPM0 daughtercard for 24 Port PoE PSE applications (sold separately)
- TPS23882EVM-084: TPS23882 daughtercard for 24-port Type 3 (2 pair) PoE PSE applications (sold separately)
- TPS23882B1EVM-035: TPS23882B daughtercard for 24-port Type 3 (2 pair) PoE PSE applications (sold separately)
- USB2ANY interface adapater: used with PSE system firmware GUI for I^2C/UART interaction with PSEMCUDAU-082 daughtercard (sold separately)
- MSP-FET programmer: used with the Uniflash GUI for programming the MSP430 device
- XDS110 Debugger: used with the UniFlash GUI for programming the MSPM0 device

Note

The MSPM0 is recommended for all new FirmPSE designs. The MSP430F5234 on PSEMCUDAUEVM-082 and the MSPM0G1107 on PSEM0MCUDAUEVM-018 are programmed with pre-production firmware for EVM testing purposes. Follow the instructions in this user's guide to flash the latest firmware from TI.com before evaluation.

3.1.2 Software

- FirmPSE code image (request access to the code image through the TIDA-050026-23882 folder, PSEM0MCUDAUEVM-018 tool folder, or the PSEMCUDAUEVM-082 tool folder)
- FirmPSE GUI (request access to the GUI through the TIDA-050026-23882 folder or the PSEMCUDAUEVM-082 tool folder)
- FirmPSE GUI MSPM0 (reach out to TI PoE team member for access request, and access GUI here)

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3.2 Testing and Results

3.2.1 Test Setup

3.2.1.1 Hardware Setup

Figure 3-1 shows the hardware test setup of the ecosystem.

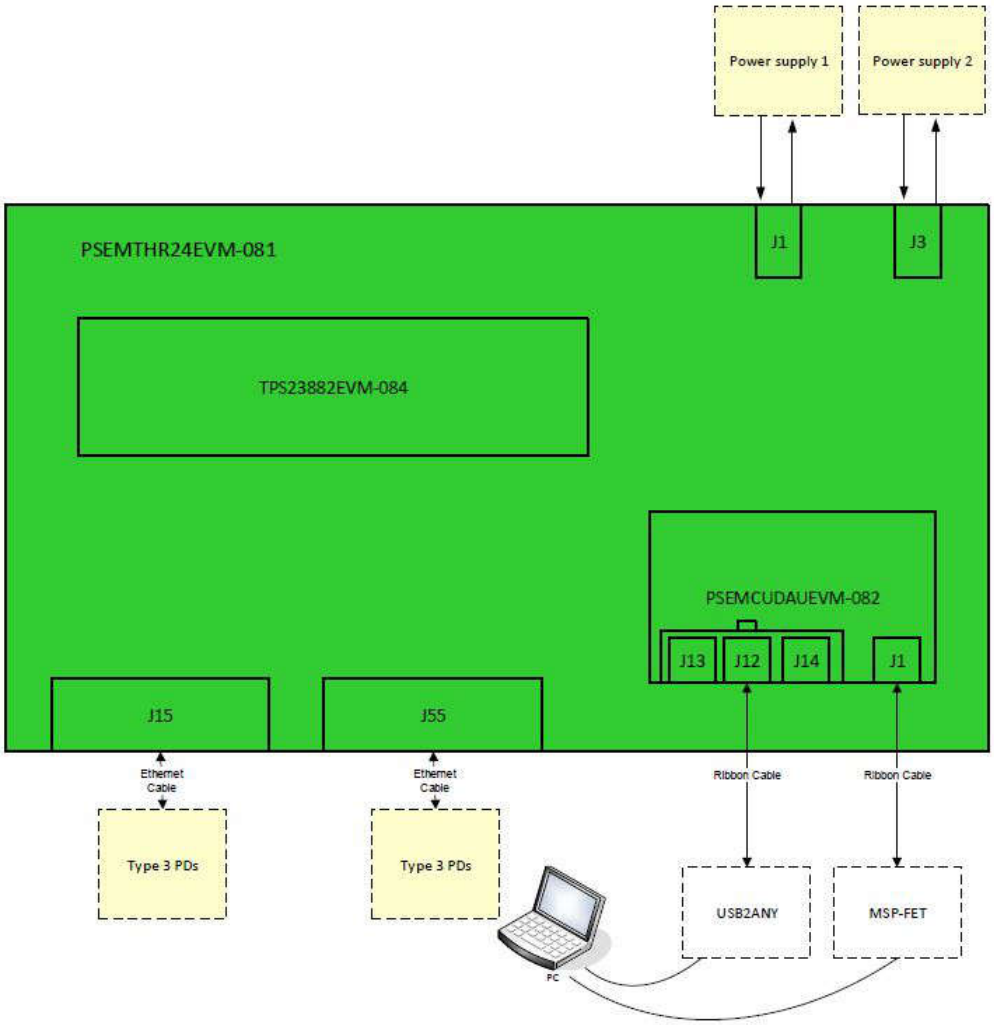


Figure 3-1. Ecosystem Setup

Note

A 30-pin ribbon cable is required to enable the full features of PSE system firmware GUI.

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3.2.1.2 LED, Test Point, Jumper, and Connector Settings

3.2.1.2.1 EVM LEDs

Table 3-1 lists the EVM LEDs and their descriptions.

Table 3-1. EVM LEDs

LED	COLOR	DESCRIPTION
PSEMTHR24EVM-081		
J15, J55	Green, Yellow	There is one green and yellow LED on each RJ45 port
PSEMCUDAUEVM-082		
D1	Green	The total power consumption is within the pre-configured guardband
PSEM0MCUDAUEVM-018		
D1	Green	The total power consumption remains within the pre-configured guardband limits.

3.2.1.2.2 EVM Test Points

Table 3-2 lists the EVM test points.

Table 3-2. EVM Test Points

TP	LABEL	DESCRIPTION
PSEMTHR24EVM-081		
TP1	55VDC	VPWR
TP2	GND	VPWR ground
TP3	OC-ALERT	System over current alert signal
TP4	SDA	I^2C data
TP5	SCL	I^2C clock
TP6	PG1	Power good signal for power supply #1
TP7	PG2	Power good signal for power supply #2
TP8	PSE_3.3V	3.3V for PSE devices
TP9	GND	PSE_3.3V ground
TP10	3.3V_ISO	Isolated 3.3V for MSP430
TP11	3.3V	3.3V for debug
TPS12 , TP13	GND_ISO	3.3V_ISO ground
TP14	OSS	OSS signal from MCU to PSE
TPS23882EM-084 and TPS23882B1EVM-035		
TP1	PSE_3.3	3.3V for PSE devices
TP2	VPWR	VPWR for PSE devices
TP3, TP4, TP14, TP19	GND	VPWR and PSE_3.3V ground
TP5	3.3V_ISO	Isolated 3.3V
TP6	RESET	Reset signal from MCU
TP7	OSS	OSS signal from MCU
TP8	INT	INT signal to MCU
TP9	SDA	I^2C data from/to MCU
TP10	SCL	I^2C clock from MCU
TP11	PSE_RST	Reset signal to PSE
TP12	PSE_OSS	OSS signal to PSE
TP13	PSE_INT	INT signal from PSE
TP15	GND_ISO	3.3V_ISO ground
TP16	PSE_SCL	I^2C clock signal to PSE
TP17	PSE_SDAI	I^2C data to PSE

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Table 3-2. EVM Test Points (continued)

TP	LABEL	DESCRIPTION
TP18	PSE_SDAO	I^2C data from PSE

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3.2.1.2.3 EVM Jumpers

Table 3-3 lists the EVM test jumpers and their descriptions.

Table 3-3. EVM Test Jumpers

JUMPER	DEFAULT PIN POSITION	DESCRIPTION
PSEMTHR24EVM-081		
J13	1-2	3.3V comes from PSE daughtercard
J14	1-2	Connect 3.3V_ISO to supply the circuit
J17, J22, J38, J43, J19, J23, J32, J28, J52, J47, J31, J26	1-2	Enable port LED
J45, J42, J24, J21, J44, J49, J53, J30, J33, J51, J54	1-2	Enable port LED
J57, J62, J78, J83, J59, J63, J72, J68, J92, J87, J71, J66	1-2	Enable port LED
J85, J82, J64, J61, J84, J80, J89, J93, J70, J91, J94	1-2	Enable port LED
TPS23882EVM-084		
J3	1-2, 3-4	PSE devices' address configuration

3.2.1.2.4 EVM Input and Output Connectors

Table 3-4 lists the EVM input and output connectors.

Table 3-4. EVM Input and Output Connectors

CONNECTOR	DESCRIPTION
PSEMTHR24EVM-081	
J1, J3	DC power supply input (44-57V VDC, 41A)
J2, J4, J6, J7	Edge connector for DC bus when connecting 2 boards together
J5	Power to PSE daughtercard
J8, J9	Edge connector for PSE signals (I^2C, OSS, RESET and INT) when connecting 2 boards together
J10	Connector to USB2ANY for direct I^2C access to PSE devices(for debug purpose only)
J11	Connectors to PSE daughter for PSE signals (I^2C, OSS, RESET and INT)
J12	Connectors to MSP430 daughter for PSE signals (I^2C, OSS, RESET and INT), system level signals (OC-ALERT, PG) and isolated 3.3V
J15, J55	PSE ports magjacks
J34, J35, J36, J74, J75, J76	PSE port connector to PSE daughter card
J95, J96	For MSP430 daughter card mechanical mounting purpose
TPS23882EM-084 and TPS23882B1EVM-035	
J1	Pair with J5 on motherboard
J4	Pair with J11 on motherboard
J5	Pair with J34, J35, J36, J74, J75, J76 on motherboard
PSEMCUDAUEVM-082	
J1	JTAG connector
J3, J7, J8, J9	Extended GPIO access
J11	Pair with J12 on motherboard
J12, J13, J14	USB2ANY connector (30 pin)
J17, J18	For MSP430 daughter card mechanical mouting purpose
PSEM0MCUDAUEVM-018	
J3, J4, J6, J10	Extended GPIO access
J9	Pair with J12 on motherboard
J12, J13, J14	USB2ANY connector (30 pin)
J11, J15	For MSP430 daughtercard mechanical mounting purpose

3.2.1.3 System Firmware GUI Setup

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3.2.1.3.1 PSE System Firmware GUI Installation

TI's PSE system firmware GUI is used with the PSE system EVM kit (PSEMTHR24EVM-081, PSEMCUDAUEVM-082, TPS23882EVM-084, TPS23882B1EVM-035) to configure the system, generate the code image and flash to MSP430/MSPM0 device. PSE system firmware GUI using MSPM0 can be requested here. Download the MSP430 system firmware GUI from TIDA-050026-23882 folder or PSEMCUDAUEVM-082 tool folder.

3.2.1.3.2 PSE System Firmware GUI Operation

Start the PSE system firmware GUI by double-selecting the GUI icon and selecting the Start button. A window similar to Figure 3-2 appears. The Offline mode is selected by default.

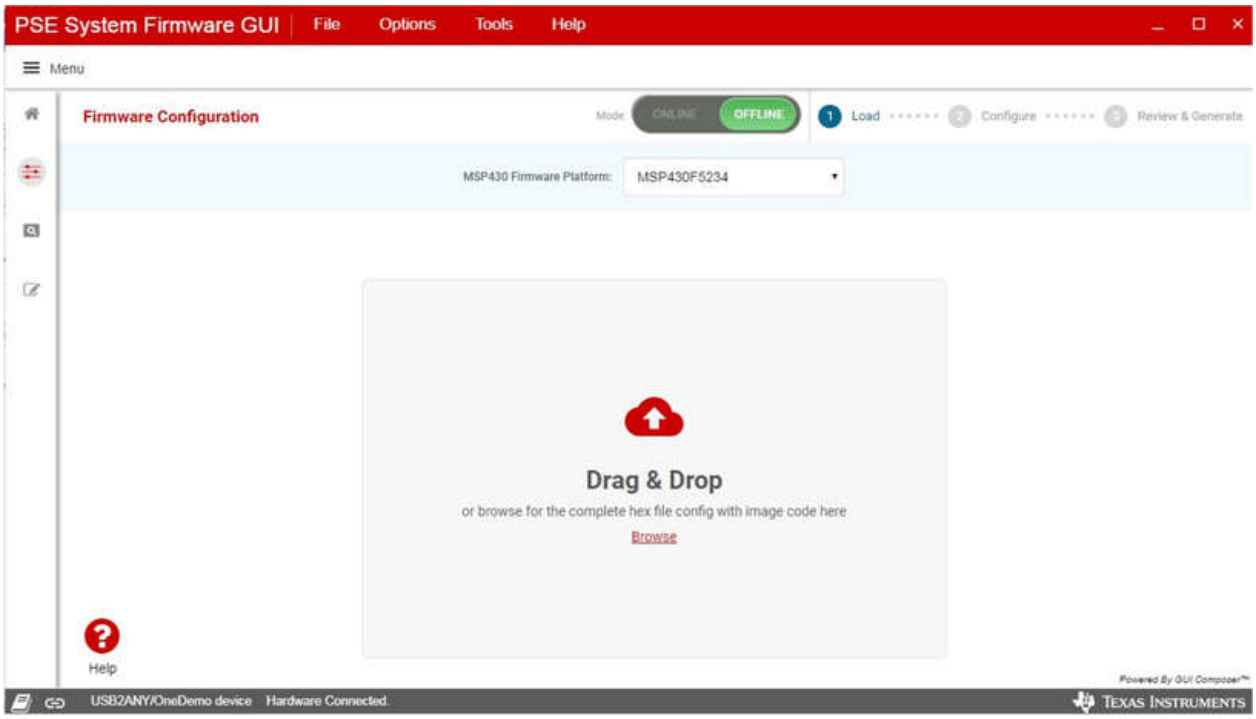


Figure 3-2. GUI Start-up

Select the MSP430 device you want to start with and then load the PSE system firmware code image (access from TIDA-050026-23882 folder, PSEM0MCUDAUEVM-018 tool folder or PSEMCUDAUEVM-082 tool folder). When finished, select *Proceed* to go to the configuration page.

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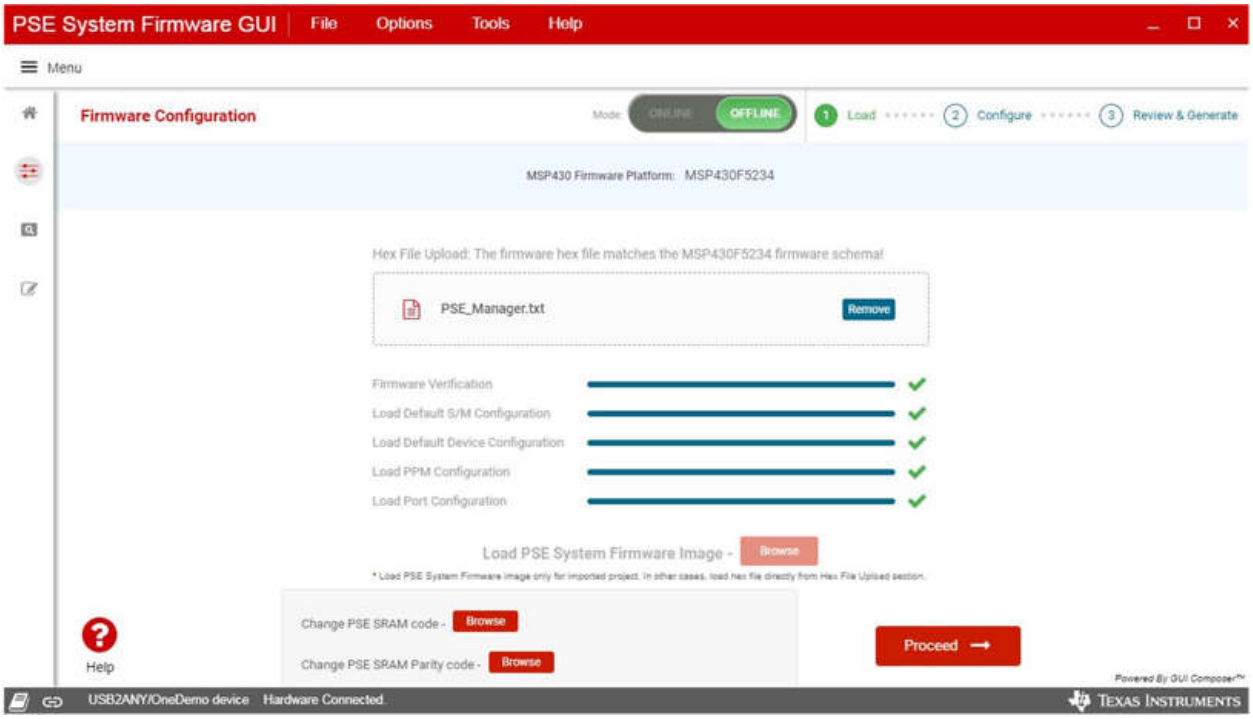


Figure 3-3. GUI Device Selection and Image Load

The configurations are split into four sections: system configuration, port power management (PPM) configuration, device configuration, and port configuration.

The system configuration is applied to the whole system. This tab is always available on the to the right of the GUI. The following parameters can be configured through the system configuration tab:

- Legacy detection functions

  Legacy devices released prior to the PoE standard can be powered through the Ethernet cable. The PSE system firmware detects these legacy PDs and powers on with protection.
- Use of external sensing circuit

  The external sensing circuit is used to measure the total power consumption of the system. When the current exceeds the power budget, the MCU shuts down low priority ports. This increases the system response to the load step change.
- System boot-up setting
  1. Turn on the PSE port as soon as the power is up.
  2. Turn on the PSE port after the PoE enable command is sent from the host
- Port overload retry mode
  1. Re-enable immediately: after overload happens, the port is re-enabled immediately. If the overload still presents, it will try at most five times and shuts down the port if the overload is not removed within five retries. The port is re-enabled after the PD is removed from the port and reconnects to the port.
  2. Re-enable after PD is disconnected and connected: after overload happens, the port is disabled immediately and is re-enabled after the PD is removed from the port and reconnects to the port.
  3. Timer controlled: the port is re-enabled immediately after overload happens. The port keeps retrying for a period (controller by timer) and is disabled after the timer expires. The port is re-enabled after the PD is removed from the port and reconnects to the port.
- OSS signal source (from MCU or CPLD):In a multi-power supply system, when one power supply has faults and the remaining power supply is not able to supply the current power consumption, turn off low priority ports to protect the remaining power supply. The OSS function of the PSE is used to fast shutdown the low priority ports. There are 2 sources to generate the OSS signal:
  1. MCU generates the OSS signal

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2. CPLD generates the OSS signal

- Interrupt mask

  The interrupt mask in Figure 3-4 can be configured to enable interrupt events to notify the host through the MSP430 P6.0 or MSPM0 PA26.

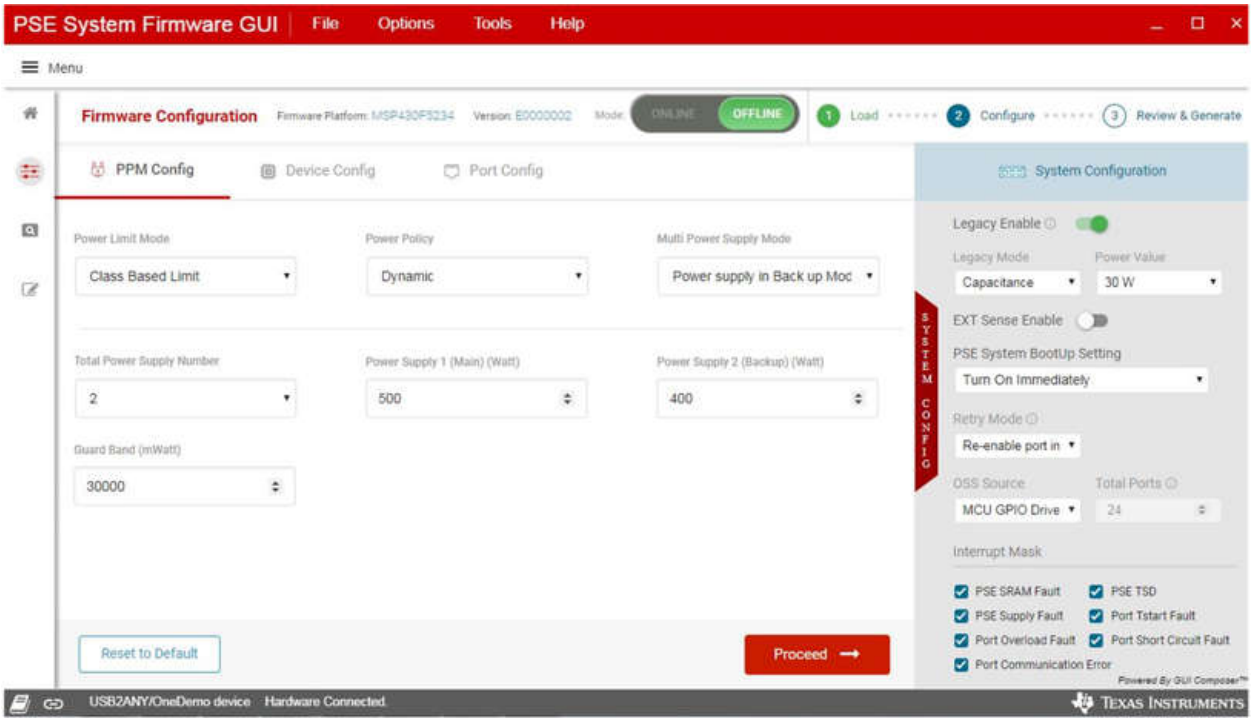


Figure 3-4. GUI System Configuration and PPM Configuration

PPM configuration is applied to the port power management mechanism. The following parameters can be configured through the PPM configuration tab:

- Power limit mode:class limit mode and port limit mode
  1. Class limit mode:in class limit mode, the port power is limited by the PD's class level. For example, if the PD is class 8, the port power limit(PCUT) is set to 90W.
  2. Port limit mode:in port limit mode, the port power is limited by the host. The host MUST set port power limit before the port is powered on.

- Power policy: static and dynamic mode
  1. Static mode:in static mode, the port power allocation is set to port power limit. In class limit mode, port power allocation is class level power of the PD and in port limit mode, the port power allocation is the port power limit configured from the host.
  2. Dynamic mode: in dynamic mode, the port power allocation equals to the actual consumed power of the port. It allocates the unused power of the port to other ports.
- Multi-power supply mode: RPS and sharing mode:
  1. Redundant power supply (RPS) mode:in RPS mode, the total power budget equals to the power budget of the main power supply when both main power supply and backup power supply are connected. The total power budget equals to backup power supply's power budget when the main power supply is disconnected.
  2. Sharing power supply mode:in sharing mode, the total power budget equals to the sum of two power supplies' power budget when both power supplies are connected. The total power budget equals to remaining power supply's power budget if one of the power supplies is disconnected.
- Total number of power supplies and the power budget of each power supply. **If there is only one power supply, the power good signal must be connected to P1.5 on MSP430 or PB7 on MSPM0.**

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- Power guard band: when the total allocated power < total power budget — guard band, there is no more low priority ports to be turned on and the guard band LED turns on.

Device configuration is mainly used to configure the mapping between the PSE device channels and the logical RJ45 ports. When mapping a 4-pair port, only channels within the same quad (channel 1–4 or channel 5–8) can be mapped to one 4-pair port.

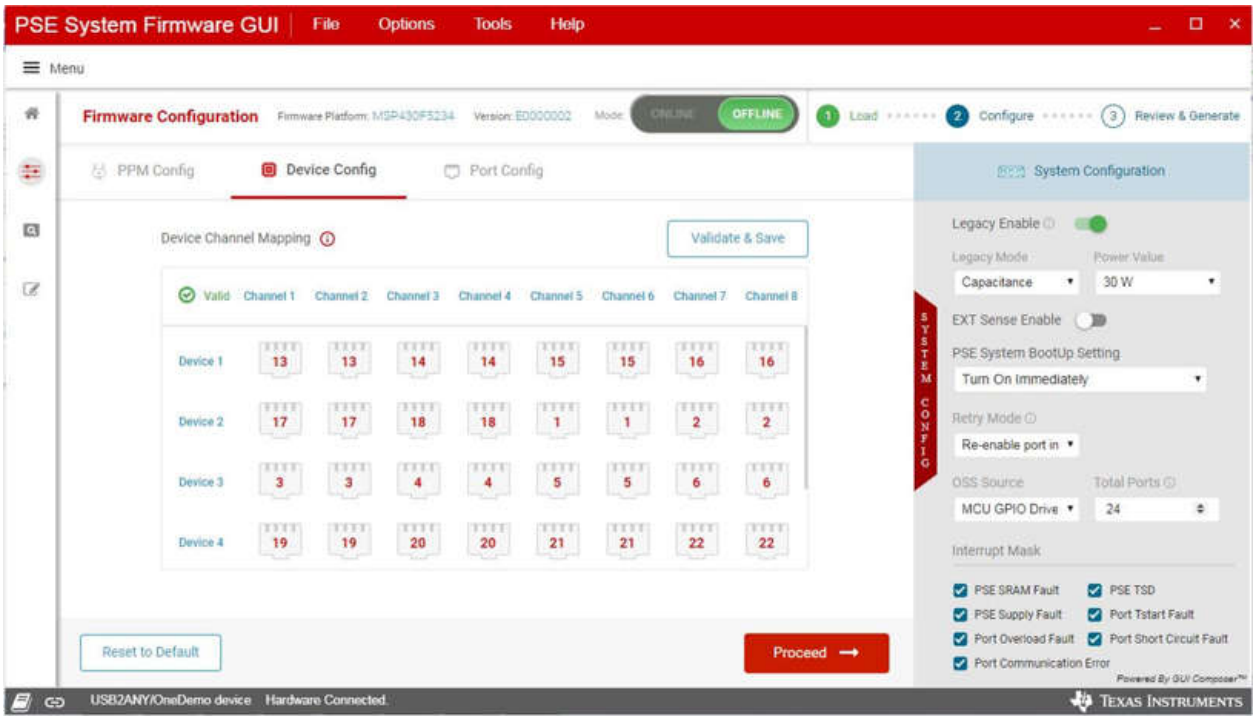


Figure 3-5. GUI Device Configuration

The *Port Configuration* is applied to the port by port settings, such as port PoE enable and disable, port priority, and port power limit (only in port limit mode).

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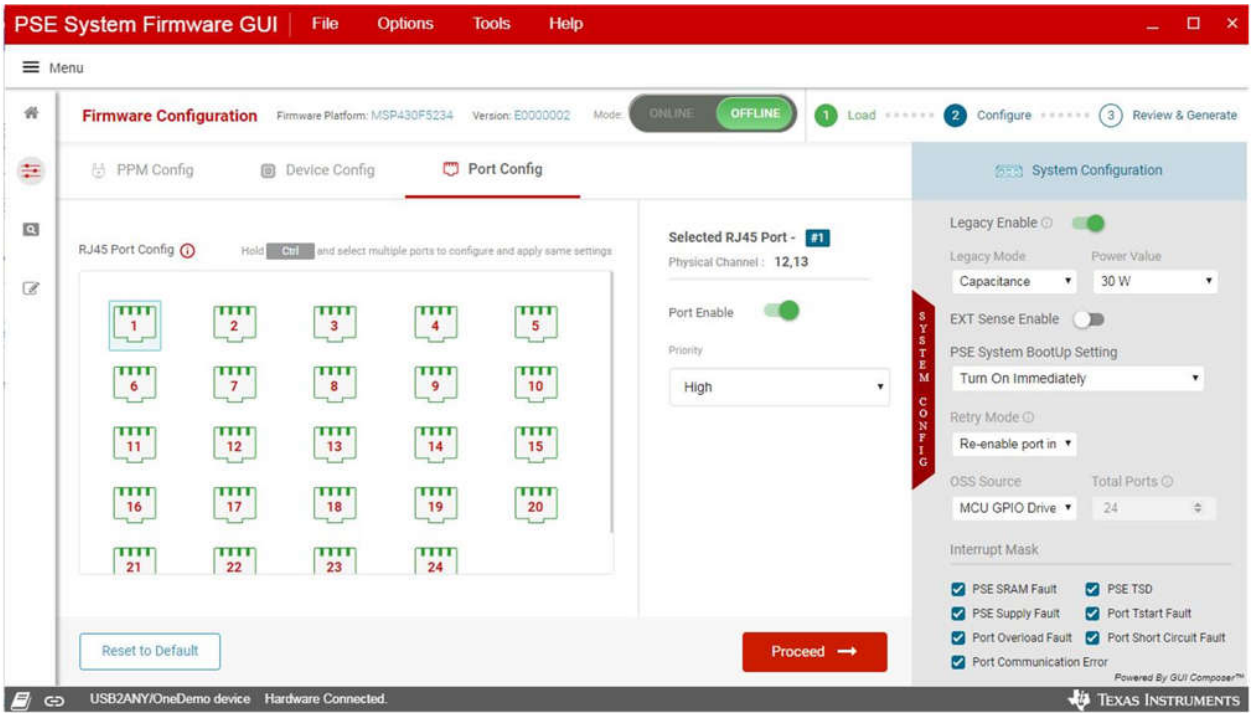


Figure 3-6. GUI Port Configuration

When everything has been configured, select the *Proceed* button. The summary page displays all of the configurations being set compared to the factory default configurations. When everything is verified, you can generate the hex file or flash the code to the MCU device directly.

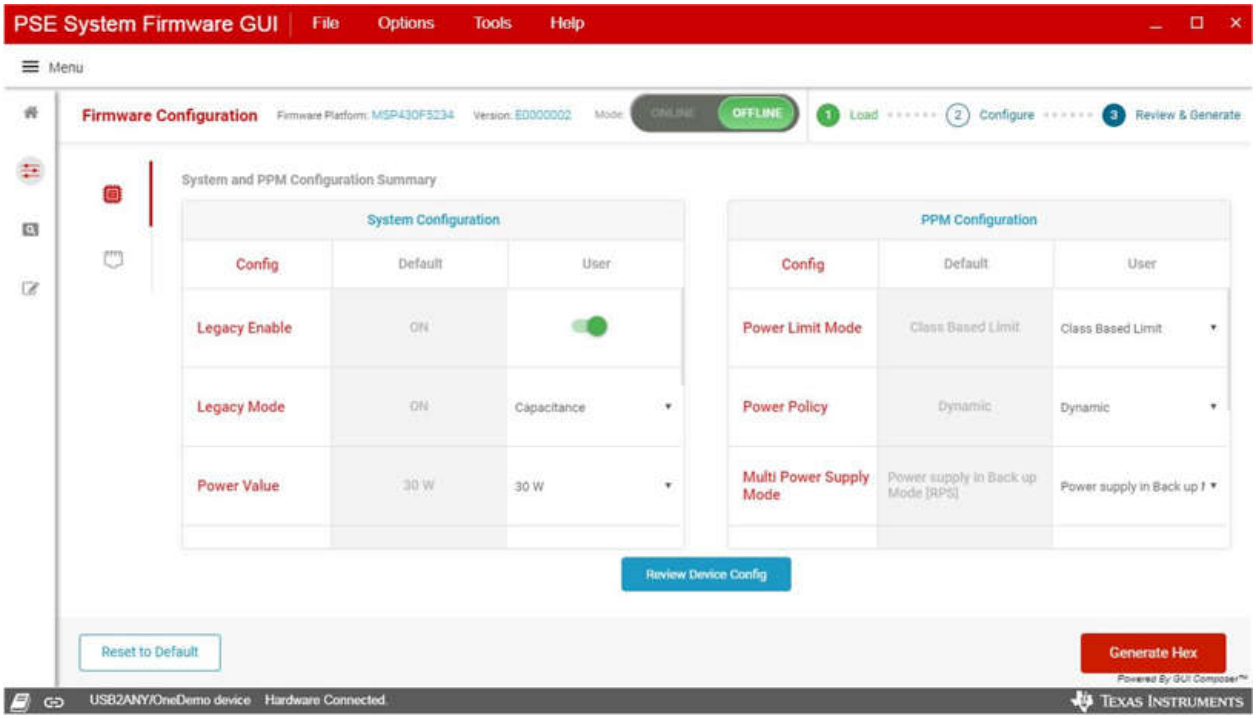


Figure 3-7. GUI Configuration Summary

When configurations are reviewed, the GUI can generate the default code image and program the device directly through **MSP-FET/XDS110**.

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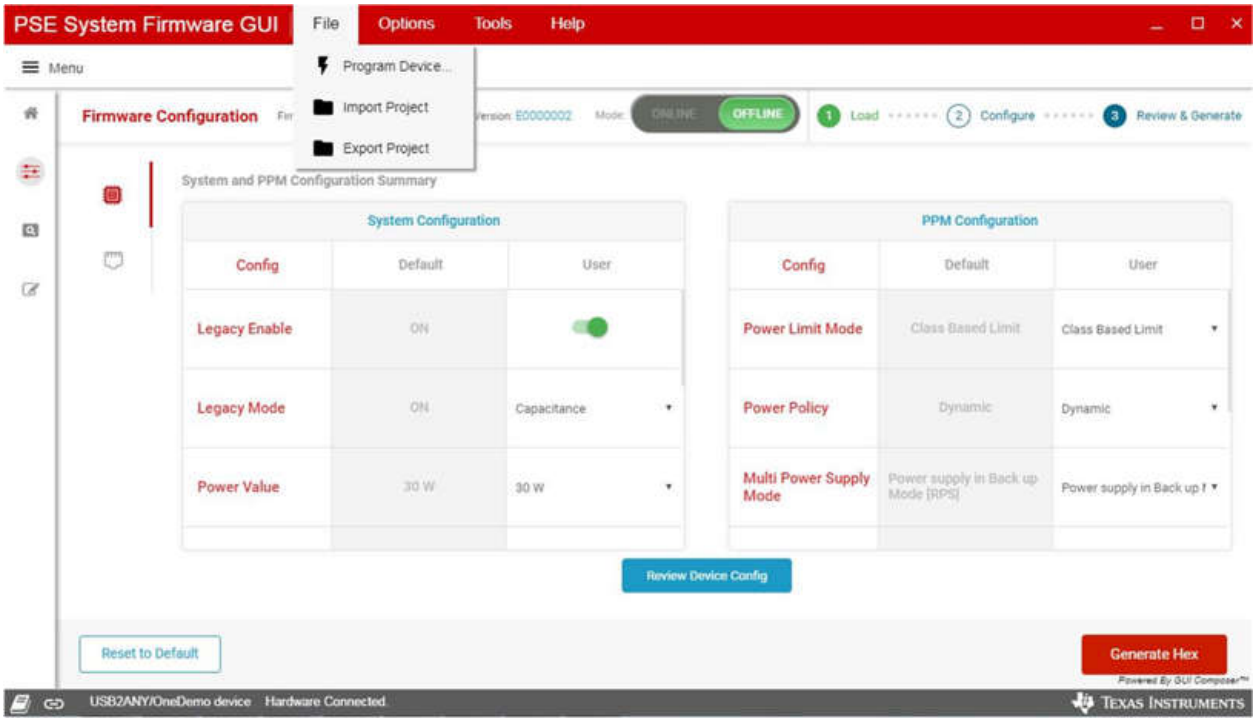


Figure 3-8. GUI Program Device and Generate Hex

When the code is successfully flashed to the MCU, the system will be up and running. MSP-FET/XDS110 can be disconnected from the laptop or PC. Connect the USB2ANY (with 30-pin ribbon cable) to a laptop or PC and the GUI will be in online mode after selecting host interface protocol.

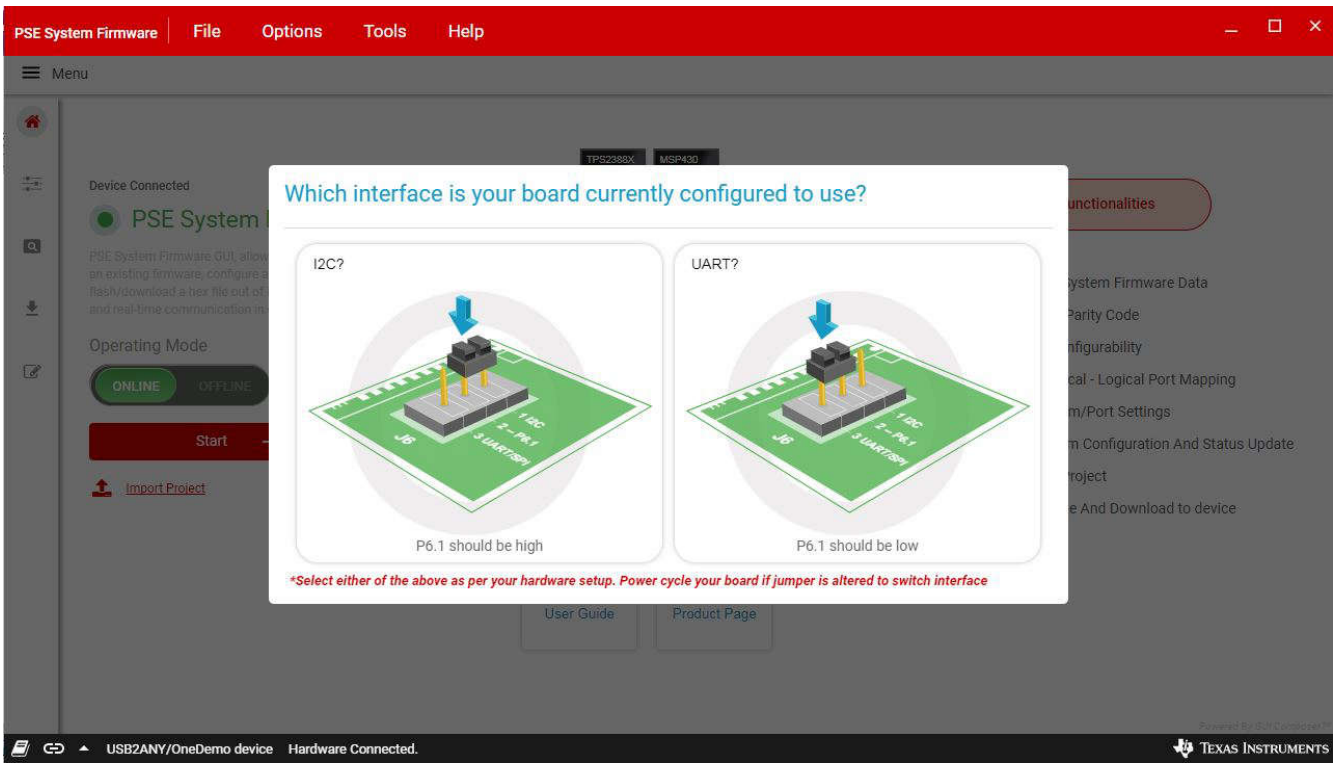


Figure 3-9. Host Interface Protocol Selection in Online Mode

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When the device is connected to GUI, real-time changes can be made on the configuration page and status page shows the real time system status. The status page shows the system, device, and port real-time status. The user can also change the system configuration in the configuration page: each change is converted to a host command to the MCU. The user can also press the *Save Configuration* button to save the current configuration as the default setting.

Note

For the FirmPSE MSPM0 GUI, the Host Interface Protocol selection only shows the I2C choice, as MSPM0 does not support UART.

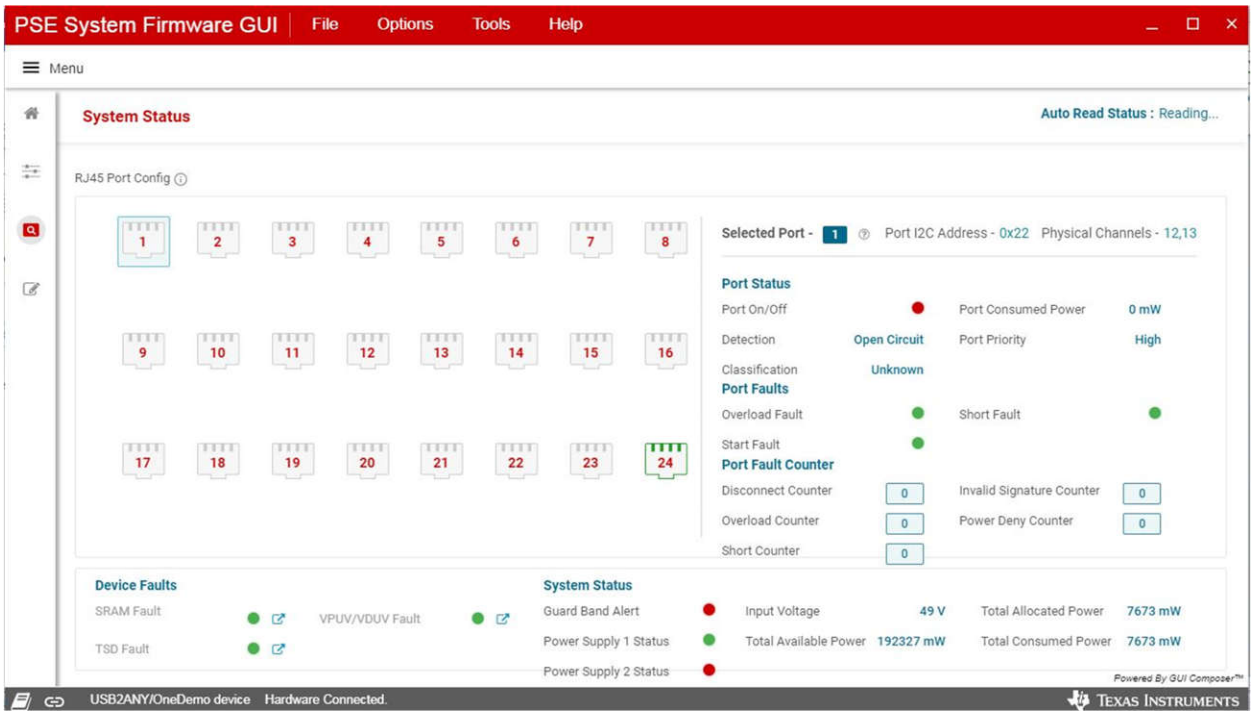


Figure 3-10. GUI Status Page

The BSL firmware update page provides the field firmware upgrade functions that the firmware can be upgraded through the same I^2C or UART port as the normal communication. This is beneficial to firmware upgrade after the product is released to customers.

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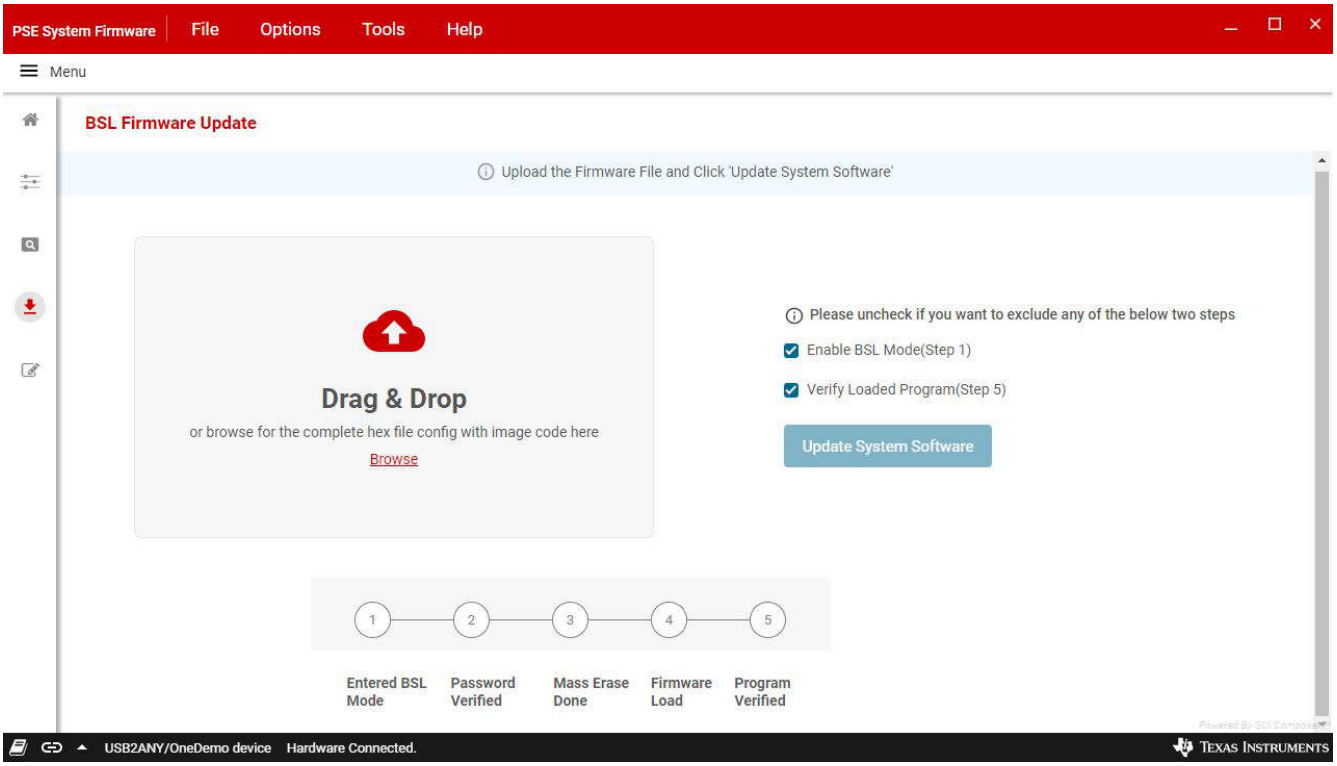


Figure 3-11. BSL Firmware Update Page

Before using BSL page to update the MSP430/MSPM0 firmware, BSL code needs to be flashed to MCU if it has not been flashed. Download Uniflash from ti.com and use it to flash the BSL code by following the steps:

Select MCU device to MSP430F5234/MSPM0G1107.

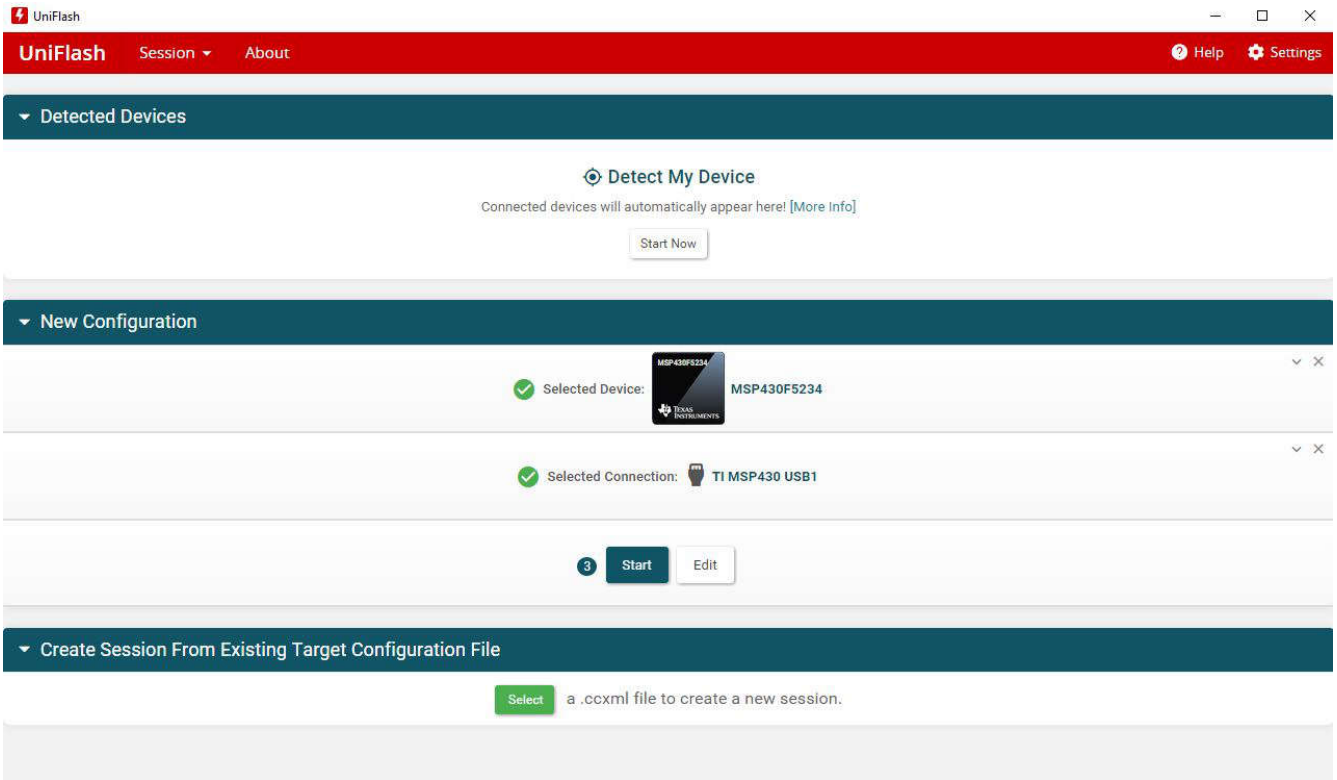


Figure 3-12. MCU Device Selection Page

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Configure the flash section.

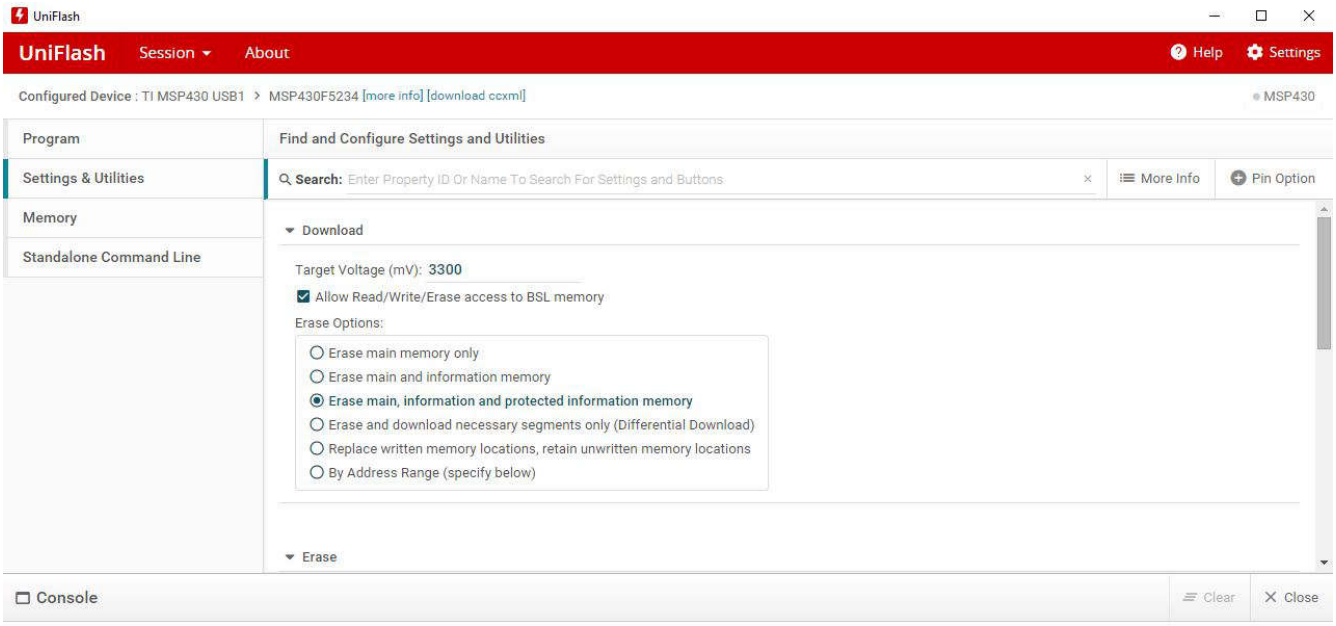


Figure 3-13. Configure Settings and Utilities Page

Load BSL code and flash.

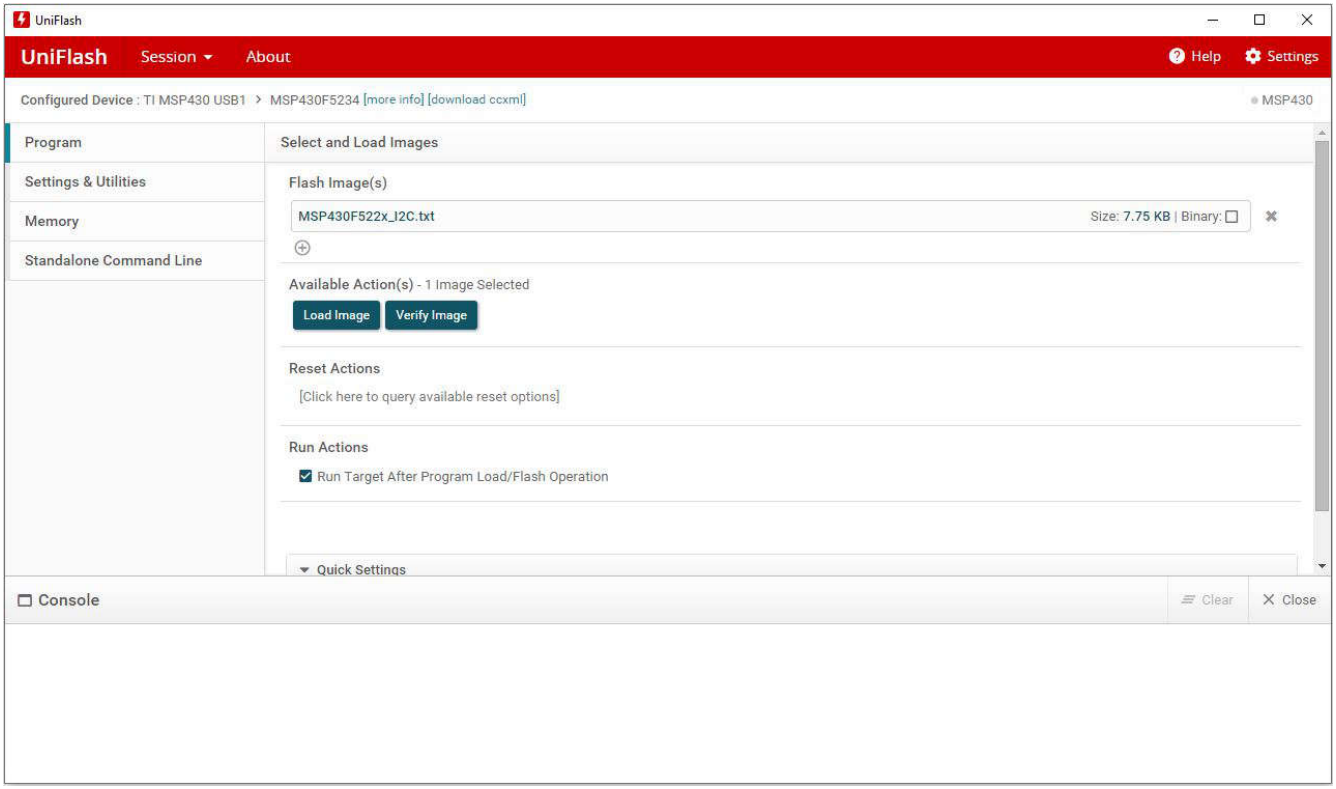


Figure 3-14. Select and Load Images Page

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In the debug page, users can read and write raw data to MCU following host interface protocol and to each PSE device's registers by providing I^2C address and register number. The password is "C430".

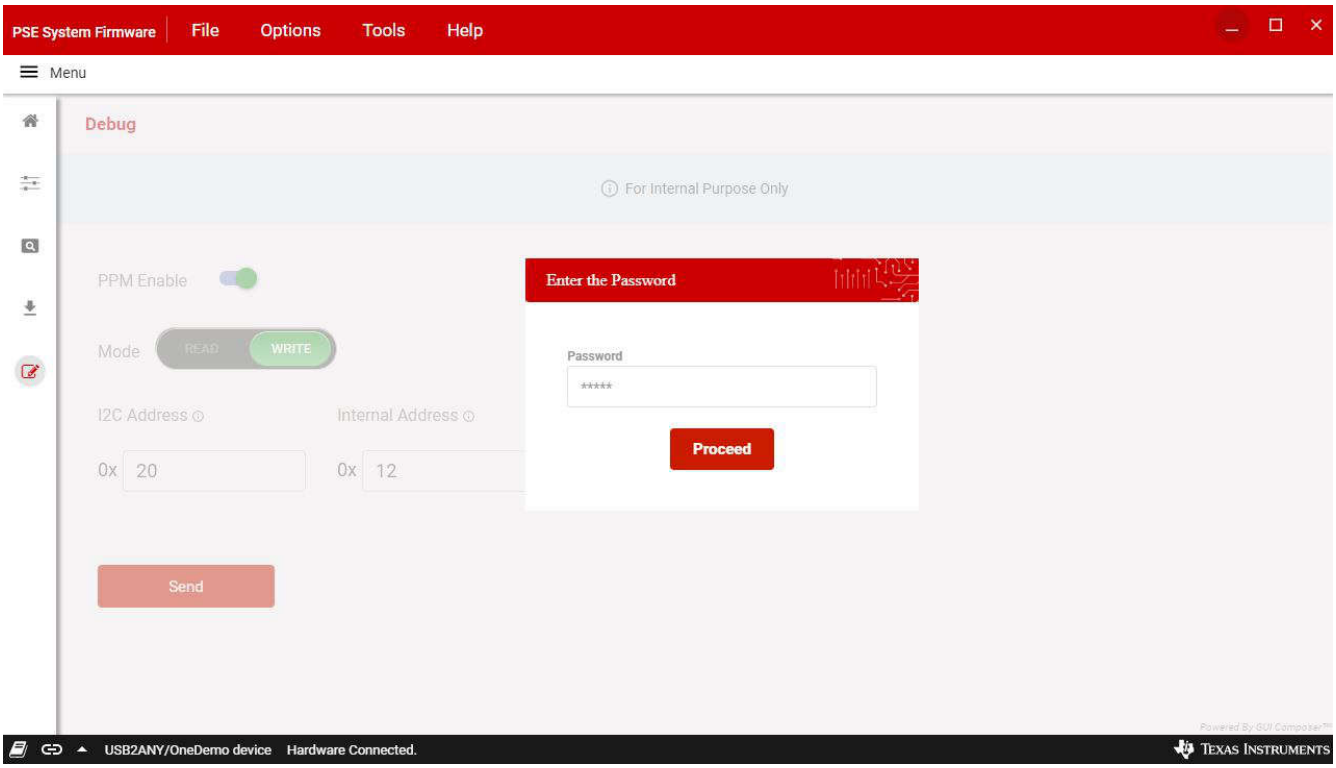


Figure 3-15. Debug Page

3.2.2 Test Results

The IEEE 802.3bt compliance test suite is currently not available. The test report will be added in the fourth quarter of 2019.

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4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematic

To download the schematics, see the design files at TIDA-050026-23882.

4.1.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050026-23882.

4.1.3 PCB Layout Recommendations

KSENSA is shared between SEN1 and SEN2, KSENSB is shared between SEN3 and SEN4, KSENSEC is shared between SEN5 and SEN6, KSENSED is shared between SEN7 and SEN8. To optimize the accuracy of the measurement, the PCB layout must be done carefully to minimize the impact of PCB trace resistance. Refer to the TPS23882 Layout section as an example.

4.1.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-050026-23882.

4.1.4 Altium Project

To download the Altium project files, see the design files at TIDA-050026-23882.

4.1.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050026-23882.

4.1.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050026-23882.

4.1.7 Software Files

To download the software files, see the design files at TIDA-050026-23882.

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5 Related Documentation

1. Texas Instruments, TPS23882 Type-3, 2-pair, 8-Channel, PoE PSE controller with SRAM and 200-mΩ RSENSE, product page
2. Texas Instruments, TPS23882B Type-3, two-pair, 8-channel PoE PSE controller with autonomous mode, SRAM and 200-mΩ RSENSE, product page
3. Texas Instruments, TPS23882EVM-084 TPS23882 Type-3, 30W, 2-pair, PSE daughter card for 24-port PSE systems, product page

5.1 Trademarks

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2019) to Revision A (November 2026)	Page
• Added TPS23882B1EVM-035, TPS23882B, and MSPM0G1107 links to *Resources* section	1
• Added content in *Description* section to include the MSPM0 and TPS23882B1EVM-035	2
• Updated note in *Description* section to include the MSPM0G1107	2
• Added MSPM0 daughtercard to *MCU - Host Communication* section	5
• Updated section title from *MSP430F523x Hardware Design* to *MSP430F523x and MSPM0G1107x Hardware Design*	5
• Updated terms "master" and "slave" to "controller" and "peripheral" respectively in *MSP430F523x and MSPM0G1107x Hardware Design* section	5
• Added Table 2-1 in *MSP430F523x and MSPM0G1107x Hardware Design*	5
• Added Table 2-4 in *MSP430F523x and MSPM0G1107x Hardware Design*	5
• Updated section title from *TPS23882* to *TPS23882 and TPS23882B*	7
• Added TPS23882B to *TPS23882 and TPS23882B* section	7
• Updated section title from *MSP430F523x* to *MSPM0G1107x and MSP430F523x*	8
• Added MSPM0G1107x to *MSPM0G1107x and MSP430F523x* section	8
• Updated content in *MSPM0G1107x and MSP430F523x* section	8
• Updated terms "master" to "controller" in *ISO7741* section	8
• Updated MSP430 and PSE devices to MCU and PSE devices in *ISO7731* section	8
• Updated "MSP430 and isolators" to "MCU and isolators" in *LM5020* SECTION	10
• Added MSPM0 daughtercard, TPS23882B1EVM-035, and the XDS110 debugger to *Hardware* section	12
• Added MSPM0 FirmPSE GUI to *Software* section	12
• Added PSEM0MCUDAUEVM-018 and D1 LED to Table 3-1 in *EVM LEDs* section	14
• Added TPS23882B1EVM-035 to Table 3-2 in *EVM Test Points* section	14
• Added TPS23882B1EVM-035 and PSEM0MCUDAUEVM-018 to Table 3-4 in *EVM Input and Output Connectors* section	16
• Added TPS23882B1EVM-035 and MSPM0 to *PSE System Firmware GUI Installation* section	17
• Added MSPM0 pins, flash instructions, and note to *PSE System Firmware GUI Installation* section	17
• Added TPS23882B product page to *Related Documentation* section	28

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