Technical White Paper

Ethernet In SSTs

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Abstract

The need for efficient power delivery from grid to module, and the shortage in raw-earth materials for constructing prior-generation models are key challenges driving the development of Solid State Transformers (SST). SSTs bridge between the mid-voltage grid and the power demanding, low-voltage equipment such as battery storage (also known as energy storage solutions), the 800V DC bus power rail in data centers, and electric vehicle charging stations.



Figure 1-1. Evolution of the Electrical Distribution Network in Data Centers

SSTs are a new implementation of transformers which trade the bulky ferrite core with windings (turns ratio of 10:1 or more) to step up or down voltage for power electronics which control and regulate the power conversion alongside a slimmer ferrite core. In contrast to traditional transformers, SSTs offer additional features such as bidirectional power flow, better energy efficiency, and significantly smaller size and weight.

This white paper explores the challenges that a system designer can face when developing an SST module, and how Texas Instruments ethernet PHYs can play a critical role in SST operations.

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1 SST Design Challenges

Designing such a complex system can present some challenges when improving upon the conventional transformer architecture.

A key benefit of SSTs over conventional transformers is power efficiency. However, efficiency is tied to faster switching frequency. To achieve this, the data that controls the switching needs to be sent faster. In addition, this data would need to pass through a series of blocks if operating in a daisy chain. Device latency becomes a factor as data would need to move through the entire chain to get to all necessary cells.

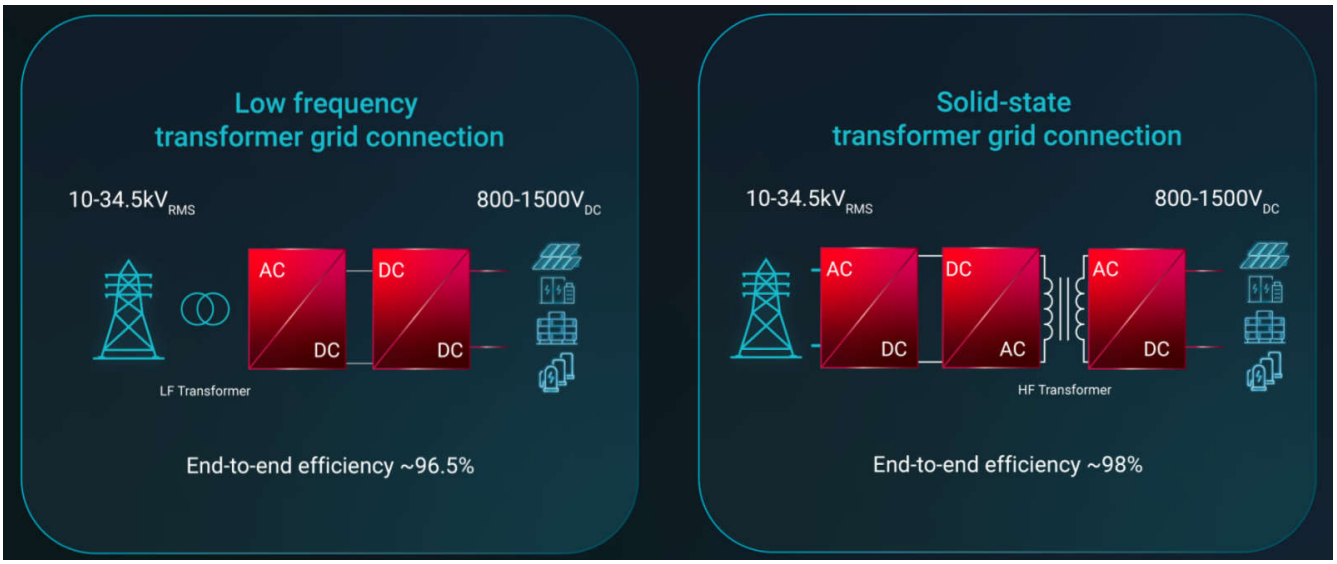


Figure 1-1. Comparison of conventional (low frequency) and solid-state transformer topologies

Another key benefit of SSTs over conventional transformers is increased power density. SSTs realize this benefit from a reduced transformer size due to faster frequency across the transformer loosening the requirements on the size due to Lorentz Law. In addition, technological developments have pushed the introduction of a single stage AC converter. This simplifies the AC-DC-AC converter into a single stage (such as a matrix converter) where the incoming signal is manipulated and sped up without intermediate rectification. With this simplification, more data must be transmitted through the MV MCU to verify proper operation of the single-stage circuit. This data must be sent within an amount of time to still adhere to the control loop bandwidth of the MV stage. In addition, as switching becomes even faster, verifying synchronization across cells are important to make sure that there are no contentions on the output.

Overall, there is a growing need for faster, more deterministic communication to enable for more power efficient, spatially dense SST modules.

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2 Need faster communication? TI Ethernet PHYs can help

Ethernet PHY transceivers can help address these common challenges. Compared to older communication types, Ethernet provides the fastest and most deterministic communication possible.

The typical control loop for SSTs has a refresh rate of 100 microseconds (10kHz). Depending on the data interface, legacy communications have been with CAN, LIN, or RS-485. However, these communication data rates only reach up to 500kbps-1Mbps. Ethernet can provide a faster communication chain capable of up to 1Gbps data rates. These data rates are also consistent up to 15m for specific types of ethernet and up to 100m for the most common type of Ethernet. This is a significant upgrade in bandwidth and distance over CAN, LIN, and RS-485.

Compared to the older communication topologies, there is an intrinsic delay due to the implementation of the network. From commander-responder acknowledgements to other bus artifacts, it takes a non-deterministic time for sending data between nodes in a multidrop environment. This makes synchronization difficult for the control loop within the SST. With most Ethernet topologies being point to point, the latency becomes much more deterministic and is in the order of nanoseconds to microseconds depending on device. In addition, there are real-time real-time communication systems such as EtherCAT for system synchronization which can enhance ethernet communication at no extra hardware cost on the PHY subsystem. In an EtherCAT system, the topology is point-to-point across a daisy chain compared to multidrop.

2.1 TI Ethernet PHY Product Selection

There are two types of ethernet that TI offers – standard ethernet and single pair ethernet. Standard ethernet supports up to 100m cabling at fixed speeds of 10Mbps, 100Mbps, and 1Gbps. This is using CAT5e or CAT6 cabling where there are either two or four twisted pairs used for communication. Single pair ethernet has similar speeds but is more fixed (1 speed per device, vs multispeed on the standard ethernet devices) and lowers the cable type to a single twisted pair for communication. However, there is a trade-off of lower cable lengths due to serialization and bidirectional communication leading to differences in the analog and digital circuitry.

For 10/100Mbps standard ethernet, DP83822xF and DP83826A will be best suited for this application. DP83826A is recommended if the lowest deterministic latency (dozens of nanoseconds) is required along with the strictest EMC testing for a module. DP83822xF is Texas Instruments' 100BASE-FX design for the MV optical connections. For 1Gbps standard ethernet, DP83869HM is best suited with copper and fiber support in both 100Mbps and 1Gbps speeds. Texas Instruments also has a 50kW SST reference design available, TIDA-011012 which utilizes a single daisy copper daisy chain with DP83826, with localized fiber connections between the LV and MV control board. This allows for 10/100Mbps data throughput on the communication loop with two PHYs per LV board.

Texas Instruments also offers Single Pair Ethernet (SPE) PHY transceivers in 10Mbps, 100Mbps, and 1Gbps. SPE allows for lighter cabling, thereby reducing cost and weight of the SST while still maintaining fast speeds and hundreds of nanoseconds of latency. For 100Mbps, DP83TC817S-Q1 is the best suited PHY for this application while for 1Gbps, DP83TG721x-Q1 will be recommended. Like standard ethernet, these devices use point to point connections which work best in a daisy chain for a control loop. Texas Instruments also offers multidrop 10Mbps PHYs which follow 10BASE-T1S. Adopting T1S ethernet in an SST provides a direct upgrade over CAN, LIN, and RS-485 due to faster speeds while maintaining the existing cabling architecture if upgrading from the latter technologies. For a pure transceiver, DP83TD53x-Q1 is an analog front end (AFE) device with OA-3 pin for digital communication to a SoC. DP83TD555J-Q1 is an enhanced T1S device which integrates the AFE alongside a Physical Layer Collision Avoidance (PLCA) layer, PHY Control layer, Media Access Control layer, and SPI receiver to easily interface T1S communication with SPI-compatible SoC's.

3 Conclusion

Solid State Transformers have growing communication requirements which Ethernet can address from faster bandwidth, lower and more deterministic latency, and even optical interfacing for electrical isolation of the mid-voltage circuitry. TI's PHY portfolio, whether it be multi-speed standard Ethernet to single-speed single-pair Ethernet, can address these growing requirements in this evolving power distribution equipment.

4 Additional Resources

- See Solid-state transformers are ready to reshape grid-scale power delivery

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