Technical Article

Design an active clamp circuit for rectifiers at a high switching frequency

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Introduction

In vehicle electrical systems, a high- to low-voltage DC/DC converter is a reversible electronic device that changes the DC from the vehicle's high-voltage (400V or 800V) battery to a lower DC voltage (12V). These converters can be unidirectional or bidirectional. Power levels from 1kW to 3kW are typical, with systems requiring components rated at 650V to 1,200V for the converter's high-voltage power net (primary side) and at least 60V on the 12V power net (secondary side).

The need for greater power density and a smaller powertrain led to increased switching frequencies for power components to several hundred kilohertz, in order to help shrink the size of magnetic components. The miniaturization of a high- to low-voltage DC/DC converter exposes many issues that are not as important at lower switching frequencies, such as electromagnetic compatibility (EMC), thermal dissipation, and active clamp for metal-oxide semiconductor field-effect transistors (MOSFETs). In this power tip, I will discuss the design of clamping circuits for synchronous rectifier MOSFETs at a high switching frequency.

Traditional active clamp

The phase-shifted full bridge (PSFB) shown in Figure 1 is a popular topology in high- to low-voltage DC/DC applications because it can achieve soft switching on switches to increase converter efficiency. But you can still expect to see high-voltage stress on the synchronous rectifier, as its parasitic capacitance resonates with the transformer leakage inductance. The voltage stress of the rectifier could be as high as Equation 1:

$$V_{ds\_\max} = 2V_{IN}x\left(N_s/N_p\right) \quad (1)$$

where Np and Ns are the transformer's primary and secondary windings, respectively.

Considering the power level of a high- to low-voltage DC/DC converter and the power losses of a resistor-capacitor-diode snubber [1], designers often use active clamp circuits for synchronous rectifier MOSFETs. Figure 1 shows the typical circuits.

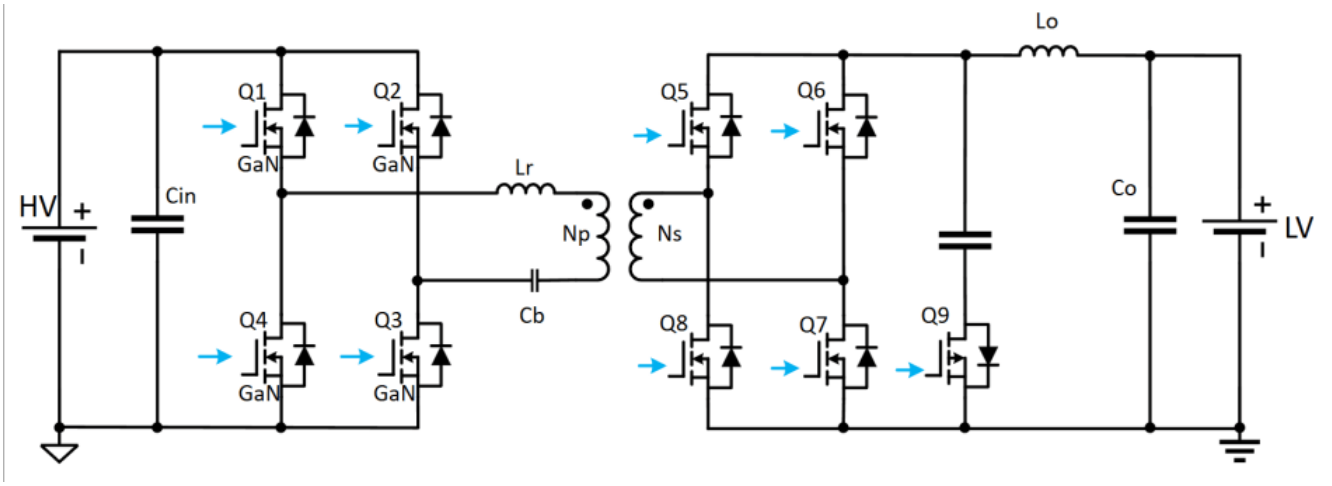

Figure 1. Traditional active clamp circuit for PSFB synchronous rectifier MOSFETs. Source: Texas Instruments

In this schematic, you can see the P-channel metal-oxide semiconductor (PMOS) Q9 and the snubber capacitor, which are the main parts of the active clamp circuit. One terminal of the snubber capacitor connects to the output choke, and the source of the PMOS connects to ground. In a traditional active clamp circuit for a PSFB, synchronous rectifier MOSFET Q5 and Q7 have the same scheme; so do Q6 and Q8. Each time after the synchronous rectifier MOSFETs shut down, the PMOS will turn on with a proper delay time.

Figure 2 shows the control scheme of the PSFB and active clamp. You can easily find that the switching frequency of PMOS will be double the f_{sw}.

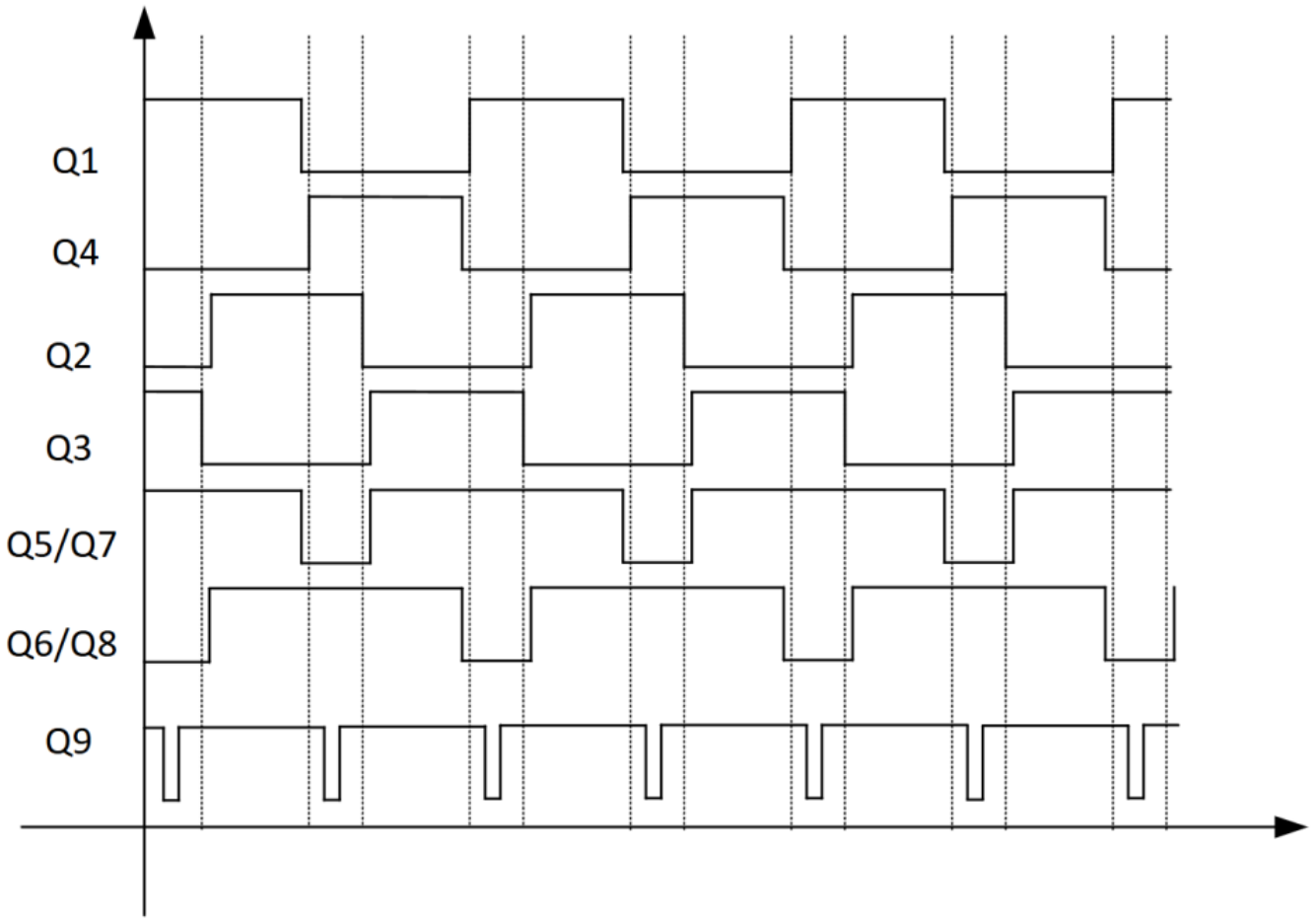

Figure 2. Control scheme of active clamp PMOS Q9 where the switching frequency of the PMOS is double the f_{sw}. Source: Texas Instruments

Evaluating active clamp loss

You can use Equation 2, Equation 3, Equation 4, Equation 5, and Equation 6 to evaluate the loss of the active clamp PMOS. Apart from P_{on_state}, all of the other losses are proportional to f_{sw}. When the switching frequency of the PMOS doubles, the loss doubles, so you will need to resolve the PMOS thermal issue. And the exact thermal issue turns out to be even worse when pushing the f_{sw} higher to meet the needs for miniaturization.

$$P_{\text{on\_state}} = I_{rms}2 \times R_{dson} \quad (2)$$

$$P_{\text{turn\_on}} = 0.5 \times V_{ds} \times I_{on} \times t_{on} \times f_{sw} \quad (3)$$

$$P_{\text{turn\_off}} = 0.5 \times V_{ds} \times I_{off} \times t_{off} \times f_{sw} \quad (4)$$

$$P_{\text{drive}} = V_{drv} \times Q_g \times f_{sw} \quad (5)$$

$$P_{\text{diode}} = I_{\text{snubber}} \times V_{sd} \times t_d \times f_{sw} \quad (6)$$

The proposed active clamp

So, what can you do? To select PMOS with better figure of merit (FOM) or to choose thermal grease with higher conductivity coefficient? Both are OK but remember the thermal issue caused by active clamp still concentrates at one part which makes the issue hard to resolve. Can we divide the thermal into several parts? A feasible way is to use two active clamp circuits and connect the terminal of the snubber capacitor to the switching node of the secondary legs, as Figure 3 shows. Then you can only turn on Q11 after Q5 and Q7 turn off, and only turn on Q10 after Q6 and Q8 turn off. Figure 4 shows the control scheme of the PSFB and proposed active clamp.

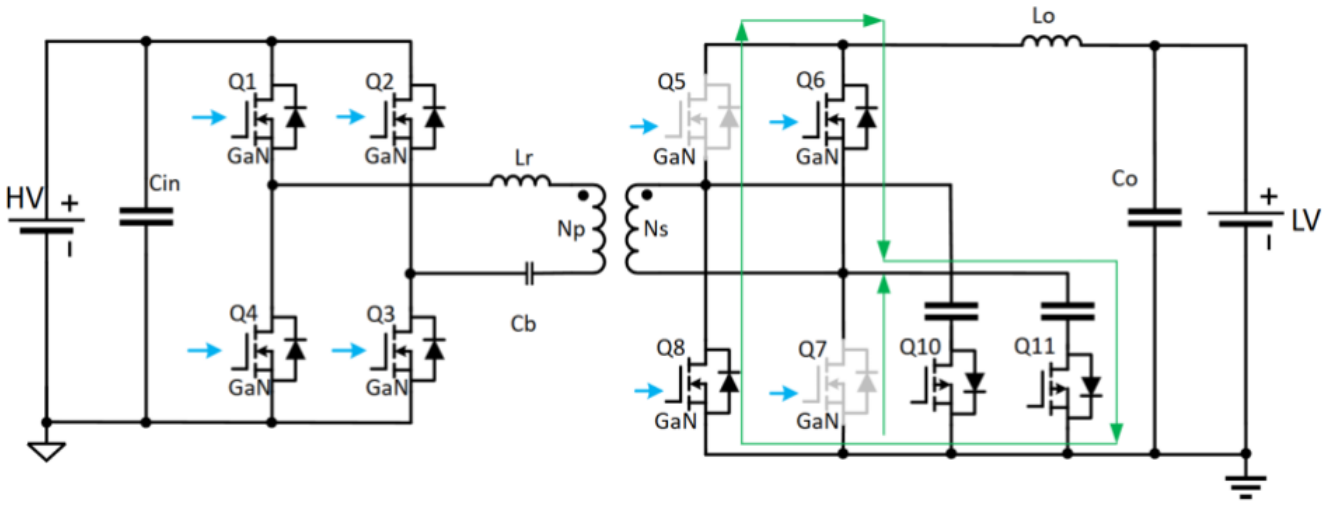

Figure 3. Proposed active clamp circuit for PSFB synchronous rectifier MOSFETs. Source: Texas Instruments

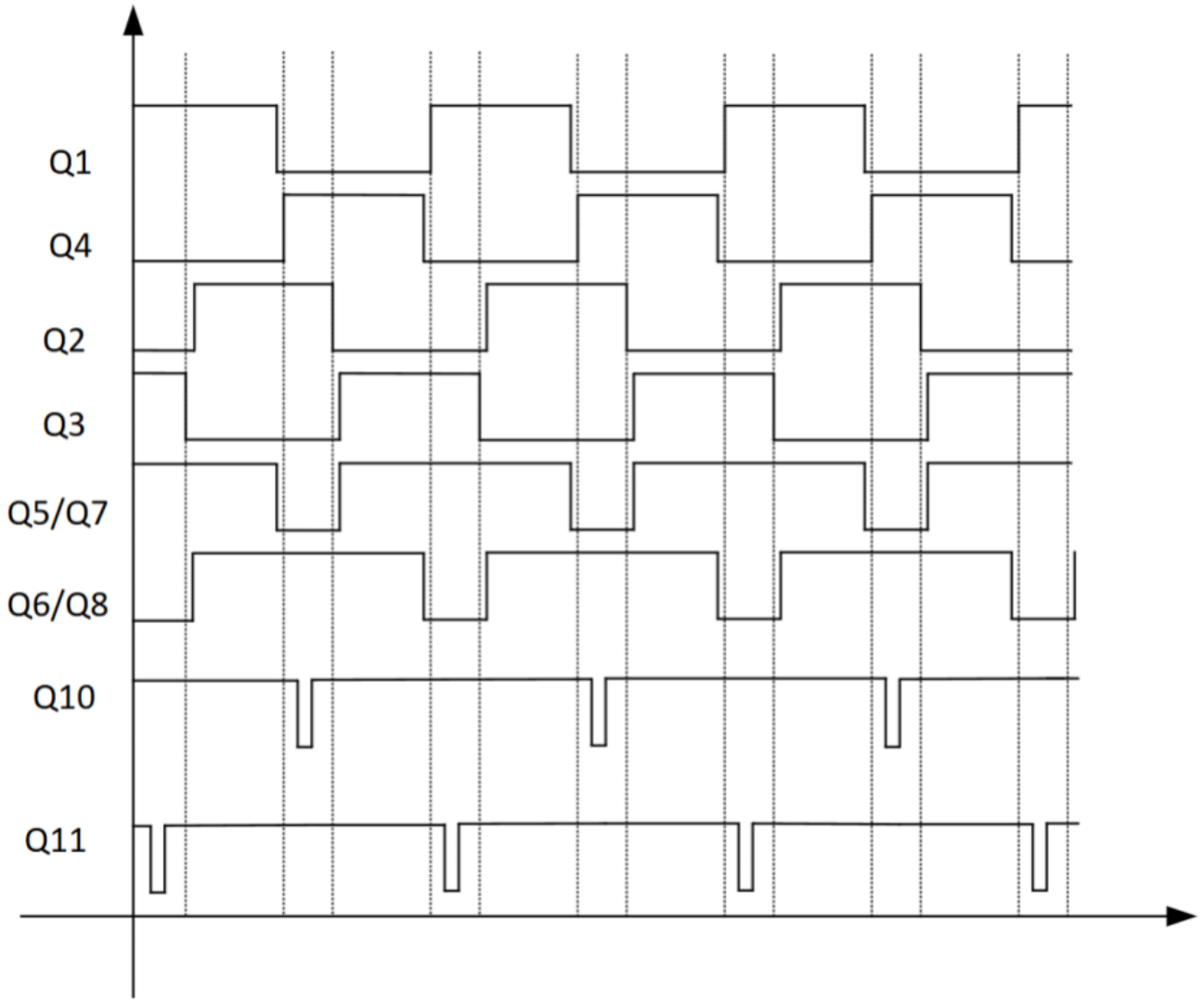

Figure 4. Control scheme of the PSFB and proposed active clamp. Source: Texas Instruments

When Q5 and Q7 turn off, Q6 and Q8 are still on. So, you can locate the clamp loops for Q5 and Q7, as indicated by the green arrows in Figure 3. The switching frequency of Q10 and Q11 are both f_{sw}, not double the f_{sw}.

So, according to Equation 2, Equation 3, Equation 4, Equation 5, and Equation 6, P_{on_state} of each PMOS will be one quarter of original, P_{turn_on}, P_{turn_off}, $P_{drive,}$ and P_{diode} will be one half of original. Obviously, the proposed method divides the loss of the clamp circuit into two parts and even less, which makes it easier to deal with the thermal issue.

Let's come back to the clamp loop. Q5 has a larger loop than Q7; it's similar to Q6 and Q8. You will need to pay attention to the layout of the synchronous rectifiers in order to get a minimum clamp loop for Q5 and Q6.

Proposed active clamp performance

Figure 5 and Figure 6 shows the related tests from the High-Voltage to Low-Voltage DC/DC Converter Reference Design with GaN HEMT from Texas Instruments, which uses the proposed active clamp circuit working at a 200kHz switching frequency. Figure 5 shows the voltage stress of the rectifier.

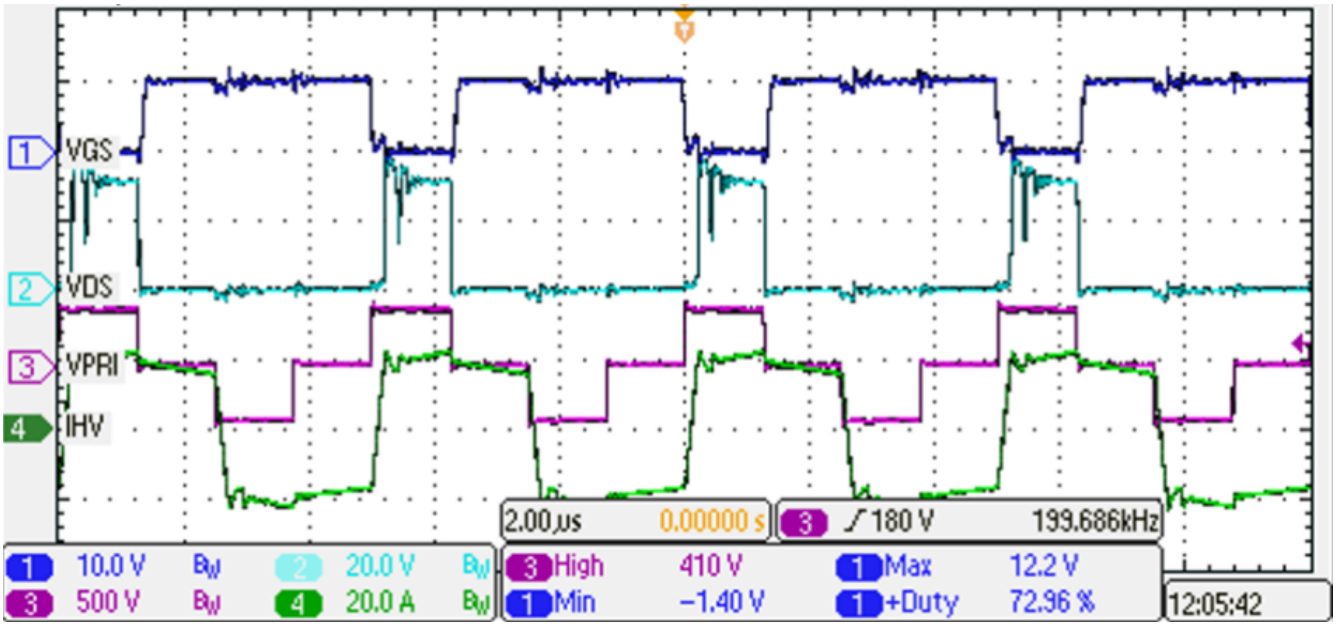

Figure 5. Voltage stress of the rectifier where CH1 is the V_{gs} of the rectifier, CH2 is the V_{ds} of the rectifier, CH3 is the voltage for the primary transformer winding, and CH4 is the current for the primary transformer winding. Source: Texas Instruments

CH1 is the V_{gs} of the rectifier, CH2 is the V_{ds} of the rectifier, CH3 is the voltage for the primary transformer winding, and CH4 is the current for the primary transformer winding. The maximum voltage stress of the rectifier is below 45V at $400V_{IN}$, $13.5V_{OUT}$, 250A I_{OUT}. The maximum temperature of the active clamp circuit is 46.6°C at $400V_{IN}$, $13.5V_{OUT}$, 180A I_{OUT} [2], as shown in Figure 6. So, the proposed control scheme achieves quite good thermal performance for the clamping MOSFET.

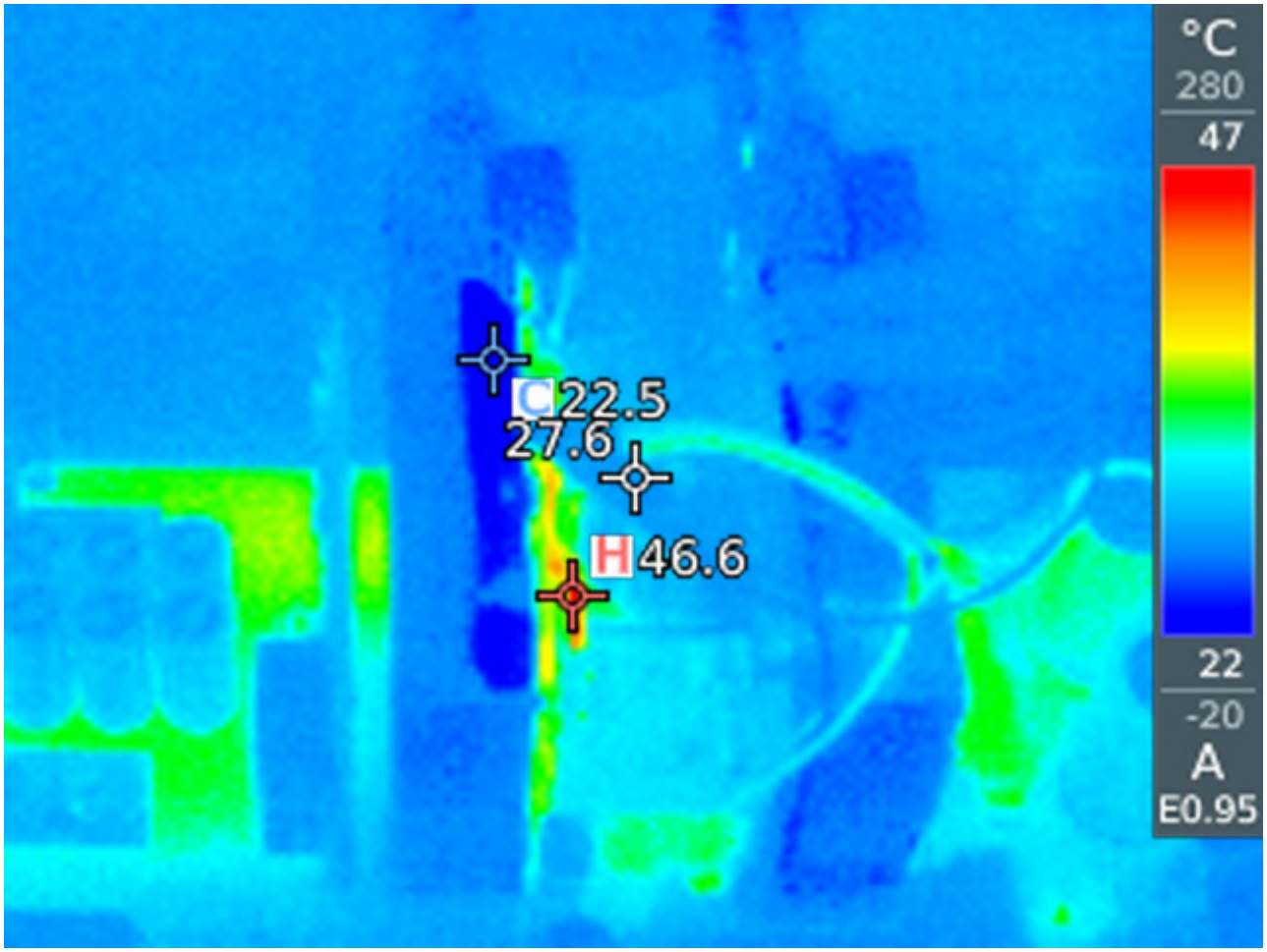

Figure 6. Thermal performance of the active clamp circuit where the maximum temperature of the active clamp circuit is 46.6°C at 400V_{IN}, 13.5V_{OUT}, 180A I_{OUT}. Source: Texas Instruments

500-kHz active clamp sans thermal issues

When promoting switching frequency from 200kHz to 500kHz, the volume of transformer will shrink about 45% [2], which will help to promote the power density of the High-Voltage to Low-Voltage DC/DC Converter. With the proposed method, BOM cost will increase a little, but designer can run the active clamp at 500kHz switching frequency without thermal issue, leading to improved performance. Considering the pulsed drain current of PMOS is far smaller than NMOS, designer can also use NMOS in active clamp with isolated driver and bias power supply if necessary.

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References

1. Betten, John. 2016. “Power Tips: Calculate an R-C Snubber in Seven Steps.” TI E2E™ design support forums technical article, May 2016.
2. “High-Voltage to Low-Voltage DC-DC Converter Reference Design with GaN HEMT.” 2024. Texas Instruments reference design test report No. PMP41078, literature No. TIDT403A. Accessed Dec. 16, 2024.

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