Technical Article

Don’t switch the hard way; achieve ZVS with a PWM full bridge

John Dorosa

The full-bridge converter

A full-bridge converter provides an efficient solution for isolated power conversion (Figure 1). Within this topology, the choice of control method will affect the overall performance of the converter. Most engineers only consider a hard-switched full bridge (HSFB) or a phase-shifted full bridge (PSFB). In this power tip, I will demonstrate a simple modification to a pulse width modulation (PWM)-controlled full bridge that can improve efficiency by achieving zero-voltage switching (ZVS) and eliminate the resonant ringing on the transformer windings.

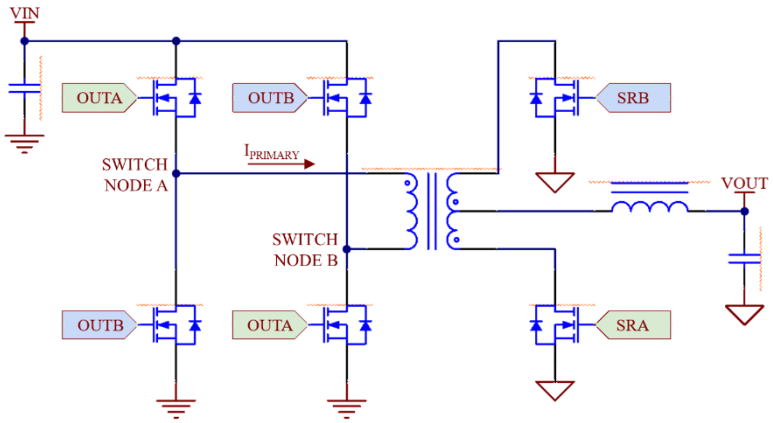

Figure 1. An example of a synchronous HSFB converter power stage. Source: Texas Instruments

The HSFB

An HSFB converter uses two output signals (OUTA and OUTB) that are 180 degrees out of phase to control the diagonal pair of FETs on the primary-side bridge, shown in Figure 1. The controller allows three states for the primary-side FETs: OUTA high and OUTB low, OUTB high and OUTA low, and both OUTA and OUTB low. To maintain regulation, the controller modulates the ratio of time spent in each state.

Figure 2 shows (from bottom to top) the OUTA and OUTB signals, the switch-node voltages on each side of the primary bridge, and the primary winding current. The switch nodes return to half of the input voltage during the dead time when both OUTA and OUTB are low.

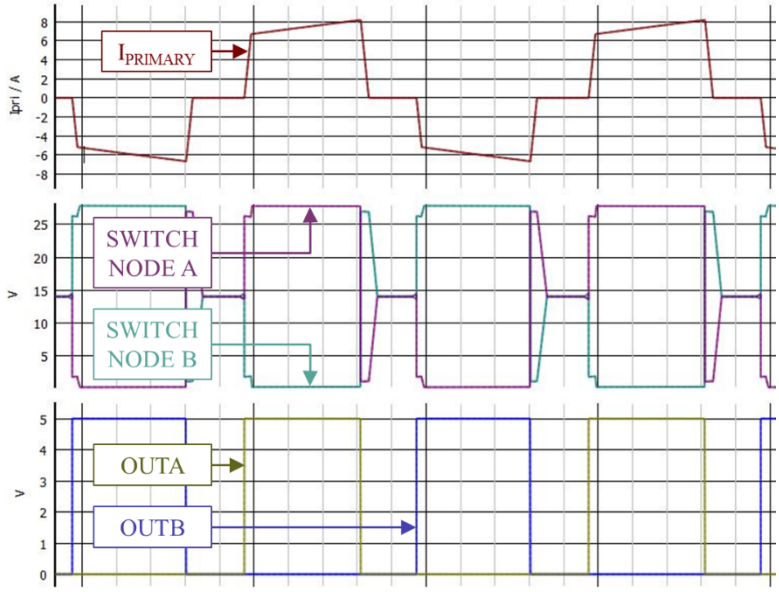

Figure 2. Conventional configuration for driving opposite FETs on the primary side (1 µs/div). Source: Texas Instruments

When no primary-side FETs are on during the dead time, the secondary current will continue to freewheel through the synchronous rectifiers. At this time, leakage energy stored on the primary side resonates with the output capacitance of the primary-side FETs, creating a large leakage spike when either OUTA or OUTB go low. This resonance impacts all four FETs on the primary side. Figure 3 shows how large the leakage spike can get. In practice, a large leakage spike may require you to use higher-voltage components.

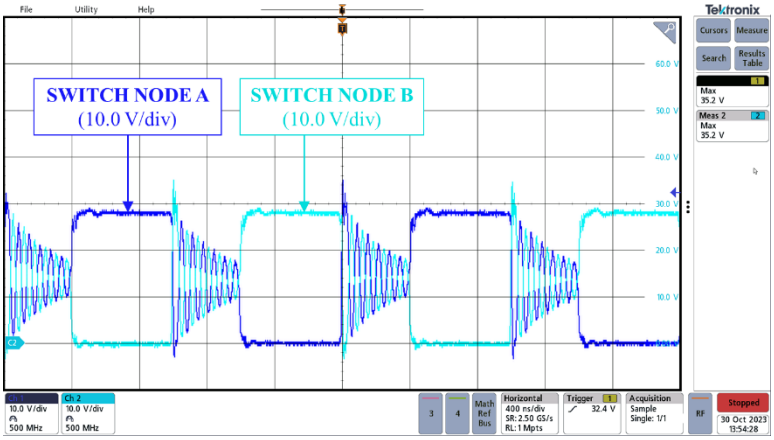

Figure 3. Primary switching nodes with a conventional configuration (400 ns/div). Source: Texas Instruments

An alternative approach with complementary logic

An alternate approach is to control the primary FETs with complementary logic on each half of the bridge. In this method, PWM high turns the high-side FET on, and PWM low turns the low-side FET on. Figure 4 shows a diagram using this approach.

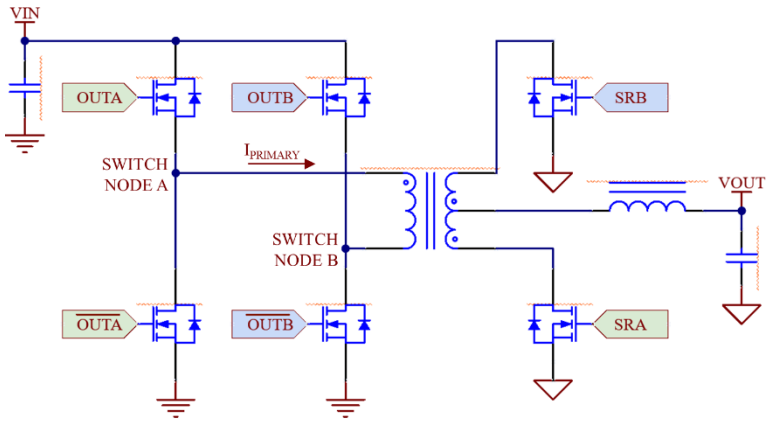

Figure 4. An example of a synchronous ZVS full-bridge converter power stage. Source: Texas Instruments

Figure 5 shows the PWM, switch-node voltages and primary current for this approach. With complementary signals on each side of the primary bridge, both low-side FETs are now on during the dead time. This enables the primary current to continue to freewheel through the two low-side FETs during what used to be the dead time in the conventional approach.

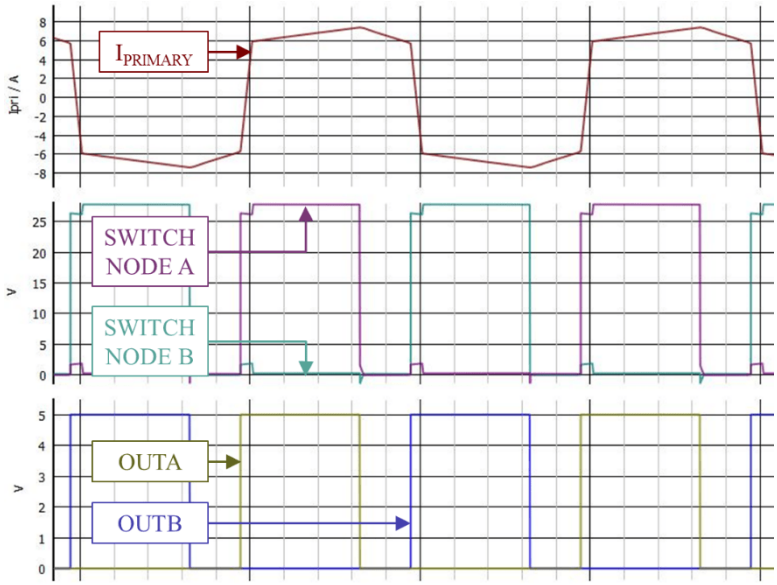

Figure 5. Complementary PWMs for driving FETs on the primary side (1 µs/div). Source: Texas Instruments

The freewheeling current on the primary side has many benefits. First, the primary-side FETs achieve ZVS. Figure 6 shows the primary switch nodes and PWM logic for one side of the full bridge during ZVS events. The drain-to-source voltage falls to zero before the introduction of the gate-drive signal, which indicates ZVS.

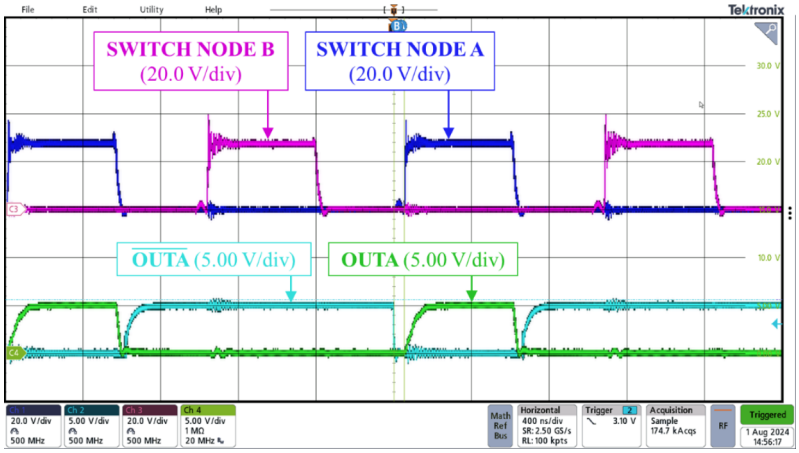

Figure 6. Primary switching nodes with complementary PWM configuration (400 ns/div). Source: Texas Instruments

Another benefit is less noise throughout the converter. The large leakage spike and resonant ringing are eliminated when going from the primary switch-node waveforms in Figure 3 to Figure 6. The secondary rectifier also has reduced noise after changing the primary to get ZVS.

Figure 7 compares the drain-to-source voltage of the secondary rectifiers for both design options. The HSFB variation has noticeably more ringing that needs a snubber to mitigate stress at the expense of decreased overall system efficiency. Changing to ZVS on the primary leads to less ringing on the secondary FET. There is still a leakage spike present, however for this case a diode clamping circuit is more suitable than a snubber.

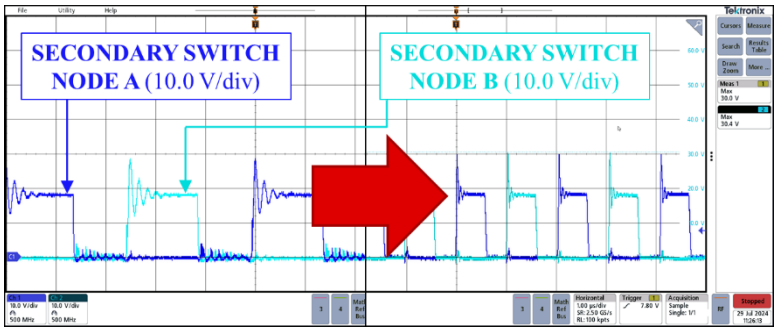

Figure 7. Conventional configuration (400 ns/div) (left); using complementary PWM signals (1.00 µs/div) (right). Source: Texas Instruments

A modified HSFB reference design

The introduction of ZVS alone provides an efficiency boost across loading conditions. Figure 8 compares a modified HSFB reference design, the "100W, 5V Output Hard-Switched Full-Bridge Converter Reference Design for 100kRad Applications", that uses ZVS logic on the primary side to the initial data that was an HSFB. The logic to the primary FETs was the only change; optimizations to the primary-side FET driver and improvements to the secondary-side protection circuit would further increase the benefits of this approach.

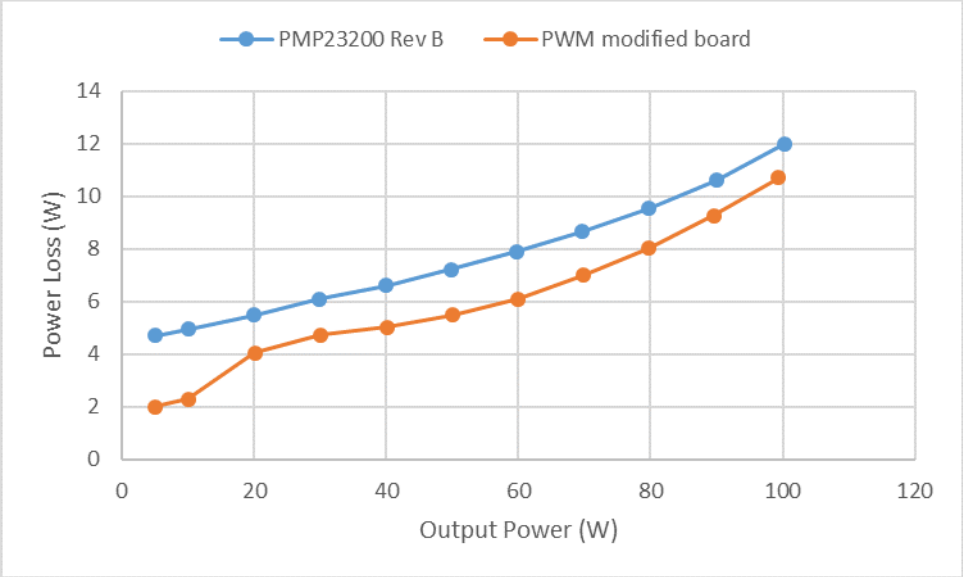

Figure 8. The total power loss versus output power for conventional (TI HSFB reference design revision B) and PWM (modified board) configurations. Source: Texas Instruments

Using complementary logic

Using complementary logic on a full-bridge converter can enable the primary FETs to achieve ZVS. This approach has many benefits for system efficiency, and the approach is easy to implement.

In test cases, a standard synchronous full-bridge converter only needs the logic adjusted to generate the complementary signals. You can make this adjustment by using a logic NOR gate; alternately, some drivers such as the Texas Instruments TPS7H6003-SP gate driver used in the HSFB reference design have a PWM mode where a single input signal drives the high-side FET when the signal is high, and drives the low-side FET when the signal is low. As you can see, this subtle change in control logic can pay big dividends in system performance.

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