Technical Article

Start Designing Your Next Sitara™ Processor Solution!

Ioanna Makris

Do you need design inspiration or are you looking to learn more about Sitara™ processors? To help you, we've rounded up some of our new and popular TI Design reference designs. Check out which ones we are featuring this month!

Parallel Redundancy Protocol (PRP) Ethernet Reference Design for Substation Automation: This reference design implements a solution for high-reliability, low-latency network communications for substation automation equipment in Smart Grid transmission and distribution networks. It supports the Parallel Redundancy Protocol (PRP) specification in the IEC 62439 standard using the PRU-ICSS. This solution is a lower-cost alternative to field programmable gate array (FPGA) approaches and provides the flexibility and performance to add features such as IEC 61850 support without additional components.

People Counting for Demand Controlled Ventilation Using 3D Time-of-Flight (ToF) Reference Design: Use this reference design as a subsystem solution that uses TI's 3D ToF image sensor combined with tracking and detection algorithms to count the number of occupants present in a given area with high resolution and accuracy. The sensor technology is developed in standard CMOS, allowing systems to achieve very high integration at a lower system cost. Because ToF image sensor processes visual data in three dimensions, the sensor can detect the exact shape of a human body along with tracking the movement and location of people with unprecedented precision, including subtle movement changes. For this reason, ToF cameras are potentially capable of performing real-time people counting and people tracking functions much more effectively than traditional surveillance cameras and video analytics.

Multi-Protocol Digital Position Encoder Master Interface Reference Design: Save cost and reduce board space! TI provides the system solution for industrial communication on Sitara processors with Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS). This TI Design describes the integrated multi-protocol digital position encoder master interface support. The supported digital position encoder master protocols are EnDat 2.2, Hiperface DSL ® and BiSS C. The integrated multi-protocol encoder master has the benefit to work without additional FPGA, application specific integrated circuit (ASIC) and programmable logic device (PLD) while supporting multiple encoder protocols - therefore saving cost and reducing board space. This reference design utilizes the Single Chip Drive Evaluation Board (TMDSIDK437X) and Universal Digital Interface to Absolute Position Encoders Reference Design (TIDA-00179).

Packet Processing Engine Reference Design for IEC61850 GOOSE Forwarding: The TI Design reference design demonstrates packet switching and filtering logic implemented in the M4 core of AM572x processor based upon the Ethertype, MAC address and Application ID (APPID) of GOOSE packets received from the PRU-ICSS. Packets are filtered and routed to destinations in order to allow the time-critical events defined in substation communication standard IEC 61580 to be serviced in a dedicated core. The design additionally shows multi-core communication between the ARM® Cortex®-A15, ARM® Cortex®-M4 and C66x DSP cores of the AM572x processors.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265