Technical Reference Manual

TPS25752A Technical Reference Manual

Table of Contents

List of Figures

List of Tables

1 Read This First

1.1 Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h or the prefix 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40.
- Registers in this document are shown in figures and described in tables.
  - Byte convention for N bytes is 0 through (N-1) bytes.
  - Bit convention for N bits is 0 through (N-1) bits.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with the bit name, the beginning and ending bit numbers above, and the read/write properties with default reset value below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure can have one of multiple meanings:
    - Not implemented on the device
    - Reserved for future device expansion
    - Reserved for TI testing
    - Reserved configurations of the device that are not supported
  - Writing nondefault values to the Reserved bits can cause unexpected behavior and are to be avoided.

1.2 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

1.3 Related Documents

- USB Power Delivery Specification Revision 3.1 www.usb.org/developers/docs
- USB Type-C Cable and Connector Specification Revision 2.0. www.usb.org/developers/docs

1.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

1.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
USB Type-C® is a registered trademark of USB Implementers Forum.
All trademarks are the property of their respective owners.

2 Introduction

2.1 Purpose and Scope

This document describes the Host Interface for the TPS25752A Type-C Port Switch / Power Delivery (PD) Controller devices.

3 PD Controller Host Interface Description

3.1 Overview

The PD Controller provides one I2C target. The I2Ct target is meant to be connected to an Embedded Controller (EC).

The Host Interface defines how the registers are accessed from I2C target port and target addresses. Target Address #1 is selected by the customer using the ADCIN1 and ADCIN2 pins on the PD controller. See also *Use of Target Addresses During Different Modes of Operation* for more details about the target addresses.

The Host Interface provides general status information to the controller of these I2C interfaces about the PD Controller, ability to control the PD Controller, status of USB Type-C® Port and communications to/from a connected device (Port Partner) and/or cable plug through USB PD messages. All Host Interface communication that uses the Unique I2C address is referred to as Unique Address Interface.

The PD Controller supports a register-based Unique Address Interface. *TPS25751 Registers* lists the Unique Address Interface registers and provides detailed Unique Address Interface register descriptions.

The key to the protocol diagrams is in the SMBus Specification, version 2.0 and is repeated here in part in Figure 3-1.

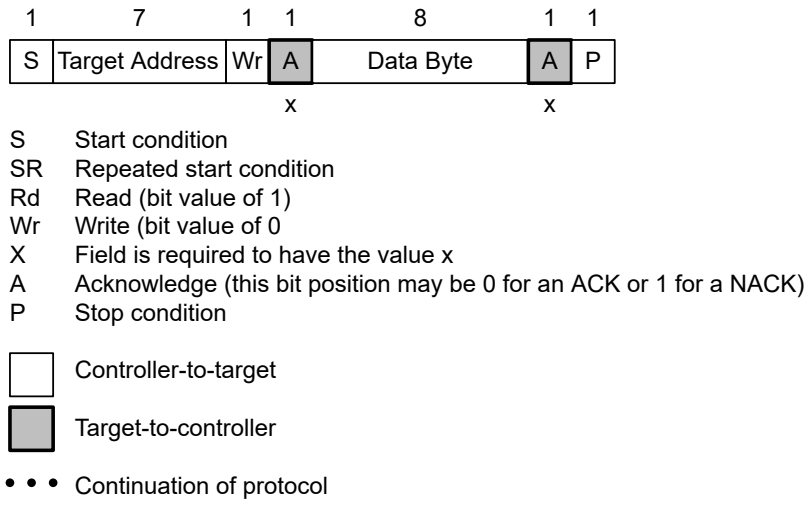


Figure 3-1. I2C Read/Write Protocol Key

3.2 Register and Field Notation

In this document the register names use an ALL CAPS notation, and the field names use a CamelBack notation. For example *TX_SOURCE_CAPS* refers to register 0x32, and *TX_SOURCE_CAPS.numValidPDOs* refers to a specific field in Byte 1 of that register. In this document I2C1 denotes I2Ct.

4 Unique Address Interface

4.1 Unique Address Interface Protocol

The Unique Address Interface allows for complex interactions between an I2C controller and a single PD Controller. The I2C target unique address is used to receive or respond to Host Interface protocol commands. Figure 4-1 and Figure 4-2 show the write and read protocols, respectively. The Byte Count used during a register

write can be longer than the number of bytes actually written, in other words the controller can issue the stop bit without writing N bytes. Similarly, during a register read, the controller can issue the stop bit before reading all N bytes. N bytes refers to the number of bytes to be read or written.

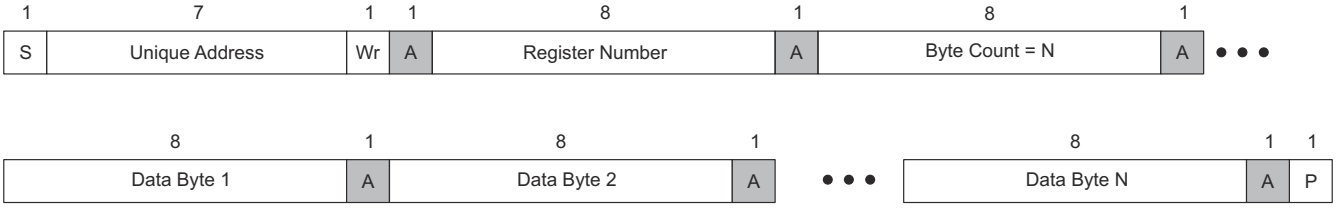


Figure 4-1. I2C Unique Address Write Register Protocol

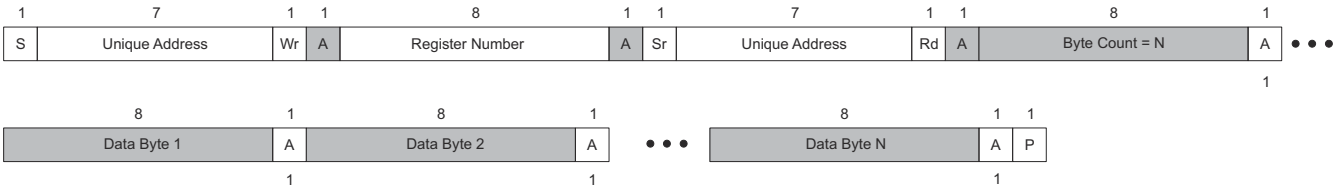


Figure 4-2. I2C Unique Address Read Register Protocol

5 PD Controller Policy Modes

5.1 Overview

The PD Controller implements a mode for "SRC Policy" (handing out Source contracts). Certain fields are refered to differently, the table below summarizes the naming conventions assumed.

Table 5-1. Naming Conventions

Reference Name	TPS25752A Reference
PP_5V, PP1 Switch	PP5V
PP_EXT, PP3 Switch	PP_EXT

5.2 Source Policy Mode

The PD Controller uses the *TX_SOURCE_CAPS* register (0x32) to know what PDO(s) to advertise. The PD Controller will automatically respond to Request messages as appropriate, and each port acts independently. The host can dynamically change the *TX_SOURCE_CAPS* register, then issue the 'SSrC' 4CC Task and the PD controller will advertise the new PDOs.

6 Register Overview

Note

Some registers contain 'Reserved' fields that should not be overwritten by an I2C Host Controller (EC). To prevent overwriting these 'Reserved' fields the host controller should follow the read-modify-write instruction before configuring any PD registers.

6.1 TPS25752A Registers

Table 6-1 lists the memory-mapped registers for the TPS25752A registers. All register offset addresses not listed in Table 6-1 should be considered as reserved locations and the register contents should not be modified.

Table 6-1. TPS25752A Registers

Offset	Acronym	Register Name	Section
3h	Mode	Mode	Section 6.1.1
6h	Customer Use	Customer Use	Section 6.1.2
8h	Command Register (CMD1) for I2Ct	Command Register (CMD1) for I2Ct	Section 6.1.3
9h	Data Register (DATA1) for CMD1	Data Register (DATA1) for CMD1	Section 6.1.4
Fh	Version	Version	Section 6.1.5
14h	Interrupt Event for I2Ct_IRQ	Interrupt Event for I2Ct_IRQ	Section 6.1.6
16h	Interrupt Mask for I2Ct_IRQ	Interrupt Mask for I2Ct_IRQ	Section 6.1.7
18h	Interrupt Clear for I2Ct_IRQ	Interrupt Clear for I2Ct_IRQ	Section 6.1.8
1Ah	Status	Status	Section 6.1.9
26h	Power Path Status	Power Path Status	Section 6.1.10
27h	Global System Configuration	Global System Configuration	Section 6.1.11
28h	Port Configuration	Port Configuration	Section 6.1.12
29h	Port Control	Port Control	Section 6.1.13
2Dh	Boot Flags	Boot Flags	Section 6.1.14
31h	Received Sink Capabilities	Received Sink Capabilities	Section 6.1.15
32h	Transmit Source Capabilities	Transmit Source Capabilities	Section 6.1.16
34h	Active PDO Contract	Active PDO Contract	Section 6.1.17
35h	Active RDO Contract	Active RDO Contract	Section 6.1.18
3Fh	Power Status	Power Status	Section 6.1.19
42h	PD3 Configuration	PD3 Configuration	Section 6.1.20
48h	Received SOP Identity Data Object	Received SOP Identity Data Object	Section 6.1.21
5Ch	IO Config	IO Config	Section 6.1.22
69h	Type C State	Type C State	Section 6.1.23
6Ah	ADC Results	ADC Results	Section 6.1.24
70h	Sleep Control Register	Sleep Control Register	Section 6.1.25
72h	GPIO Status	GPIO Status	Section 6.1.26
73h	TX Manufactrer Info SOP	TX Manufactrer Info SOP	Section 6.1.27
77h	Tx Source Capabilities Extended Data Block	Tx Source Capabilities Extended Data Block	Section 6.1.28
78h	TX Source Info	TX Source Info	Section 6.1.29
7Ah	Transmitted PPS Status Data Block	Transmitted PPS Status Data Block	Section 6.1.30
7Bh	Transmitted Battery Status Data Objects (BSDO) Register	Transmitted Battery Status Data Objects (BSDO) Register	Section 6.1.31
7Dh	Tx Battery Capabilities	Tx Battery Capabilities	Section 6.1.32
98h	Liquid Detection Configuration	Liquid Detection Configuration	Section 6.1.33
A4h	Rx MIDB	Rx MIDB	Section 6.1.34
B2h	Liquid Detection STATUS Register	Liquid Detection STATUS Register	Section 6.1.35

Complex bit access types are encoded to fit into small table cells. Table 6-2 shows the codes that are used for access types in this section.

Table 6-2. TPS25752A Access Type Codes

Access Type	Code	Description
Read Type		

Table 6-2. TPS25752A Access Type Codes (continued)

Access Type	Code	Description
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

6.1.1 Mode Register (Offset = 3h) [Reset = 00000000h]

Mode is shown in Table 6-3.

Return to the Summary Table.

Indicates the operational state of the port. The PD Controller has limited functionality in some modes.

Table 6-3. Mode Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	
31-0	Mode	R	0h	The mode described in 4 ASCII characters. 'APP ' indicates that the PD Controller is fully functioning in the application firmware where all registers are available. 'PTCH' indicates that the PD controller is in patch mode. Any value other than 'APP ' indicates that the PD controller is functioning in limited capacity. In 'PTCH' mode, only the following register addresses are accessible: MODE (0x03), Command (0x08), Data (0x09), INT_EVENT (0x14), INT_MASK (0x16), INT_CLEAR (0x18), and BOOT_FLAGS (0x2D).

6.1.2 Customer Use Register (Offset = 6h) [Reset = 0000000000000000h]

Customer Use is shown in Table 6-4.

Return to the Summary Table.

This register is allocated for customer use. It is typically used for version control, but usage flexibility remains with the customer.

Table 6-4. Customer Use Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	Customer Use	R	0h	These 8 bytes are allocated for customer use as needed. The PD Controller does not use this register. This register can only be changed during application customization, not at runtime.

6.1.3 Command Register (CMD1) for I2Ct (Offset = 8h) [Reset = 00000000h]

Command Register (CMD1) for I2Ct is shown in Table 6-5.

Return to the Summary Table.

Command register. The PD Controller clears it on initialization and after completing a command.

Table 6-5. Command Register (CMD1) for I2Ct Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Command	R/W	0h	Command register for the command interface. The PD Controller clears this register to 0x0 on initialization and after completing any recognized commands. Unrecognized commands are overwritten with !CMD.

6.1.4 Data Register (DATA1) for CMD1 (Offset = 9h) [Reset = 000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000 00000000000000000000000000000000000000h]

Data Register (DATA1) for CMD1 is shown in Table 6-6.

Return to the Summary Table.

Data register (DATA1) for the command interface (CMD1).

Table 6-6. Data Register (DATA1) for CMD1 Field Descriptions

Bit	Field	Type	Reset	Description
511-0	Data	R/W	0h	Data register (DATA1) for the command interface (CMD1). The first byte of this register will contain the return code if applicable, and the remaining bytes will contain the command's output

6.1.5 Version Register (Offset = Fh) [Reset = 00000000h]

Version is shown in Table 6-7.

Return to the Summary Table.

Bootloader/application code version. Represented as VVVV.MM.RR. The version information is returned in little Endian format i.e. byte 1 = RR, byte 2 = MM, etc.

Table 6-7. Version Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Version	R	0h	Bootloader/application code version. Represented as VVVV.MM.RR. The version information is returned in little Endian format i.e. byte 1 = RR, byte 2 = MM, etc.

6.1.6 Interrupt Event for I2Ct_IRQ Register (Offset = 14h) [Reset = 00000000000000000000h]

Interrupt Event for I2Ct_IRQ is shown in Table 6-8.

Return to the Summary Table.

Interrupt event bit field for IRQ. If any bit in this register is 1, then the IRQ pin is pulled low. Only the interrupt events enabled in INT_MASK1 (0x16) will be asserted.

Table 6-8. Interrupt Event for I2Ct_IRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
87-84	RESERVED	R	0h	
83	System Fault Indicator	R	0h	Stores fault from an external device, no additional action taken.
82	I2C Controller NACked	R	0h	A transaction on the I2C Controller was NACKed
81	Ready for Patch	R	0h	The device is ready for a patch bundle from the host
80	Patch Loaded	R	0h	A patch has been loaded to the device
79-67	RESERVED	R	0h	
66	MBRD Buffer Ready	R	0h	The memory buffer is full and ready to be read using the 'MBRd' command
65	TX Memory Buffer Empty	R	0h	The transmit memory buffer is empty
64-61	RESERVED	R	0h	
60	Liquid Detection	R	0h	The Liquid Detection state has changed.
59-52	RESERVED	R	0h	
51	Discover Mode Completed	R	0h	The Discover Modes process has completed
50-44	RESERVED	R	0h	
43	Plug Early Notification	R	0h	A connection has been detected but not yet debounced
42	Sink Transition Completed	R	0h	A source power transition has been initiated tSrcTransition ms after sending an Accept message to a Port Partner Request message
41-40	RESERVED	R	0h	
39	Message Data Error	R	0h	An erroneous message has been received from the Port Partner
38	Protocol Error	R	0h	An unexpected message has been received from the Port Partner
37	RESERVED	R	0h	
36	Missing Get Capabalities Message Error	R	0h	The Port Partner did not respond to a Get_Sink_Cap message
35	Power Event Occurred Error	R	0h	An OVP, ILIM, or TSD event on VBUS has been detected.
34	Can Provide Voltage or Current Later Error	R	0h	A "Wait" message has been sent or received indicating the Source cannot provide acceptable power at the present time
33	Cannot Provide Voltage or Current Error	R	0h	The USB PD Source cannot provide an acceptable voltage and/or current. A Reject message has been sent to the Sink or a Capability Mismatch has been received from the Sink
32	Device Incompatible Error	R	0h	A USB PD device with an incompatible specification version has been connected, or the Port Partner is not USB PD capable
31	RESERVED	R	0h	
30	CMD1 Complete	R	0h	Set whenever a non-zero value in CMD1 register is set to zero or ! CMD.
29	MIDB Received	R	0h	A Manufacturer Info message has been received
28	RESERVED	R	0h	
27	PD Status Updated	R	0h	The contents of the PD_STATUS (0x40) register have changed
26	Status Updated	R	0h	The contents of the STATUS (0x1A) register have changed
25	RESERVED	R	0h	
24	Power Status Updated	R	0h	The contents of the POWER_STATUS (0x3F) register have changed
23	Power Path Switch Changed	R	0h	The contents of the POWER_PATH_STATUS (0x26) register have changed
22	RESERVED	R	0h	

Table 6-8. Interrupt Event for I2Ct_IRQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	USB Host No Longer Present	R	0h	The UsbHostPresent field in the STATUS register has transitioned to a value other than 11b
20	USB Host Present	R	0h	The UsbHostPresent field in the STATUS register has transitioned to 11b
19-16	RESERVED	R	0h	
15	Sink Cap Message Received	R	0h	A Sink Capabilities message has been received from the Port Partner
14	RESERVED	R	0h	
13	New Contract as Provider	R	0h	A PD contract has been formed as a Source. This is asserted after the PS_RDY message has been sent. See ACTIVE_CONTRACT_PDO (0x34) register and ACTIVE_CONTRACT_RDO (0x35) register for details
12-10	RESERVED	R	0h	
9	Overcurrent	R	0h	An Overcurrent field (VBUS or VCONN) in the POWER_PATH_STATUS (0x26) register has changed
8-6	RESERVED	R	0h	
5	Data Swap Complete	R	0h	A Data Role Swap has completed. See STATUS (0x1A) register and PD_STATUS (0x40) register for port state.
4	RESERVED	R	0h	
3	Plug Insert or Removal	R	0h	USB Plug Status has changed. See STATUS (0x1A) register for more plug details.
2	RESERVED	R	0h	
1	PD Hardreset	R	0h	A PD Hard Reset has been performed. See PD_STATUS.HardResetDetails for more information.
0	RESERVED	R	0h	

6.1.7 Interrupt Mask for I2Ct_IRQ Register (Offset = 16h) [Reset = 00000000000000000000h]

Interrupt Mask for I2Ct_IRQ is shown in Table 6-9.

Return to the Summary Table.

Interrupt mask bit field for INT_EVENT1. Bytes 1 to 10 of this register must be configured through the Application Customization Tool to enable the corresponding interrupt events. For Byte 11, Bit 1 is enabled by default - It is recommended to set the remaining implemented bits as needed by the host application.

Table 6-9. Interrupt Mask for I2Ct_IRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
87-84	RESERVED	R	0h	
83	System Fault Indicator	R/W	0h	Set to indicate a fault from an external device in the system.
82	I2C Controller NACKed	R/W	0h	Set to enable notification when a transaction on the I2C Controller is NACKed
81	Ready for Patch	R/W	0h	Set to enable notification when the device is ready for a patch bundle from the host. This bit is set by default by the device.
80	Patch Loaded	R/W	0h	Set to enable notification when a patch is loaded
79-67	RESERVED	R	0h	
66	MBRD Buffer Ready	R/W	0h	Set to enable notification when the memory buffer is full and ready to be read using the 'MBRd' command
65	TX Memory Buffer Empty	R/W	0h	Set to enable notification when the transmit memory buffer is empty
64-61	RESERVED	R	0h	
60	Liquid Detection	R/W	0h	Set to enable notification when the Liquid Detection state changes
59-52	RESERVED	R	0h	
51	Discover mode Completed	R/W	0h	Set to enable notification when the Discover Modes process has completed
50-47	RESERVED	R	0h	
46	Unable to Source Error	R/W	0h	Set to enable notification when the Source is unable to increase the voltage to the negotiated contract voltage
45-44	RESERVED	R	0h	
43	Plug Early Notification	R/W	0h	Set to enable notification when a connection is detected but not yet debounced
42	Sink Transition Completed	R/W	0h	Set to enable notification when a source power transition is initiated after accepting a Port Partner Request message
41-40	RESERVED	R	0h	
39	Message Data Error	R/W	0h	Set to enable notification when an erroneous message is received from the Port Partner
38	Protocol Error	R/W	0h	Set to enable notification when an unexpected message is received from the Port Partner
37	RESERVED	R	0h	
36	Missing Get Capabalities Message Error	R/W	0h	Set to enable notification when the Port Partner does not respond to a Get_Sink_Cap or Get_Source_Cap message
35	Power Event Occurred Error	R/W	0h	Set to enable notification when an OVP, ILIM, or TSD event on VBUS is detected
34	Can Provide Voltage or Current Later Error	R/W	0h	Set to enable notification when a "Wait" message is sent or received for Source power availability
33	Cannot Provide Voltage or Current Error	R/W	0h	Set to enable notification when the USB PD Source cannot provide an acceptable voltage and/or current
32	Device Incompatible Error	R/W	0h	Set to enable notification when a USB PD device with an incompatible specification version is connected, or the Port Partner is not USB PD capable
31	RESERVED	R	0h	
30	CMD1 Complete	R/W	0h	Set to enable notification when a CMD1 (0x08) register command has completed

Table 6-9. Interrupt Mask for I2Ct_IRQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	MIDB Received	R/W	0h	Set to enable notification when a Manufacturer Info message is received
28	RESERVED	R	0h	
27	PD Status Updated	R/W	0h	Set to enable notification when the contents of the PD_STATUS (0x40) register change
26	Status Updated	R/W	0h	Set to enable notification when the contents of the STATUS (0x1A) register change
25	RESERVED	R	0h	
24	Power Status Updated	R/W	0h	Set to enable notification when the contents of the POWER_STATUS (0x3F) register change
23	Power Path Switch Changed	R/W	0h	Set to enable notification when the contents of the POWER_PATH_STATUS (0x26) register change
22	RESERVED	R	0h	
21	USB Host No Longer Present	R/W	0h	Set to enable notification when the UsbHostPresent field in the STATUS register transitions to a value other than 11b
20	USB Host Present	R/W	0h	Set to enable notification when UsbHostPresent field in the STATUS register transitions to 11b
19-16	RESERVED	R	0h	
15	Sink Cap Message Received	R/W	0h	Set to enable notification when a Sink Capabilities message is received from the Port Partner
14	RESERVED	R	0h	
13	New Contract as Provider	R/W	0h	Set to enable notification when a PD contract is formed as a Source
12-10	RESERVED	R	0h	
9	Overcurrent	R/W	0h	Set to enable notification when an Overcurrent field (VBUS or VCONN) in the POWER_PATH_STATUS (0x26) register changes
8-4	RESERVED	R	0h	
3	Plug Insert or Removal	R/W	0h	Set to enable notification when USB Plug Status changes
2	RESERVED	R	0h	
1	PD Hardreset	R/W	0h	Set to enable notification when a PD Hard Reset is performed
0	RESERVED	R	0h	

6.1.8 Interrupt Clear for I2Ct_IRQ Register (Offset = 18h) [Reset = 00000000000000000000h]

Interrupt Clear for I2Ct_IRQ is shown in Table 6-10.

Return to the Summary Table.

Interrupt clear bit field for INT_EVENT1. Writing 1 to a specific bit will clear that specific event in INT_EVENT1. Bits set in this register are cleared from INT_EVENT1.

Table 6-10. Interrupt Clear for I2Ct_IRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
87-83	RESERVED	R	0h	
82	I2C Controller NACKed	R/W	0h	Write 1 to clear the I2C Controller NACK event
81	Ready for Patch	R/W	0h	Write 1 to clear the patch bundle ready event
80	Patch Loaded	R/W	0h	Write 1 to clear the patch loaded event
79-67	RESERVED	R	0h	
66	MBRD Buffer Ready	R/W	0h	Write 1 to clear the memory buffer full event
65	TX Memory Buffer Empty	R/W	0h	Write 1 to clear the transmit memory buffer empty event
64-61	RESERVED	R	0h	
60	Liquid Detection	R/W	0h	Write 1 to clear the Liquid Detection state changed event
59-57	RESERVED	R	0h	
56	Ext DCDC Sink Safe State	R/W	0h	Write 1 to clear the Power Role Swap accepted or Explicit PD Contract Accept received event
55-52	RESERVED	R	0h	
51	Discover mode Completed	R/W	0h	Write 1 to clear the Discover Modes process completed event
50-47	RESERVED	R	0h	
46	Unable to Source Error	R/W	0h	Write 1 to clear the Source unable to increase voltage to negotiated contract voltage event
45-44	RESERVED	R	0h	
43	Plug Early Notification	R/W	0h	Write 1 to clear the connection detected but not yet debounced event
42	Sink Transition Completed	R/W	0h	Write 1 to clear the source power transition initiated event
41-40	RESERVED	R	0h	
39	Message Data Error	R/W	0h	Write 1 to clear the erroneous message received event
38	Protocol Error	R/W	0h	Write 1 to clear the unexpected message received event
37	RESERVED	R	0h	
36	Missing Get Capabalities Message Error	R/W	0h	Write 1 to clear the Port Partner Get_Sink_Cap or Get_Source_Cap no response event
35	Power Event Occurred Error	R/W	0h	Write 1 to clear the OVP, ILIM, or TSD on VBUS event
34	Can Provide Voltage or Current Later Error	R/W	0h	Write 1 to clear the Source power availability "Wait" event
33	Cannot Provide Voltage or Current Error	R/W	0h	Write 1 to clear the Source capability mismatch event
32	Device Incompatible Error	R/W	0h	Write 1 to clear the incompatible or non-USB PD capable Port Partner connected event
31	RESERVED	R	0h	
30	CMD1 Complete	R/W	0h	Write 1 to clear the CMD1 command completed event
29	MIDB Received	R/W	0h	Write 1 to clear the Manufacturer Info message received event
28	RESERVED	R	0h	
27	PD Status Updated	R/W	0h	Write 1 to clear the PD_STATUS (0x40) register contents changed event
26	Status Updated	R/W	0h	Write 1 to clear the STATUS (0x1A) register contents changed event
25	RESERVED	R	0h	

Table 6-10. Interrupt Clear for I2Ct_IRQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	Power Status Updated	R/W	0h	Write 1 to clear the POWER_STATUS (0x3F) register contents changed event
23	Power Path Switch Changed	R/W	0h	Write 1 to clear the POWER_PATH_STATUS (0x26) register contents changed event
22	RESERVED	R	0h	
21	USB Host No Longer Present	R/W	0h	Write 1 to clear the UsbHostPresent field in the STATUS register transitioned to a value other than 11b event
20	USB Host Present	R/W	0h	Write 1 to clear the UsbHostPresent field in the STATUS register transitioned to 11b event
19-16	RESERVED	R	0h	
15	Sink Cap Message Received	R/W	0h	Write 1 to clear the Sink Capabilities message received event
14	RESERVED	R	0h	
13	New Contract as Provider	R/W	0h	Write 1 to clear the PD contract formed as Source event
12-10	RESERVED	R	0h	
9	Overcurrent	R/W	0h	Write 1 to clear the Overcurrent field change event
8-4	RESERVED	R	0h	
3	Plug Insert or Removal	R/W	0h	Write 1 to clear the USB Plug Status Changed event
2	RESERVED	R	0h	
1	PD Hardreset	R/W	0h	Write 1 to clear the PD Hard Reset event
0	RESERVED	R	0h	

6.1.9 Status Register (Offset = 1Ah) [Reset = 0000000020h]

Status is shown in Table 6-11.

Return to the Summary Table.

Status bit field for events.

Table 6-11. Status Register Field Descriptions

Bit	Field	Type	Reset	Description
39-26	RESERVED	R	0h	
25-24	Acting as Legacy	R	0h	Indicates when PD Controller has gone into a mode where it is acting like a legacy (non PD) device. It can take approximately 10 seconds for the PD controller to determine that it is attached to a legacy source or sink. 0h = PD Controller is not in a legacy (non PD) mode 2h = PD Controller is acting like a legacy source
23-22	RESERVED	R	0h	
21-20	VBUS Status	R	0h	Indicates the present state of VBUS. 0h = At vSafe0V (less than 0.8V) 1h = At vSafe5V (4.75V to 5.5V) 2h = Within expected limits 3h = Not within any of the other specified ranges
19-7	RESERVED	R	0h	
6	Data Role	R	0h	PD controller data role. This is only valid once there is a connection. 0h = Upward-facing port (UFP) 1h = Downward-facing port (DFP)
5	Port Role	R	1h	Current state of PD Controller CCx terminations. This also indicates the PD Controller Power Role, once connected. This bit does not toggle during Unattached state transitions. 1h = PD Controller is Source (CCx pull-up active)
4	Plug Orientation	R	0h	Plug orientation indicator. Indicates port orientation when known (requires connection). 0h = Upside-up orientation (plug CC on CC1) 1h = Upside-down orientation (plug CC on CC2)
3-1	Connection State	R	0h	Details of a connected plug. 0h = No connection 1h = Port is disabled 2h = Corrosion Mitigaion (Ra/Ra) 3h = Debug connection (Rd/Rd) 4h = No connection Ra detected (Ra but no Rd) 5h = Debug connection (Rp/Rp) 6h = Connection present no Ra detected 7h = Connection present Ra detected
0	Plug Present	R	0h	Status of the plug 0h = No plug is connected 1h = A plug is connected

6.1.10 Power Path Status Register (Offset = 26h) [Reset = 0000000000h]

Power Path Status is shown in Table 6-12.

Return to the Summary Table.

Power Path Status. This is a hardware dependent register.

Table 6-12. Power Path Status Register Field Descriptions

Bit	Field	Type	Reset	Description
39-38	Power Source	R	0h	Indicates current PD Controller power source. 0h = Reserved 1h = PD Controller is powered from VIN_3V3 3h = Reserved
37-15	RESERVED	R	0h	
14-12	PP3 Switch	R	0h	Indicates current state of PP3 (PP_EXT). 0h = PP3 switch disabled 1h = PP3 switch currently disabled due to fault 2h = PP3 switch enabled (system output)
11-9	RESERVED	R	0h	
8-6	PP1 Switch	R	0h	Indicates current state of PP1 switch (PP5V). 0h = PP1 switch disabled 1h = PP1 switch currently disabled due to fault 2h = PP1 switch enabled (system output)
5-2	RESERVED	R	0h	
1-0	PPCable1 Switch	R	0h	Indicates current state of PP_CABLE1 switch. 0h = PP_CABLE1 switch disabled 1h = PP_CABLE1 switch currently disabled 2h = PP_CABLE1 switch CC1 enabled (system output) 3h = PP_CABLE1 switch CC2 enabled (system output)

6.1.11 Global System Configuration Register (Offset = 27h) [Reset = 00000000000000000000000018101h]

Global System Configuration is shown in Table 6-13.

Return to the Summary Table.

Global system configuration (all ports). This register contains configuration bits that define hardware that is common to all ports and in most cases will not change in normal operation or will not require immediate action if changed. Any modifications to this register will cause a port disconnect and reconnect with the new settings. Initialized by Application Customization.

Table 6-13. Global System Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
115-19	RESERVED	R	0h	
18-16	PP3 Config	R/W	1h	PP3 configuration. This register configures PP3 switch controls. 0h = PP3 not used and disabled 1h = PP3 is a Source (output)
15-14	ILIM Over Shoot	R/W	2h	PP_5V ILIM configuration. Controls the amount of overshoot used by the FW to select the current limit for the PP5V to VBUS. 0h = No additional overshoot margin 1h = Overshoot margin of at least 100 mA 2h = Overshoot margin of at least 200 mA 3h = Overshoot margin of at least 500 mA
13-11	RESERVED	R	0h	
10-8	PP1 Config	R/W	1h	PP1 configuration (PP_5V). 0h = Not used (disabled) 1h = PP1 configured as source
7-1	RESERVED	R	0h	
0	PP Cable1 Switch Config	R/W	1h	Enable PP_CABLE1. If this bit is asserted the PD controller will enable VCONN on PP_CABLE1 when required for USB specification compliance.

6.1.12 Port Configuration Register (Offset = 28h) [Reset = 00000000000000000000000000220001h]

Port Configuration is shown in Table 6-14.

Return to the Summary Table.

Configuration for port-specific hardware. This register configures hardware that is specific for each port and in most cases will not change in normal operation or will not require immediate action if changed. Any modifications to this register will cause a port disconnect and reconnect with the new settings. Initialized by Application Customization.

Table 6-14. Port Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
143-136	iSense Offest	R/W	0h	Configure 0A voltage when bidirectional current sensor is used in the design. (14mv per LSB)
135-130	RESERVED	R	0h	
129-128	Fixed PDO ILIM	R/W	0h	Added current offset for Fixed PDO Contract, used for modifying current offset for PD+BQ or PD+DCDC applications. 0h = 125mA 1h = 250mA 2h = 400mA 3h = 500mA
127-124	RESERVED	R	0h	
123	Power Path	R/W	0h	Power Path depending on port, otherwise off 0h = Off 1h = PP3
122	ADC Pin	R/W	0h	ADC GPIO Pin 0h = GPIO0 1h = GPIO2
121-112	Gain (mV/A)	R/W	0h	Gain starting at 1mV/A (1mV/A per LSB as mV/A).
111-107	Sample Rate	R/W	0h	Sample rate starting at 10ms (10ms per LSB as ms).
106-104	IMON Factor	R/W	0h	IMON Factor starting at 100% (5% per LSB as %).
103-99	IMON Peak	R/W	0h	IMON Peak starting at 5A (1mA per LSB as mA).
98-96	ADC Shift	R/W	0h	ADC error shift. Range is 0 to 7
95-77	RESERVED	R	0h	
76-74	Source UVP Threshold Selection	R/W	0h	Source UVP threshold Selection
73-31	RESERVED	R	0h	
30-29	APDO ILIM Over Shoot	R/W	0h	Current limit overshoot for APDO contracts. Configures the current limit overshoot when power role is source and negotiated PD contract is variable type. This field is used to increase the current limit configuration of a supported BQ device. 0h = 25mA overshoot for APDO current 1h = 50mA above negotiated variable PDO current 2h = 75mA above negotiated variable PDO current 3h = Static 2900mA current limit
28-27	APDO VBUS UVP Threshold	R/W	0h	VBUS UVP threshold for APDO contracts. Configures the VBUS UVP threshold when power role is source and negotiated PDO contract is variable type. 0h = 90% below negotiated variable PDO voltage 1h = 88% below negotiated variable PDO voltage 2h = 92% below negotiated variable PDO voltage 3h = Reserved
26-22	RESERVED	R	0h	
21-20	OVP for PP5V	R/W	2h	VBUS OVP settings while sourcing from PP1 (PP5V). See data-sheet for voltage range. 0h = Use setting 0: 5.25 V 1h = Use setting 1: 5.5 V 2h = Use setting 2: 5.8 V 3h = Use setting 3: 6.1 V
19-18	RESERVED	R	0h	

Table 6-14. Port Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-16	VBUS OVP Usage	R/W	2h	OVP configuration settings. These two bits are used to select the OVP trip-point. The PD controller automatically computes the lowest threshold that does not overlap with the expected maximum voltage (including maximum tolerance allowed by USB PD specification). The OVP trip-point will be set at the selected percentage of the computed threshold. 0h = 100% 1h = 105% 2h = 111% 3h = 114%
15	RESERVED	R	0h	
14-13	USB3 Rate	R/W	0h	USB3 configuration. 0h = USB3 not supported 1h = USB3 Gen1 signaling rate supported 2h = USB3 Gen2 signaling rate supported 3h = Reserved
12	DebugAccessory Support	R/W	0h	Assert this bit to enable DebugAccessory support.
11	USB Communication Capable	R/W	0h	Assert this bit in systems that are USB communications capable. This will be reported in the USB communcations capable field of PDO1.
10-2	RESERVED	R	0h	
1-0	TypeC State machine	R/W	1h	Configuration of the Type-C State machine. This fields sets the default Type-C state of the PD controller. 1h = Source state machine only 3h = Reserved

6.1.13 Port Control Register (Offset = 29h) [Reset = 00015002h]

Port Control is shown in Table 6-15.

Return to the Summary Table.

Configuration bits affecting system policy. These bits may change during normal operation and are used for controlling the respective port. The PD Controller will not take immediate action upon writing. Changes made to this register will take effect the next time the appropriate policy is invoked. Initialized by Application Customization.

Table 6-15. Port Control Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	
28-26	Charger Advertise Enable	R/W	0h	Configure the types of legacy chargers to emulate. 0h = BC 1.2 SDP only 1h = BC 1.2 CDP only 2h = BC 1.2 DCP only 3h = Reserved 4h = Reserved 5h = DCP Auto 1 (2.7V and DCP) 6h = DCP Auto 2 (1.2V 2.7V and DCP) 7h = Reserved
25	DCD Enable	R/W	0h	Enable for Data-Contact Detection. Assert this bit to enable Data Contact Detect as defined by BC 1.2 for sinks.
24	Resistor 15k Present	R/W	0h	Configure D+ and D- termination. Assert this bit if there is a 15kOhm pull-down on D+ and D- (USB2.0 Host Phy pull-downs enabled). This should not be used for DCP or DCP Auto modes. 0h = System does NOT have 15 kOhm pull-down 1h = System has 15 kOhm pull-down
23-21	RESERVED	R	0h	
20	Enable Current Monitor	R/W	0h	Assert this bit to enable the PP5V current monitor (peak and average) that are read from the ADC_RESULTS register. While asserted the PD controller will remain in the active power mode.
19	Unconstrained Power	R/W	0h	Unconstrained Power configuration. This also sets the Unconstrained Power bit defined by USB PD. 0h = No unconstrained power 1h = Unconstrained power present
18-17	RESERVED	R	0h	
16	Automatic ID Request	R/W	1h	Configure identity discovery for SOP. If this bit is asserted, the PD Controller will automatically issue Discover Identity VDM for all SOP types when appropriate.
15	Initiate Swap to DFP	R/W	0h	Configure DR_Swap to DFP initiation. If this bit is asserted, the PD Controller automatically initiates and sends DR_Swap requests to the Port Partner when appropriate if presently operating as UFP.
14	Process Swap to DFP	R/W	1h	Configure response to DR_Swap to DFP. If this bit is asserted, the PD Controller will automatically accept a DR_Swap request to become a DFP. Otherwise, the PD Controller will reject such a request.
13	Initiate Swap to UFP	R/W	0h	Configure DR_Swap to UFP initiation. If this bit is asserted, the PD Controller automatically initiates and sends DR_Swap requests to the Port Partner when appropriate if presently operating as DFP.
12	Process Swap to UFP	R/W	1h	Configure response to DR_Swap to UFP. If this bit is asserted, the PD Controller will automatically accept a DR_Swap request to become a UFP. Otherwise, the PD Controller will reject such a request.
11-2	RESERVED	R	0h	

Table 6-15. Port Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	TypeC Current	R/W	2h	Type-C Current advertisement. This setting is ignored if a Source role is not enabled and active. This setting is also ignored during an explicit USB PD contract, where the Rp value is used for collision avoidance as required by the USB PD specification. Note that when PP5V is low, the FW will only use the default Type-C current regardless of the value in this field. 0h = USB Default Current 1h = 1.5 A 2h = 3.0 A 3h = Reserved

6.1.14 Boot Flags Register (Offset = 2Dh) [Reset = 0000000000h]

Boot Flags is shown in Table 6-16.

Return to the Summary Table.

Detailed status of boot process. This register provides details on PD Controller boot flags, Customer OTP configuration, and silicon revision

Table 6-16. Boot Flags Register Field Descriptions

Bit	Field	Type	Reset	Description
39-32	RESERVED	R	0h	
31-29	Patch Config Source	R	0h	Source of patch configuration. This field indicates the source of the configuration patch that has been successfully loaded. 0h = No configuration has been loaded 5h = A configuration has been loaded from EEPROM 6h = A configuration has been loaded from I2C 7h = Reserved
28-20	RESERVED	R	0h	
19	System TSD	R	0h	System thermal shut-down indicator. This bit is asserted if the PD controller is rebooting after the system thermal sensor caused a reset.
18	RESERVED	R	0h	
17	PP3 Switch	R	0h	PP3 switch status. This bit is asserted when the PP3 sink path was enabled during dead-battery mode
16-14	RESERVED	R	0h	
13	Region 1 CRC Fail	R	0h	Region 1 CRC status indicator. This bit is asserted when the CRC of data read from Region 1 of EEPROM memory failed.
12	Region 0 CRC Fail	R	0h	Region 0 CRC status indicator. This bit is asserted when the CRC of data read from Region 0 of EEPROM memory failed.
11	RESERVED	R	0h	
10	Patch Download Error	R	0h	Asserted when a patch download error occurs.
9	Region 1 EEPROM Error	R	0h	Region 1 status indicator. This bit is asserted when an error occurred attempting to read Region 1 of EEPROM memory. A retry may have been successful.
8	Region 0 EEPROM Error	R	0h	Region 0 status indicator. This bit is asserted when an error occurred attempting to read Region 0 of EEPROM memory. A retry may have been successful.
7	Region 1 Invalid	R	0h	Region 1 header status indicator. This bit is asserted when Region 1 header of the EEPROM memory was invalid.
6	Region 0 Invalid	R	0h	Region 0 header status indicator. This bit is asserted when Region 0 header of the EEPROM memory was invalid.
5	Region 1	R	0h	Region 1 attempted indicator. This bit is asserted when Region 1 of the EEPROM memory was attempted.
4	Region 0	R	0h	Region 0 attempted indicator. This bit is asserted when Region 0 of the EEPROM memory was attempted.
3	I2C EEPROM Present	R	0h	EEPROM presence indicator. This bit is asserted when an EEPROM device was discovered during boot.
2-1	RESERVED	R	0h	
0	Patch Header Error	R	0h	Asserted when a patch bundle header errors.

6.1.15 Received Sink Capabilities Register (Offset = 31h) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000h]

Received Sink Capabilities is shown in Table 6-17.

Return to the Summary Table.

Received Sink Capabilities. This register stores latest Sink Capabilities message received over BMC.

Table 6-17. Received Sink Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
423-232	RESERVED	R	0h	
231-200	Sink PDO 7	R	0h	Seventh Sink Capabilities PDO received
199-168	Sink PDO 6	R	0h	Sixth Sink Capabilities PDO received
167-136	Sink PDO 5	R	0h	Fifth Sink Capabilities PDO received
135-104	Sink PDO 4	R	0h	Fourth Sink Capabilities PDO received
103-72	Sink PDO 3	R	0h	Third Sink Capabilities PDO received
71-40	Sink PDO 2	R	0h	Second Sink Capabilities PDO received
39-8	Sink PDO 1	R	0h	First Sink Capabilities PDO received
7-3	RESERVED	R	0h	
2-0	Number Valid PDOs	R	0h	Number of valid SPR PDOs in this register. Each PDO is 4 bytes. (max of 7)

6.1.16 Transmit Source Capabilities Register (Offset = 32h) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000001h]

Transmit Source Capabilities is shown in Table 6-18.

Return to the Summary Table.

Source Capabilities for sending. This register stores PDOs and settings for outgoing Source Capabilities PD messages. Initialized by Application Customization.

Table 6-18. Transmit Source Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
503-248	RESERVED	R	0h	
247-216	TX Source PDO 7	R/W	0h	SPR Seventh Source Capabilities PDO contents.
215-184	TX Source PDO 6	R/W	0h	SPR Sixth Source Capabilities PDO contents.
183-152	TX Source PDO 5	R/W	0h	SPR Fifth Source Capabilities PDO contents.
151-120	TX Source PDO 4	R/W	0h	SPR Fourth Source Capabilities PDO contents.
119-88	TX Source PDO 3	R/W	0h	SPR Third Source Capabilities PDO contents.
87-56	TX Source PDO 2	R/W	0h	SPR Second Source Capabilities PDO contents.
55-24	TX Source PDO 1	R/W	0h	SPR First Source Capabilities PDO contents.
23-10	RESERVED	R	0h	
9-8	Power Path for PDO 1	R/W	0h	Configures which PP to use for PDO1. 0h = PP5V is used for this PDO 2h = PP_EXT1 is used for this PDO
7-3	RESERVED	R	0h	
2-0	Number Valid PDOs	R/W	1h	Number of valid PDOs in this register. Each PDO is 4 bytes. (max of 7)

6.1.17 Active PDO Contract Register (Offset = 34h) [Reset = 000000000000h]

Active PDO Contract is shown in Table 6-19.

Return to the Summary Table.

Power data object for active contract. This register stores PDO data for the current explicit USB PD contract, or all zeroes if no contract.

Table 6-19. Active PDO Contract Register Field Descriptions

Bit	Field	Type	Reset	Description
47-42	RESERVED	R	0h	
41-32	First PDO Control Bits	R	0h	Contains PDO specific information of the first PDO. It does not matter which PDO was selected, this field is always drawn from the first PDO.
31-0	Active PDO	R	0h	Power data object. This field contains the contents of the PDO requested by PD controller as sink and accepted by source, once it is accepted by source.

6.1.18 Active RDO Contract Register (Offset = 35h) [Reset = 00000000000000000000000000000000h]

Active RDO Contract is shown in Table 6-20.

Return to the Summary Table.

Power data object for the active contract. This register stores the RDO of the current explicit USB PD contract, or all zeroes if no contract.

Table 6-20. Active RDO Contract Register Field Descriptions

Bit	Field	Type	Reset	Description
127-124	Requested Object Position	R	0h	Corresponding PDO location in the Source_Capabilities Message.
123	RESERVED	R	0h	
122	Requested Capability Missmatch	R	0h	Set when Source cannot satisfy the Sink's power or voltager requirements per Souce Capabilities
121	Requested USB Communication Capable	R	0h	When set, the device has USB data lines and is capable of communicating using USB2, USB3 or USB4 protocols
120	Requested No USB Suspend	R	0h	This flag is used to indicate what actions are taken in USB Suspend.
119	RequestedUnchunked Supported	R	0h	When set, the port supports chunked and unchucked messagse.
118-116	RESERVED	R	0h	
115-106	Requested Operating Current	R	0h	Operating current (10mA per LSB)
105-96	Requested Max Min Operation Current	R	0h	Shall be assigned same as Operating Current field
95-32	RESERVED	R	0h	
31-28	Object Position	R	0h	Corresponding PDO location in the Source_Capabilities Message.
27	Give Back Flag	R	0h	When set, the device will respond to a GotoMin message by reducing its load to minimum operating current
26	Capability Missmatch	R	0h	Set when Source cannot satisfy the Sink's power or voltage requirements per Souce Capabilities
25	USB Communication Capable	R	0h	When set, the device has USB data lines and is capable of communicating using USB2, USB3 or USB4 protocols
24	No USB Suspend	R	0h	This flag is used to indicate what actions are taken in USB Suspend.
23	Unchunked Supported	R	0h	When set, the port supports chunked and unchucked messagse.
22-20	RESERVED	R	0h	
19-10	Operating Current	R	0h	Operating current (10mA per LSB)
9-0	Max Min Operation Current	R	0h	Shall be assigned same as Operating Current field

6.1.19 Power Status Register (Offset = 3Fh) [Reset = 0000h]

Power Status is shown in Table 6-21.

Return to the Summary Table.

Details about the power of the connection. This register reports status regarding the power of the connection.

Table 6-21. Power Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	
9-8	Charger Advertise Status	R	0h	Charger Advertise Status 0h = Charger advertise disabled or not run 1h = Charger advertisement in process 2h = Charger advertisement complete 3h = Reserved
7-1	RESERVED	R	0h	
0	Power Connection	R	0h	Asserted if there is a connection. This bit is asserted when STATUS.PlugPresent is TRUE AND STATUS.ConnState is greater than 5h. 0h = Connection requests power 1h = Connection provides power (PD Controller as sink) 3h = Explicit PD contract sets current

6.1.20 PD3 Configuration Register (Offset = 42h) [Reset = 00080010h]

PD3 Configuration is shown in Table 6-22.

Return to the Summary Table.

PD3.0 configuration settings.

Table 6-22. PD3 Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	
20	Support PPS Status	R/W	0h	Supports PPS Status Message. If this bit is asserted the PD controller will respond to a Get_PPS_Status message with the contents of the TX_PPS_SDB register (0x7A).
19	Support Get Revision	R/W	1h	Supports Revision Message. If this bit is asserted the PD controller will respond to a Get_Revision USB PD message with the supported PD Spec Version.
18	Support Get Source Info	R/W	0h	Support Source Info Message. If this bit is asserted the PD controller will respond to a Get_Source_Info USB PD message with the contents of TX_SOURCE_INFO (0x78) register.
17-13	RESERVED	R	0h	
12	Support Manufacture Info Message	R/W	0h	Support Manufacturing Info message. If this bit is asserted the PD controller will respond to a Get_Manufacturer_Info USB PD message with the contents of the TX_MIDB_SOP register (0x73).
11	Support Battery Status Message	R/W	0h	Support Battery Status message. If this bit is asserted the PD controller will respond to a Get_Battery_Status USB PD message with the contents of the TX_BSDO register (0x7B).
10	Support Battery Capabilities Message	R/W	0h	Support Battery Capability message. If this bit is asserted the PD controller will respond to a Get_Battery_Capabilities USB PD message with the contents of the TX_BCDB register (0x7D).
9	RESERVED	R	0h	
8	Support Source Extended Message	R/W	0h	Enable Source Capabilities Extended. If this bit is asserted the PD controller will respond to a Get_Source_Capabilities_Extended USB PD message with the contents of the TX_SCEDB register (0x77).
7	Auto Get MIDB	R/W	0h	Enable Auto send GetManufaturerInfo. If this bit is asserted, the PD controller will automatically send a Get_Manufacturer_Info USB PD msesage after receiving a Discovery_Identity USB PD message. The contents of the message will be stored in TX_MIBDB_SOP register (0x73)
6-5	RESERVED	R	0h	
4	Unchunked Supported	R/W	1h	Enable unchunked support. If this bit is asserted the PD controller will support unchunked messaging (up to 260 bytes). The host is responsible to consume the unchunked message before the PD controller will be able to receive another long unchunked message.
3-0	RESERVED	R	0h	

6.1.21 Received SOP Identity Data Object Register (Offset = 48h) [Reset = 00000000000000000000000000000000000000000000000000000000h]

Received SOP Identity Data Object is shown in Table 6-23.

Return to the Summary Table.

Received Discover Identity ACK (SOP). Latest Discover Identity response received over USB PD using SOP.

Table 6-23. Received SOP Identity Data Object Register Field Descriptions

Bit	Field	Type	Reset	Description
199-168	RX ID SOP VDO 6	R	0h	6th VDO. The sixth Data Object for Discover Identity response is context-specific.
167-136	RX ID SOP VDO 5	R	0h	5th VDO. The fifth Data Object for Discover Identity response is context-specific.
135-104	RX ID SOP VDO 4	R	0h	4th VDO. The fourth Data Object for Discover Identity response is context-specific as defined in USB PD.
103-72	RX ID SOP VDO 3	R	0h	Product VDO. The third Data Object for Discover Identity response.
71-40	RX ID SOP VDO 2	R	0h	Cert Stat VDO. The second Data Object for Discover Identity response.
39-8	RX ID SOP VDO 1	R	0h	ID Header VDO. The first Data Object in Discover Identity response.
7-6	Response Type	R	0h	Type of response received. 0h = SOP Discover Identity REQ not sent or pending 1h = Responder ACK received 2h = Responder NAK received or response timeout 3h = Responder BUSY received
5-3	RESERVED	R	0h	
2-0	Number Valid VDOs	R	0h	Number of valid VDO's in this register. (Max of 6)

6.1.22 IO Config Register (Offset = 5Ch) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000CCBh]

IO Config is shown in Table 6-24.

Return to the Summary Table.

Application-specific GPIO Configurations. This register cannot be modified at run-time, the GPIO configurations are set according to the configuration during the boot process.

Table 6-24. IO Config Register Field Descriptions

Bit	Field	Type	Reset	Description
391-384	GPIO 12 Mapped Event	R	0h	Event table mapping for GPIO12. See GPIO Event table.
383-376	GPIO 11 Mapped Event	R	0h	Event table mapping for GPIO11. See GPIO Event table.
375-368	GPIO 10 Mapped Event	R	0h	Event table mapping for GPIO10. See GPIO Event table.
367-352	RESERVED	R	0h	
351-344	GPIO 7 Mapped Event	R	0h	Event table mapping for GPIO7. See GPIO Event table.
343-336	GPIO 6 Mapped Event	R	0h	Event table mapping for GPIO6. See GPIO Event table.
335-328	GPIO 5 Mapped Event	R	0h	Event table mapping for GPIO5. See GPIO Event table.
327-320	GPIO 4 Mapped Event	R	0h	Event table mapping for GPIO4. See GPIO Event table.
319-312	GPIO 3 Mapped Event	R	0h	Event table mapping for GPIO3. See GPIO Event table.
311-304	GPIO 2 Mapped Event	R	0h	Event table mapping for GPIO2. See GPIO Event table.
303-296	GPIO 1 Mapped Event	R	0h	Event table mapping for GPIO1. See GPIO Event table.
295-288	GPIO 0 Mapped Event	R	0h	Event table mapping for GPIO0. See GPIO Event table.
287-269	RESERVED	R	0h	
268-256	GPIO Event Polarity	R	0h	Controls polarity of a selected output event for each GPIO. Assert the bit for a given GPIO to invert the polarity of the event mapped to it. This field has no impact for input GPIO Events.
255-230	RESERVED	R	0h	
229	GPIO 5 Analog Input Control	R	0h	Assert when GPIO5 is used as an analog input. This must also be asserted when PORT_CONTROL.ChargerDetectEnable or ChargerAdvertiseEnable is non-zero.
228	GPIO 4 Analog Input Control	R	0h	Assert when GPIO4 is used as an analog input. This must also be asserted when PORT_CONTROL.ChargerDetectEnable or ChargerAdvertiseEnable is non-zero.
227	RESERVED	R	0h	
226	GPIO AI Enable GPIO 2	R	0h	Assert when GPIO2 is used as an analog input.
225	RESERVED	R	0h	
224	GPIO AI Enable GPIO 0	R	0h	Assert when GPIO0 is used as an analog input.
223-205	RESERVED	R	0h	
204-192	Internal Pull Up Enable	R	0h	Controls weak pull-up setting for each configurable GPIO (1=Enabled, 0=Disabled).
191-173	RESERVED	R	0h	
172-160	Internal Pull Down Enable	R	0h	Controls weak pull-down setting for each configurable GPIO (1=Enabled, 0=Disabled).
159-109	RESERVED	R	0h	
108-96	Open Drain Output Enable	R	0h	Controls push-pull (0) vs. open-drain (1) setting for each configurable GPIO.
95-77	RESERVED	R	0h	
76-64	Initial Value	R	0h	Controls default output level for each GPIO enabled as output (0=Drive Low, 1=Drive High)
63-45	RESERVED	R	0h	
44-32	GPIO Interrupt Enable	R	0h	Controls interrupt enable for each GPIO (1=Interrupt Enabled, 0=Interrupt Disabled). Note that all GPIO pins may not be configured as inputs (see the data-sheet).

Table 6-24. IO Config Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	
12-0	GPIO Output Enable	R	CCBh	Controls output enable for each GPIO (1=Output Enabled, 0=Hi-Z). Note that all GPIO may not be configurable as an output (see data-sheet).

6.1.23 Type C State Register (Offset = 69h) [Reset = 00000000h]

Type C State is shown in Table 6-25.

Return to the Summary Table.

Contains current status of both CCn pins.

Table 6-25. Type C State Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TypeC Port State	R	0h	Present state of Type-C state-machine. 0h = Disabled 5h = ErrorRecovery 24h = Unattached.Accessory 2Bh = AttachWait.Accessory 45h = Try.SRC 50h = TryWait.SRC 60h = Attached.SRC 62h = CorrosionMitigation 63h = DebugAccessory 64h = AttachWait.SRC 67h = Unattached.SRC
23-16	CC2 Pin State	R	0h	State of CC2 pin 0h = Not connected 1h = Ra detected (Source only) 2h = Rd detected (Source only)
15-8	CC1 Pin State	R	0h	State of CC1 pin 0h = Not connected 1h = Ra detected (Source only) 2h = Rd detected (Source only)
7-0	CC Pin for PD	R	0h	CC pin used for PD communication. 0h = Not connected 1h = CC1 is used for USB PD communication 2h = CC2 is used for USB PD communication

6.1.24 ADC Results Register (Offset = 6Ah) [Reset = 00000000000000000000000000h]

ADC Results is shown in Table 6-26.

Return to the Summary Table.

Provides access to measurements from the internal ADC. The PD controller periodically measures the pins mentioned in this register and updates the register accordingly. The frequency of the update depends upon the mode of the PD controller. For example, in Unconnected Sleep the PD controller will not update these registers. This register should only be used for debug purposes and not for end solutions.

Table 6-26. ADC Results Register Field Descriptions

Bit	Field	Type	Reset	Description
103-96	RESERVED	R	0h	
95-88	IVBUS_Peak	R	0h	Most recent current peak estimate through poewr path. If PORT_CONTROL.EnableCurrentMonitor = 1, this field is an estimate of the recent peak current. It is cleared upon attach for a new connection.(16.5mA per LSB)
87-80	GPIO2	R	0h	Most recent voltage on the GPIO2 pin. (14mV per LSB)
79-72	GPIO0	R	0h	Most recent voltage on the GPIO0 pin. (14mV per LSB)
71-64	GPIO5	R	0h	Most recent voltage on the GPIO5 pin. (14mV per LSB)
63-56	GPIO4	R	0h	Most recent voltage on the GPIO4 pin. (14mV per LSB)
55-48	RESERVED	R	0h	
47-40	IVBUS_Mean	R	0h	Most recent current mean estimate through power path. If PORT_CONTROL.EnableCurrentMonitor = 1, this field is an estimate of the recent mean current. It is cleared upon attach for a new connection.(16.5mA per LSB)
39-32	RESERVED	R	0h	
31-24	VBUS	R	0h	Most recent voltage on the VBUS pin. (98mV per LSB)
23-16	LDO3V3	R	0h	Most recent voltage on the LDO_3V3 pin. (14mV per LSB)
15-8	ADCIN2	R	0h	Most recent voltage on the ADCIN2 pin. (14mV per LSB)
7-0	ADCIN1	R	0h	Most recent voltage on the ADCIN1 pin. (14mV per LSB)

6.1.25 Sleep Control Register (Offset = 70h) [Reset = 03h]

Sleep Control Register is shown in Table 6-27.

Return to the Summary Table.

Sleep configurations.

Table 6-27. Sleep Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	
2-1	Sleep Time	R/W	1h	Minimum time the PD controller waits before entering sleep mode. 0h = Reserved 1h = 100 ms 2h = 1000 ms 3h = Reserved
0	Sleep Mode Allowed	R/W	1h	If this bit is asserted the PD controller will enter sleep modes after device is idle for Sleep Time.

6.1.26 GPIO Status Register (Offset = 72h) [Reset = 0000000000000000h]

GPIO Status is shown in Table 6-28.

Return to the Summary Table.

Captures status and settings of all GPIO pins. Check the device-specific datasheet for the available GPIO because it may vary by device type.

Table 6-28. GPIO Status Register Field Descriptions

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	
39	GPIO 7 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
38	GPIO 6 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
37	GPIO 5 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
36	GPIO 4 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
35	GPIO 3 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
34	GPIO 2 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
33	GPIO 1 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
32	GPIO 0 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
31-13	RESERVED	R	0h	
12	GPIO 12 Data	R	0h	Asserted if a logic high is detected on the GPIO.
11	GPIO 11 Data	R	0h	Asserted if a logic high is detected on the GPIO.
10	GPIO 10 Data	R	0h	Asserted if a logic high is detected on the GPIO.
9-8	RESERVED	R	0h	
7	GPIO 7 Data	R	0h	Asserted if a logic high is detected on the GPIO.
6	GPIO 6 Data	R	0h	Asserted if a logic high is detected on the GPIO.
5	GPIO 5 Data	R	0h	Asserted if a logic high is detected on the GPIO.
4	GPIO 4 Data	R	0h	Asserted if a logic high is detected on the GPIO.
3	GPIO 3 Data	R	0h	Asserted if a logic high is detected on the GPIO.
2	GPIO 2 Data	R	0h	Asserted if a logic high is detected on the GPIO.
1	GPIO 1 Data	R	0h	Asserted if a logic high is detected on the GPIO.
0	GPIO 0 Data	R	0h	Asserted if a logic high is detected on the GPIO.

6.1.27 TX Manufactrer Info SOP Register (Offset = 73h) [Reset = 00000000000000000000000000000000000000000000000h]

TX Manufactrer Info SOP is shown in Table 6-29.

Return to the Summary Table.

Transmit Manufacturer Info Data Block SOP (MIDB). The host must enable this feature using the SupportManufacturerInfoMsg bit in the PD3 Configuration register (0x42). If the SupportManufacturerInfoMsg bit is set to 0, then when a Get_Manufacturer_Info message is received the PD controller responds with a Not_Supported message. If the SupportManufacturerInfoMsg bit is set to 1, then the PD controller responds to a Get_Manufacturer_Info message with a target specified as "Port". If received Get_Manufacturer_Info message has a target specified as "Battery", then the PD controller responds by appending the ASCII string "Not Supported" followed by a zero byte.

Table 6-29. TX Manufactrer Info SOP Register Field Descriptions

Bit	Field	Type	Reset	Description
175-0	Manufacturer String	R/W	0h	Manufacturer String as defined in USB PD. This must be a null terminated string. The PD controller always sends all 22 bytes.

6.1.28 Tx Source Capabilities Extended Data Block Register (Offset = 77h) [Reset = 00000000000000000000000000000000h]

Tx Source Capabilities Extended Data Block is shown in Table 6-30.

Return to the Summary Table.

Transmit Source Capabilities Extended Data Block (SCEDB). If the PD3 configuration register (0x42) bit SourceCapExtMsg is set to zero, the PD controller responds to a Get_Source_Cap_Extended USB PD message with a Not_Supported message. If the SourceCapExtMsg bit is set to 1 then the response is generated from the contents of this register based on USB PD requirements. The VID, PID, and XID fields are taken from the PD internal firmware configurable through the Application Customization Tool, the FW version is taken from the PD internal firmware, then the contents of this register are appended.

Table 6-30. Tx Source Capabilities Extended Data Block Register Field Descriptions

Bit	Field	Type	Reset	Description
119-111	RESERVED	R	0h	
110-104	Source PDP	R/W	0h	Source's PDP rating as defined by the USB PD specification.
103-100	Number Hot Swappable Batteries	R/W	0h	Number of hot swappable batteries / battery slots as defined by the USB PD specification. (Max of 4)
99-96	Number Fixed Batteries	R/W	0h	Number of fixed batteries / battery slots as defined by the USB PD specification. (Max of 4)
95-88	Source Inputs	R/W	0h	Source inputs as defined by the USB PD specification.
87-80	Touch Temperature	R/W	0h	Touch temperature as defined by the USB PD specification.
79-64	Peak Current 3	R/W	0h	Peak Current 3 as defined by the USB PD specification.
63-48	Peak Current 2	R/W	0h	Peak Current 2 as defined by the USB PD specification.
47-32	Peak Current 1	R/W	0h	Peak Current 1 as defined by the USB PD specification.
31-24	Touch Current	R/W	0h	Touch current as defined by the USB PD specification.
23-16	Compliance	R/W	0h	Compliance as defined by the USB PD specification.
15-8	Hold Up Time	R/W	0h	Hold up time as defined by the USB PD specification.
7-0	Voltage Regulation	R/W	0h	Voltage regulation as defined by the USB PD specification.

6.1.29 TX Source Info Register (Offset = 78h) [Reset = 8000000080000000h]

TX Source Info is shown in Table 6-31.

Return to the Summary Table.

Transmit Source info. If the PD3 configuration register (0x42) bit SupportGetSourceInfo is set to 0 and a Get_Source_Info message is received, then this register is ignored and the PD controller sends a Not_Supported message. If the SupportGetSourceInfo bit is set to 1 and a Get_Source_Info message is received then the contents of this register are sent in response. This register is automatically updated by the PD firmware and does not require any EC implementation.

Table 6-31. TX Source Info Register Field Descriptions

Bit	Field	Type	Reset	Description
63	PortType	R/W	1h	Managed or Guaranteed Capability Port: Managed = 0, Guaranteed = 1
62	DPSPort	R/W	0h	DPS Port. If set, then PortType shall be 0 (Managed Capability Port)
61-50	RESERVED	R	0h	
49-41	Port Maximum PDP 0.5W	R/W	0h	Maximum power the port will provide in 0.5W steps. (0.5W per LSB)
40-32	Port Guaranteed PDP 0.5W	R/W	0h	Minimum power the port is ensured to always be able to provide in 0.5W steps. (0.5W per LSB)
31	Port Type	R/W	1h	Managed or Guaranteed Capability Port: Managed = 0, Guaranteed = 1
30-24	RESERVED	R	0h	
23-16	Port Maximum PDP	R/W	0h	Power the port is designed to supply. (1W per LSB)
15-8	Port Present PDP	R/W	0h	Power the port is presently capable of supplying. (1W per LSB)
7-0	Port Reported PDP	R/W	0h	Power the port is actually advertising. (1W per LSB)

6.1.30 Transmitted PPS Status Data Block Register (Offset = 7Ah) [Reset = 00000000h]

Transmitted PPS Status Data Block is shown in Table 6-32.

Return to the Summary Table.

Transmit PPS Status Data Block (BSDO). If the PD3 configuration register (0x42) bit SupportPPSStatus is set to zero and a Get_PPS_Status message is received, then this register is ignored and the PD controller sends a Not_Supported message. If the SupportPPSStatus bit is set to 1 and a Get_PPS_Status message is received then the contents of this register are sent in response.

Table 6-32. Transmitted PPS Status Data Block Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	
27	OMF	R/W	0h	Operating Mode Flag (OMF), indicates if running in Constant Voltage (CV - 0b) or Current Limit (CL - 1b) mode.
26-25	PTF	R/W	0h	Present Temperature Flag (PTF), indicates if temperature is normal (01b), warning zone (10b), or over-temperature (11b).
24	RESERVED	R	0h	
23-16	Output Current	R/W	0h	Output current as defined by the USB PD spec. (50mA per LSB). 0xFF = this field not supported
15-0	Output Voltage	R/W	0h	Output voltage as defined by the USB PD spec.(20mV per LSB, 0xFFFF = this field not supported)

6.1.31 Transmitted Battery Status Data Objects (BSDO) Register (Offset = 7Bh) [Reset = 00000000000000000000000FFFF0200h]

Transmitted Battery Status Data Objects (BSDO) Register is shown in Table 6-33.

Return to the Summary Table.

Transmit Battery Status Data Objects (BSDO). The host should also program the Tx Source Capabilities Extended register (0x77) in order to specify the number of each type of battery such that it is consistent with the contents of this register. This feature must be enabled in the PD3_CONFIG register (0x42) SupportBatteryStatusMsg bit. The PD controller does not take any automatic action if this register is written. If the SupportBatteryStatusMsg bit is set to 0 and a Get_Battery_Status message is received, then this register is ignored and the PD controller sends a Not_Supported message. If the SupportBatteryStatusMsg bit is set to 1, and a Get_Battery_Status message is received then the contents of this register are sent in response.

Table 6-33. Transmitted Battery Status Data Objects (BSDO) Register Field Descriptions

Bit	Field	Type	Reset	Description
127-112	Battery 3 Present Info	R/W	0h	Battery status data object returned for battery index 3.
111-104	Battery 3 Battery Info	R/W	0h	Battery status data object returned for battery index 3.
103-96	RESERVED	R	0h	
95-80	Battery 2 Present Capacity	R/W	0h	Battery status data object returned for battery index 2.
79-72	Battery 2 Battery Info	R/W	0h	Battery status data object returned for battery index 2.
71-64	RESERVED	R	0h	
63-48	Battery 1 Present Capacity	R/W	0h	Battery status data object returned for battery index 1.
47-40	Battery 1 Battery Info	R/W	0h	Battery status data object returned for battery index 1.
39-32	RESERVED	R	0h	
31-16	Battery 0 Present Capacity	R/W	FFFFh	Battery status data object returned for battery index 0.
15-8	Battery 0 Battery Info	R/W	2h	Battery status data object returned for battery index 0.
7-0	RESERVED	R	0h	

6.1.32 Tx Battery Capabilities Register (Offset = 7Dh) [Reset = 0000000000000000000000000000000000000000000000000000000000000000h]

Tx Battery Capabilities is shown in Table 6-34.

Return to the Summary Table.

Transmit Battery Capability Data Block (BCDB). The host should also program the Tx Source Capabilities Extended register (0x77) in order to specify the number of each type of battery such that it is consistent with the contents of this register. This feature must be enabled in the PD3_CONFIG register (0x42) bit SupportBatteryCapMsg. The PD controller does not take any automatic action if this register is written. If the SupportBatteryCapMsg is 0 and a Get_Battery_Capabilities message is received, then the contents of this register are ignored and the PD controller sends a Not_Supported message. If the SupportBatteryCapMsg is 1 and a Get_Battery_Capabilities message is received, then the contents of this register are sent in response.

Table 6-34. Tx Battery Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
287-280	Battery Type	R/W	0h	Battery type for battery index 0.
279-264	Battery Last Full Charge Capacity	R/W	0h	Battery last full charge capacity for battery index 0.
263-248	Battery Design Capacity	R/W	0h	Battery design capacity for battery index 0.
247-232	PID 3	R/W	0h	PID for battery index 0.
231-216	VID 3	R/W	0h	VID for battery index 0.
215-208	Battery Type	R/W	0h	Battery type for battery index 2.
207-192	Battery Last Full Charge Capacity	R/W	0h	Battery last full charge capacity for battery index 2.
191-176	Battery Design Capacity	R/W	0h	Battery design capacity for battery index 2.
175-160	PID 2	R/W	0h	PID for battery index 2.
159-144	VID 2	R/W	0h	VID for battery index 2.
143-136	Battery Type	R/W	0h	Battery type for battery index 1.
135-120	Battery Last Full Charge Capacity	R/W	0h	Battery last full charge capacity for battery index 1.
119-104	Battery Design Capacity	R/W	0h	Battery design capacity for battery index 1.
103-88	PID 1	R/W	0h	PID for battery index 1.
87-72	VID 1	R/W	0h	VID for battery index 1.
71-64	Battery Type	R/W	0h	Battery type for battery index 0.
63-48	Battery Last Full Charge Capacity	R/W	0h	Battery last full charge capacity for battery index 0.
47-32	Battery Design Capacity	R/W	0h	Battery design capacity for battery index 0.
31-16	PID 0	R/W	0h	PID for battery index 0.
15-0	VID 0	R/W	0h	VID for battery index 0.

6.1.33 Liquid Detection Configuration Register (Offset = 98h) [Reset = 00000000000000052000000h]

Liquid Detection Configuration is shown in Table 6-35.

Return to the Summary Table.

Liquid Detection Configuration

Table 6-35. Liquid Detection Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
87-80	Pulldown Threshold ADC	R/W	0h	Additional threshold check for pulldown resistor modifying threshold (e.g. RA in cable) (14mV per LSB as mV)
79	RESERVED	R	0h	
78	Single Pin Monitoring	R/W	0h	When enabled, only single LD pin is used for detection
77-76	Liquid Pins to Monitor	R/W	0h	Determine pins to monitor during liquid detection. 0 = UnusedPins (SBU), 1 = CC, 2= DPDM, 3= RSVD
75	Monitor During Unattach	R/W	0h	Monitor for liquid detection while unattached to a device.
74	Monitor During Attach	R/W	0h	Monitor for liquid detection while attached to a device. This may not be set if CC pins are used for liquid detection.
73	Enable Corrosion Mitigation	R/W	0h	Enable corrosion mitigation. Corrosion mitigation will disconnect the port, disable the port, and pull down CC pins. Type-C error-recovery will be triggered when the port transitions to no-moisture state.
72	Enable Liquid Detection	R/W	0h	Enables liquid detection on the pins connected to the GPIO on the PD Controller. In order for this to function correctly the proper external liquid detection circuitry must be in place.
71-64	High Threshold ADC Liquid	R/W	0h	High Threshold ADC Liquid (14mV per LSB as mV)
63-56	Low Threshold ADC Liquid	R/W	0h	Low Threshold ADC Liquid (14mV per LSB as mV)
55-48	High Threshold ADC No Liquid	R/W	0h	High Threshold ADC No Liquid, provides hysteresis for exit out of Liquid Detected. (14mV per LSB as mV)
47-40	Low Threshold ADC No Liquid	R/W	0h	Low Threshold ADC No Liquid, provides hysteresis for exit out of Liquid Detected. (14mV per LSB as mV)
39-32	Number of Samples	R/W	0h	Number of samples used for averaging. Valid values must be powers of two (1, 2, 4, 8, ...)
31-28	Liquid Detection Retries	R/W	5h	Number of times to retry checking for liquid on a port. Must be set to greater than 2 for CC liquid detection.
27-24	Liquid Detection Retries Wait Time	R/W	2h	Time to wait between retrying checking for liquid on a port. Must be set to at least 100ms for CC liquid detection. (100ms per LSB as ms)
23-20	Sample Time in 10ms Liquid	R/W	0h	Sample Time in multiples of 10ms (10ms per LSB as ms)
19-16	Sample Time in 10ms Non-Liquid	R/W	0h	Sample Time in multiples of 10ms (10ms per LSB as ms)
15-8	Wait Time In Sec Liquid	R/W	0h	Wait in multiples of 1s when liquid is detected (1000ms per LSB as ms)
7-0	Wait Time In Sec Non-Liquid	R/W	0h	Wait in multiples of 1s when liquid is not detected. (1000ms per LSB as ms)

6.1.34 Rx MIDB Register (Offset = A4h) [Reset = 00000000000000000000000000000000000000000000000000000000h]

Rx MIDB is shown in Table 6-36.

Return to the Summary Table.

This register stores the manufacturer info received after sending a Get_Manufacturer_Info PD Message

Table 6-36. Rx MIDB Register Field Descriptions

Bit	Field	Type	Reset	Description
175-0	Manufactuer Info	R	0h	The received manufacturer info message.

6.1.35 Liquid Detection STATUS Register (Offset = B2h) [Reset = 0000000000h]

Liquid Detection STATUS Register is shown in Table 6-37.

Return to the Summary Table.

Register for liquid detection functionality status

Table 6-37. Liquid Detection STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
39-32	Liquid Detected High Measurement	R	0h	LD1 ADC measurement when GPIO is driving circuit to VDD. (14mV per LSB as mV)
31-24	Liquid Detected Low Measurment	R	0h	LD1 ADC measurment when GPIO is driving circuit to GND. (14mV per LSB as mV)
23-16	No Liquid Detected High Measurement	R	0h	LD0 ADC measurement when GPIO is driving circuit to VDD. (14mV per LSB as mV)
15-8	No Liquid Detected Low Measurment	R	0h	LD0 ADC Measurement when GPIO is driving circuit to GND. (14mV per LSB as mV)
7	Liquid Measurment Status	R	0h	Indicates liquid detection measurment is currently ongoing on the device.
6-3	Liquid Retry Count	R	0h	Number of times liquid detection has been completed.
2	Mitigation Status	R	0h	Indicates port is currently in corrosion mitigation and will not attach to a device.
1	Liquid Status State	R	0h	Indicates liquid has been detected on the port at least LQDRetries number of times.
0	Liquid Detection State	R	0h	Indicates if liquid was seen on the port during the current measurement.

7 4CC Task Detailed Descriptions

7.1 Overview

This section describes the 4CC Tasks defined by the PD Controller Host Interface. The Tasks are categorized into various sub-groups in this section. All Tasks that return data using the DATAx registers will always ensure the proper output data is loaded into those registers before setting the CMDx register to 0 to indicate Task completion. DATAx is never modified by PD Controller after CMDx has been changed to 0, to ensure the Host can retrieve data from the previously-executed Task, and to ensure the Host can load these registers for a future Task without risk of overwriting. Note that other registers can continue to be updated after a Task completes, as Tasks can have additional side effects.

Many of the Tasks return a status code in the first byte of the DATAx register. The standard Task response byte is defined in Table 7-1. The remaining DATAx bytes can be used at each Task's discretion.

Table 7-1. Standard Task Response

Description	**Tasks are a special form of Tasks that return a status code in the first byte of the DATAX register.**			
Output DATAX	Bit	Name	Description	
	Byte 1: Task Return Code			
	7:4	Reserved	Reserved for standard Tasks. May be used by certain Tasks for Task-specific return codes. Successful return codes can use this byte provided TaskResult is 0x0.	
	3:0	TaskResult	Standard Task return codes.	
			0x0	Task completed successfully.
			0x1	Task timed-out.
			0x2	Reserved.
			0x3	Task rejected.
			0x4	Task rejected because the Rx Buffer was locked. This is for Tasks that can require the PD controller to use the Rx Buffer.
			0x5-0xF	Reserved for standard Tasks. May be used by certain Tasks for Task-specific error codes. Treated as an error when encountered.

7.2 CPU Control Tasks

7.2.1 'Gaid' - Return to Normal Operation

Table 7-2. 'Gaid' - Return to Normal Operation

Description	The 'Gaid' Task causes a warm restart of the PD Controller processor.
INPUT DATAX	None
OUTPUT DATAX	None
Task Completion	Technically this Task never completes because the processor restarts. However, because all HI registers return to their default state upon reboot, all CMDx/DATAx registers will return to 0, which will mark this Task as complete.
Side Effects	The 'Gaid' Task causes a warm restart of the PD Controller processor. PD Controller can momentarily NAK I2C transactions while rebooting.
Additional Information	The PD controller is in the 'APP ' mode, then it immediately goes to the Error Recovery state then after delaying 1 second (typical) it does a warm restart. The register settings revert back to the original AppConfig configuration set by the user in the Application Customization Tool.

7.2.2 'GAID' - Cold Reset Request

Table 7-3. 'GAID' - Cold Reset Request

Description	The 'GAID Task causes a cold restart of the PD Controller processor.
INPUT DATAX	None
OUTPUT DATAX	None
Task Completion	Technically this Task never completes because the processor restarts. However, because all HI registers return to their default state upon reboot, all CMDx/DATAx registers will return to 0, which will mark this Task as complete. This Task forces the PD Controller to reboot its OTP bootloader.
Side Effects	The 'Gaid' Task causes a warm restart of the PD Controller processor. PD Controller can momentarily NAK I2C transactions while rebooting.
Additional Information	The PD controller immediately goes to the Error Recovery state, then after delaying 1 second (typical) it does a cold restart. The register settings revert back to the default state of the PD before entering 'APP' mode.

7.3 PD Message Tasks

7.3.1 'SWDF' - PD DR_Swap to DFP

Table 7-4. 'SWDF' - PD DR_Swap to DFP

Description	The 'SWDF' Task instructs PD Controller to attempt to become a DFP through DR_Swap at the first opportunity while maintaining policy engine compliance.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code.
Task Completion	The 'SWDF' Task completes either when the DR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the DFP. The 'SWDF' Task shall be considered rejected if: • The UFP indicated through Source or Sink Capabilities that it does not support Data Role Swap. • The DR_Swap is Rejected. The 'SWDF' Task shall be considered successful if: • PD Controller is already in the DFP data role. • The DR_Swap is Accepted and completes normally.
Side Effects	When the 'SWDF' Task completes successfully PD Controller will have transitioned to the DFP data role, which impacts other registers. If the DR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
Additional Information	None

7.3.2 'SWUF' - PD DR_Swap to UFP

Table 7-5. 'SWUF' - PD DR_Swap to UFP

Description	The 'SWUF' Task instructs PD Controller to attempt to become a UFP through DR_Swap at the first opportunity while maintaining policy engine compliance.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code.
Task Completion	The 'SWUF' Task completes either when the DR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the UFP. The 'SWUF' Task shall be considered rejected if: • The DFP indicated through Source or Sink Capabilities that it does not support Data Role Swap. • The DR_Swap is Rejected. The 'SWUF' Task shall be considered successful if: • PD Controller is already in the UFP data role. • The DR_Swap is Accepted and completes normally.
Side Effects	When the 'SWDF' Task completes successfully PD Controller will have transitioned to the UFP data role, which impacts other registers. If the DR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
Additional Information	None

7.3.3 'GSkC' - PD Get Sink Capabilities

Table 7-6. 'GSkC' - PD Get Sink Capabilities

Description	**The 'GSkC' Task instructs PD Controller to issue a Get_Sink_Cap message to the Port Partner at the first opportunity while maintaining policy engine compliance.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code.
Task Completion	The 'GSkC' Task completes either when the Sink Capabilities message is received or the Task otherwise fails. • The Port Partner is a Source and indicated it was not Dual-Role Power. • The Port Partner responds to the Get_Sink_Cap message with a Reject or Not_Supported message. The 'GSkC' Task shall be considered timed-out if: • The Port Partner fails to respond within the time required by the PD spec. The 'GSkC' Task shall be considered successful if: • The Get_Sink_Cap message is sent, GoodCRC'ed and a Sink Capabilities response is received and processed.
Side Effects	When the 'GSkC' Task completes successfully the *RX_SINK_CAPS* register (0x31) will have been updated.
Additional Information	None

7.3.4 'SSrC' - PD Send Source Capabilities

Table 7-7. 'SSrC' - PD Send Source Capabilities

Description	**The 'SSrC' Task instructs the PD Controller to send a SourceCapabilities message at the first opportunity while maintaining policy enginecompliance.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code.
Task Completion	The 'SSrC' Task completes either when the Sink Capabilities message GoodCRC is received or the Task otherwise fails. The 'SSrC' Task shall be considered rejected if: • PD Controller is not in a Source role. The 'SSrC' Task shall be considered timed-out if: • The Source Capabilities message was sent but no GoodCRC was received. The 'SSrC' Task shall be considered successful if: • The Source Capabilities message was sent and a GoodCRC is received.
Side Effects	Other registers can change as a result of the contract negotiation that begins with the new Source Capabilities message.
Additional Information	None

7.3.5 'GPPI' - PD Get Port Partner Information

The 'GPPI' Task can be used to cause the PD controller to issue these types of USB PD Get messages:

- Get_Sink_Cap_Extended (control message)
- Get_Manufacturer_Info (Extended message)

The PD controller does not have dedicated registers to store the response to these messages. The host must get that response from the DATAX register associated with this Task.

The host must NOT use 'GPPI' to send Get_Sink_Capabilities messages, because the USB PD spec requires specific actions be taken by the PD controller any time those messages are received. While executing the 'GPPI' Task, the PD controller does not parse the returned message to carry out those checks. Instead, the host must use 'GSkC' to send Get_Sink_Capabilities.

This Task is defined to enable supporting any new Get message that can be defined by USB PD in the future.

Table 7-8. 'GPPI' - Send a USB PD Get* Message

Description	**The 'GPPI' Task instructs PD Controller to issue a specific USB PDmessage to the Port Partner at the first opportunity while maintaining policyengine compliance.**			
INPUT DATAX	**Bit**	**Name**	**Description**	
	15	Reserved		
	14:13	FrameType	00b	SOP
			01b	SOP'
			10b	SOP''
			11b	Reserved
	12:8	NumBytes		
	7	Reserved		
	6:5	MessageCategory	00b	Control message (no payload)
			01b	Data message (requires payload)
			10b	Extended message (requires payload)
			11b	Reserved
	4:0	MessageType	This field must be the MessageType as defined in the USB PD specification. It specifies the Type of message the PD controller will send.	
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also *Standard Task Response*.			
Task Completion	The 'GPPI' Task completes either when the appropriate message is received or the Task otherwise fails. The 'GPPI' Task shall be considered rejected if: • Sending the requested message can violate the USB PD spec. For example, the Port Partner is a Sink and indicated (through previous Source or Sink Capabilities) it was not Dual-Role Power. • The PortPartner replies with a Reject or Not_Supported message. The 'GPPI' Task shall be considered timed-out if: • The requested message is sent, GoodCRC'ed and the recipient (Port Partner or Cable Plug) fails to respond within the time required by the PD spec. • A PD Hard Reset or a disconnection happens before the Task completes. The 'GPPI' Task shall be considered successful if: • The requested message is sent, GoodCRC'ed and an appropriate response is received and processed. The 'GPPI' Task shall be aborted when the Rx Buffer is locked. The Rx Buffer is locked after data from a receive message is placed in the DATAX register. The Rx Buffer is unlocked after disconnect and by the 'MBRd' Task.			
Side Effects	If necessary, the PD controller can issue a VCONN_Swap in order to send the requested message to a Cable Plug. If the PD controller is in the sink power role and it reads Rp = SinkTxNG, it will wait until Rp = SinkTxOK before initiating the atomic message sequence requested by this 'GPPI' Task. This can cause an non-deterministic delay in completing the Task.			

Table 7-8. 'GPPI' - Send a USB PD Get* Message (continued)

Description	The 'GPPI' Task instructs PD Controller to issue a specific USB PDmessage to the Port Partner at the first opportunity while maintaining policyengine compliance.
Additional Information	The PD controller will continue trying to execute this Task until it times out or aborts as described above. Some scenarios where this can happen are: • The PD controller is required to be the VCONN_Source in order to send any message on SOP or SOP'. The PD controller will continue trying to become the VCONN provider until it is successful. • The PD controller with a sink power role (that is PresentRole = Sink) is required to wait for Rp = SinkTxOK before initiating an Atomic Message Sequence. The PD controller will continue waiting for Rp = SinkTxOK until it is able to send the appropriate message required for this 'GPPI' Task. The host must wait until CMDx reads as 0 or INT_EVENT1.CmdComplete is asserted before issuing the 'MBRd' 4CC Task to read the Rx Buffer after issuing this 'GPPI' Task. While executing the 'GPPI' Task, the PD controller uses the same shared buffer that is used to store other extended messages. Therefore, the host must not use the 'GPPI' Task when any other atomic message sequence is ongoing. To read the PD response received as a result of issuing the 'GPPI' Task after it is completed, the host must use the 'MBRd' 4CC command. The 'MBRd' Task must also be used to unlock the Rx Buffer for other incoming message.

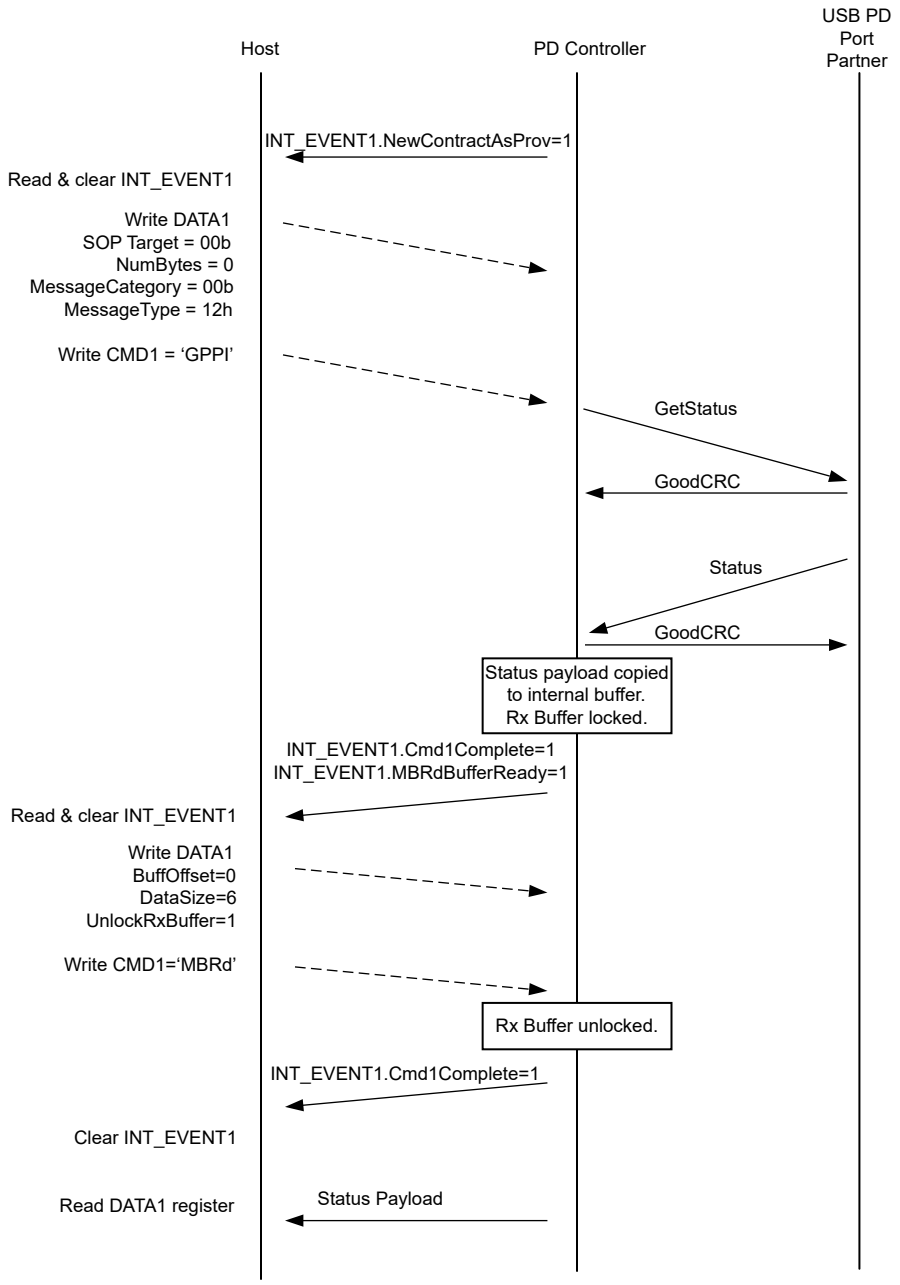


Figure 7-1. Example Sequence for 'GPPI' Task When Host Uses INT_EVENT1

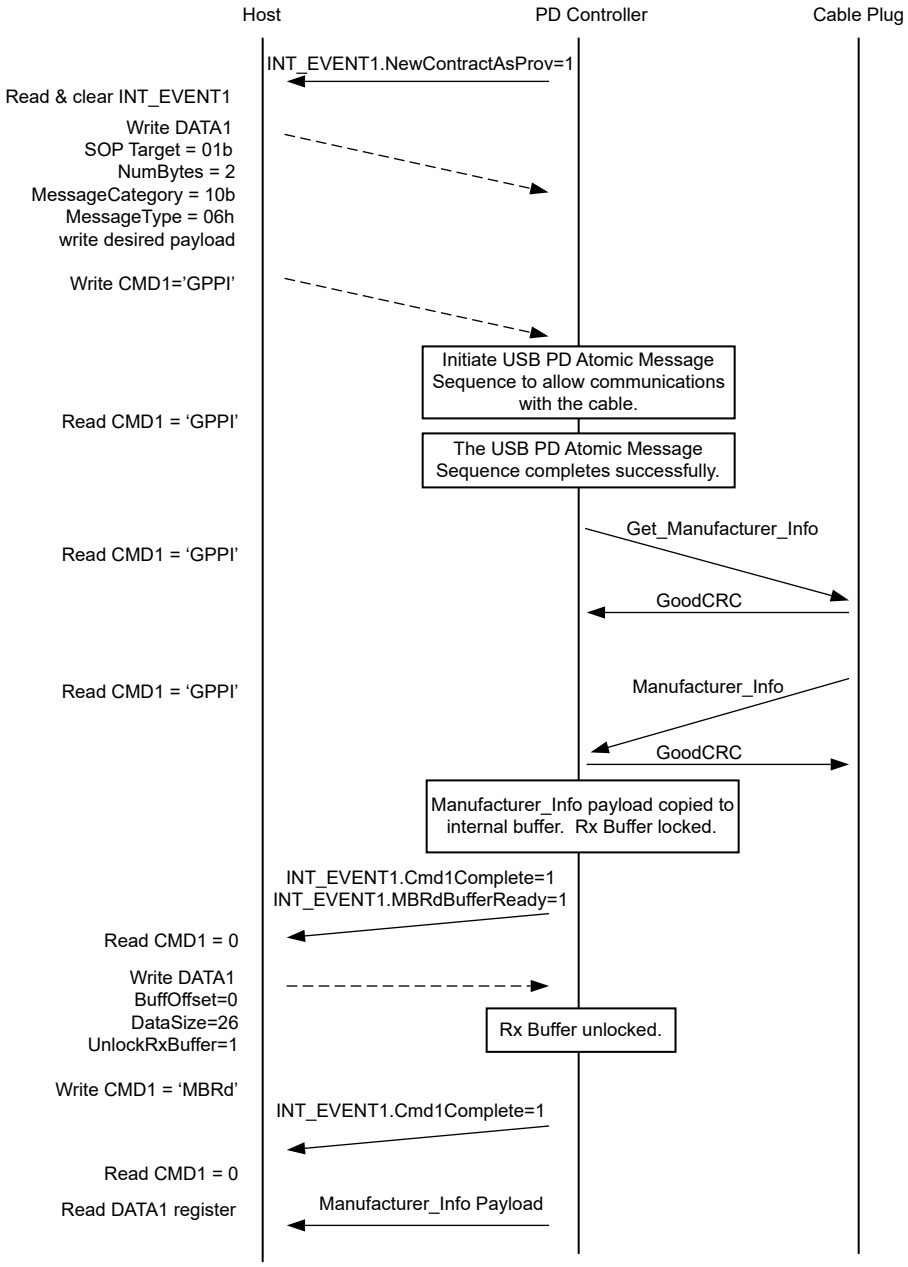


Figure 7-2. Example Sequence for 'GPPI' Task When Host Uses CMD1 Polling

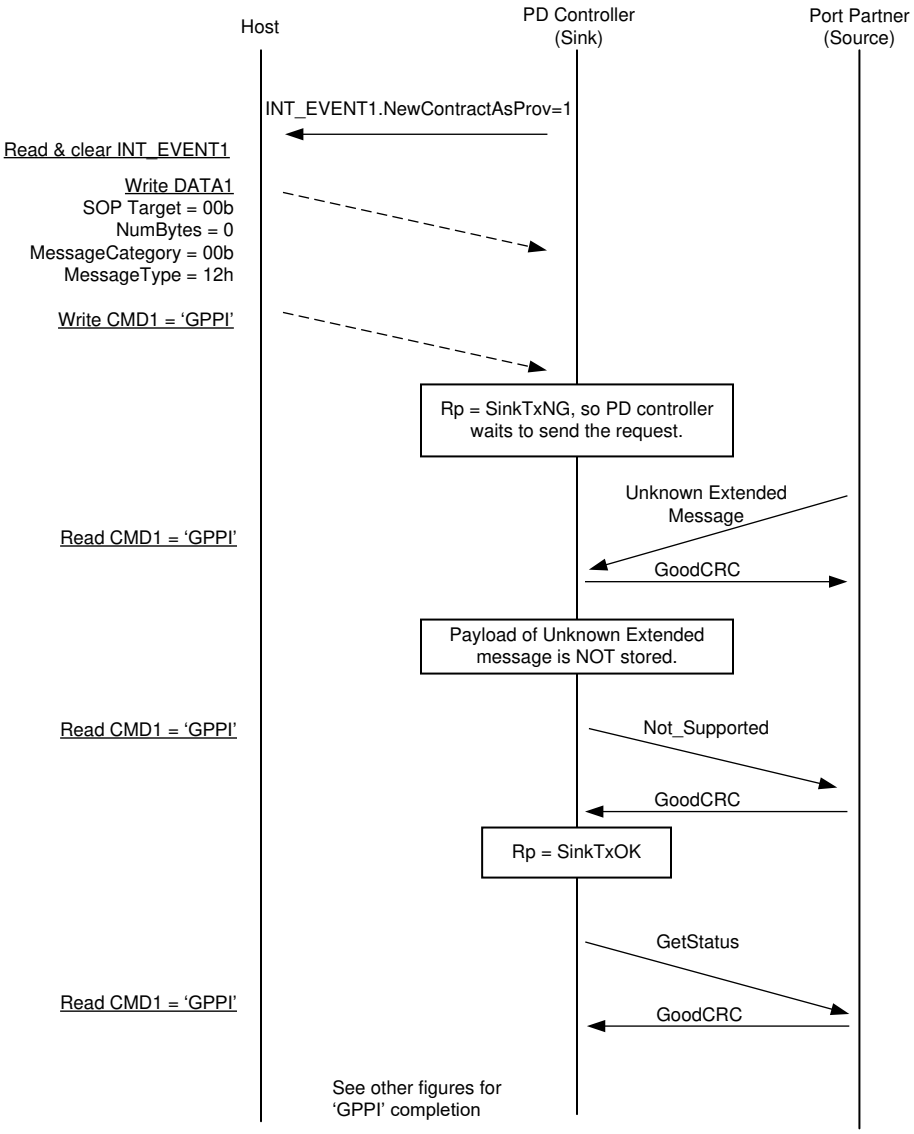


Figure 7-3. 'GPPI' Interrupted by an Unknown Message

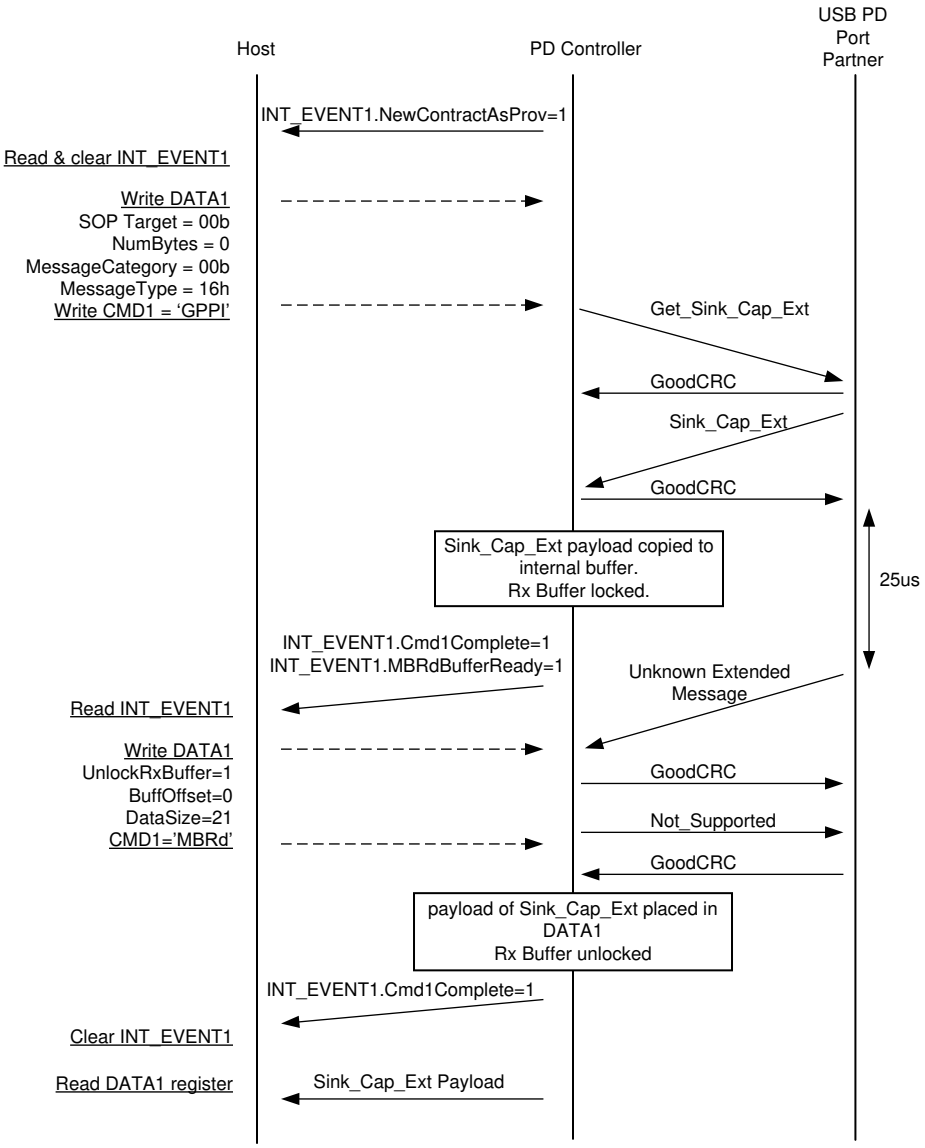


Figure 7-4. 'GPPI' Interrupted by an Unknown Extended Message

7.3.6 'MBRd' - Message Buffer Read

Table 7-9. 'MBRd' - Read from PD message buffer.

Description	**The MBRd Task instructs the PD Controller to read data from the extended message buffer previously received from the Port Partner.**			
INPUT DATAX	**Bit**	**Name**	**Description**	
	23	Reserved	Reserved (Write as 0).	
	22	UnlockRxBuffer	This input controls whether or not the PD controller unlocks its internal buffer after this Task is completed. It is recommended to unlock the internal buffer as soon as possible to make room for other incoming messages. It is important that the host only set this bit to 1 after it has received an alert that the Rx Buffer is locked (that is INT_EVENTx.MBRdBufferReady asserted).	
			0b	Do not clear the internal buffer, another 'MBRd' Task can be used later.
			1b	Clear the internal buffer after this Task completes and the requested data is in the DATAx register.
	21:16	DataSize	Number of data bytes to be read in from the message buffer. Up to 62 bytes can be read at after.	
	15:0	BuffOffset	Buffer Offset. Values 0 to 259 are possible.	
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	511:16	DataByte1	First Byte of data read at BuffOffset.	
	15:0	MessageSize	Size of message in bytes.	
Task Completion	The MBRd Task completes after buffer data of DataSize at BuffOffset has been read from the message buffer.			
Side Effects	None			
Additional Information	This Task is required for the host to obtain the information from the response due to the usage of the 'GPPI' Task . The PD controller has a single buffer per port that is shared for these messages.			

7.4 Patch Bundle Update Tasks

The following tasks are used for updating a Patch Bundle.

7.4.1 'PBMs' - Start Patch Burst Mode Download Sequence

Table 7-10. 'PBMs' - Start Patch Burst Download Sequence

Description	**The 'PBMs' Task starts the patch loading sequence. This Task initializes the firmware in preparation for a patch bundle load sequence and indicates what the patch bundle will contain.**			
INPUT DATAX	**Bit**	**Name**	**Description**	
	Byte 6: Burst Mode Timeout			
	7:6	Reserved		
	5:0	Timeout value	Timeout value for this task. A non-zero value must be used, it is recommended to always use 0x32 in this field (5 seconds) (LSB of 100ms).	
	Byte 5: I2C target for downloading patch.			
	7	Reserved		
	6:0	I2C Target Address	The following target addresses are not valid: • 0x00 • The I2Ct target address of any port selected using the ADCINx pins. Refer to data-sheet.	
	Bytes 0-3: Low Region Binary bundle size in of bytes: [Byte3, Byte2, Byte1, Byte0]			
	31:24	Byte3 of bundle size		
	23:16	Byte2 of bundle size		
	15:8	Byte1 of bundle size		
	7:0	Byte0 of bundle size		
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	7:0	PatchStartStatus	Status of the patch start.	
			0x00	Patch start success
			0x04	Invalid bundle size
			0x05	Invalid target address
			0x06	Invalid Timeout value
Task Completion	The 'PBMs' Task completes after output has a valid PatchStartStatus. If MODE register (0x03) is equal to 'APP ', then this Task will be rejected.			
Side Effects	When the 'PBMs' is successful, the second target address will be set to the input value.			
Additional Information	The host can only issue a 'PBMs' Task to the I2Ct port of the PD controller. If the host issues 'PMBs' a second time, then the PD controller ignores the DATAX input, restarts the burst-mode timer, and resets the pointer to the beginning of the patch space in RAM. If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMs' Task.			

7.4.2 'PBMc' - Patch Burst Mode Download Complete

Table 7-11. 'PBMc' - Patch Burst Download Complete

Description	The 'PBMc' Task ends the patch loading sequence. Send this Task after all patch data has been transferred. This Task will initiate the CRC check on the binary patch data that has been transferred, and if the CRC is successful, the patch_init function contained within the patch will be executed.			
INPUT DATAX	None			
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	319:288	acCalculatedCRC	The CRC calculated in FW for the configuration data.	
	287:256	acTransferredCRC	The CRC transferred along with the configuration data	
	255:240	Reserved	reads as 0	
	239:224	acIndicatedDataSize	The indicated DataSize in the transferred configuration data.	
	223:216	acHeaderVersion	The indicated header version in the transferred configuration data.	
	215:208	acFailCode	An error code indicating why the app config data failed to apply, if it failed to apply	
			0x00	AC_FAIL_NONE: No failure
			0x01	AC_FAIL_WRONG_HEADER_VERSION: The header version is expected to be 1 and was not
			0x02	AC_FAIL_TOO_MUCH_DATA: The DataSize field indicates that you are trying to load more configuration data that there is allocated SRAM for
			0x03	AC_FAIL_CRC_CHECK_FAIL: The CRC comparison failed
	207:200	acState	The current internal state of the AppConfig state machine	
			0x00	AC_NODATA: No configuration data found yet, because we haven't started looking
			0x01	AC_LOADING_DEFAULT: Attempting to load configuration data from a factory default
			0x02	AC_LOADING_SRAM: Attempting to load configuration data from SRAM
			0x03	AC_LOADING_FLASH: Attempting to load configuration data from Flash
			0x04	AC_LOADING_I2C: Attempting to load configuration data from I2C
			0x05	AC_LOADING_DONE: Done loading configuration data, we found valid data
			0x06	AC_ERROR: A generic error state
			0x07	AC_DONE_SUCCESS: Completely done with the app customization process and the records were applied successfully.
			0x08	AC_DONE_FAIL: Completely done with the app customization process and the records were not applied
	199:192	configBundleGood	1 if the top-level state machine found a valid configuration bundle, otherwise 0.	
	191:160	rpRomVersionExpected	The romVersionExpected in the transferred bundle's patch header	
	159:144	rpBundleTotalSize	The bundleTotalSize in the transferred bundle's patch header	
	143:128	rpBundleFlags	The bundleFlags in the transferred bundle's patch header	
	127:96	rpPatchBodyCrc	The patchBodyCrc in the transferred bundle's patch header	
	95:64	rpPatchHeaderCrc	The patchHeaderCrc in the transferred bundle's patch header	

Table 7-11. 'PBMc' - Patch Burst Download Complete (continued)

Description	**The 'PBMc' Task ends the patch loading sequence. Send this Task after all patch data has been transferred. This Task will initiate the CRC check on the binary patch data that has been transferred, and if the CRC is successful, the patch_init function contained within the patch will be executed.**			
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	63:48	rpBundleSignature	The bundleSignature in the transferred bundle's patch header	
	47:40	rpState	The current internal state of the RomPatch state machine.	
			0x00	RP_NOPATCH: No patch has been loaded
			0x01	RP_LOADING: In the process of loading patch data
			0x02	RP_LOADINGDONE: All patch data has been received
			0x03	RP_RUNNING: A patch has been loaded and is running. Could also indicate that a NULL patch is active.
			0x04	RP_EARLYLOAD_SKIPPED: Indicates that the early boot process does not need to wait for a patch over I2C
			0x05	RP_UARTBOOTED: Checking for a patch in RAM
			0x06	RP_ERROR: A generic error state
	39:32	patchBundleGood	0x01 if the top-level state machine found a good ROM patch, otherwise 0x00.	
	31:24	AppConfigPatchCompleteStatus	0x00	
			0x40	Warning
			0x80	Failure
	23:16	DevicePatchCompleteStatus	A return code indicating whether the RomPatch state machine executed successfully. This value is always valid, and reflective of the internal state of the RomPatch mechanism, but must only be considered if the bundle transferred did in fact include patch data.	
			0x00	Success
			0x20	Not ready
			0x40	Not a patch
			0x41	Patch header checksum mismatch
			0x42	Patch not compatible with this version of ROM
			0x43	Patch code checksum mismatch
			0x44	Null patch received
			0x45	Error patch received
	15:8	cpReturn	Always returns success, there is no way for it to fail.	
	Byte 1: Return Code			
	7:4	rpReturnIndicator	The most significant nibble of the rpReturn value.	
			0x0	Success
			0x2	Informational
			0x4	Warning
			0x8	Error
	3:0	acReturnIndicator	The most significant nibble of the acReturn value.	
			0x0	Success
			0x2	Informational
			0x4	Warning
			0x8	Error
Task Completion	The 'PBMc' Task completes if output has a valid DevicePatchCompleteStatus and AppConfigPatchCompleteStatus. This Task is rejected if the DATAX input for the 'PBMs' command does not contain the total patch size. If MODE register (0x03) is equal to 'APP ', then this Task will be rejected. When this task is rejected the task returns the *Standard Task Response*.			
Side Effects	Before this Task completes it will change the I2C target address from the patch address back to the normal value. Upon successful completion of this Task the PD controller will change the MODE register (0x03) to 'APP ' and move to the application mode.			

Table 7-11. 'PBMc' - Patch Burst Download Complete (continued)

Description	**The 'PBMc' Task ends the patch loading sequence. Send this Task after all patch data has been transferred. This Task will initiate the CRC check on the binary patch data that has been transferred, and if the CRC is successful, the patch_init function contained within the patch will be executed.**
Additional Information	When the CMD1 register goes to 0 check the Output DATAX register for status. If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMc' Task.

7.4.3 'PBMe' - End Patch Burst Mode Download Sequence

Table 7-12. 'PBMe' - Patch Burst Mode Exit

Description	The 'PBMe' Task ends the patch loading sequence. This Task instructs the PD controller to complete the patch loading process.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code.
Task Completion	The 'PBMe' Task completes after it has ended the patch loading sequence. If MODE register (0x03) is equal to 'APP ', then this Task will be rejected.
Side Effects	When the 'PBMe' is successful, the second target address will be restored to the value configured by the ADCINx pins. The PD controller leaves the MODE register (0x03) as 'PTCH' and will wait for the patching process to restart.
Additional Information	If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMe' Task.

7.4.4 'FLrd' - Flash Memory Read

Table 7-13. 'FLrd' - External EEPROM Read

Description	**The 'FLrd' Task reads the flash at the specified address.**		
INPUT DATAX	**Bit**	**Name**	**Description**
	31:0	Flash Address	Flash Address
OUTPUT DATAX	**Bit**	**Name**	**Description**
	127:0	Memory Contents	Memory contents (little-endian).
Task Completion	The 'FLrd' Task completes after selected memory locations are loaded.		
Side Effects	The PD controller ignores the I2Cc_IRQ pin until this Task is completed.		
Additional Information	None		

7.4.5 'FLad' - Flash Memory Write Start Address

Table 7-14. 'FLad' - External EEPROM Start Address

Description	**The 'FLad' Task sets start address in preparation the flash write.**		
INPUT DATAX	**Bit**	**Name**	**Description**
	31:0	Flash Address	Flash address (treated as 32-bit little-endian value).
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 7-1.		
Task Completion	The 'FLad' Task completes after selected memory address is loaded.		
Side Effects	The PD controller ignores the I2Cc_IRQ pin until this Task is completed.		
Additional Information	None		

7.4.6 'FLwd' - Flash Memory Write

Table 7-15. 'FLwd' - External EEPROM Memory Write

Description	**The 'FLwd' Task writes data beginning at the flash start address defined by the 'FLad' Task. The address is auto-incremented.**			
INPUT DATAX	**Bit**	**Name**	**Description**	
	511:0	Flash Address	Up to 32 bytes of flash data.	
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	7:0	ReturnCode	Status of write.	
			0x00h	Flash memory write successful
			0xFFh	Error, flash is busy
Task Completion	The 'FLwd' Task completes after selected the flash is written.			
Side Effects	The PD controller ignores the I2Cc_IRQ pin until this Task is completed.			
Additional Information	None			

7.4.7 'FLvy' - Flash Memory Verify

Table 7-16. 'FLvy' - External EEPROM Verify

Description	**The 'FLvy' Task verifies if the patch/configuration is valid.**			
INPUT DATAX	**Bit**	**Name**	**Description**	
	31:0	Flash Address	Flash Address	
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	7:0	ReturnCode		
			0x00h	The patch/configuration is valid.
			0x01h	The patch/configuration is not valid.
Task Completion	The 'FLvy' Task completes after header is checked and validated.			
Side Effects	The PD controller ignores the I2Cc_IRQ pin until this Task is completed.			
Additional Information	None			

7.5 System Tasks

7.5.1 'I2Cr' - I2C Read Transaction

Table 7-17. 'I2Cr' - Executes I2C Read Transaction on I2Cc

Description	**The 'I2Cr' task can be used to cause the PD controller to read from a specified target address and register offset using a I^2C read transaction through the I2Cc_SDA and I2Cc_SCL pins.**		
INPUT DATAX	**Bit**	**Name**	**Description**
	Byte 3: Number of bytes to read from the target.		
	7:0	NumBytes	
	Byte 2: Register offset to use in the I2C read transaction.		
	7:0	RegisterOffset	
	Byte 1: Target Address		
	7	Reserved	
	6:0	Target to use for the transaction.	
OUTPUT DATAX	**Bit**	**Name**	**Description**
	Bytes 2-65: Data Bytes read from the target (in order received)		
	511:0	Data	
	Byte 1: Standard Task Return Code. See also Table 7-1.		
Task Completion	The PD controller completes after it has successfully read the specified number of bytes, or the I^2C transaction terminated for some other reason.		
Side Effects	This task causes the PD controller to issue a command on the I2Cc port. It can result in INT_EVENTx.I2CControllerNACKed being asserted.		
Additional Information	The 'I2Cr' command cannot be sent within 150ms from sending a previous 'I2Cr' command. This allows the PD controller to complete all I2C transactions.		

7.5.2 'I2Cw' - I2C Write Transaction

Table 7-18. 'I2Cw' - Executes I2C Write Transaction on I2Cc

Description	**The 'I2Cw' task can be used to cause the PD controller to write a particular I^2C transaction using I2Cc_SDA and I2Cc_SCL.**		
INPUT DATAX	**Bit**	**Name**	**Description**
	Bytes 4-14: Payload for the I2C transaction		
	Byte 3: Register Offset for the I2C transaction		
	7:0	Register offset	
	Bytes 2: Length		
	7:0	Number of bytes in the transaction payload.	
	Byte 1: Target Address		
	7	Reserved	
	6:0	Target to use for the transaction.	
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 7-1.		
Task Completion	The PD controller maintains a queue of transactions to send on the I2Cc port. If the PD controller has been configured to send transactions upon certain events, it is possible there is a transaction in the queue when the 'I2Cw' task is received. In that case the task will complete successfully after the transaction is inserted into the queue. If the PD controller fails to insert the task into the queue for any reason, the task is rejected. Therefore, when this task is completed successfully it does not guarantee that the I2C transaction is complete. If possible, the host must use the 'I2Cr' 4CC task to confirm the write was successful.		
Side Effects	When successful, this task will cause the PD controller to issue a command on the I2Cc port. This can result in INT_EVENTx.I2CControllerNACKed being asserted.		
Additional Information	If the DATAX register is written with more than 14 bytes, all bytes beyond byte 14 are ignored. The PD controller has a limit on the maximum length of the I^2C write transaction.		

7.5.3 'GPsh' - set GPIO high

Table 7-19. 'GPsh' - GPIO set output high

Description	This Task sets the selected GPIO pin output to logic high.		
INPUT DATAX	**Bit**	**Name**	**Description**
	Byte 1: GPIO number		
	7:0	GPIOnum	GPIO number, check device data-sheet for available GPIO's. For example, GPIOnum = 0 corresponds to GPIO0.
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 7-1.		
Task Completion	The ‘GPsh’ Task completes after the new GPIO value is committed to the GPIO register.		
Side Effects	There are many possible expected or unexpected side effects of changing the PD Controller’s GPIOs manually. GPIOs that are connected to PD Controller GPIO Events can not behave properly if they are modified by the ‘GPIO’ Command. Extreme care must be taken with the use of this Task.		
Additional Information	GPIOs must be configured as an ouptut in the AppConfig for the 'GPsh' to work. Use the "Output Enable" field to set the GPIO to be an output pin. Use the "Initial Value" field to set the initial value.		

7.5.4 'GPsl' - set GPIO low

Table 7-20. 'GPsl' - GPIO set output low

Description	This Task sets the selected GPIO pin output to logic low.		
INPUT DATAX	**Bit**	**Name**	**Description**
	Byte 1: GPIO number		
	7:0	GPIOnum	GPIO number, check device data-sheet for available GPIO's. For example, GPIOnum = 0 corresponds to GPIO0.
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 7-1.		
Task Completion	The ‘GPsl’ Task completes after the new GPIO value is committed to the GPIO register.		
Side Effects	There are many possible expected or unexpected side effects of changing the PD Controller’s GPIOs manually. GPIOs that are connected to PD Controller GPIO Events can not behave properly if they are modified by the ‘GPIO’ Command. Extreme care must be taken with the use of this Task.		
Additional Information	GPIOs must be configured as an ouptut in the AppConfig for the 'GPsl' to work. Use the "Output Enable" field to set the GPIO to be an output pin. Use the "Initial Value" field to set the initial value.		

8 User Reference

8.1 PD Controller Application Customization

The PD Controller application binary can be pushed over I2C using the I2Ct port, or the PD controller can read it from an external EEPROM at target address 0x50 on the I2Cc port. The PD Controller application binary provides a way to customize and initialize the settings of the PD Controller. It allows for any register bit accessible through the Host Interface to be changed *before* the PD Controller application starts normal operation, to configure system-related settings that must be correct before any application decision is made. TI provides a GUI tool to create the PD Controller application binary.

8.2 Loading a Patch Bundle

The patch bundle can contain Application Customization data and a Patch binary that modifies the default application firmware in the PD controller. This section will describe how the host can load the patch bundle. The host uses the I2Ct bus for all transactions related to loading the patch bundle. As noted in the flow diagram below, the I2C target address varies depending upon which mode the PD controller is in. The Patch Burst Mode allows the host to push the Patch Bundle to multiple PD controllers simultaneously.

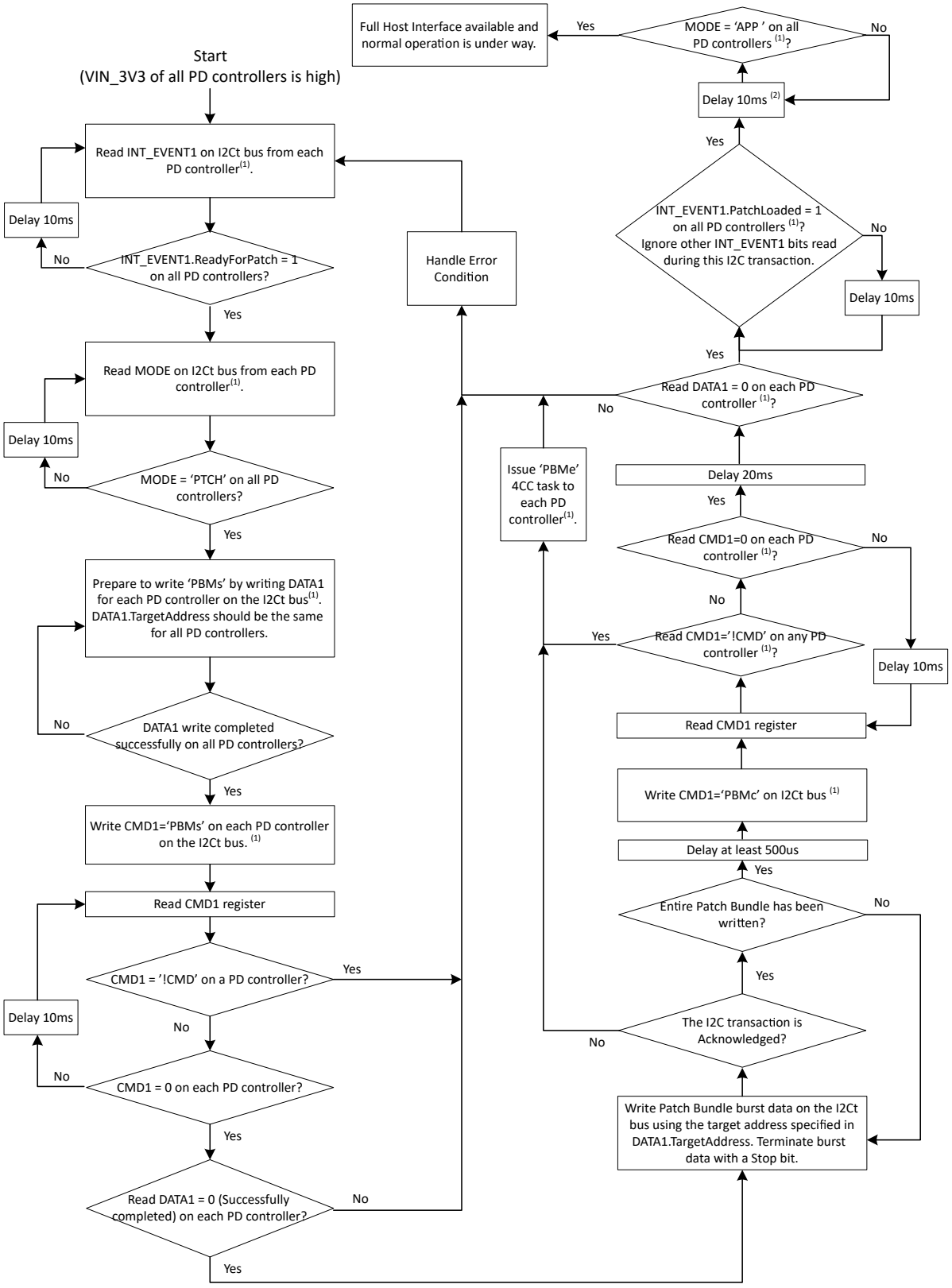
The following flow diagram illustrates the normal successful patch loading process. Other error handling steps can be necessary depending upon the nature of the errors encountered for a particular system. The EC can reset and restart the patch process by issuing a 'PBMe' 4CC Task.

The following table summarizes the target addresses in the different modes of operation.

Table 8-1. Use of Target Addresses During Different Modes of Operation

MODE Register Read-Back Value	I2Ct
	Target Address 1
'BOOT'	As configured by ADCINx pins. This is the "Fundamental" I2C target address. BOOT indicates that the PD controller is in the boot stage due to a bad firmware image or incorrect ADCINx settings. APP indicates that the firmware has successfully loaded and is in normal operation. PTCH indicates that the PD controller is waiting for a patch or is in the patch process using the PBMx commands.
'PTCH'(1)	
'APP '(2)	

(1) A successful 'PBMs' Task puts the PD controller into the 'PTCH' mode.
(2) A successful 'PBMc' Task puts the PD controller into the 'APP ' mode.



(1) Use the fundamental I2C target address of each PD controller.
(2) This delay before reading the MODE register, is optional but recommended.

Figure 8-1. Flow for Pushing a Patch Bundle Over the I2Ct Bus to Multiple PD Controllers at the Same Time

While the host is writing the Patch Bundle burst data, the I2C protocol in the following figure must be followed. The host can send the entire Patch Bundle in a single I2C transaction, or it can break it up into multiple transactions. The PD controller increments the pointer into its patch memory space with each byte received on the Patch Target address that was configured by DATA1.TargetAddress as part of the 'PBMs' 4CC Task. The EC can re-issue a 'PBMs' 4CC Task or it can issue a 'PBMe' 4CC Task in order to reset the pointer.

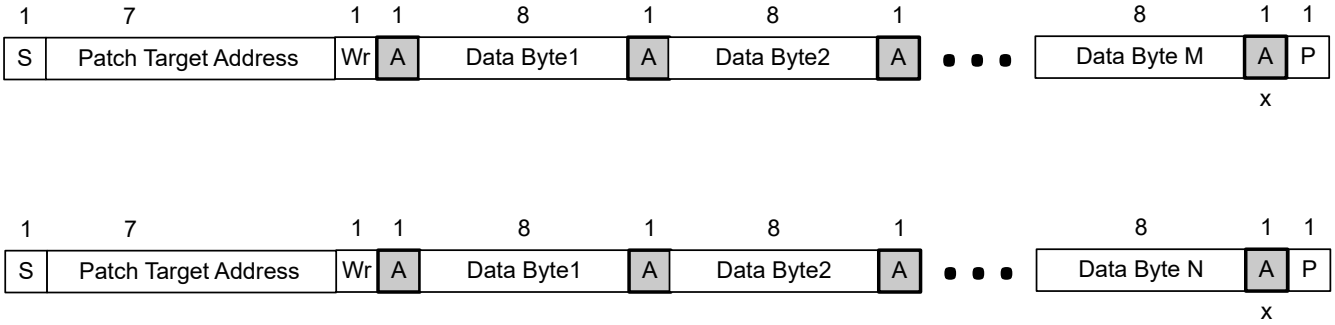
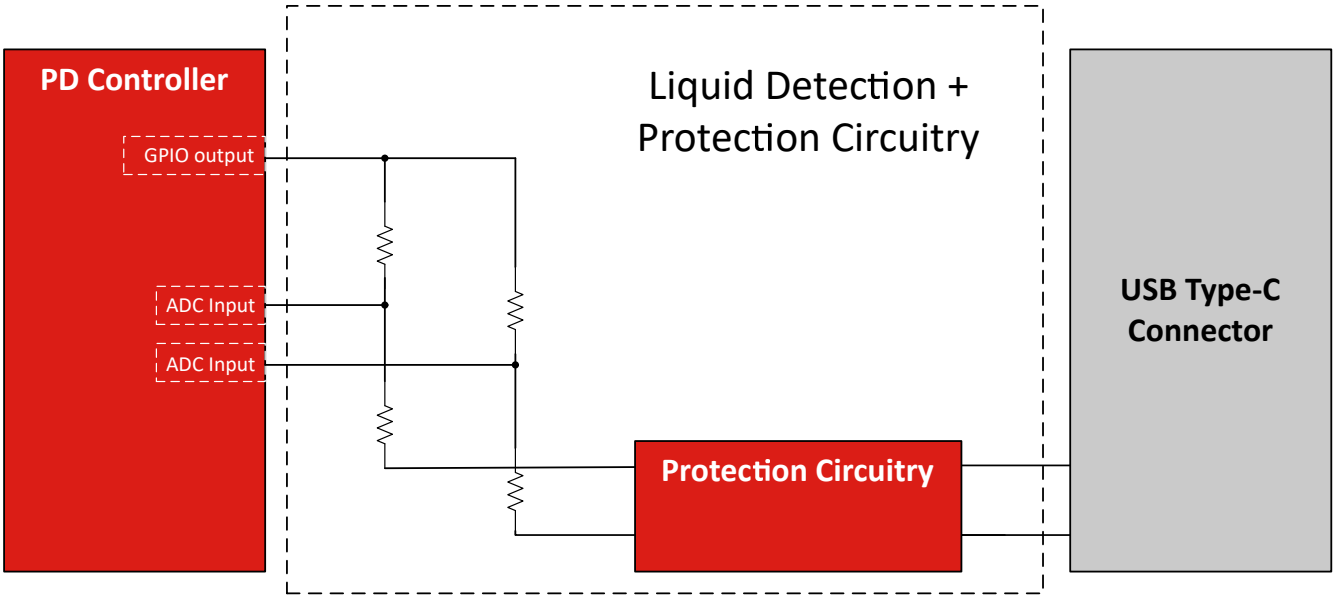


Figure 8-2. Protocol of Patch Bundle Burst Data Assuming it is Broken Into Two Transactions

8.3 Liquid Detection Registers

Liquid detection control and status are contained in registers which can be read in the host interface. Settings for the liquid detection algorithm are changed when the algorithm is not running and remain static static when the algorithm is active. Liquid detection is run when the device is unattached and when the device is attached per user config. When the device is unattached and running liquid detection, the device runs liquid detection in active mode between sleep cycles and then returns to a lower power sleep mode if no liquid is detected.

The liquid detection external circuity is connected to LD1/LD2 for sensing the voltage differential on the ADC pins and a GPIO must be connected to the external circuit. The circuit is hooked up to pins from the USB Type-C Connector and can be used with used or unused pairs of signals, as well as a single signal.



The liquid detection configuration register (0x98) is used to configure and run the liquid detection algorithm. The liquid detection status register (0xb2) is used to monitor the status of the liquid detection algorithm and read any status updates that occur.

The algorithm drives the external circuit to VDD and GND to sense if the pins on the connector have been shorted to VBUS or GND. The sensing is done on two ADC input signals and an average is taken of the measurements to maintain accurate measurements. If a pin is shorted to a voltage that trips the OVP in T

The algorithm handles liquid detection and corrosion mitigation. In dead battery mode, corrosion mitigation is not allowed. To allow for corrosion mitigation, clear the dead battery flag. Corrosion mitigation sets the Type-C state machine into the Error Recoery state, where the CC terminations are set to Hi-Z. To remove this condition, the device must no longer sense liquid on the pins.

To configure the device for liquid detection, write to the following register fields:

Table 8-2. Liquid Detection Register 0x98 Field Parameters

Field Name	Field Location	Field Value
Wait Time in Seconds - Non-Liquid State	7:0	0xA
Wait Time in Seconds - Liquid State	15:8	0xA
Sample Time in 10ms - Non-Liquid State	19:16	0x1
Sample Time in 10ms - Liquid State	23:20	0x1
Liquid Detection Retries Wait Time in 100ms	27:24	0
Liquid Detection Retries	31:28	0
Number of Samples	39:32	3
Short to VDD Detection Threshold - Non-Liquid State	47:40	0x8f
Short to GND Detection Threshold - Non-Liquid State	55:48	0x24
Short to VDD Detection Threshold - Liquid State	63:56	0x8f
Short to GND Detection Threshold - Liquid State	71:64	0x24
Enable Liquid Detection	72	1
Enable Corrosion Mitigation	73	1
Monitor During Attach	74	1
Monitor During Unattach	75	1
Liquid Pins to Monitor	77:76	0

8.4 GPIO Events

Table 8-3. GPIO Events

Event #	Event Name	I/O	Description
161	DebugAccessoryAndButtonPressActive	Output	GPIO is asserted high high when USB-C Debug Accessory Mode (DAM) is detected AND ButtonPressSwitch input even is low.
160	ButtonPressSwitch	Input	This event transitions based on a button press in the system. When the event is low, it impacts DebugAccessoryAndButtonPressActive.
159	InputInterrupt	Input	When input is driven low, the PD device stores an input for reading.
157	LiquidDetected	Output	GPIO is asserted when liquid is detected on the SBU1/2 pins. When liquid is no longer detected on the SBU1/2 pins the GPIO will be de-asserted.
155	LiquidCircuitryControl	Output	GPIO used to drive control voltage to the external liquid detection circuit. The GPIO will toggle during liquid detection.
146	PPHVDisable	Input	When set low by the system, PD controller disables the PPHV switch but maintains the PD contract. When transitions to high, PPHV switch will be closed if active PD contract is present.

Table 8-3. GPIO Events (continued)

Event #	Event Name	I/O	Description
131	EXTDCDC_IRQ	Input	GPIO event is driven to notify there has been an update in the external DCDC or BQ device. The I2C event External DCDC event received is enabled to send an I2C interrupt to the MCU. The 4CC command I2Cr is sent from the microcontroller to read the contents of the external device.
76	PdNegotiationInProcess	Output	When in source mode, this GPIO is asserted after a Request message is received, before sending the Accept message. The GPIO is de-asserted after the PS_RDY message is sent. When in sink mode, this GPIO is asserted right before sending a Request message, and de-asserted after a PS_RDY message is received. In either mode, the GPIO is de-asserted when a detach occurs.
73	EnableSource	Output	PD controller will assert this GPIO when acting as a source (implicit or explicit contract)
65	Load_Switch_Drive	Output	When the PD controller enables the PP_EXT1 sinking path, it will pull the selected GPIO low to enable a load-switch. When the PD controller disables the PP_EXT1 sinking path, it will drive the selected GPIO high.
61	Dp_Dm_Mux_Enable_Event	Output	This GPIO must be used to enable/disable a USB 2.0 D+/D- mux. The GPIO is driven high upon connection, and low upon disconnect on the port.
50	Debug_Accessory_Mode_Event	Output	Output: This GPIO is asserted high when a Debug Accessory is attached on the port.
45	Prevent_DRSwap_To_UFP_Event	Input	When the GPIO is high, the PD controller will reject any DR_Swap messages from the Port Partner requesting to change the data-role from DFP to UFP.
44	UFP_Indicator_Event	Output	The GPIO is driven high when the data role of any port in the PD controller is UFP.
35	Fault_Condition_Active_Low_Event	Output	Asserts low on an overcurrent event on the port.
33	Fault_Input_Event	Input	When set low by the system, the port enters the Type-C Error Recovery State. When set high, no action is taken.
29	UFP_DFP_Event	Output	Output: Asserted high when the port is operating as UFP. Asserted low when port is operating as DFP.
13	SourcePDOContractBit2	Output	Output: Bit2 of binary encoded outputs indicating when a Source PDO1 through PDO7 on the port has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
12	SourcePDOContractBit1	Output	Output: Bit1 of binary encoded outputs indicating when a Source PDO1 through PDO7 on the port has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
11	SourcePDOContractBit0	Output	Output: Bit0 of binary encoded outputs indicating when a Source PDO1 through PDO7 on the port has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
10	SourcePDO4Contract	Output	Output: Asserted high when a Source PDO4 on the port has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO4 has been negotiated.
9	SourcePDO3Contract	Output	Output: Asserted high when a Source PDO3 on the port has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO3 has been negotiated.
8	SourcePDO2Contract	Output	Output: Asserted high when a Source PDO2 on the port has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO2 has been negotiated.

Table 8-3. GPIO Events (continued)

Event #	Event Name	I/O	Description
7	SourcePDO1Contract	Output	Output: Asserted high when a Source PDO1 on the port has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO1 has been negotiated.
3	Cable_Orientation_Event	Output	Output: Indicates the plug orientation on the port. Low when the plug is connected upside-up (CC1 connected to CC in cable) or disconnected. High when plug is connected upside-down (CC2 connected to CC in cable).
1	PlugEvent	Output	Output: Asserted high when plug event (attached state) has occurred on the port, otherwise low.
0	NullEvent	NA	No event associated with this GPIO.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from April 30, 2026 to August 30, 2026 (from Revision * (April 2026) to Revision A (August 2026)) **Page**

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025