LMG5126 Evaluation Module



Description

The LMG5126EVM evaluation module showcases the features and performance of the LMG5126 wide input voltage synchronous GaN boost converter. This EVM is designed for ease of configuration, enabling the user to evaluate many different applications on the same module. The standard configuration is designed to provide a regulated output voltage of 24V and switching at 400kHz. The output voltage can be dynamically adjusted using the ATRK, DTRK pin.

Get Started

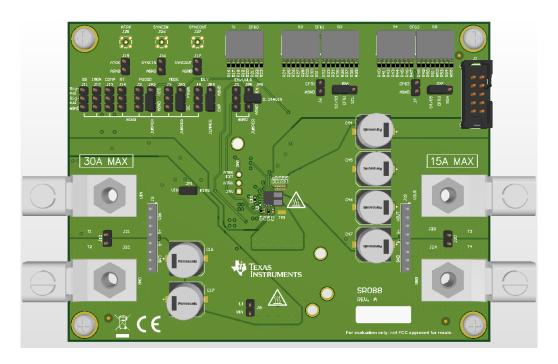
1. Connect EVM to power supply and load

Features

- Stackable
- · Output voltage tracking
- Wide input voltage range
- Inductor current monitoring and average current limit
- Bypass mode, PGOOD indicator, and Dual Random Spread Spectrum (DRSS)
- · Soft-start and peak current limit
- Optional synchronization (SYNC)
- Programmable line undervoltage lockout (UVLO) and hysteresis

Applications

- Automotive Class H audio power amplifier
- · Automotive LED headlight



Evaluation Module Overview www.ti.com

1 Evaluation Module Overview

1.1 Introduction

The LMG5126EVM evaluation module provides the design engineer with a fully functional synchronous boost converter to evaluate the LMG5126 synchronous GaN boost converter. The EVM operates over an input voltage range of 8V to 18V and can handle input transients up to 42V. The EVM provides an output voltage of 24V with 240W maximum power. Using a heat sink can increase the maximum power up to 400W. The output voltage can also be adjusted up to 60V using the ATRK/DTRK pin. Figure 1-1 shows the standard application circuit for the LMG5126EVM evaluation module.

1.2 Kit Contents

- One LMG5126EVM PCB assembly
- · EVM Disclaimer Read Me

1.3 Specification

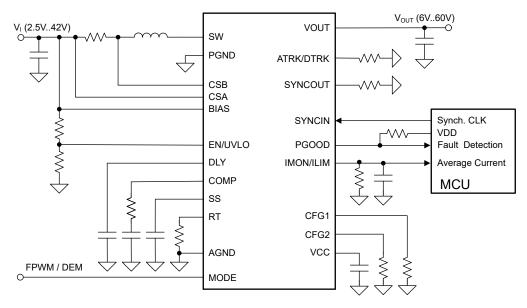


Figure 1-1. Typical Application Circuit

1.4 Device Information

The LMG5126 is a synchronous GaN boost converter. The device enters bypass mode when input voltage is higher than the desired output voltage.

- Wide input voltage range: 2.5V to 42V
- Output voltage: 6V to 60V
- Peak current regulation scheme
- · Dynamic output voltage tracking
 - Analog and digital PWM tracking input
- · Minimum quiescent current
 - Low shut down Iq of 50μA

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2 Hardware

2.1 EVM Characteristics, Test Point, and Connector Description

This section describes the operating conditions for the EVM, as well as the configuration points of the evaluation module.

2.1.1 EVM Characteristics

Table 2-1 details the EVM characteristics.

Table 2-1. EVM Characteristics

| Parameter | Test C | Test Condition | | | MAX | UNIT |
|----------------------|--|---|---|------|-------------------------|------|
| INPUT VOLTAGE CHARA | ACTERISITCS | | | | | |
| Input voltage range | Operation | | 8 | 14 | 18 | V |
| | UVLO voltage levels | Turn-on | | 4.2 | | V |
| | | Turn-off | | 3.2 | | V |
| Input current | No load operation V _{in} = 12V, V _{out} = 24V | | | 1.7 | | mA |
| OUTPUT CHARACTERIS | SITICS | 1 | | | | |
| Output voltage | $R_{ATRK} = 40.2k\Omega$ | | | 24 | | V |
| | $R_{ATRK} = 75k\Omega$ | | | 45 | | V |
| Output power | Vin=16V, JP4 Pin1-2 short feature deactivated) | Vin=16V, JP4 Pin1-2 shorted (average current limit feature deactivated) | | 240 | 400 (with heat sink) | W |
| SYSTEM CHARACTERIS | SITCS | <u>'</u> | | | | |
| Switching frequency | | | | 400 | | kHz |
| Full load efficiency | V _{IN} = 12V, V _{OUT} = 24V | | | 95.6 | | % |

2.1.2 EVM Connectors and Test Points

Section 2.1.2 describes the connection points of the evaluation module. Table 2-2 to Table 2-4 describe these connections. Table 2-2 lists the power connections of the evaluation module. These connections are intended to handle relatively large currents.

Table 2-2. Power Connections

| Connector | Pin | Description |
|-----------|-------|--|
| T1 | VIN+ | Positive input voltage power for the evaluation module |
| T2 | VIN- | Negative input voltage power for the evaluation module |
| Т3 | VOUT+ | Positive output voltage power for the evaluation module |
| T4 | VOUT- | Negative output voltage power for the evaluation module |
| J9 | VIN | Positive input voltage pin 1 - pin 3, negative input pin 6 - pin 8 (Pin 4 and 5 are only for sensing the input voltage) |
| J19 | VOUT | Positive output voltage pin 1 - pin 3, negative output pin 6 - pin 8 (Pin 4 and 5 are only for sensing the output voltage) |

Table 2-3 lists the EVM jumpers and test points that configure the LMG5126 and LMG51261 as desired. These jumpers can set different modes of operation or provide signals to different pins of the LMG5126 and LMG51261.

Table 2-3. Programmable Jumper Connections

| Connector | Pins | Description | Default Connection | | |
|---------------|-------------|---|--------------------|--|--|
| JP1 | BIAS to VIN | Connecting BIAS pin of LMG5126 to the VIN | Х | | |
| Pin1 to pin 2 | | Connecting PGOOD pin to the VCC enabling the power good indicator | × | | |
| | OPEN | If power good indicator is not used this pin can be left floating | | | |



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Table 2-3. Programmable Jumper Connections (continued)

| Connector | Pins | Description | Default Connection |
|-----------|----------------|--|--------------------|
| IDO | Pin 1 to pin 2 | Connecting MODE pin to VCC to enable FPWM mode | |
| JP3 | Pin 2 to Pin 3 | Connecting MODE pin to AGND to enable DEM | X |
| | Pin1 to pin 2 | Connecting DLY pin to a resistor to disable delay function and average current limit feature | |
| JP4 | Pin 2 to Pin 3 | Connecting DLY pin to a capacitor to enable delay function | Х |
| | Pin 2 to JP8 | Connecting DLY pin to GND to disable delay function and average current limit feature | |
| | Pin 1 to pin 2 | UVLO/EN Connected to VIN as VIN ramps up the UVLO/EN pin also ramps up and LMG5126 is enabled once the UVLO threshold is surpassed. | |
| JP5 | Pin 2 to pin 3 | Connects EN2 to AGND disabling LMG5126 | |
| | Pin 2 to JP9 | EN UVLO pin tied to resistor divider network consisting of R14, R15 and C51, where this resistor divider network sets the UVLO threshold for enabling LMG5126. | Х |
| JP6 | Pin 1 to Pin 2 | Uses DIP switches S2 and S3 for CFG1 settings | X |
| JPO | Pin 2 to Pin 3 | Sets CFG1 as I2C pin for I2C version | |
| JP7 | Pin 1 to pin 2 | Uses DIP switches S4 and S5 for CFG2 settings | Х |
| JF1 | Pin 2 to pin 3 | Sets CFG2 as I2C pin for I2C version | |
| JP8 | Pin 1 to pin 2 | Connecting ATRK to 40.2k resistor to set Vout to 24V | Х |
| JFO | Pin 2 to pin 3 | Connecting ATRK to J15 to supply from external | |
| J25 | MMCX jack | Digital PWM signal input to the ATRK/DTRK Pin | |
| J26 | MMCX jack | External syncing | |
| J27 | MMCX jack | External SYNCOUT | |

Table 2-4 indicates the dedicated voltage probe points of the EVM. These points are used to make measurements on the EVM.

Table 2-4. Probe Points

| Sense Point | Name | Description |
|-------------|------------|--|
| TP1 | SW | Sense point for switch node of the Boost converter |
| J1 | I2C | I2C measuring header with analog ground |
| J2 | PGOOD | Power Good measuring header with analog ground |
| J3 | MODE | MODE pin measuring header with analog ground |
| J4 | DLY | DLY pin measuring header with analog ground |
| J5 | UVLO | UVLO pin measuring header with analog ground |
| J6 | CFG1 | CFG1 pin measuring header with analog ground |
| J7 | CFG2 | CFG2 pin header with analog ground |
| J8 | CS | Terminals of the current sense resistors |
| J10 | Vin sense | Sense pins for the input voltage |
| J11 | SS | SS pin measuring header with analog ground |
| J12 | ILIM/IMON | ILIM/IMON pin header with analog ground |
| J13 | COMP | COMP pin header with analog ground |
| J14 | RT | RT pin header wit analog ground |
| J15 | ATRK | ATRK pin header with analog ground |
| J16 | SYNCIN | SYNCIN pin header with analog ground |
| J17 | SYNCOUT | SYNCOUT pin header with analog ground |
| J18 | PGND | Connection to PGND |
| J20 | Vout sense | Sense pins for the output voltage |

www.ti.com EVM Configurations

3 EVM Configurations

Section 3 shows modifications outside of the default configuration that are used to further evaluate the LMG5126.

3.1 Output Voltage Tracking

Section 3.1 describes how to setup the evaluation module for dynamic output voltage tracking.

The LMG5126EVM is typically configured to have fixed output voltage of 24V. Figure 3-1 shows the resistor from the ATRK, DTRK pin to the analog ground sets the output voltage to 24V. R_{ATRK} is R11 referring to the schematic.

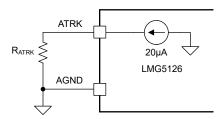


Figure 3-1. Fixed Output Voltage Configuration

To dynamically change the output voltage by analog signal, R_{ATRK} is removed and the ATRK, DTRK pin voltage is driven directly to change the output voltage. See the LMG5126 Wide-Input, 2.5MHz, Boost Converter data sheet for selecting the voltage range and setting the ATRK pin voltage to produce the desired output voltage. Figure 3-2 shows the configuration to change the output voltage dynamically by applying voltage or supplying analog signal.

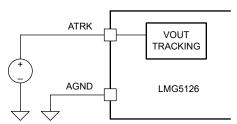


Figure 3-2. Variable Output Voltage Configuration via analog signal

Applying an analog voltage of around 0.8V and 1.5V to the ATRK, DTRK pin sets the output voltage of 24V and 45V respectively.

To dynamically change the output voltage digitally, R_{ATRK} is removed and the ATRK/DTRK pin is fed a PWM signal directly to change the output voltage. See the LMG5126 Wide-Input, 2.5MHz, Boost Converter data sheet for setting the PWM duty cycle of DTRK pin voltage to produce the desired output voltage. Figure 3-3 shows the configuration to change the output voltage dynamically by applying a digital signal.

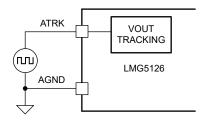


Figure 3-3. Variable Output Voltage Configuration via digital signal

Applying a PWM signal on the ATRK/DTRK pin with duty cycle of 32% and 60%, sets the output voltage to 24V and 45V, respectively.

EVM Configurations www.ti.com

3.2 Device Configuration

The LMG5126 can be configured using three pins SYNCOUT, CFG1 and CFG2. In the LMG5126EVM, these pins can be configured through the five DIP switches by selecting one of the 16 levels presented for each of the two configuration pins when the jumpers on connectors JP6 and JP7 are connecting CFG1 to DIP1 and CFG2 to DIP2, respectively. Each DIP switch has eight toggling switches that either connects or disconnects a fixed valued resistor from the configuration pins. At one time, there can be only one of the 16 levels, for each configuration pin, selected to configure the LMG5126 as seen below and according to the information given on the LMG5126 Wide-Input, 2.5MHz, Boost Converter data sheet.

The SYNCOUT-pin defines the overvoltage protection level and the ATRK, DTRK-pin 20uA current used for output voltage programming by resistor.

Table 3-1. SYNCOUT-Pin Settings

| 14510 0 11 0 1110 0 0 1 1 111 0 0 1111 9 0 | | | | | | |
|--|-------------------------|--|--|--|--|--|
| OVP level | 20μA ATRK current | | | | | |
| 25V | ON | | | | | |
| 25V | OFF | | | | | |
| 35V | ON | | | | | |
| 35V | OFF | | | | | |
| 50V | ON | | | | | |
| 50V | OFF | | | | | |
| 65V | ON | | | | | |
| 65V | OFF | | | | | |
| | 25V 25V 35V 35V 50V 65V | | | | | |

The CFG1-pin setting defines the clock dithering, the peak current limit (ICL_latch) operation, current sense voltage level and the gate driver strength.

Table 3-2. CFG1-Pin Settings

| Level | Spread Spectrum | Sense Voltage | ICL_ _{latch} | Gate Drive Strength |
|-------|-----------------|---------------|-----------------------|---------------------|
| 1 | DRSS ON | 30mV | Enabled | Weak |
| 2 | DRSS ON | 60mV | Enabled | Weak |
| 3 | DRSS ON | 30mV | Enabled | Strong |
| 4 | DRSS ON | 60mV | Enabled | Strong |
| 5 | DRSS ON | 30mV | Disabled | Weak |
| 6 | DRSS ON | 60mV | Disabled | Weak |
| 7 | DRSS ON | 30mV | Disabled | Strong |
| 8 | DRSS ON | 60mV | Disabled | Strong |
| 9 | DRSS OFF | 30mV | Enabled | Weak |
| 10 | DRSS OFF | 60mV | Enabled | Weak |
| 11 | DRSS OFF | 30mV | Enabled | Strong |
| 12 | DRSS OFF | 60mV | Enabled | Strong |
| 13 | DRSS OFF | 30mV | Disabled | Weak |
| 14 | DRSS OFF | 60mV | Disabled | Weak |
| 15 | DRSS OFF | 30mV | Disabled | Strong |
| 16 | DRSS OFF | 60mV | Disabled | Strong |

The CFG2-pin defines if the device is configured for a single-or multichip setup, which then defines the operation mode of SYNCIN and SYNCOUT pin. PGOOD OVP can also be set.

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Table 3-3. CFG2-Pin Settings

| Level | Single or Multichip | SYNCOUT | SYNCIN | PGOOD OVP Enable |
|-------|---------------------|---------|--------|------------------|
| 1 | Single | OFF | OFF | ON |
| 2 | Single | OFF | ON | ON |
| 3 | Primary | 90° | ON | ON |
| 4 | Primary | 120° | ON | ON |
| 5 | Primary | 180° | ON | ON |
| 6 | Secondary | OFF | ON | ON |
| 7 | Secondary | 90° | ON | ON |
| 8 | Secondary | 120° | ON | ON |
| 9 | Single | OFF | OFF | OFF |
| 10 | Single | OFF | ON | OFF |
| 11 | Primary | 90° | ON | OFF |
| 12 | Primary | 120° | ON | OFF |
| 13 | Primary | 180° | ON | OFF |
| 14 | Secondary | OFF | ON | OFF |
| 15 | Secondary | 90° | ON | OFF |
| 16 | Secondary | 120° | ON | OFF |

S1 through S5 are 8-bit DIP switches.

- S1 is for SYNCOUT
 - S1-position 1 selects level 1,..., S1-position 8 selects Level 8
- S2 and S3 are for CFG1
 - S2-position 1 selects level 1,..., S2-position 8 selects Level 8
 - S3-position 1 selects level 9,..., S3-position 8 selects Level 16
- S4 and S5 are for CFG2
 - S4-position 1 selects level 1,..., S4-position 8 selects Level 8
 - S5-position 1 selects level 9,..., S5-position 8 selects Level 16

Select position 7 for S1 by default to set level 7 for SYNCOUT:

- OVP level 65V
- 20uA ATRK current source ON

Select position 2 for S3 by default to set level 10 for CFG1:

- DRSS OFF
- Sense voltage = 60mV
- ICL latch enabled
- Gate driver strength: weak

Select position 1 for S4 by default to set level 1 for CFG2:

- Single chip operation
- SYNCOUT OFF
- SYNCIN OFF
- PGOOD OVP Enable ON

Implementation Results Www.ti.com

4 Implementation Results

4.1 Test Setup and Procedure

4.1.1 Test Setup

Figure 4-1 shows the required test setup to evaluate the LMG5126EVM



Figure 4-1. EVM Test Setup

4.1.2 Test Procedure and Equipment

The following test equipment is needed to test the LMG5126EVM:

- Power supply: the input voltage source (V_{IN}) is a variable supply. The power supply needs to be at least 20V
 and be able to supply more than 30A of current. Turn off the power supply. Connect the positive output of the
 power supply to T1 and the negative output to T2.
- Electronic load: connect the load to T3 for the positive connection and T4 for the negative connection. The electronic load needs to be able to dissipate 350W at 60V.

Multimeters: for DC measurements, connected as shown in Figure 6-1.

- Voltmeter 1 (V_{IN}): Capable of measuring the input voltage range up to at least 20V
 - Voltmeter 2 (V_{OLIT}): Capable of measuring output voltage of 60V
 - Ammeter 1 (I_{IN}): Capable of 30A DC measurement. A shunt resistor can also be used to measure the input current
 - Ammeter 2 (I_{OUT}): Capable of at least 15A DC measurement
- Oscilloscope: minimum of 20MHz bandwidth and 10x probes.
- Set the power supply voltage to 12V and the electronic load to 0.1A. The electronic load voltage must be in regulation with a nominal 24V output.
- Slowly increase the load while monitoring the output voltage between J23-VOUT and J24-GND. The voltage must remain in regulation with a nominal 24V output as the load is increased up to 7A.
- Slowly sweep the input voltage from 8V to 18V. The output voltage must remain in regulation with a nominal 24V output.
- Slowly sweep the input voltage from 18V to 8V. The output voltage must remain in regulation with a nominal 24V output.

4.1.3 Precautions





5 Application Curves

5.1 Efficiency

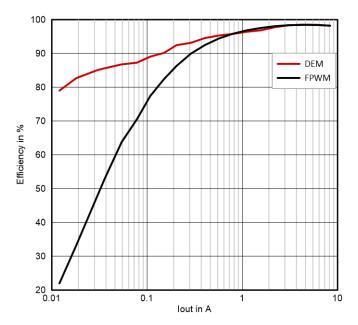


Figure 5-1. Efficiency vs. Output Current, Vin=14.4V, Vout=24V

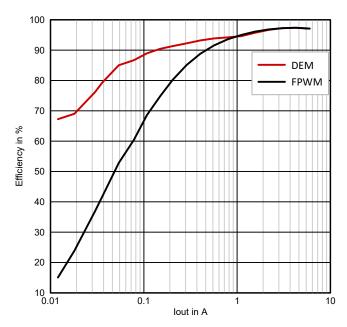


Figure 5-2. Efficiency vs. Output Current, Vin=14.4V, Vout=45V

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5.2 Steady State Waveforms



Figure 5-3. V_{in} = 14.4V, V_{out} = 24V, DEM, I_{load} = 0.1A

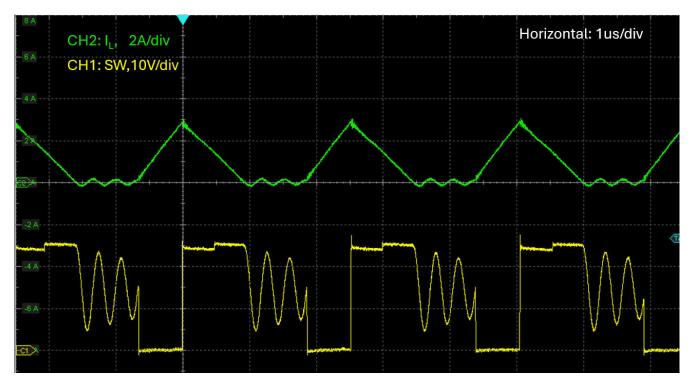


Figure 5-4. V_{in} = 14.4V, V_{out} = 24V, DEM, I_{load} = 0.5A

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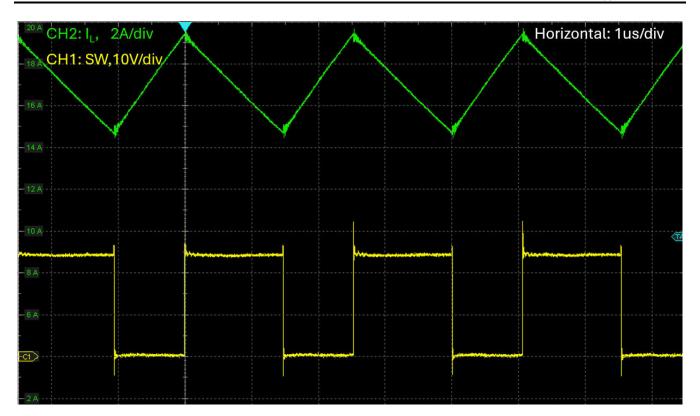


Figure 5-5. V_{in} = 14.4V, V_{out} = 24V, DEM, I_{load} = 10A



6 Hardware Design Files

6.1 Schematic

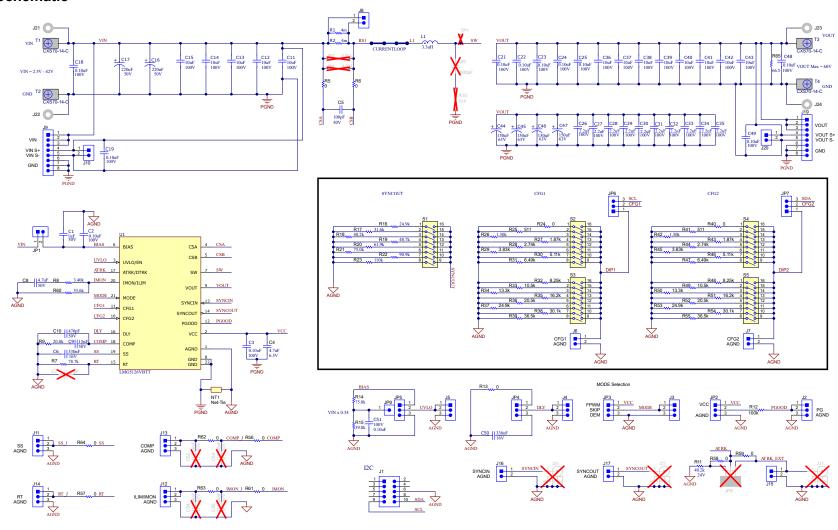


Figure 6-1. Schematic



6.2 PCB Layers

Figure 6-2 through Figure 6-3 illustrate the EVM PCB layout.

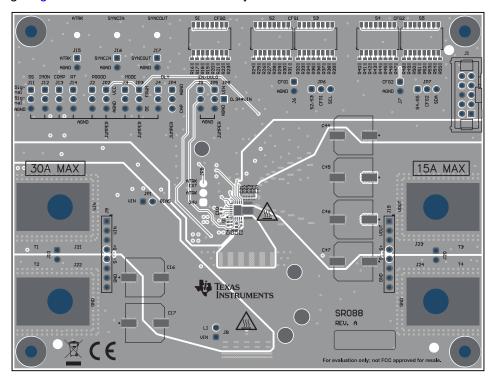


Figure 6-2. Top Silk Screen

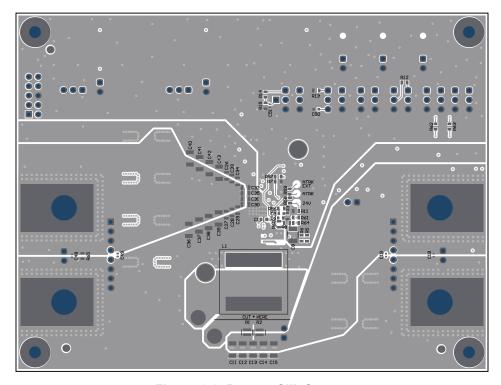


Figure 6-3. Bottom Silk Screen

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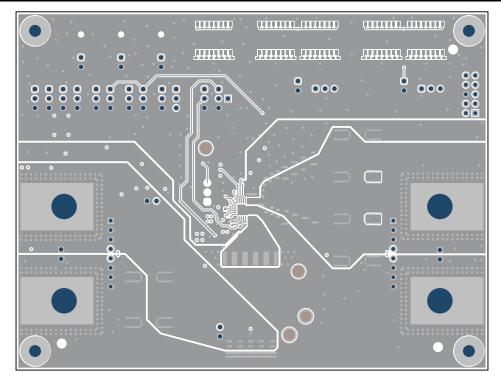


Figure 6-4. Top Layer

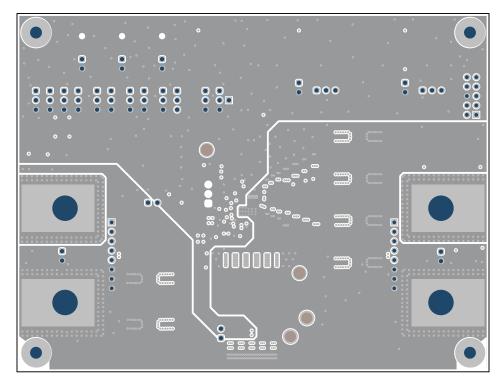


Figure 6-5. Signal Layer 1



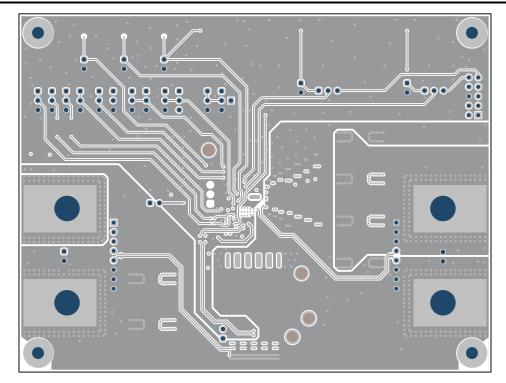


Figure 6-6. Signal Layer 2

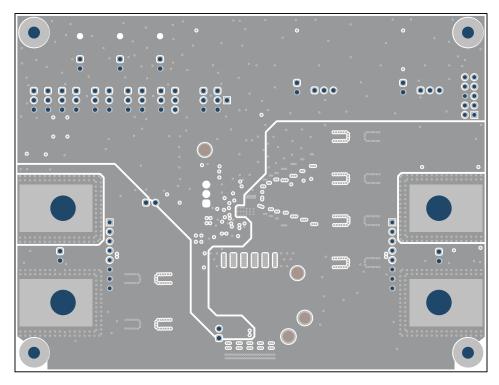


Figure 6-7. Signal Layer 3

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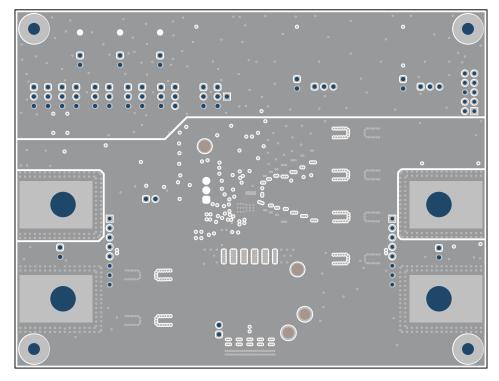


Figure 6-8. Signal Layer 4

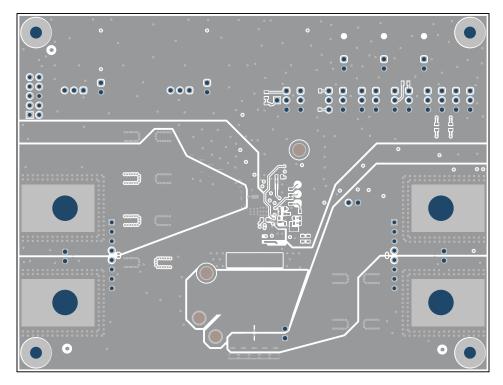


Figure 6-9. Bottom Layer

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6.3 Bill of Materials

Section 6.3 details the EVM bill of materials.

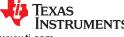
Table 6-1. Bill of Materials

| Designator | Quantity | Value | PartNumber | Manufacturer | Description |
|---|----------|-------|----------------------|--------------|--|
| C1 | 1 | 1μF | GCM188D71H105KE36J | Murata | 1 μF ±10% 50V Ceramic Capacitor X7T 0603 (1608 Metric) |
| C2, C3, C18, C19, C21, C22, C23, C24, C25, C48, C49, C51 | 12 | 100nF | GRM155R62A104ME14D | Murata | Chip Multilayer Ceramic Capacitors for General Purpose, 0402, 0.10uF, X5R, 15%, 20%, 100V |
| C4 | 1 | 4.7uF | GRM155R60J475ME87D | MuRata | CAP, CERM, 4.7uF, 6.3V, +/- 20%, X5R, 0402 |
| C5 | 1 | 100pF | CGA2B2C0G1H101J050BA | TDK | CAP, CERM, 100pF, 50V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402 |
| C6, C50 | 2 | 330nF | GRT188R71C334KE01D | Murata | Multi-Layer Ceramic Capacitor 330nF 16V X7R ±10% 0603 Paper T/R |
| C8 | 1 | 4.7uF | CGA6P3X7R1H475K250AB | TDK | CAP, CERM, 4.7uF, 50V, +/- 10%, X7R, AEC-Q200 Grade 1, 1210 |
| C9 | 1 | 15nF | GCD188R71H153KA01D | Murata | Chip Multilayer Ceramic Capacitors for Automotive, 0603, 15000pF, X7R, 15%, 10%, 50V, Grade 1 |
| C10 | 1 | 470pF | GRM1555C1H471JA01D | MuRata | CAP, CERM, 470pF, 50V, +/- 5%, C0G/NP0, 0402 |
| C11, C12, C13, C14, C15, C36, C37, C38, C39, C40, C41, C42, C43 | 13 | | GRM32EC72A106KE05L | Murata | 10μF ±10% 100V Ceramic Capacitor X7S 1210 (3225 Metric) |
| C16, C17 | 2 | 220µF | EEHZU1H221P | Panasonic | Aluminum Hybrid Polymer Capacitors 220uF 20% 50V Life 4000Hours AEC-Q200 RADIAL SMT |



Table 6-1. Bill of Materials (continued)

| Designator | Quantity | Value | PartNumber | Manufacturer | Description |
|---|----------|-------|---------------------|---------------------|--|
| C26, C27, C28, C29, C30, C31, C32, C33, C34, C35 | 10 | 2.2µF | GRM21BD72A225ME01K | Murata | Chip Multilayer Ceramic Capacitor for General Purpose 2.2uF ±20% 100V X7T SMD 0805 |
| C44, C45, C46, C47 | 4 | 150µF | EEHZU1J151P | Panasonic | Aluminum Hybrid Polymer Capacitors 150uF 20% 63V Life 4000Hours AEC-Q200 RADIAL SMT |
| FID4, FID5, FID6 | 3 | | N/A | N/A | Fiducial mark. There is nothing to buy or mount. |
| H1, H2, H3, H4 | 4 | | NY PMS 440 0025 PH | B&F Fastener Supply | Machine Screw, Round, #4-40x 1/4, Nylon, Philips panhead |
| J1 | 1 | | N2510-6002-RB | ЗМ | Header (shrouded), 100mil, 5x2, High-Temperature, Gold, TH |
| J21, J22, J23, J24 | 4 | | 108-0740-001 | Cinch Connectivity | Standard Banana Jack, Uninsulated, 15A |
| JP9 | 1 | | 61300111121 | Wurth Elektronik | Header, 2.54mm, 1x1, Gold, TH |
| L1 | 1 | 3.3uH | XGL1712-332MED | Coilcraft | Shielded Power Inductors 3.3µH ±20% 41.7A 1.9mOhms |
| R1, R2 | 2 | 4m | KRL2012E-M-R004F-T5 | Susumu | 4 mOhms ±1% 1W Chip Resistor Wide 0805 (2012 Metric), 0508 Automotive AEC-Q200, Current Sense Metal Foil |
| R5, R6, R62, R63 | 4 | 0 | ERJ-3GEY0R00V | Panasonic | RES, 0, 5%, 0.1W, AEC-Q200 Grade 0, 0603 |
| R7 | 1 | 78.7k | CRCW060378K7FKEA | Vishay-Dale | RES, 78.7k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R8 | 1 | 3.40k | CRCW06033K40FKEA | Vishay-Dale | RES, 3.40k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |



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Table 6-1. Bill of Materials (continued)

| Designator | Quantity | Value | PartNumber | Manufacturer | Description |
|--|----------|-------|------------------|---------------------------|--|
| R9 | 1 | 20.0k | CRCW060320K0FKEA | Vishay-Dale | RES, 20.0k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R11, R18 | 2 | 40.2k | CRCW060340K2FKEA | Vishay-Dale | RES, 40.2k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R12 | 1 | 100k | CRCW0603100KFKEA | Vishay-Dale | RES, 100k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R13, R24, R40, R56, R57, R58, R59, R61, R64 | 9 | 0 | RMCF0603ZT0R00 | Stackpole Electronics Inc | RES, 0, 1%, 0.1W, AEC-Q200 Grade 0, 0603 |
| R14, R21 | 2 | 75.0k | CRCW060375K0FKEA | Vishay-Dale | RES, 75.0k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R15 | 1 | 39.0k | RC0603FR-0739KL | Yageo | RES, 39.0k, 1%, 0.1W, 0603 |
| R16, R37, R53 | 3 | 24.9k | CRCW060324K9FKEA | Vishay-Dale | RES, 24.9k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R17 | 1 | 31.6k | CRCW060331K6FKEA | Vishay-Dale | RES, 31.6k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R19 | 1 | 48.7k | CRCW060348K7FKEA | Vishay-Dale | RES, 48.7k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R20 | 1 | 61.9k | CRCW060361K9FKEA | Vishay-Dale | RES, 61.9k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R22 | 1 | 90.9k | CRCW060390K9FKEA | Vishay-Dale | RES, 90.9k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R23 | 1 | 110k | CRCW0603110KFKEA | Vishay-Dale | RES, 110k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R25, R41 | 2 | 511 | CRCW0603511RFKEA | Vishay-Dale | RES, 511, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R26, R42 | 2 | 1.30k | CRCW06031K30FKEA | Vishay-Dale | RES, 1.30k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R27, R43 | 2 | 1.87k | CRCW06031K87FKEA | Vishay-Dale | RES, 1.87k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R28, R44 | 2 | 2.74k | CRCW06032K74FKEA | Vishay-Dale | RES, 2.74k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R29, R45 | 2 | 3.83k | CRCW06033K83FKEA | Vishay-Dale | RES, 3.83k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |



Table 6-1. Bill of Materials (continued)

| Designator | Quantity | Value | PartNumber | Manufacturer | Description |
|------------|----------|-------|------------------|--------------|--|
| R30, R46 | 2 | 5.11k | CRCW06035K11FKEA | Vishay-Dale | RES, 5.11k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R31, R47 | 2 | 6.49k | CRCW06036K49FKEA | Vishay-Dale | RES, 6.49k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R32, R48 | 2 | 8.25k | CRCW06038K25FKEA | Vishay-Dale | RES, 8.25k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R33, R49 | 2 | 10.5k | CRCW060310K5FKEA | Vishay-Dale | RES, 10.5k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R34, R50 | 2 | 13.3k | CRCW060313K3FKEA | Vishay-Dale | RES, 13.3k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R35, R51 | 2 | 16.2k | CRCW060316K2FKEA | Vishay-Dale | RES, 16.2k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R36, R52 | 2 | 20.5k | CRCW060320K5FKEA | Vishay-Dale | RES, 20.5k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R38, R54 | 2 | 30.1k | CRCW060330K1FKEA | Vishay-Dale | RES, 30.1k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R39, R55 | 2 | 36.5k | CRCW060336K5FKEA | Vishay-Dale | RES, 36.5k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R60 | 1 | 53.6k | CRCW060353K6FKEA | Vishay-Dale | RES, 53.6k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |
| R65 | 1 | 66.5k | CRCW060366K5FKEA | Vishay-Dale | RES, 66.5k, 1%, 0.1W, AEC- Q200 Grade 0, 0603 |

www.ti.com Additional Information

7 Additional Information

7.1 Trademarks

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8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (July 2025) to Revision B (December 2025) | | Page |
|---|---|------|
| • U | Ipdated switching from: 420kHz to: 400kHz | |
| | Deleted disconnection of jumper JP10 and JP2 instructions | |
| • U | Ipdated table name from: CHG0-Pin Settings to: SYNCOUT-Pin Settings | 6 |
| | dded pin setting position information | |
| | dded Application Curves section | |
| | Ipdated Bill of Materials | |
| | • | |

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 - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
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 - 2.3 Tl's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. Tl's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by Tl and that are determined by Tl not to conform to such warranty. If Tl elects to repair or replace such EVM, Tl shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- · Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types lated in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 Japan

- 3.3.1 Notice for EVMs delivered in Japan: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
 - https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html
- 3.3.2 Notice for Users of EVMs Considered "Radio Frequency Products" in Japan: EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

- 1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
- 3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above. User will be subject to penalties of Radio Law of Japan.

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- 3.3.3 Notice for EVMs for Power Line Communication: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page 電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html
- 3.4 European Union
 - 3.4.1 For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

- 4 EVM Use Restrictions and Warnings:
 - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
 - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
 - 4.3 Safety-Related Warnings and Restrictions:
 - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
 - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
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- 5. Accuracy of Information: To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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- 10. Governing Law: These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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