Application Note

Optimizing Dead-Time Control Based on TI GaN ZVD Technology

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ABSTRACT

This document was translated from a simplified Chinese source. (ZHCAG92)

Soft-switching technologies (ZVS and ZCS) are widely used in various power supply topologies and have become critical for reducing losses, improving efficiency, and optimizing EMI. Traditional soft-switching implementations typically use a fixed dead-time configuration. When the dead time does not exactly match the soft-switching time, additional third-quadrant conduction losses occur. This is particularly significant in GaN devices with relatively high reverse conduction voltage. TI's new-generation GaN devices provide Zero-Voltage Detection (ZVD) functionality. The ZVD signal can be used as a feedback signal to achieve more optimized dead-time adjustment, thereby reducing third-quadrant dead-time losses. This application note provides a detailed introduction to the features of TI GaN ZVD and uses an LLC topology as an example to verify the advantages of ZVD technology in system applications through simulation and experimental results.

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1 Introduction

1.1 Fundamentals of Soft Switching

Due to internal parasitic effects, a MOSFET requires a certain amount of time to fully turn on and turn off. During hard switching, the rising current and falling voltage during MOSFET turn-on overlap, resulting in instantaneous switching losses. In addition, the rapid voltage and current transitions associated with hard switching generate high-frequency noise, leading to significant EMI issues. To address these drawbacks, some power converters employ specific design techniques to enable MOSFETs to operate under soft-switching conditions, such as Zero-Voltage Switching (ZVS) turn-on or Zero-Current Switching (ZCS) turn-off.

Taking an LLC converter as an example. Over the operating frequency range of an LLC converter, the resonant tank presents an inductive load to the primary side, and the primary-side current lags the voltage. During the dead time when all primary-side switches are turned off, the circulating current charges and discharges the MOSFET junction capacitances (Coss), allowing the MOSFET voltage to fall to 0V before the next turn-on, thereby achieving ZVS.

Figure 1-1 provides a detailed illustration of the primary-side ZVS process of an LLC converter. Subfigure (a) shows the voltage and current waveforms of the switches during the dead time. Subfigure (b) shows the circulating path of the resonant inductor current ILR on the primary side during the dead time. For simplicity, only the Coss capacitors and body diodes of the four full-bridge MOSFETs are shown in the figure. When Qp1,3 turn off, the voltage on VHB1 gradually decreases from its initial value VS to 0, while the voltage on VHB2 gradually increases from 0V to VS. Note that IDS in the figure is defined as the MOS drain-source terminal current, which is the sum of the channel current, body diode current, and Coss current.

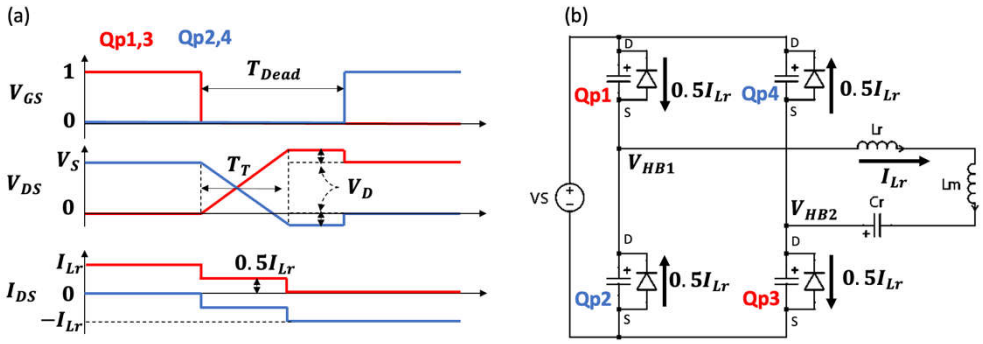

Figure 1-1. LLC Primary-Side ZVS Process

The total time TT required to complete the charging and discharging of Coss is:

$$T_T = 2C_{OSS}\frac{VS}{I_r} \quad (1)$$

After t = TT, the junction capacitor charge transfer is complete, and VHB1 and VHB2 are clamped by the body diodes of Qp2 and Qp4 at -VD and VS+VD, respectively (VD is the body diode forward voltage drop), until the switches turn on again. The necessary and sufficient conditions for primary-side ZVS in an LLC converter are:

1. The MOSFET dead time TD must be greater than TZ to ensure complete transfer of the junction capacitor charge.
2. The bridge-leg current must lag the voltage and must not reverse direction during the dead time.

For secondary-side ZCS in an LLC converter, based on the characteristics of its circuit, the secondary-side current operates in Boundary Conduction Mode (BCM) under heavy load and Discontinuous Conduction Mode (DCM) under medium and light loads. Therefore, the current is close to or equal to 0 when the rectifier MOSFETs turn on and turn off, achieving Zero-Current Switching (ZCS) for both turn-on and turn-off.

1.2 Dead-Time Losses in Soft Switching

Although soft-switching technology can largely avoid the overlapping switching losses associated with hard switching, the reverse conduction voltage of MOSFETs introduces a certain amount of reverse conduction loss during the dead time. Taking an LLC converter as an example, the loss mechanism during the primary-side ZVS dead time is shown in Figure 1-2:

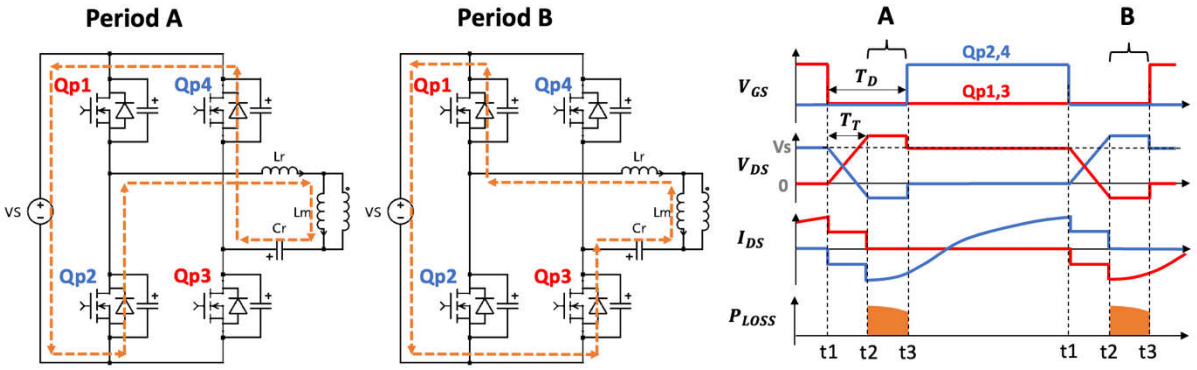

Figure 1-2. LLC Primary-Side Dead-Time Loss

At time t1, the switches of bridge leg A (Qp1, 3) turn off, and the remaining current in the loop flows through the switch Coss, causing the Vds voltage to enter the commutation state. At time t2, the Vds of all switches completes commutation and the Coss voltage is clamped. However, because bridge leg B (Qp2, 4) has not yet turned on, the remaining current in the loop continues to flow through the body diode until bridge leg B turns on at t3. Therefore, during the t2-t3 interval, losses caused by body diode conduction occur. This loss can be estimated using Equation 2:

$$P_{DT\_pri} = 2 \cdot V_D \cdot I_{Lr} \cdot \left(T_D - T_T\right) \cdot f_{SW} \tag{2}$$

where V_D is the MOSFET body diode forward voltage drop, I_{Lr} is the series resonant inductor current, T_D is the dead time, T_T is the transition time calculated using Equation (1), and f_{SW} is the switching frequency. In an LLC topology, I_{Lr} during the dead time can be calculated from the switching frequency and magnetizing inductance.

The loss mechanism during the LLC secondary-side ZCS dead time is shown in Figure 1-3:

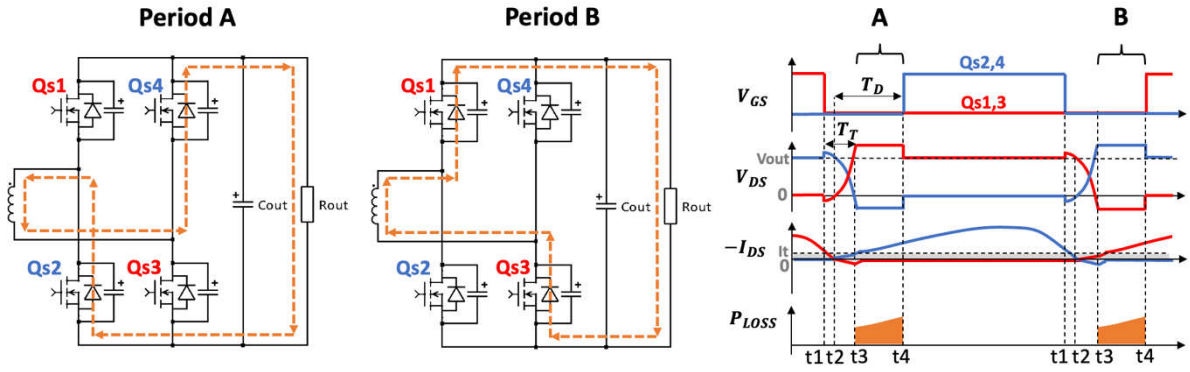

Figure 1-3. LLC Secondary-Side Dead-Time Loss (Heavy Load)

The example in Figure 1-3 uses a current-controlled secondary-side synchronous rectification strategy. At time t1, the current of synchronous rectifier bridge leg A (Qs1, 3) falls below the synchronous rectification threshold It, causing bridge leg A to turn off. t2 is the actual zero-crossing point of the B bridge-leg current. During the t1-t3 interval, the secondary-side switch Coss provides a low-impedance current path for bridge leg A. Therefore, the Vds of all switches commutates during this interval until the switch voltage is clamped at t3, and the current of

bridge leg B (Qs2, 4) returns through the body diode of bridge leg B. During the t3 to t4 interval, third-quadrant dead-time losses occur on the secondary side, which can be estimated using Equation 3:

$$P_{DT\_sec} = 2 \cdot V_D \cdot I_{TR} \cdot \left(T_D - T_T\right) \cdot f_{SW} \quad (3)$$

where I_{TR} is the secondary-side current, whose magnitude is related to the load, and T_T is the transition time required for commutation of the secondary-side Coss. For simplicity, the effect of the t1-t2 interval is ignored in Equation 3. It should also be noted that in DCM, the zero-crossing point t2 of the B bridge-leg current occurs very close to t3, and the loss can be approximately estimated using Equation 4:

$$P_{DT\_sec} = 2 \cdot V_D \cdot I_{TR} \cdot T_D \cdot f_{SW} \quad (4)$$

Under the same dead-time and switching-frequency conditions, the LLC primary-side dead-time loss is independent of the load, while the secondary-side dead-time loss generally increases with increasing load. Therefore, under light-load conditions, primary-side dead-time loss becomes a non-negligible factor.

1.3 Challenges in GaN Applications

The use of GaN technology in power topologies helps further increase system power density and efficiency. GaN devices have much lower junction capacitance than Si MOSFETs and can achieve soft switching with shorter dead-time requirements. GaN also features low turn-off losses and is suitable for topologies with primary-side Zero-Voltage Switching (ZVS) turn-on, such as LLC and Phase-Shifted Full Bridge (PSFB), which can further reduce the adverse impact of hard turn-off on efficiency.

One challenge in GaN device applications arises from their unique third-quadrant characteristics. According to the analysis above, dead-time loss is related to the reverse conduction voltage of the device. For Si MOSFETs, this voltage is equal to the forward voltage drop of the body diode, which is generally below 1V. For GaN devices, the reverse conduction voltage is significantly higher than that of Si MOSFETs, depending on their third-quadrant characteristics.

The reverse conduction voltage of a GaN device can be described by Equation 5:

$$V_{SD} \approx \left(V_{th} - V_{gs}\right) + I_{SD} \cdot R_{REV} \quad (5)$$

where V_{th} is the threshold voltage. As a reference, the typical threshold voltage of a 650V GaN device is approximately 1.7V. R_{REV} is the equivalent third-quadrant on-resistance. Figure 1-4 describes the simplified behavior of a GaN device in the third quadrant.

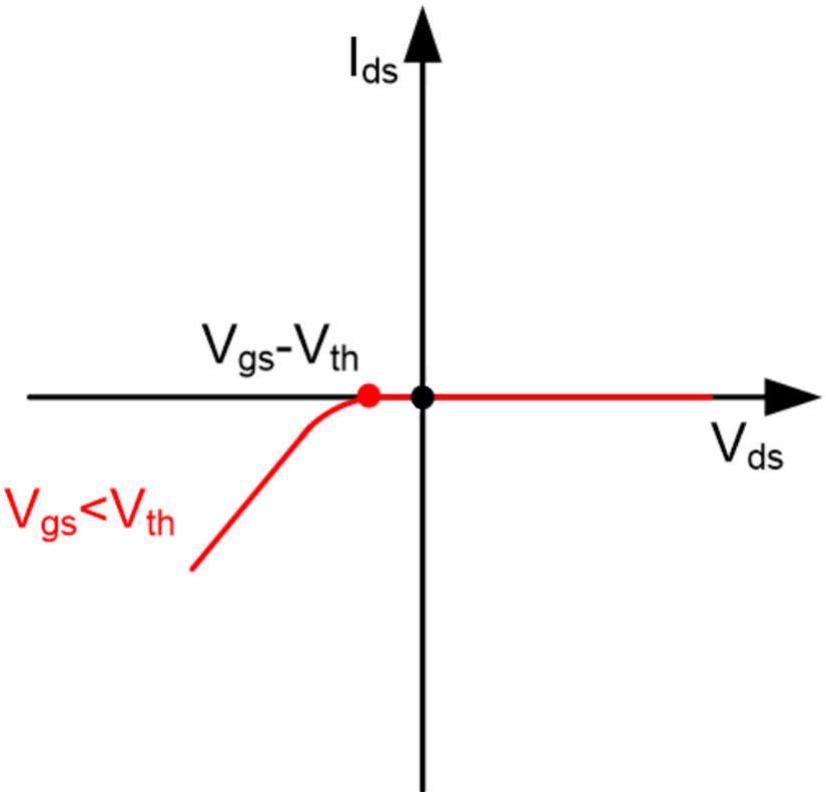

Figure 1-4. Simplified Behavior of a GaN Device in the Third Quadrant

As shown above, a GaN device requires a negative voltage greater than V_{gs}-V_{th} to turn on in the third quadrant. In practical applications, a negative gate bias voltage is typically used to prevent false turn-on caused by noise. For example, with a gate bias of -1.5V, the reverse voltage starts at 3.2V and further increases as the load current increases.

Because GaN has a higher reverse conduction voltage drop than Si MOSFETs, in high-power supply systems, if the dead time is not optimized and adjusted, the combined primary- and secondary-side dead-time losses can reach several tens of watts. This can have a highly adverse impact on overall system efficiency.

2 Adaptive Dead-Time Control Based on ZVD

2.1 TI GaN ZVD Function

Some power products use adaptive dead-time compensation to reduce the dead-time losses caused by the high reverse conduction voltage of GaN. The following methods are commonly used:

1. Voltage detection method: Measure the bridge-leg voltage or the VDS of an individual device to indirectly detect the charging and discharging state of the FET Coss. Once a specific threshold is reached, soft switching is considered complete. This method is the most direct and provides the highest accuracy, but it requires additional operational amplifier or comparator circuitry and has relatively poor noise immunity.
2. Current detection method: Measure the resonant tank current and calculate the theoretical dead time using an equation or lookup table. This method determines soft switching indirectly and therefore has limited accuracy. In practical applications, a certain margin must be reserved.

TI's new-generation GaN products provide Zero-Voltage Detection (ZVD) functionality. This function provides a ZVD digital signal that indicates whether the GaN device has achieved ZVS during the switching cycle. An adaptive dead-time control algorithm can be designed based on the ZVD function to reduce dead-time losses to a reasonable level, helping simplify the design of adaptive dead-time compensation in the system.

Taking the LMG3526 as an example, its ZVD operating principle is shown in Figure 2-1. When the input signal (IN) goes high, the internal logic checks whether the device has achieved ZVS during the switching cycle. Once a ZVS event meeting the specified conditions is detected, a ZVD signal pulse with a width of TWD_ZVD is output from the ZVD pin after a delay of TDL_ZVD.

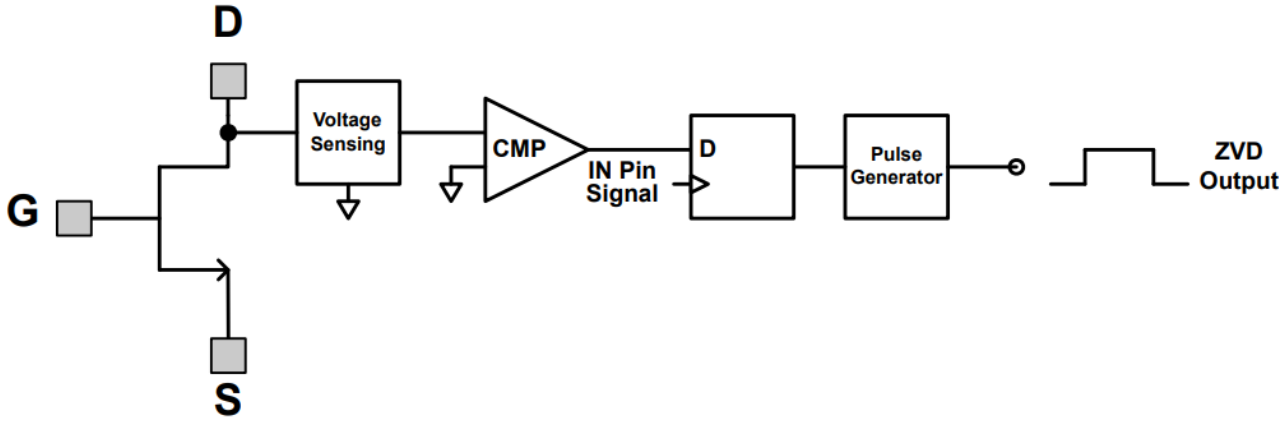

Figure 2-1. LMG3526 Zero-Voltage Detection (ZVD) Block Diagram

It should be noted that not every ZVS event triggers ZVD. The ZVD signal is triggered only when a certain third-quadrant conduction time (T3rd_ZVD) is met. If the IDS current has just crossed zero at the time of ZVS, and the device has not entered third-quadrant conduction or the third-quadrant conduction time is insufficient, the ZVD signal will not be triggered.

Figure 2-2 shows the ZVD timing diagram of the LMG3526. It provides a more detailed explanation of the triggering conditions for the ZVD signal.

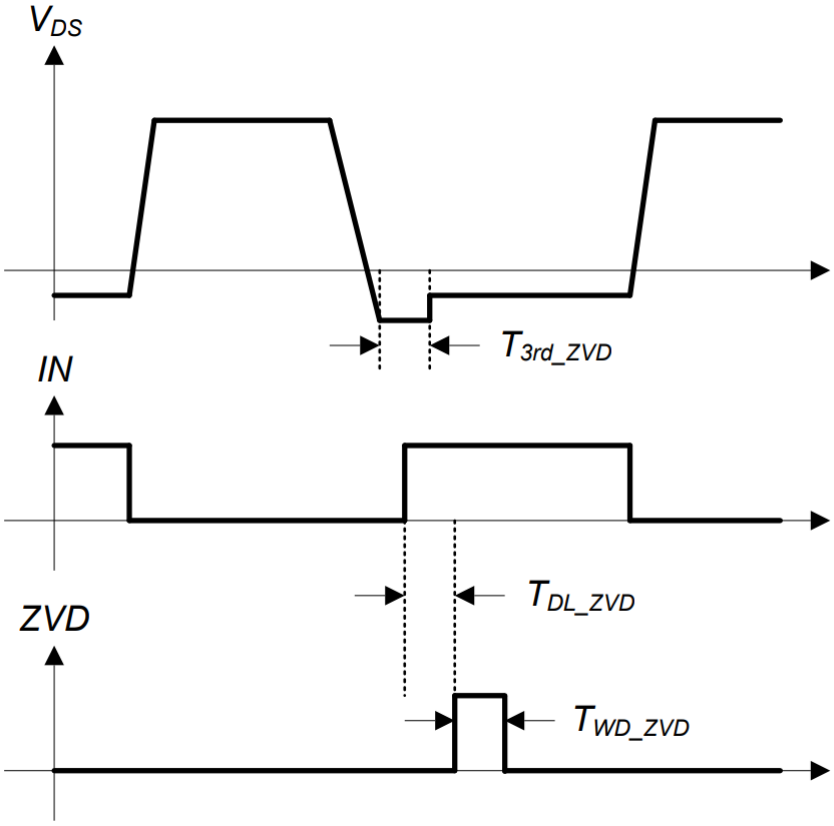

Figure 2-2. LMG3526 Zero-Voltage Detection (ZVD) Timing Diagram

In the figure, T3rd_ZVD is the minimum third-quadrant conduction time. If the third-quadrant conduction time is less than this value, the device cannot detect ZVD. TDL_ZVD is the delay between the rising edge of the LMG3526 input pin (IN) and the rising edge of the ZVD signal output. TWD_ZVD is the hold time of the ZVD signal. When the input pin signal goes high, the logic circuit checks whether the device VDS has reached below 0V to determine whether the device has achieved zero-voltage switching during the switching cycle. Once ZVS is detected, a pulse output with a width of TWD_ZVD is generated from the ZVD pin after a delay of TDL_ZVD.

It should be noted that there is also a turn-on delay (td(ON)) between the rising edge of IN and the rising edge of the internal GaN FET gate voltage. Due to td(ON), the time at which VDS exits third-quadrant conduction in Figure 2-2 occurs later than the rising edge of IN.

2.2 LLC Primary-Side Adaptive Dead-Time Control

We aim to design an adaptive dead-time algorithm that minimizes the third-quadrant conduction time as much as possible while avoiding hard switching. The above requirements can be achieved by combining the TI GaN ZVD signal with a simple control mechanism. When a ZVD signal occurs during a switching cycle, it indicates that the GaN third-quadrant conduction time is too long, and the dead time should be reduced in the next control cycle. When no ZVD signal occurs during a switching cycle, it indicates that the GaN reverse conduction time is too short, or that ZVS has been lost (non-ZVS), and the dead time should be increased in the next control cycle. The flowchart of this strategy is shown in Figure 2-3.

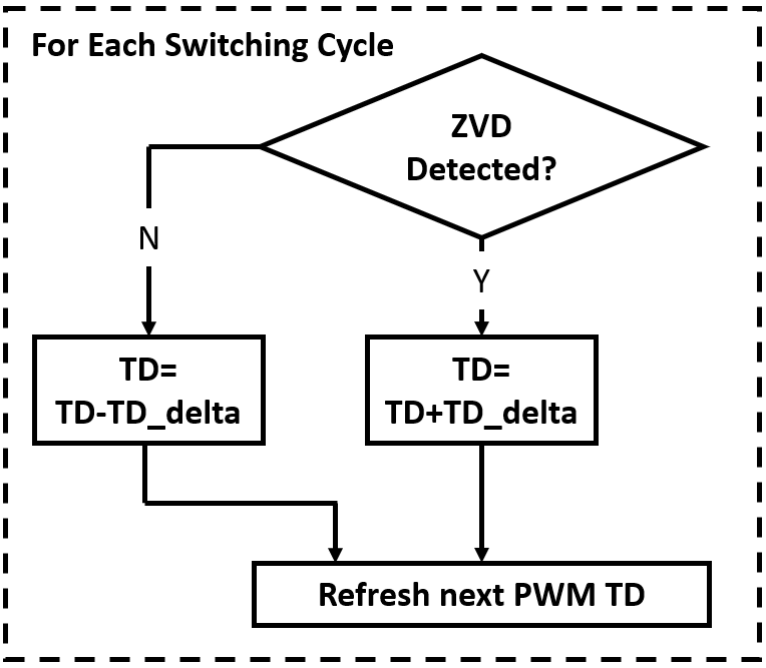

Figure 2-3. Cycle-by-Cycle Adjustment of Primary-Side Dead Time Based on the ZVD Signal

This control method ultimately causes the dead time to converge to approximately TT+T3rd_ZVD rather than TT. Due to the existence of T3rd_ZVD, the absence of a ZVD signal does not necessarily mean that the GaN device is actually in a non-ZVS state. This provides a certain margin in the design, but also introduces a minimum dead-time loss that cannot be eliminated. In practical applications, based on the symmetry of the LLC primary side, only one of the four primary-side switches needs to be monitored by ZVD. The dead times of the remaining three switches can be further shortened by using a fixed compensation value to eliminate the effect of T3rd_ZVD. Therefore, theoretically, the LLC primary side can achieve zero dead-time loss for three switches (TD = TT) and minimized dead-time loss for one switch (TD = TT+T3rd_ZVD).

2.3 LLC Secondary-Side Adaptive Dead-Time Control

The LLC secondary-side adaptive dead-time control strategy is similar to that of the primary side. The dead-time loss under the current-controlled synchronous rectification strategy was discussed in Section 1.2. The secondary-side dead time is defined as the difference between the zero-crossing point of the secondary-side phase current and the turn-on point of the synchronous rectifier. To achieve zero secondary-side dead-time loss, according to the analysis in Equation 3 and Equation 4, the dead time under BCM conditions should satisfy TD=TT, while under DCM conditions, the dead time should be approximately 0. Using the control method described in Section 2.2, the dead time can converge to TD = TT+T3rd_ZVD under BCM conditions and to TD = min(Tprop, TT)+T3rd_ZVD under DCM conditions, where Tprop is the propagation delay between the synchronous rectification signal and the actual current zero-crossing point.

Secondary-side adaptive dead-time control can also simplify the synchronous rectification design and effectively prevent current spikes or oscillations caused by premature turn-on of the synchronous rectifier. Figure 2-4 shows the current spike caused by non-ZVS turn-on of the synchronous rectifier due to an excessively short dead time (TD<TT). When ZVD-based adaptive dead-time control is used, all secondary-side synchronous rectifiers turn on under ZVS conditions, preventing the occurrence of current spikes.

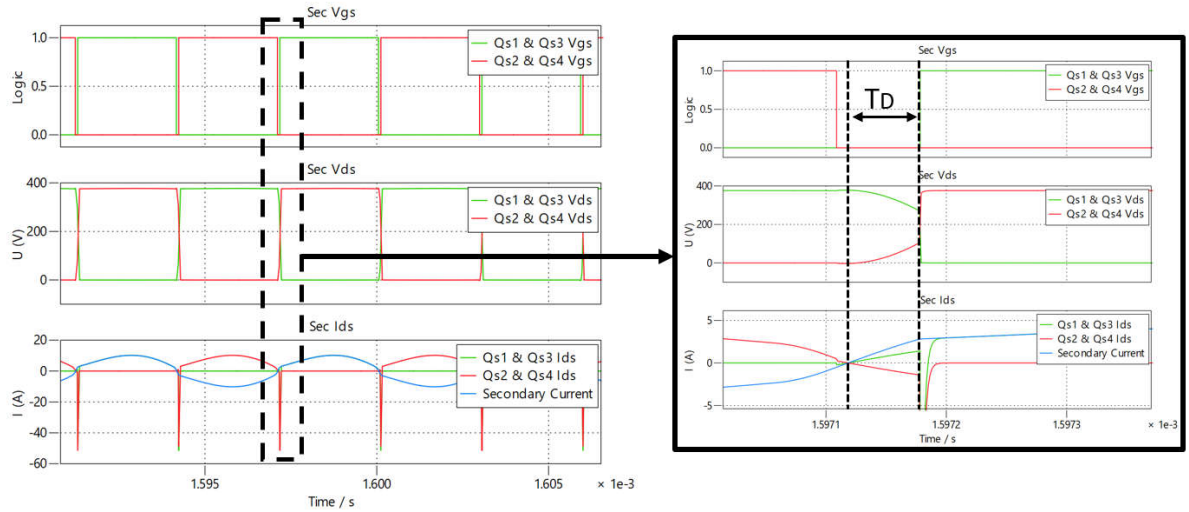

Figure 2-4. Current Spike Caused by Excessively Short Secondary-Side Synchronous Rectification Dead Time

3 PLECS Simulation Verification

PLECS simulations were conducted to verify the effectiveness of the adaptive dead-time control technology. The simulated topology is a full-bridge LLC converter with a nominal input voltage of 400V, nominal output voltage of 48V, and rated power of 3kW. Its topology and key circuit parameters are shown in Figure 3-1:

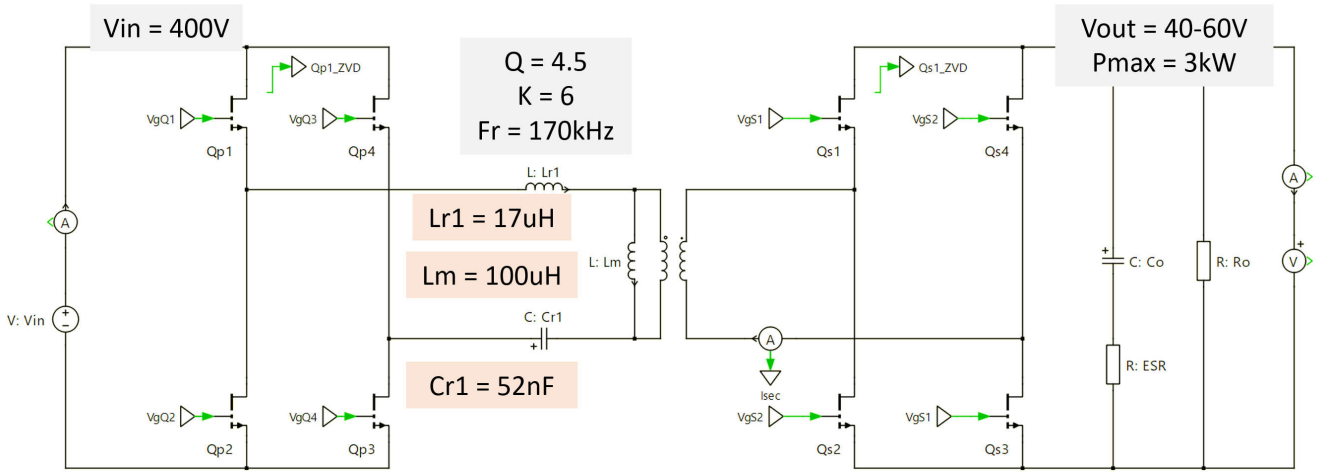

Figure 3-1. Simulation Circuit Topology and Key Parameters

The ZVD function of the LMG3526 can be modeled based on the official PLECS model using the approach shown in Figure 3-2. The PLECS implementation of the adaptive dead-time control strategy can refer to Figure 3-3.

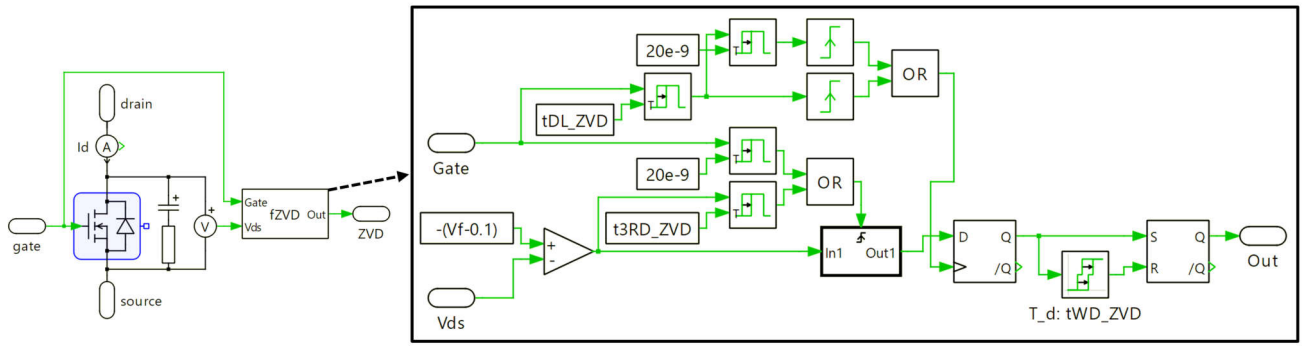

Figure 3-2. PLECS Model of the LMG3526 ZVD Function

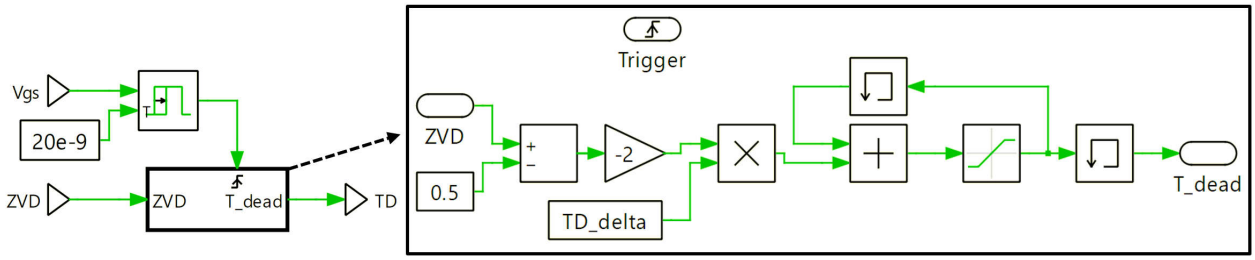

Figure 3-3. PLECS Model of the Adaptive Dead-Time Controller

Figure 3-4 shows the primary-side waveforms under steady-state conditions. The dead time of Qs1 has converged to TT+T3rd_ZVD. The enlarged waveform shows the turn-on state of the non-ZVD-monitored switch Qs2. By compensating the dead time of Qs2, the effect of T3rd_ZVD can be eliminated. Here, the dead time of Qs2 is approximately equal to TT, and the time for the GaN device to enter the third quadrant is very short.

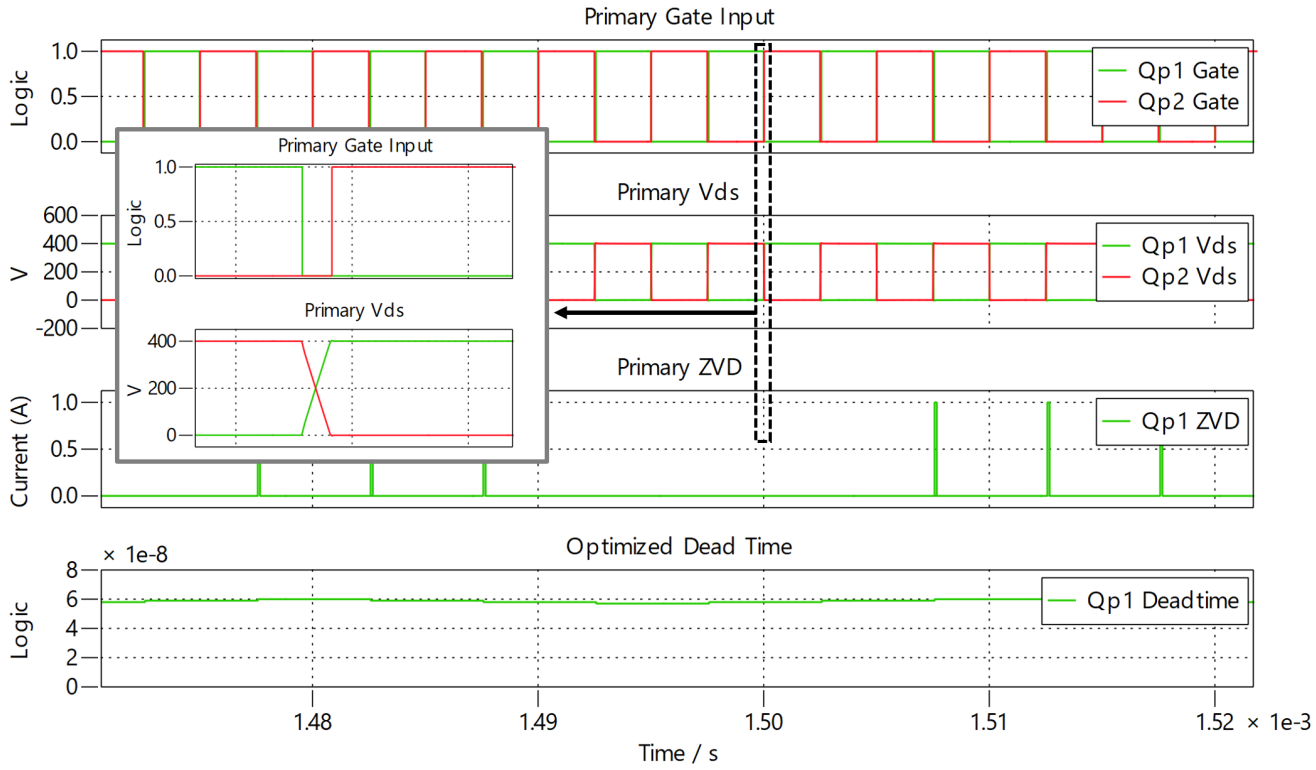

Figure 3-4. Primary-Side Steady-State Simulation Results

Figure 3-5 and Figure 3-6 show the secondary-side waveforms under steady-state BCM and DCM conditions, respectively. Similar to the primary-side case, the dead time of Qp1 converges to TT+T3rd_ZVD. The enlarged waveform shows the turn-on state of the non-ZVD-monitored switch Qp2. The compensated dead time is approximately equal to TT, and the third-quadrant loss is very small.

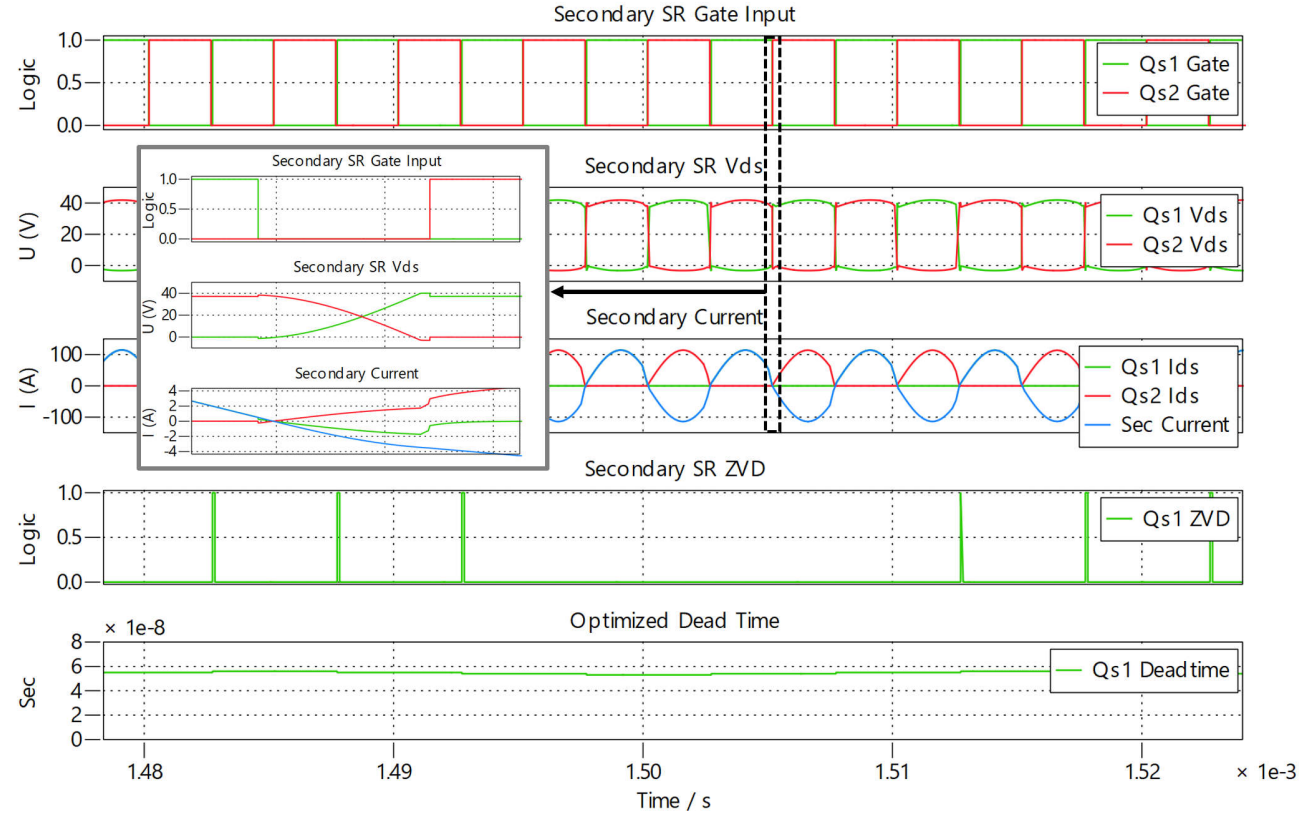

Figure 3-5. Secondary-Side BCM Steady-State Simulation Results

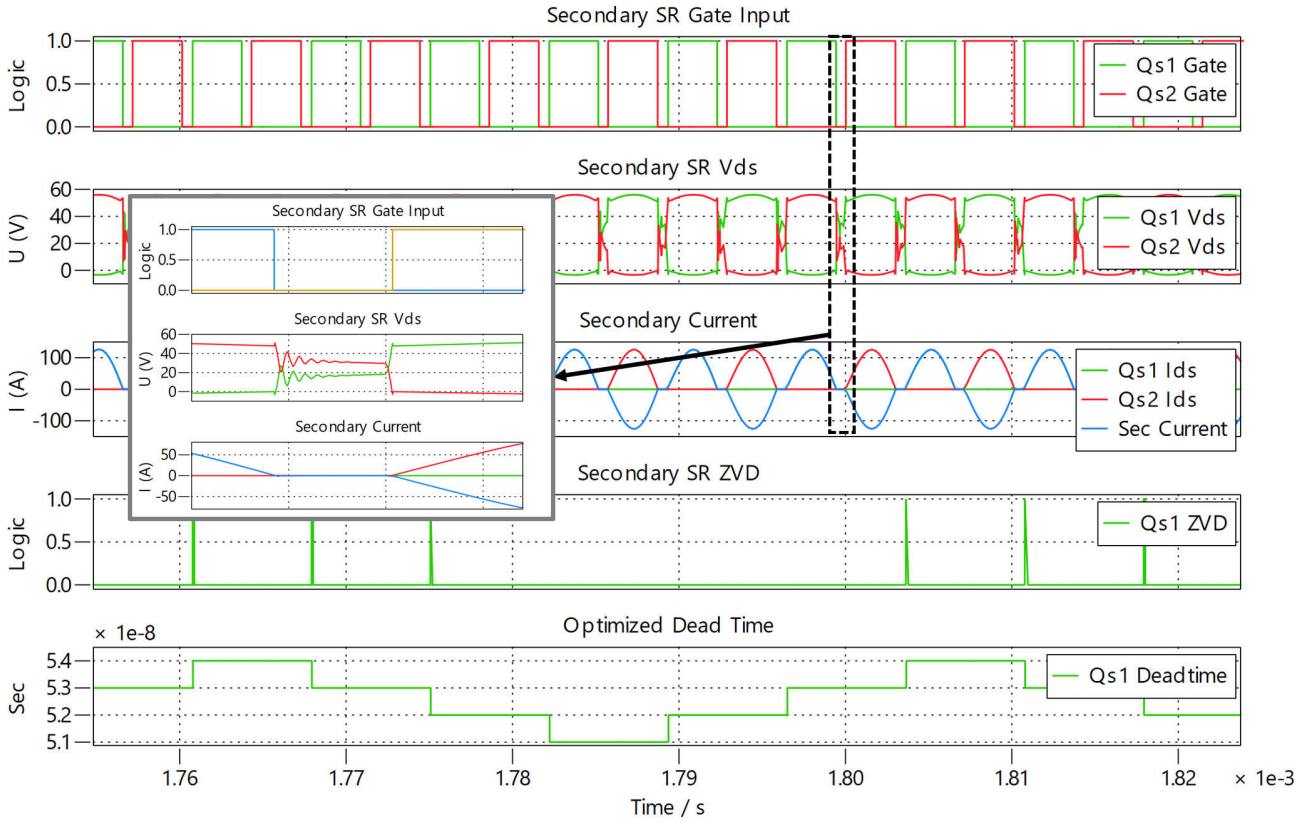

Figure 3-6. Secondary-Side DCM Steady-State Simulation Results

Table 3-1 summarizes the third-quadrant conduction losses on the primary and secondary sides under different operating conditions. When ZVD-based adaptive dead-time control is used, the third-quadrant conduction losses of the GaN devices on both the primary and secondary sides are significantly reduced. The only exception occurs under heavy load below resonance, where the peak secondary-side DCM current is relatively high and the Rdson voltage drop can temporarily exceed the reverse conduction voltage, resulting in a significant increase in third-quadrant conduction loss. Even under this abnormal condition, adaptive dead-time control can minimize the third-quadrant conduction loss to the greatest extent possible.

Table 3-1. Primary- and Secondary-Side Third-Quadrant Conduction Losses Under Different Simulation Conditions

Power	Side	fs = 140kHz		Fs = 170kHz (Resonant)		fs = 200kHz	
		ZVD-DT	250ns Fix	ZVD-DT	250ns Fix	ZVD-DT	250ns Fix
P = 3000W	Primary	0.08W	1.02W	0.07W	0.95W	0.13W	1.38W
	Secondary	9.7W	14.8W	0.03W	3.7W	0.09W	5.03W
P = 1500W	Primary	0.09W	1.45W	0.09W	1.21W	0.07W	1.06W
	Secondary	0.07W	1.06W	0.03W	0.73W	0.07W	1.84W

4 Conclusion

This paper introduces the third-quadrant characteristics of GaN and provides an in-depth discussion of the mechanisms behind dead-time losses of GaN devices in soft-switching topologies. An adaptive dead-time adjustment mechanism based on TI GaN ZVD technology is proposed to adaptively optimize the primary- and secondary-side dead times of LLC/CLLC topologies, reduce dead-time losses, and minimize the adverse impact of the high reverse conduction voltage of GaN devices on system performance.

5 References

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Last updated 10/2025