EVM User's Guide: DP83TD530

DP83TD530EVM User's Guide

1 Description

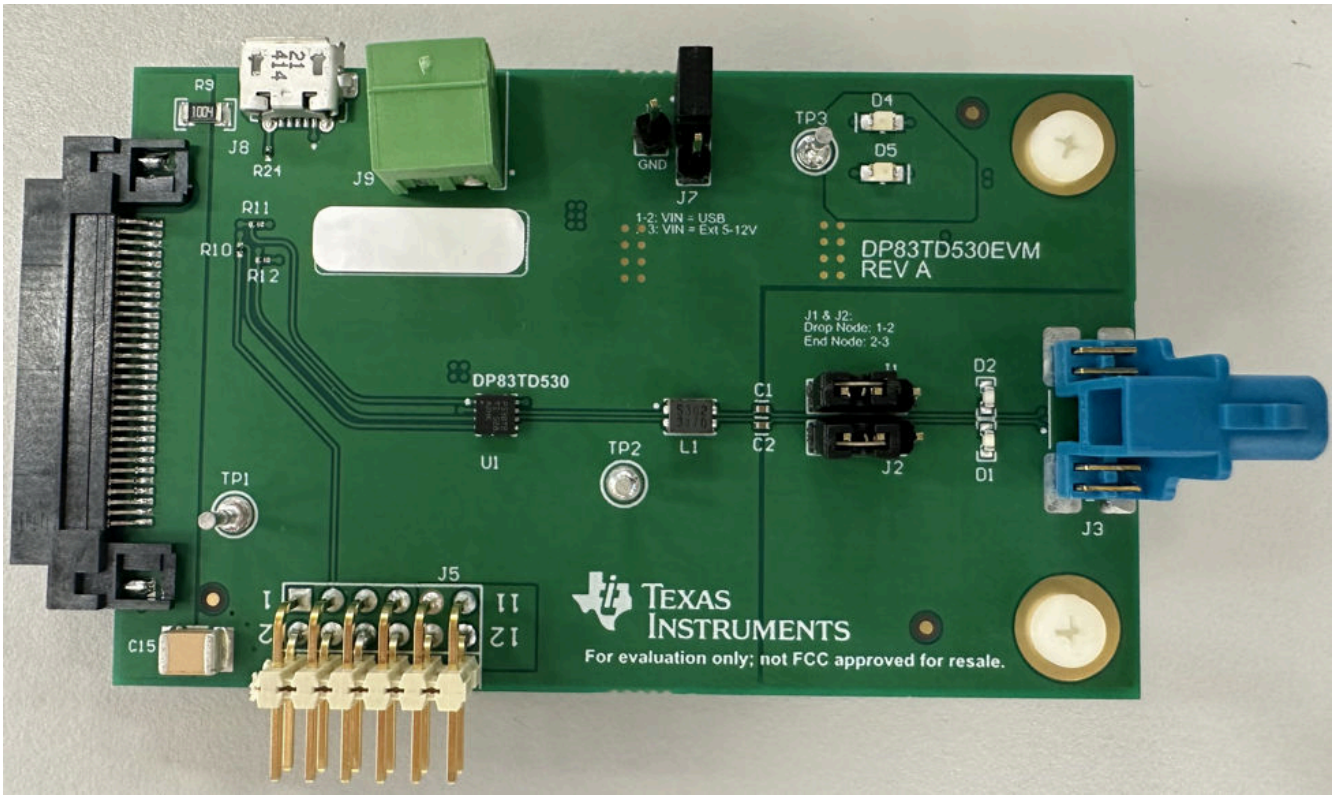
This User's Guide discusses how to properly operate and configure the DP83TD530EVM. For best layout practices, schematic files, and Bill of Materials, see the associated support documents.

2 Get Started

1. Configure the board headers for desired power configuration/MDI termination
2. Connect the DP83TD535EVM to and MCU board using the 3-pin Interface
3. For any issues, reach out to us on the TI E2E forum

3 Features

- DP83TD530 IEEE802.3cg and 10BASE-T1S Compliant
- 10BASE-T1S Interface through Rosenberger Daisy-Chain MTD adapter & cabling
- Status LEDs for VBAT/VCC/VDDIO power rails
- Variable I/O Voltage Range: 1.8-V, 2.5-V, and 3.3-V
- Configurable MDI termination through jumpers for device to act as End Node or Drop Node



DP83TD530EVM

4 Evaluation Module Overview

4.1 Introduction

DP83TD530EVM supports 10-Mbps half-duplex speed and is IEEE 802.3cg and 10BASE-T1S compliant. The EVM can be powered by an external 5V-12V power supply, or through a microUSB cable. On-board OA-3pin interface options are provided to communicate and register access with the PHY through a compatible SoC.

4.2 Kit Contents

The DP83TD530EVM kit includes with the following:

- DP83TD535EVM
- 1x Untwisted Pair Cable (LAQ-116-1000Z-Z)

Not supplied:

- Micro-USB cable
- Rosenberger multidrop connector (E7C10T-900X5Z)

4.3 Specification

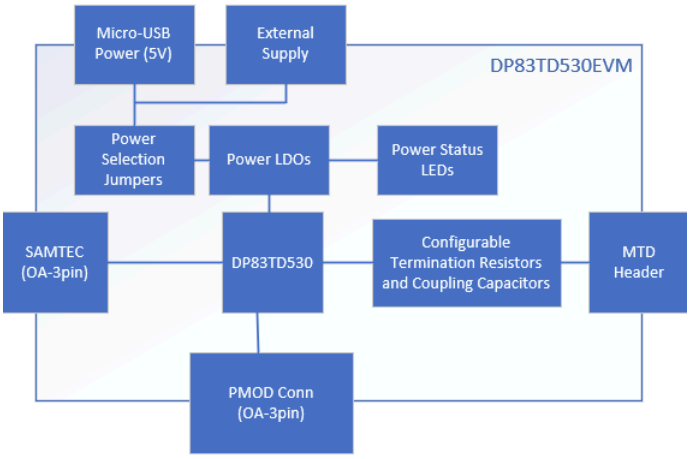


Figure 4-1. DP83TD530EVM Block Diagram

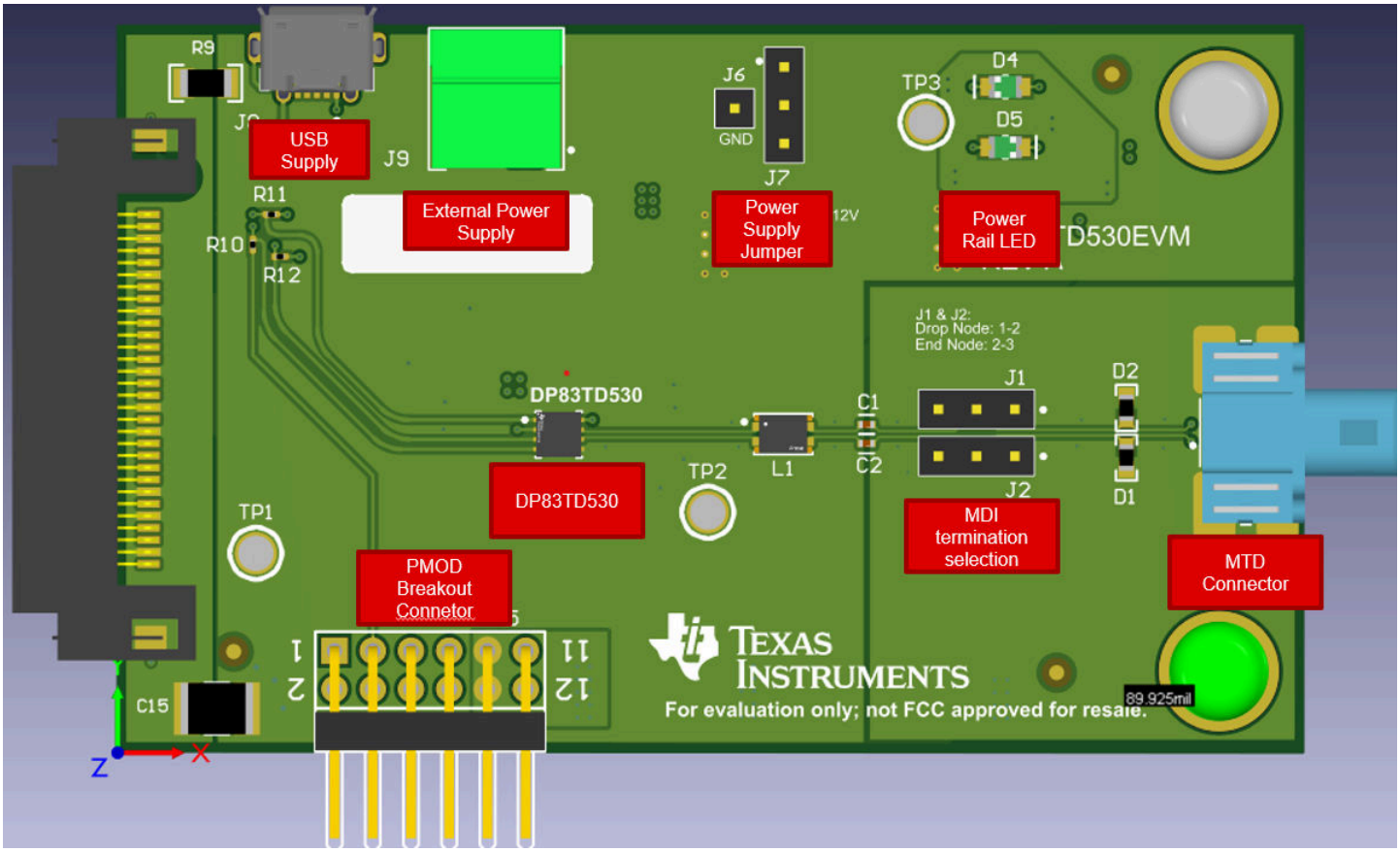


Figure 4-2. DP83TD530EVM Key Interfaces

5 Hardware

5.1 Board Setup Details

5.1.1 Setup

Follow these quick set up instructions for the DP83TD530EVM:

- Populate jumpers J7 at pins 1-2
- Configure J2 and J3 jumper to Drop Node or End Node
  - Drop Node: Connect pin 1 to 2
  - End Node: Connect pin 2 to 3
- Connect external host to TX/RX/ED pins of J5
- Connect micro-USB to J8 for 5V supply

5.1.2 Power Supply Selection

5.1.2.1 USB Power Supply Option

- DP83TD530EVM USB Power
  - Populate jumpers J7 at pins 1-2

5.1.2.2 External Power Supply Operation

- DP83TD530EVM External Power
  - Populate jumpers J7 at pins 2-3
  - Supply 5-12V on J9(pin 2 = GND)

5.1.2.3 VDDIO Rail Selection

By default, DP83TD530EVM operates at 3.3V for the VDDIO rail. For VDDIO operation at 2.5V or 1.8V, follow the resistor modifications below:

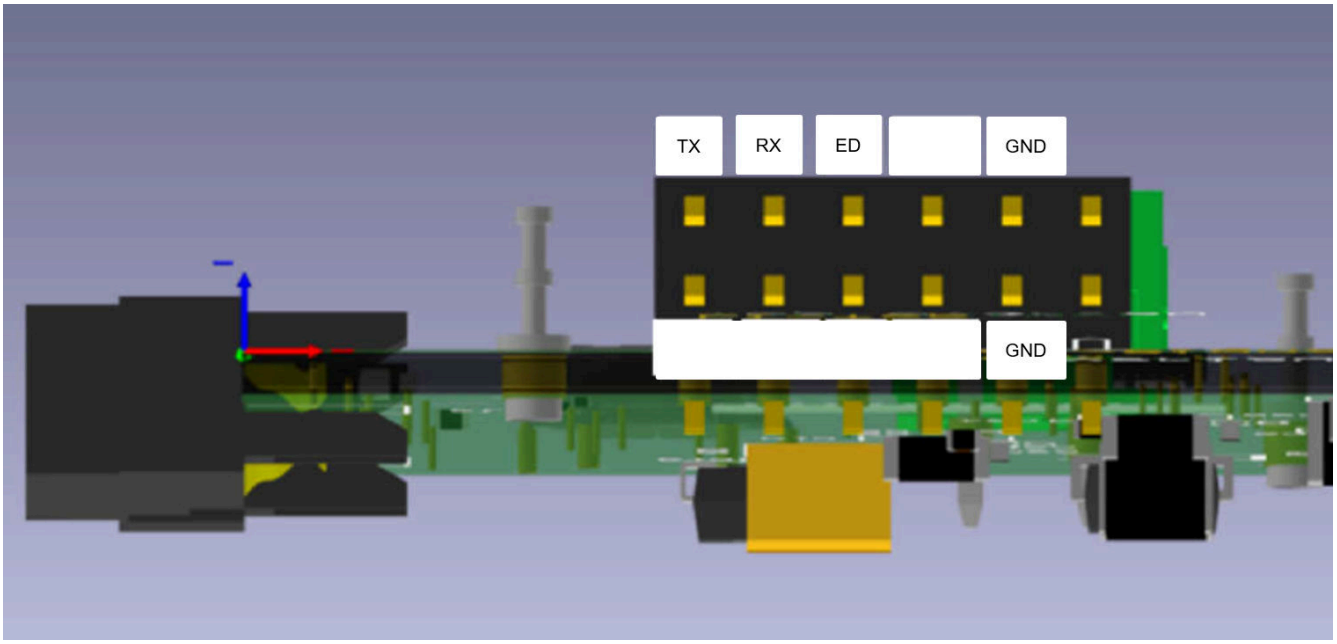
Table 5-1. VDDIO Selection

VDDIO Rail	R13	R15	R18
3.3V	0Ω	DNP	N/A
2.5V	DNP	0Ω	2.87kΩ
1.8V	DNP	0Ω	1.78kΩ

5.1.3 Interface Connections

5.1.3.1 PMOD Interface

The PMOD breakout connector J7 provides access to the OA-3pin (TX/RX/ED)



The external host supporting OA-3pin connects to TX/RX/ED pins, driving the TX pin with RESET pulse on or before PHY power-up to activate DP83TD530 transmit mode.

DP83TD530 Register Access:

Driving TX pin with Config command to put DP83TD530 into configuration command to access the registers through 3-pins interface. Here is the pinout when the PHY is in configuration mode:

- ED pin = MDIO
- RX pin = MDC

5.1.3.2 MDI Interface

Rosenberger's Daisy-Chain Adapter (E7C10T-900X5-Y) and MTD cabling is used to connect to the PHY's MDI interface on J1. If this cable assembly cannot be sourced, the MDI can also connect to any single-pair Ethernet cable direct to the pins in J1, or to pin 2 of J2 (Line+) and J3 (Line-).

6 Hardware Design Files

6.1 Schematics

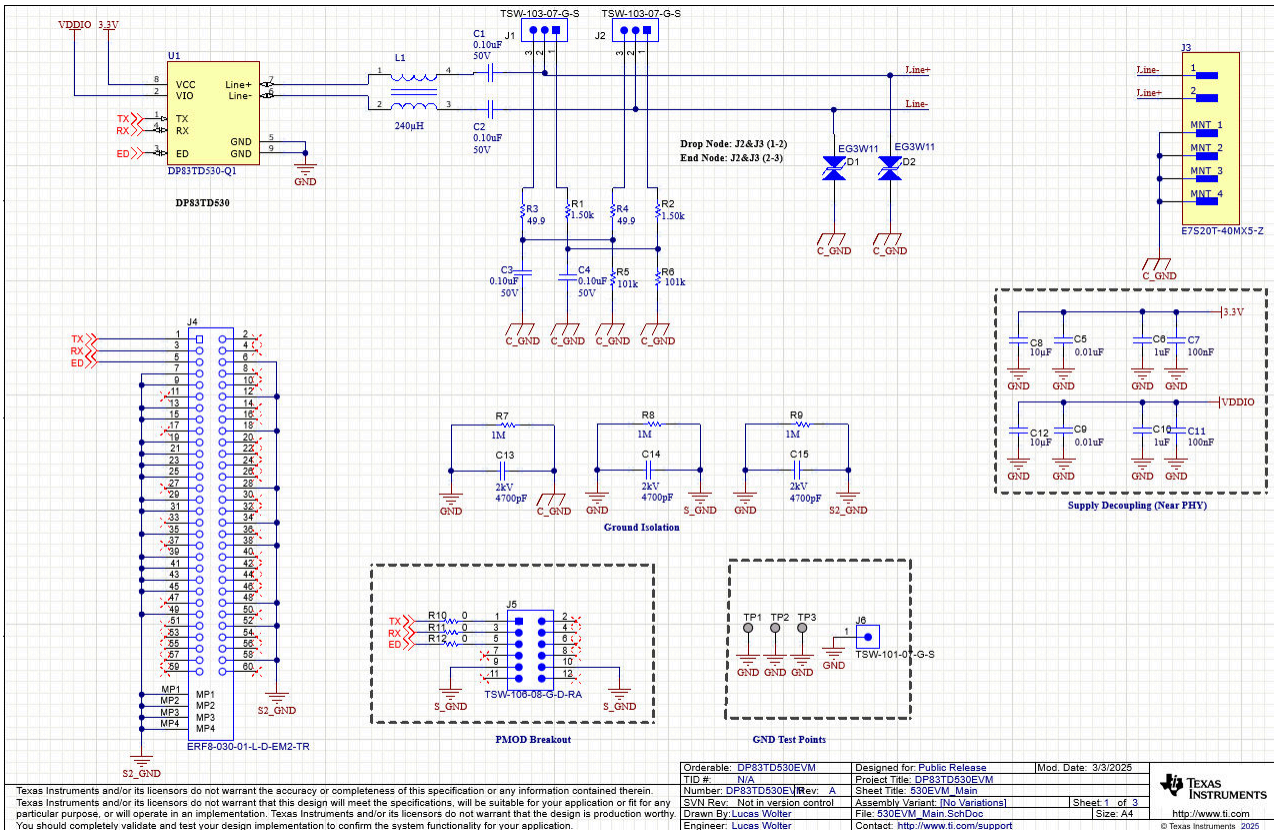


Figure 6-1. DP83TD530EVM Main Schematic Block

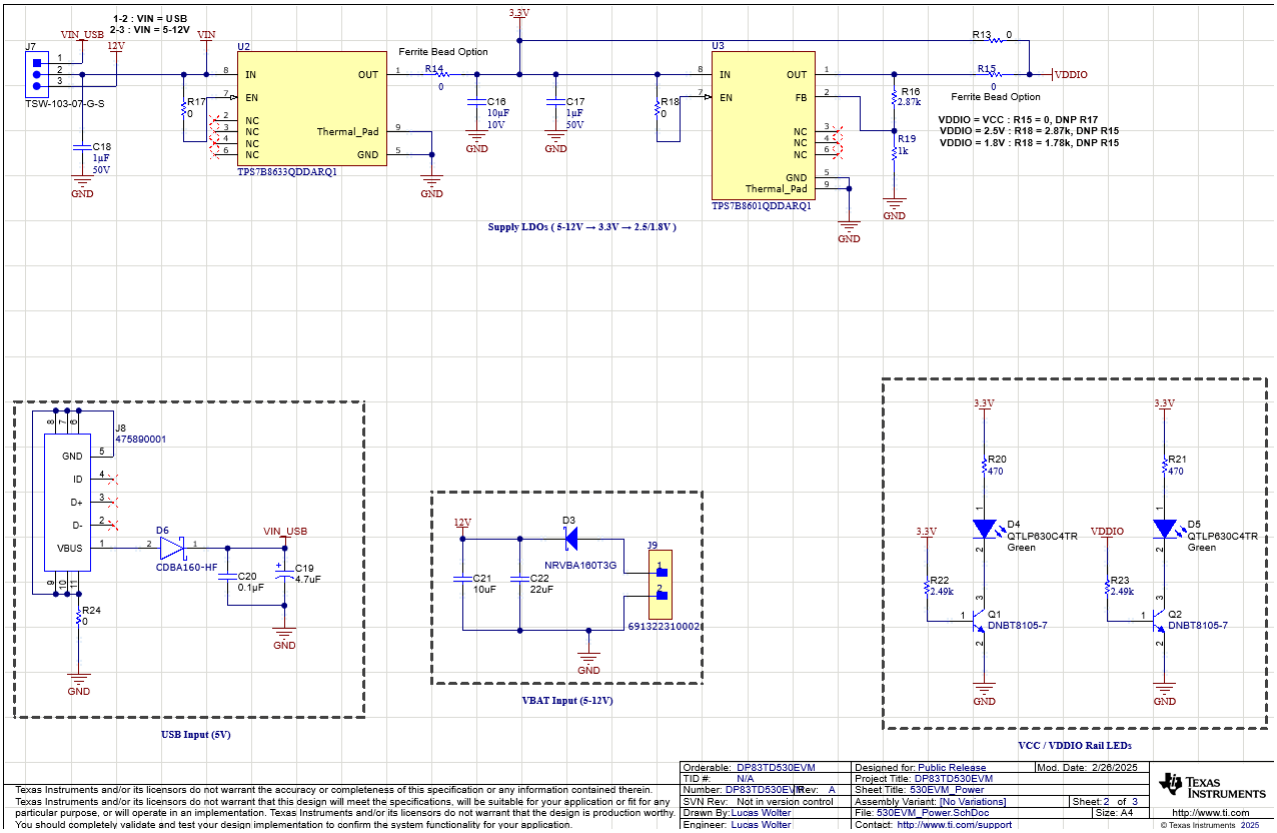


Figure 6-2. DP83TD530EVM Power Block

6.2 PCB Layout

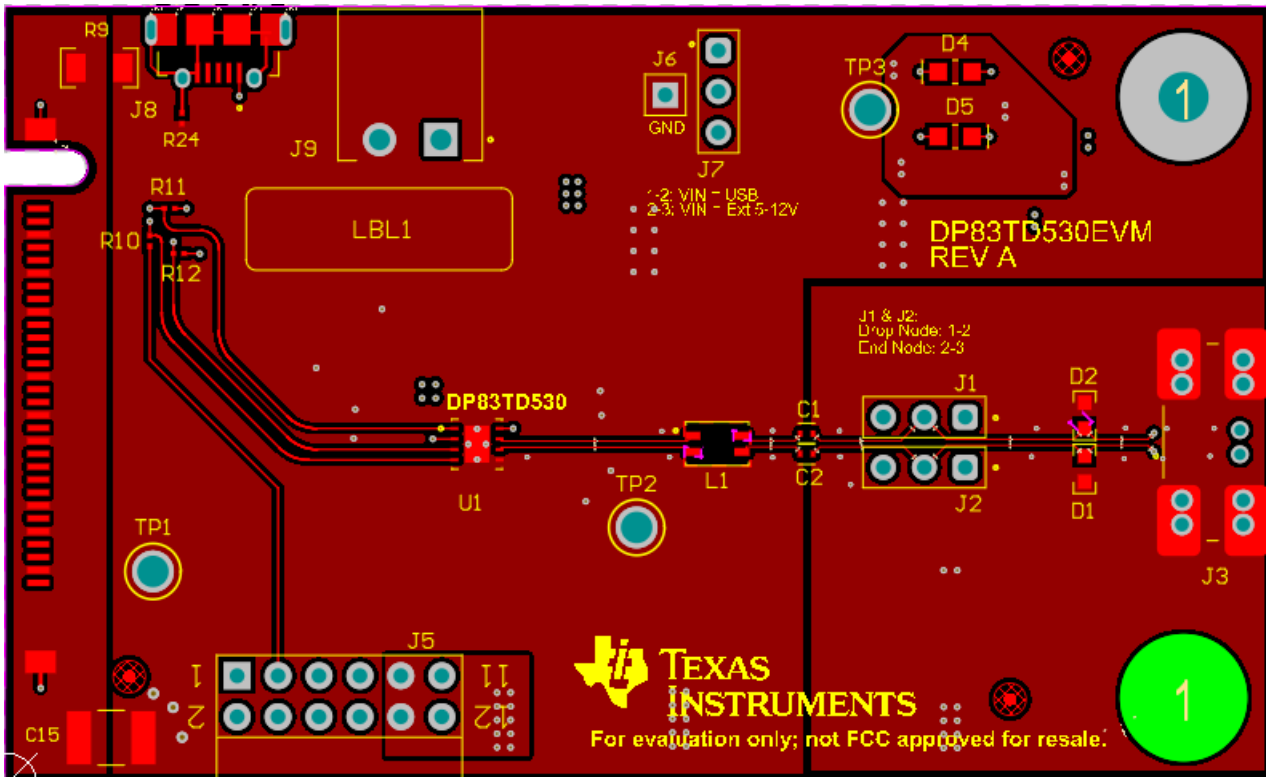


Figure 6-3. Top Layer

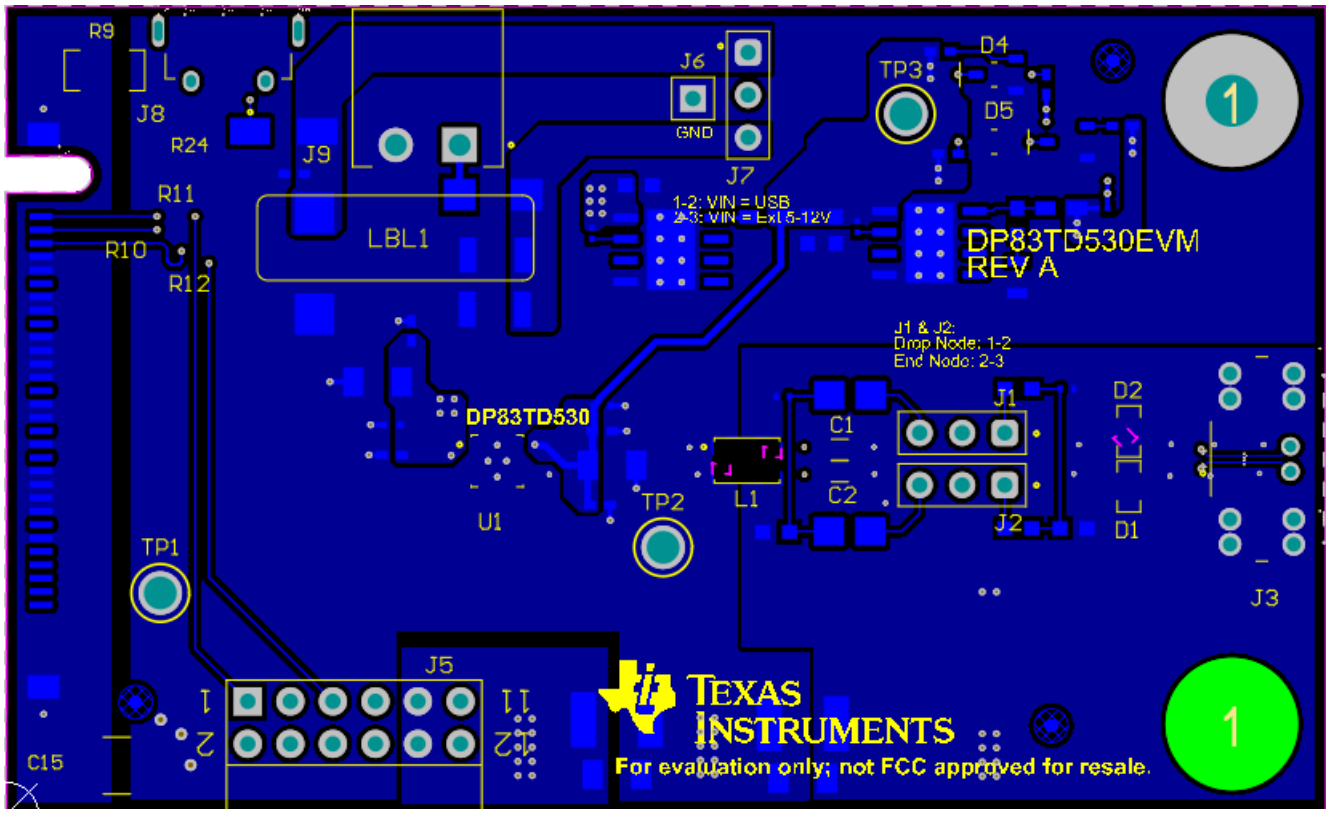


Figure 6-4. Bottom Layer

6.3 Bill of Materials (BOM)

ITEM NO	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY	SUPPLIER 1	SUPPLIER PART NUMBER 1
1	!PCB1	Printed Circuit Board	Any	DP83TD530EVM	1		
2	C1, C2, C3, C4	Chip Multilayer Ceramic Capacitors for General Purpose, 0402, 0.10uF, X7R, 15%, 10%, 50V	Murata	GRM155R71H104KE14D	4		
3	C5, C9	CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	TDK	CGA2B3X7R1H103K050BB	2	Digi-Key	445-6893-1-ND
4	C6, C10	CAP, CERM, 1 uF, 35 V, +/- 10%, X5R, 0402	MuRata	GRM155R6YA105KE11D	2	Digi-Key	490-10019-1-ND
5	C7, C11	0402 0.1 uF 10 V ±10 % Tolerance X5R SMT Multilayer Ceramic Capacitor	YAGEO	CC0402KRX5R6BB104	2	Digikey	311-1336-1-ND
6	C8, C12	CAP, CERM, 10 µF, 25 V,+/- 20%, X7R, AEC-Q200 Grade 1, 1206	MuRata	GRM31CR71E106MA12L	2	Digi-Key	490-6519-1-ND
7	C13, C14, C15	CAP, CERM, 4700 pF, 2000 V, +/- 10%, X7R, 1812	AVX	1812GC472KAT1A	3	Digi-Key	478-3003-1-ND
8	C16	CAP, CERM, 10 uF, 10 V, +/- 20%, X7R, 0603	MuRata	GRM188Z71A106MA73D	1	Mouser	81-GRM188Z71A106MA3D
9	C17, C18	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0603	Taiyo Yuden	UMK107AB7105KA-T	2	Digi-Key	587-3247-1-ND
10	C19	CAP, TA, 4.7 uF, 35 V, +/- 10%, 1.3 ohm, SMD	Vishay-Sprague	293D475X9035D2TE3	1	Digi-Key	718-1084-1-ND

11	C20	CAP, CERM, 0.1 µF, 10 V,+/- 10%, X7R, 0402	Kemet	C0402C104K8RACTU	1	Digi-Key	399-3520-1-ND
12	C21	CAP, CERM, 10 uF, 25 V, +/- 20%, X7R, AEC-Q200 Grade 1, 1210	TDK	CGA6P1X7R1E106M250AC	1	Digi-Key	445-5720-1-ND
13	C22	CAP, CERM, 22 uF, 16 V, +/- 20%, X7R, AEC-Q200 Grade 1, 1210	TDK	CGA6P1X7R1C226M250AC	1	Digi-Key	445-5723-1-ND
14	D1, D2	Diode, TVS, Bi, AEC-Q101, 0603	Panasonic	EZA-EG3W11AV	2		
15	D3	Diode, Schottky, 60 V, 1 A, AEC-Q101, SMA	ON Semiconductor	NRVBA160T3G	1		
16	D4, D5	LED, Green, SMD	Everlight	QTLP630C4TR	2		
17	D6	Diode Schottky 60 V 1A Surface Mount DO-214AC (SMA)	Comchip Technology	CDBA160-HF	1		
19	H1, H2	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	2	Digi-Key	H542-ND
20	H3, H4	Standoff, Hex, 0.5	Keystone	1902C	2	Digi-Key	36-1902C-ND
21	J1, J2, J7	Header, 100mil, 3x1, Gold, TH	Samtec	TSW-103-07-G-S	3	Digi-Key	SAM1029-03-ND
23	J4	Receptacle, 0.8mm, 30x2, Gold, Edge Mount	Samtec	ERF8-030-01-L-D-EM2-TR	1	Digi-Key	ERF8-030-01-L-D-EM2-TR-ND
24	J5	Header, 100mil, 6x2, Gold, R/A, TH	Samtec	TSW-106-08-G-D-RA	1	Digi-Key	SAM1037-06-ND
25	J6	Header, 100mil, 1pos, Gold, TH	Samtec	TSW-101-07-G-S	1	Digi-Key	SAM1029-01-ND
27	J9		Wurth Electronics	691322310002	1	Digikey	732-2088-ND
28	L1	Common Mode Filters / Chokes, L=240?H, L x W x T :	TDK	ACT1210E-241-2P-TL00	1	Digikey	445-ACT1210E-241-2P-TL00CT-ND

29	LBL1	Thermal Transfer Printable Labels, 0.650	Brady	THT-14-423-10	1	Newark	97C5133
30	Q1, Q2	Transistor, NPN, 60 V, 1 A, AEC-Q101, SOT-23	Diodes Inc.	DNBT8105-7	2	Digi-Key	DNBT8105DICT-ND
31	R1, R2	RES, 1.50 k, 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD071K5L	2		
32	R3, R4	Res Thin Film 1206 49.9 Ohm 0.1% 1W ±25ppm/C Pad SMD T/R	Vishay Thin Film	PHP01206E49R9BST5	2	Digikey	PHP49.9ACT-ND
33	R5, R6	RES, 101 k, 0.5%, 0.1 W, 0603	Yageo America	RT0603DRE07101KL	2		
34	R7, R8, R9	RES 1M OHM 1% 1/4W 1206	Yageo America	RC1206FR-071ML	3	Digi-Key	311-1.10MFRCT-ND
35	R10, R11, R12, R13, R17, R18, R24	RES, 0, 5%, 0.05 W, 0201	Vishay-Dale	CRCW02010000Z0ED	7	Newark	72M6743
36	R14	RES 0 OHM JUMPER 1/4W 0603	Stackpole Electronics	HCJ0603ZT0R00	1	Digikey	HCJ0603ZT0R00CT-ND
37	R16	RES, 2.87 k, 0.1%, 0.1 W, 0603	Susumu Co Ltd	RG1608P-2871-B-T5	1	Digi-Key	RG16P2.87KBCT-ND
38	R19	1 kOhms ±0.1% 0.125W, 1/8W Chip Resistor 0805 (2012 Metric) Anti-Sulfur, Automotive AEC-Q200, Moisture Resistant Thin Film	Vishay Dale	TNPU08051K00BZEN00	1		
39	R20, R21	RES, 470, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW0402470RJNED	2	Digi-Key	541-470JCT-ND
40	R22, R23	RES, 2.49 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04022K49FKED	2	Digi-Key	541-2.49KLCT-ND
41	TP1, TP2, TP3	Terminal, Turret, TH, Double	Keystone	1573-2	3	Digi-Key	36-1573-2-ND

42	U1	DP83TD530-Q1	Texas Instruments	DP83TD530-Q1	1		
43	U2	Automotive 500-mA, 40-V, ultra-low-IQ, low-dropout (LDO) linear regulator with power good 8-SO PowerPAD -40 to 150	Texas Instruments	TPS7B8633QDDARQ1	1		
44	U3	450-mA, wide VIN, low IQ, adjustable output, low-dropout regulator	Texas Instruments	TPS7B8601QDDARQ1	1		

7 Additional Information

7.1 Terminology

ACRONYM	DEFINITION
PHY	Physical Layer Transceiver
MAC	Media Access Controller
SMI	Serial Management Interface
MDIO	Management Data I/O
MDC	Management Data Clock
ED	Energy Detect
VBAT	Battery Supply Rail
VCC	Analog Supply Rail
VDDIO	Digital Supply Rail
OA-3pin	Open Alliance 3-pin Interface

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

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