User's Guide

DS160PR410EVM-RSC Evaluation Module (EVM)

Davor Glisic

ABSTRACT

The DS160PR410EVM-RSC and DS160PR410EVM-SMA evaluation modules provide a complete high-bandwidth platform for evaluating the signal conditioning features of the Texas Instruments DS160PR410 Quad-Channel PCI-Express Gen-4 Linear Redriver. These evaluation boards can be used for standard compliance testing, performance evaluation, and initial system prototyping.

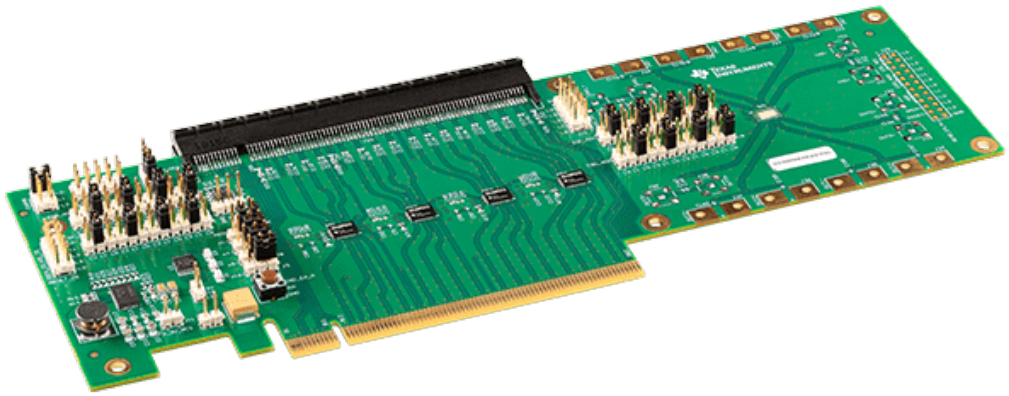

Figure 1-1. DS160PR410EVM-RSC - Top Side Photo

Table of Contents

List of Figures

List of Tables

Trademarks

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1 Introduction

The DS160PR410EVM-RSC evaluation module option features eight DS160PR410 linear redrivers that can extend the transmission distance of a PCIe Gen-4 x16 bus. It can directly be plugged into a PCIe slot on a Server / PC motherboard using one end of the board, and paired up with a PCIe Riser Card using the straddle mount connector attached to the other end of the board.

The DS160PR410EVM-SMA evaluation board option features a single, standalone DS160PR410 device with the high-speed I/Os routed to SMA connectors. The SMA connectors can interface to multiple connector types through commercially available breakout cables, adaptors, and boards (not included).

This document describes the DS160PR410EVM-RSC evaluation module.

1.1 Features

- PCIe x16 Riser Card option with eight 4-channel unidirectional linear redrivers operating at rates up to 25 Gbps
- Linear equalization for seamless support of link training and PCIe channel extension
- CTLE boosts up to 18 dB at 8 GHz
- Programmable device configuration through GPIO or I2C / SMBus
- Onboard 12-V to 3.3-V, 2-A step-down DC-DC converter
- Industrial temperature range: –40°C to 85°C
- Flow-through layout in 4 mm × 6 mm, 40-pin, leadless WQFN 0.4-mm pitch package

1.2 Applications

- PCI Express Gen-1, 2, 3, and 4
- High-speed interfaces up to 25 Gbps
- Enterprise server motherboard, workstation
- Enterprise storage
- Enterprise add-in card, end-point

1.3 Description

1.3.1 DS160PR410 4-Level I/O Control Inputs

Each DS160PR410 has six (GAIN, VOD, EQ1_ADDR1, EQ0_ADDR0, EN_SMB, and RX_DET) 4-level input pins that are used to control the configuration of the device. These 4-level inputs use a resistor divider to help set the four valid levels and provide a wider range of control settings.

Table 1-1. 4-Level Control Pin Settings

PIN LEVEL	PIN SETTING
L0	1 kΩ to GND
L1	13 kΩ to GND
L2	Float
L3	59 kΩ to GND

1.3.2 DS160PR410 Modes of Operation

Each DS160PR410 can be configured to operate in either Pin Mode, SMBus / I2C Slave Mode, or SMBus / I2C Master Mode. The mode of operation of the DS160PR410 is determined by the pin strap setting on the EN_SMB pin as shown in Table 1-2.

Table 1-2. Modes of Operation

EN_SMB PIN LEVEL	MODE OF OPERATION
L0	Pin Mode
L1	SMBus / I2C Master Mode
L2	Reserved
L3	SMBus / I2C Slave Mode

1.3.3 DS160PR410 SMBus / I2C Register Control Interface

Each DS160PR410 may be configured through a standard I2C or SMBus interface that may operate up to 1 MHz. The slave address of the DS160PR410 is determined by the pin strap settings on the EQ1_ADDR1 and EQ0_ADDR0 pins. The device can be configured for best signal integrity and power settings in the system using the I2C or SMBus interface. Certain status information is also available through this interface. The possible SMBus/I2C slave addresses are shown in Table 1-3.

Table 1-3. SMBus / I2C Slave Address Settings

EQ1_ADDR1 PIN LEVEL	EQ0_ADDR0 PIN LEVEL	8-BIT WRITE ADDRESS (HEX)	7-BIT ADDRESS (HEX)
L0	L0	0x30	0x18
L0	L1	0x32	0x19
L0	L2	0x34	0x1A
L0	L3	0x36	0x1B
L1	L0	0x38	0x1C
L1	L1	0x3A	0x1D
L1	L2	0x3C	0x1E
L1	L3	0x3E	0x1F
L2	L0	0x40	0x20
L2	L1	0x42	0x21
L2	L2	0x44	0x22
L2	L3	0x46	0x23
L3	L0	0x48	0x24
L3	L1	0x4A	0x25
L3	L2	0x4C	0x26
L3	L3	0x4E	0x27

1.3.4 DS160PR410 Equalization Control

Each channel of the DS160PR410 features a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. Table 1-4 shows available equalization gain that can be set through EQ0_ADDR0 and EQ1_ADDR1 control pins when operating in Pin Mode.

Table 1-4. Equalization Control Settings

EQ INDEX	EQ1_ADDR1 PIN LEVEL	EQ0_ADDR0 PIN LEVEL	CTLE BOOST AT 4 GHz (dB)	CTLE BOOST AT 8 GHz (dB)
0	L0	L0	–0.3	–0.8
1	L0	L1	0.4	1.3
2	L0	L2	3.3	5.7
3	L0	L3	3.8	7.1
4	L1	L0	4.9	8.4
5	L1	L1	5.2	9.1
6	L1	L2	5.4	9.8
7	L1	L3	6.5	10.7
8	L2	L0	6.7	11.3
9	L2	L1	7.7	12.6
10	L2	L2	8.7	13.6
11	L2	L3	9.1	14.4
12	L3	L0	9.4	15.0
13	L3	L1	10.3	15.9
14	L3	L2	10.6	16.5
15	L3	L3	11.8	17.8

The equalization gain of each channel of each device can also be set by writing to SMBus / I2C registers in Slave or Master Modes. Refer to the *DS160PR410 Programming Guide* (SNLU255) for details.

1.3.5 DS160PR410 RX Detect State Machine

Each DS160PR410 deploys an RX Detect state machine that governs the RX detection cycle as defined in the PCI Express specification. At power up or after a manually triggered event, the redriver determines whether or not a valid PCI Express termination is present at the far end of the link. The RX_DET pin of DS160PR410 provides additional flexibility to system designers to appropriately set the device in their desired mode, according to Table 1-5.

Table 1-5. 4-Level Control Pin Settings

PWDN PIN LEVEL	RXDET PIN LEVEL	DESCRIPTION
L	L0	Reserved
L	L1	Reserved
L	L2	PCI Express RX detection state machine is enabled. Recommended for PCI Express use cases. Pre Detect: Hi-Z, Post Detect: 50 Ω.
L	L3	PCI Express RX detection state machine is disabled. Recommended for non-PCI Express use cases. Inputs are always 50 Ω.
H	X	Manual reset, inputs are Hi-Z

1.3.6 DS160PR410 Equalization DC Gain Control

When operating in Pin Mode, the VOD and GAIN pins can be used to set the overall datapath DC (low frequency) gain of the DS160PR410 as shown in Table 1-6 and Table 1-7.

Table 1-6. VOD Control

VOD PIN LEVEL	VOD SETTING
L0	–6 dB
L1	–3.5 dB
L2	0 dB (Recommended for most use cases)
L3	–1.6 dB

Table 1-7. GAIN Control

GAIN PIN LEVEL	GAIN SETTING
L0	Reserved
L1	Reserved
L2	0 dB (Recommended for most use cases)
L3	3.5 dB

The DC gain of each channel of each device can also be set by writing to SMBus / I2C registers in Slave or Master Modes. Refer to the *DS160PR410 Programming Guide* (SNLU255) for details.

1.3.7 DS160PR410EVM-RSC Global Controls and Access Points

Table 1-8 shows DS160PR410EVM-RSC global controls that affect all devices on the board.

Table 1-8. EVM Global Controls

COMPONENT	NAME	FUNCTION / DESCRIPTION
J1	3x2 Header	EN_SMB control tied to EN_SMB pins of all 8 DS160PR410 devices on the EVM L0: All devices set to Pin Mode (Default) L1: All devices set to SMBus / I2C Master Mode L2: Reserved L3: SMBus / I2C Slave Mode
J2	5x2 Header	SMBus / I2C interface. All 8 DS160PR410 devices on the EVM are on the same bus and can be accessed through this interface.
J3	3x1 Header	PWDN control tied to PWDN1 and PWDN2 pins of all 8 DS160PR410 devices on the EVM PWDN tied to GND: All devices enabled (Default) PWDN tied to 3.3V_REG: All devices disabled. PWDN floating: Tie PCIe system PRSNT signal to PWDN using J5 for the PWDN control (optional for PCIe use case)
J4	3x1 Header	Access point to the WP (write protect) pin of the onboard EEPROM devices WP tied to GND: I2C Access to the EEPROM enabled WP floating: I2C Access to the EEPROM disabled (default)
J5	2x1 Header	Alternative PWDN Control PWDN floating: Use J3 for the PWDN control PWDN tied to PRSNT: PRSNT signal controls PWDN (optional for PCIe use case)
J6, J7, J8, J9	3x1 Headers	PCIe PRSNT Signal Controls Tie pins 1-2 on J6, J7, J8, and J9: Allow support any PCIe bus width (default) Tie pins 2-3 of J6, leave J7, J8, and J9 floating: Force x1 PCIe bus width Tie pins 2-3 of J7, leave J6, J8, and J9 floating: Force x4 PCIe bus width Tie pins 2-3 of J8, leave J6, J7, and J9 floating: Force x8 PCIe bus width Tie pins 2-3 of J9, leave J6, J7, and J8 floating: Force x16 PCIe bus width
J10	2x1 Header	Onboard regulator input. Apply 12 V when using the EVM as a standalone system. DO NOT APPLY power if plugging the EVM into a system as the power is provided through the gold finger connector (J13).
J11	2x1 Header	Onboard regulator 3.3-V output.
J12	2x1 Header	Access point to the GND reference.

1.3.8 DS160PR410EVM-RSC Downstream Devices Control

Table 1-9 shows DS160PR410EVM-RSC downstream devices controls that affect DS1-DS4 devices on the board.

Table 1-9. EVM Downstream Devices Controls

COMPONENT	NAME	FUNCTION / DESCRIPTION
J14	12x2 Header	EQ1_ADDR1 controls for each downstream device. Use pins 1-6 for configuring EQ1_ADDR1 pin of DS1 device. Use pins 7-12 for configuring EQ1_ADDR1 pin of DS2 device. Use pins 13-18 for configuring EQ1_ADDR1 pin of DS3 device. Use pins 19-24 for configuring EQ1_ADDR1 pin of DS4 device. Install a shunt to achieve L0, L1, or L3 level on the pin. Leave floating to achieve L2 level on the pin.
J15	12x2 Header	EQ0_ADDR0 controls for each downstream device. Use pins 1-6 for configuring EQ0_ADDR0 pin of DS1 device. Use pins 7-12 for configuring EQ0_ADDR0 pin of DS2 device. Use pins 13-18 for configuring EQ0_ADDR0 pin of DS3 device. Use pins 19-24 for configuring EQ0_ADDR0 pin of DS4 device. Install a shunt to achieve L0, L1, or L3 level on the pin. Leave floating to achieve L2 level on the pin.
J16	5x2 Header	Downstream Devices Global Controls VOD: L0 (pins 1-2): –6 dB VOD Setting on all downstream devices VOD: L1 (pins 3-4): –3.5 dB VOD Setting on all downstream devices VOD: L2 (floating pins 1-6): 0 dB VOD Setting on all downstream devices (default) VOD: L3 (pins 5-6): –1.6 dB VOD Setting on all downstream devices GAIN: L2 (floating pins 7-8): 0 dB GAIN Setting on all downstream devices (default) GAIN: L3 (pins 7-8): 3.5 dB GAIN Setting on all downstream devices RX_DET: L2 (floating pins 9-10):RX Detect state machine enabled on all downstream devices (default) RX_DET: L3 (pins 9-10): RX Detect state machine disabled on all downstream devices Install a shunt to achieve L0, L1, or L3 level on the pin. Leave floating to achieve L2 level on the pin.

1.3.9 DS160PR410EVM-RSC Upstream Devices Control

Table 1-10 shows DS160PR410EVM-RSC upstream devices controls that affect US1-US4 devices on the board.

Table 1-10. EVM Upstream Devices Controls

COMPONENT	NAME	FUNCTION / DESCRIPTION
J17	12x2 Header	EQ1_ADDR1 controls for each upstream device. Use pins 1-6 for configuring EQ1_ADDR1 pin of US1 device. Use pins 7-12 for configuring EQ1_ADDR1 pin of US2 device. Use pins 13-18 for configuring EQ1_ADDR1 pin of US3 device. Use pins 19-24 for configuring EQ1_ADDR1 pin of US4 device. Install a shunt to achieve L0, L1, or L3 level on the pin. Leave floating to achieve L2 level on the pin.
J18	12x2 Header	EQ0_ADDR0 controls for each upstream device. Use pins 1-6 for configuring EQ0_ADDR0 pin of US1 device. Use pins 7-12 for configuring EQ0_ADDR0 pin of US2 device. Use pins 13-18 for configuring EQ0_ADDR0 pin of US3 device. Use pins 19-24 for configuring EQ0_ADDR0 pin of US4 device. Install a shunt to achieve L0, L1, or L3 level on the pin. Leave floating to achieve L2 level on the pin.

Table 1-10. EVM Upstream Devices Controls (continued)

COMPONENT	NAME	FUNCTION / DESCRIPTION
J19	5x2 Header	Upstream Devices Global Controls VOD: L0 (pins 1-2): –6 dB VOD Setting on all upstream devices VOD: L1 (pins 3-4): –3.5 dB VOD Setting on all upstream devices VOD: L2 (floating pins 1-6): 0 dB VOD Setting on all upstream devices (default) VOD: L3 (pins 5-6): –1.6 dB VOD Setting on all upstream devices GAIN: L2 (floating pins 7-8): 0 dB GAIN Setting on all upstream devices (default) GAIN: L3 (pins 7-8): 3.5 dB GAIN Setting on all upstream devices RX_DET: L2 (floating pins 9-10):RX Detect state machine enabled on all upstream devices (default) RX_DET: L3 (pins 9-10): RX Detect state machine disabled on all upstream devices Install a shunt to achieve L0, L1, or L3 level on the pin. Leave floating to achieve L2 level on the pin.

1.4 Quick-Start Guide (Pin Mode)

1. Check that the shunts are at the following positions as shown in Figure 1-1.
   - The redrivers are configured to operate in Pin Mode (EN_SMB pins tied to L0 using J1 header).
   - The redrivers are enabled (PWDN pins tied to GND using J3 header). Alternatively, for PCIe applications, the PWDN pins may be driven by PCIe Present (PRSNT) signal by leaving J3 open and placing a shunt across pins 1 and 2 of J5.
   - The board is configured for any PCIe bus width (PRSNT signal controls set as shown in Figure 1-1 using J6, J7, J8, and J9 headers).
   - DC Gain of the RX CTLEs of all redrivers is set to 0 dB by leaving J16 (pins 7-8) open for the downstream redrivers and by leaving J19 (pins 7-8) open for the upstream redrivers.
   - VOD of all redrivers is set to 0 dB by leaving J16 (pins 1-2, 3-4, and 5-6) open for the downstream redrivers and by leaving J19 (pins 1-2, 3-4, and 5-6) open for the upstream redrivers.
   - RX_Detect state machine of all redrivers is enabled by leaving J16 (pins 9-10) open for the downstream redrivers and by leaving J19 (pins 9-10) open for the upstream redrivers.
   - EQ level of the RX CTLEs of all redrivers is set to 8.4 dB at 8 GHz by using J14 and J15 for the downstream redrivers, and J17 and J18 for the upstream redrivers.
2. If necessary, adjust EQ levels of the downstream and/or upstream redrivers by arranging shunts on J14 and J15 for the downstream redrivers, and J17 and J18 for the upstream redrivers.
3. Plug the EVM into a PCIe x16 server motherboard slot.
4. Install a compatible PCIe end point card into the EVM's straddle connector.

1.5 Quick-Start Guide (SMBus Slave Mode)

1. Configure all devices to operate in the SMBus Slave Mode by setting their EN_SMB pins to the L3 level. This is accomplished by placing a shunt on J1 to L3 location.
2. Set a unique SMBus Slave address for each device by placing shunts in the following arrangement:
   - On J14 connector, place shunts in L0 locations for all downstream devices (DS1-DS4).
   - On J15 connector, place a shunt to L0 location for the device DS1, to L1 location for DS2, to L3 location for DS4; no shunt for the DS3 sets its EQ0_ADD0 pin to the L2 level.
   - On J17 connector, place shunts in L1 locations for all upstream devices (US1-US4).
   - On J18 connector, place a shunt to L0 location for the device US1, to L1 location for US2, to L3 location for US4; no shunt for the US3 sets its EQ0_ADD0 pin to the L2 level.
3. Enable all devices by pulling their PWDN pins to GND. This is accomplished by placing a shunt on J3 between PWDN and GND.
4. Connect USB2ANY Adapter to J2 (Note that the USB2ANY Adapter is not supplied with the DS160PR410EVM-RSC).
5. Install SigCon Architect Version 3.0.0.10 application. It comes with the DS160PR410 profile.
6. Plug the EVM into a PCIe x16 server motherboard slot.
7. Install a compatible PCIe end point card into the EVM' s straddle connector.
8. Start the SigCon Architect application.
9. In the DS160PR410 Configuration Page, click on "Auto Detect" box to detect the EVM Model. If necessary, edit devices addresses in the Edit Device Addresses box.

10. Select Low Level Page to initialize the register map tree in the application. Failure to perform this step may cause the application to crash.
11. In the DS160PR410 High Level Page, select Block Diagram as shown in Figure 1-1.
12. Select desired EQ Settings and Driver VOD.
13. Select device(s) to which you want to apply the selected settings and click Apply to All Channels.

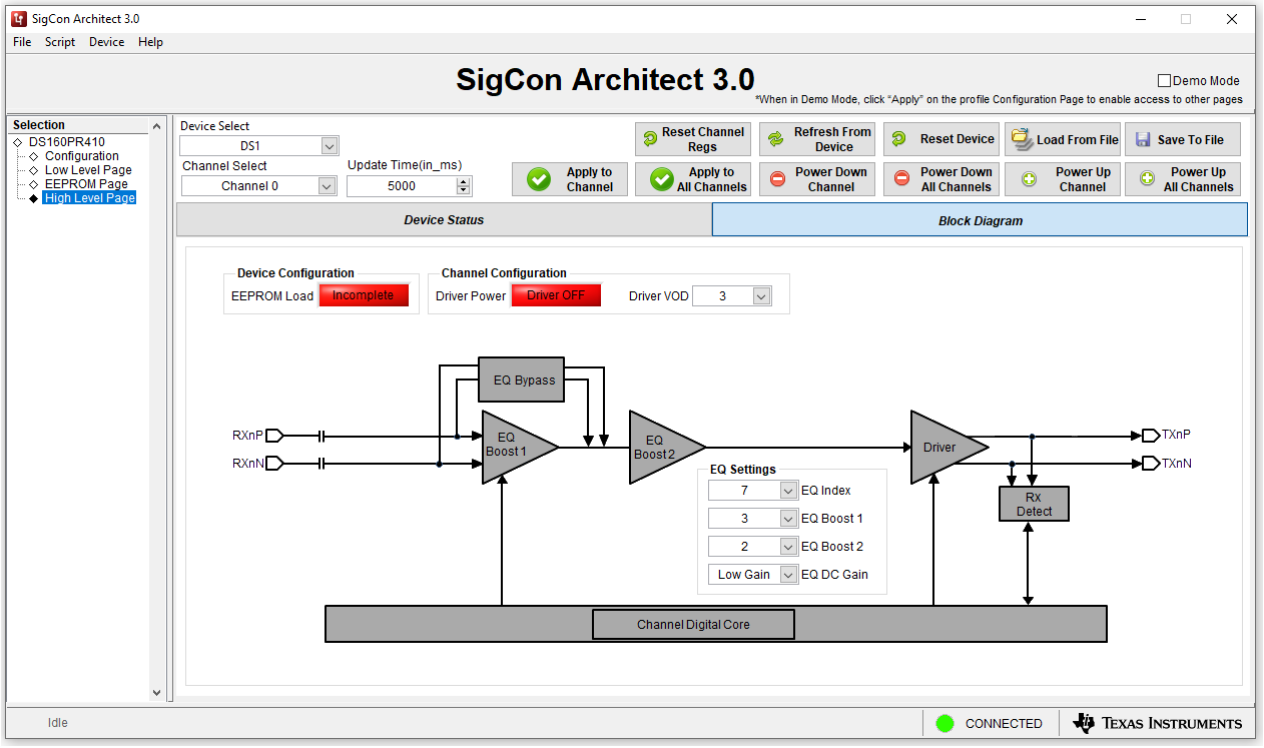

Figure 1-1. SigCon Architect DS160PR410 High Level Page

2 Test Setup and Results

Figure 2-1 shows a typical system setup with the DS160PR410EVM-RSC placed between a CPU on a server motherboard and an PCIe end point (Network Interface Card or NIC). Additional "Extender" cards are inserted to increase the channel loss and demonstrate the redriver's ability to extend the reach.

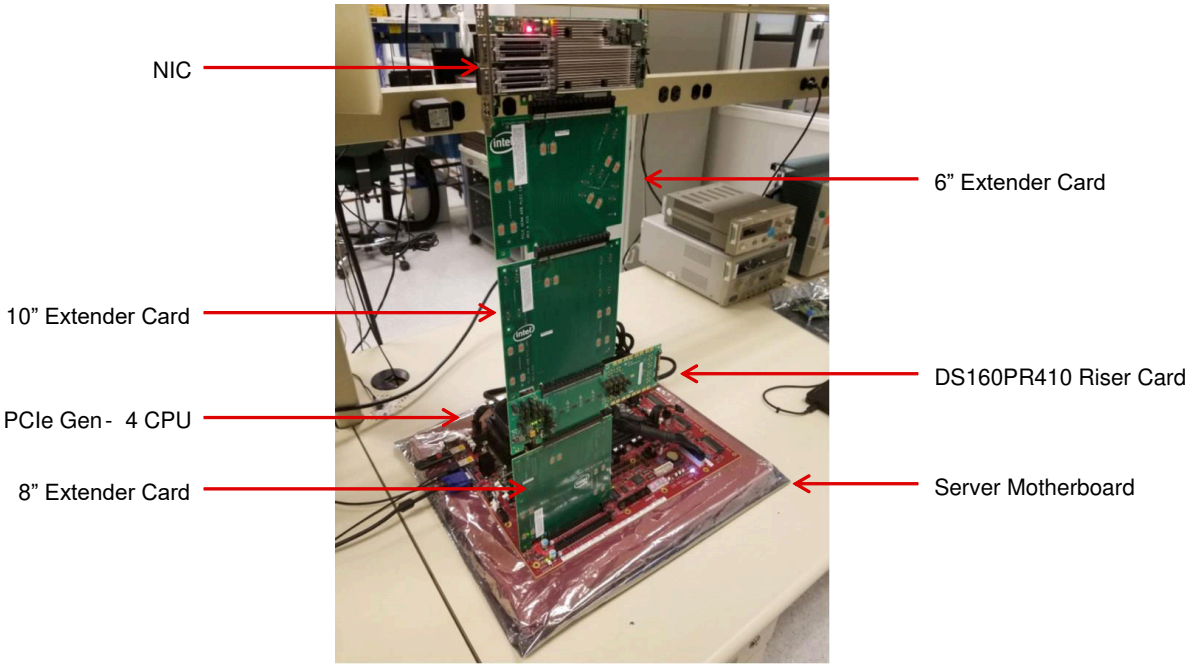

Figure 2-1. Example Test Setup

Figure 2-2 is a typical test result achieved with a system shown in Figure 2-1. As the result indicates, the end point (Mellanox NIC) with the DS160PR410EVM-RSC placed in the datapath achieves a stable Gen4, x16 PCIe link.

```
Address Decoding Per Root Port...
DMI uses subtractive decode.

*********************************************************************
*                                                                   *
*   Socket 1 (R0) PCIe Port Mappings                                *
*   Segment #0, Buses 0x00,0x80,0x94,0xae,0xc8,0xe2,0xfe,0xff       *
*                                                                   *
*********************************************************************

=============================================================================================================
| PCIe port |          0a          | 0b | 0c | 0d | 1a  | 1b | 1c | 1d | 2a  | 2b | 2c | 2d | 3a | 3b | 3c | 3d |
-------------------------------------------------------------------------------------------------------------
| config as |          x16         |    |    |    | x16 |    |    |    | x16 |    |    |    | x4 | x4 | x4 | x4 |
-------------------------------------------------------------------------------------------------------------
|   width   |          x16         |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
|   speed   |         Gen4         |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
| slot/down |         slot         |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
|  ASPM en  |          L1          |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
| secbusno  |          95h         |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
| subbusno  |          95h         |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
| linkstate |        Up.L0         |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
| VendorID  | Mellanox Technologies |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
| DeviceID  |         1019h        |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
|   RevID   |          00h         |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
|  ASPM en  |          no          |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
=============================================================================================================


Address Decoding Per Root Port...
Port 0a MBAS=          C8000000h MLIM=          C80FFFFFh
```

Figure 2-2. Example Test Results

3 Board Layout

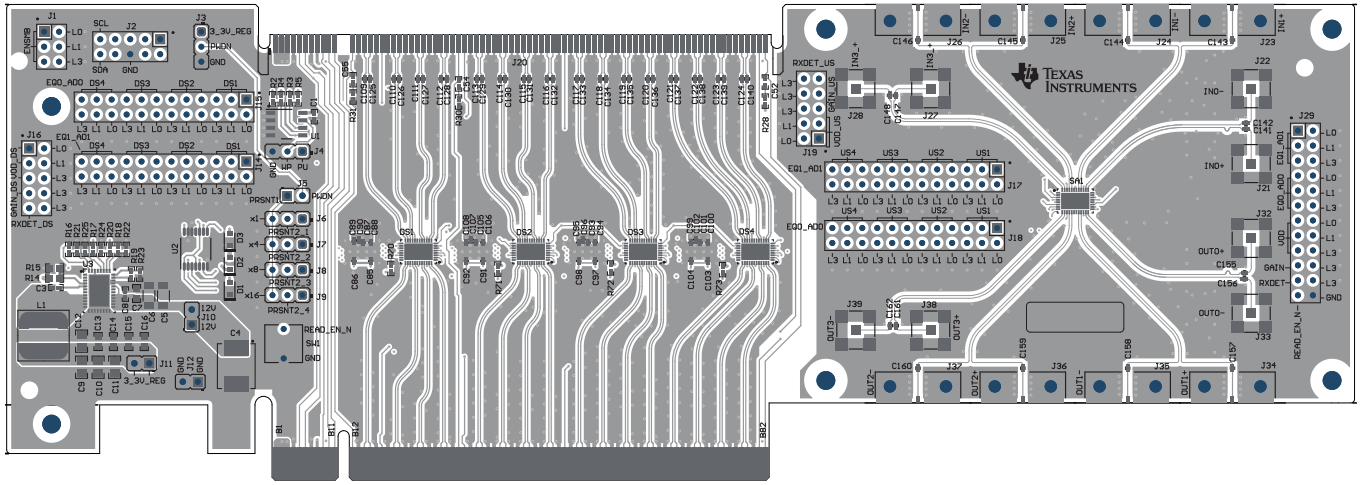

Figure 3-1. Top Layer

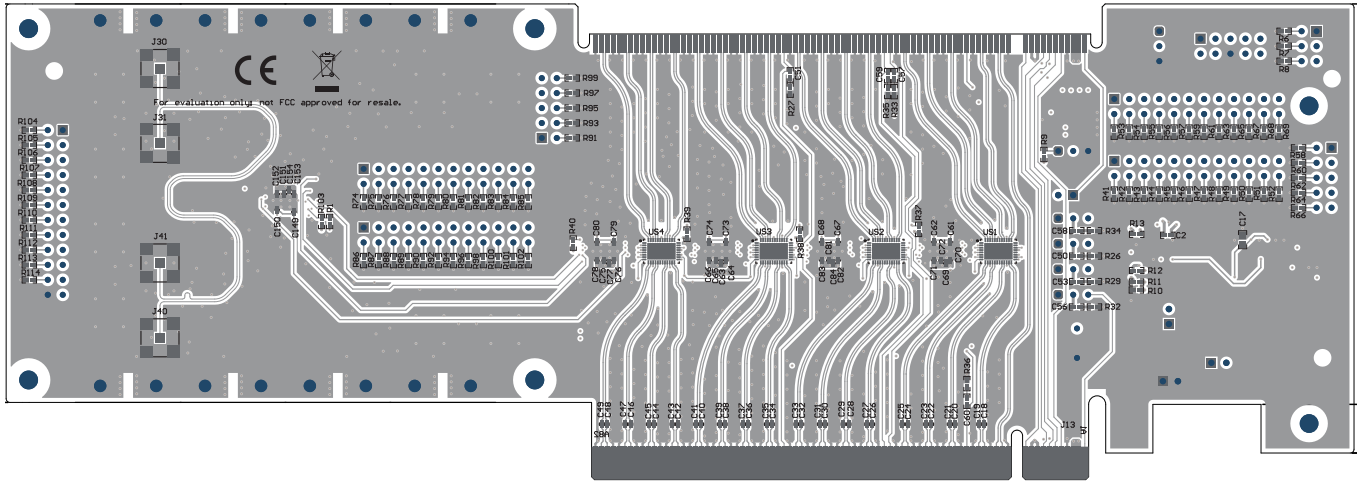

Figure 3-2. Bottom Layer

4 Schematics

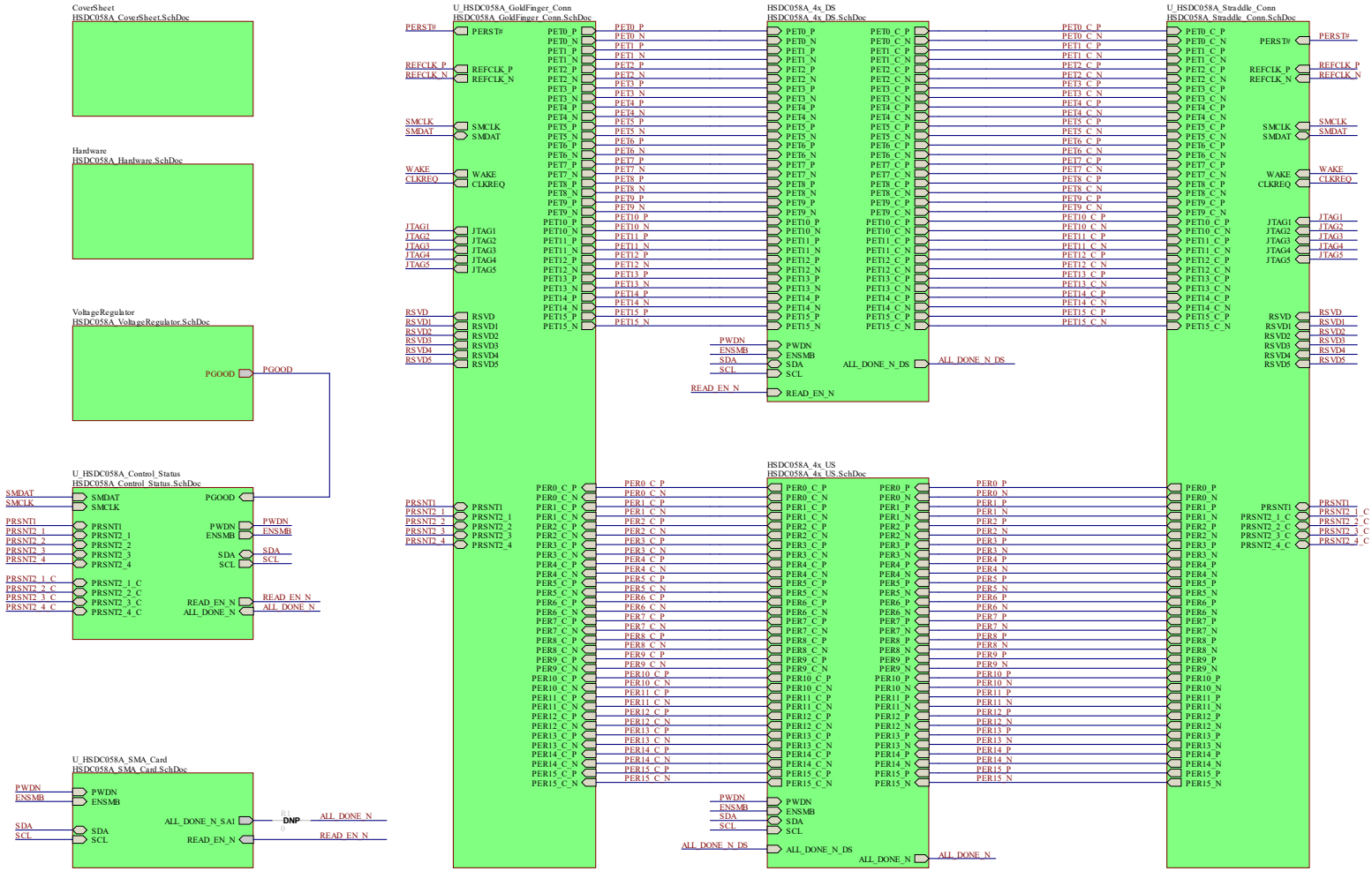

Figure 4-1. Top Level Schematic Page

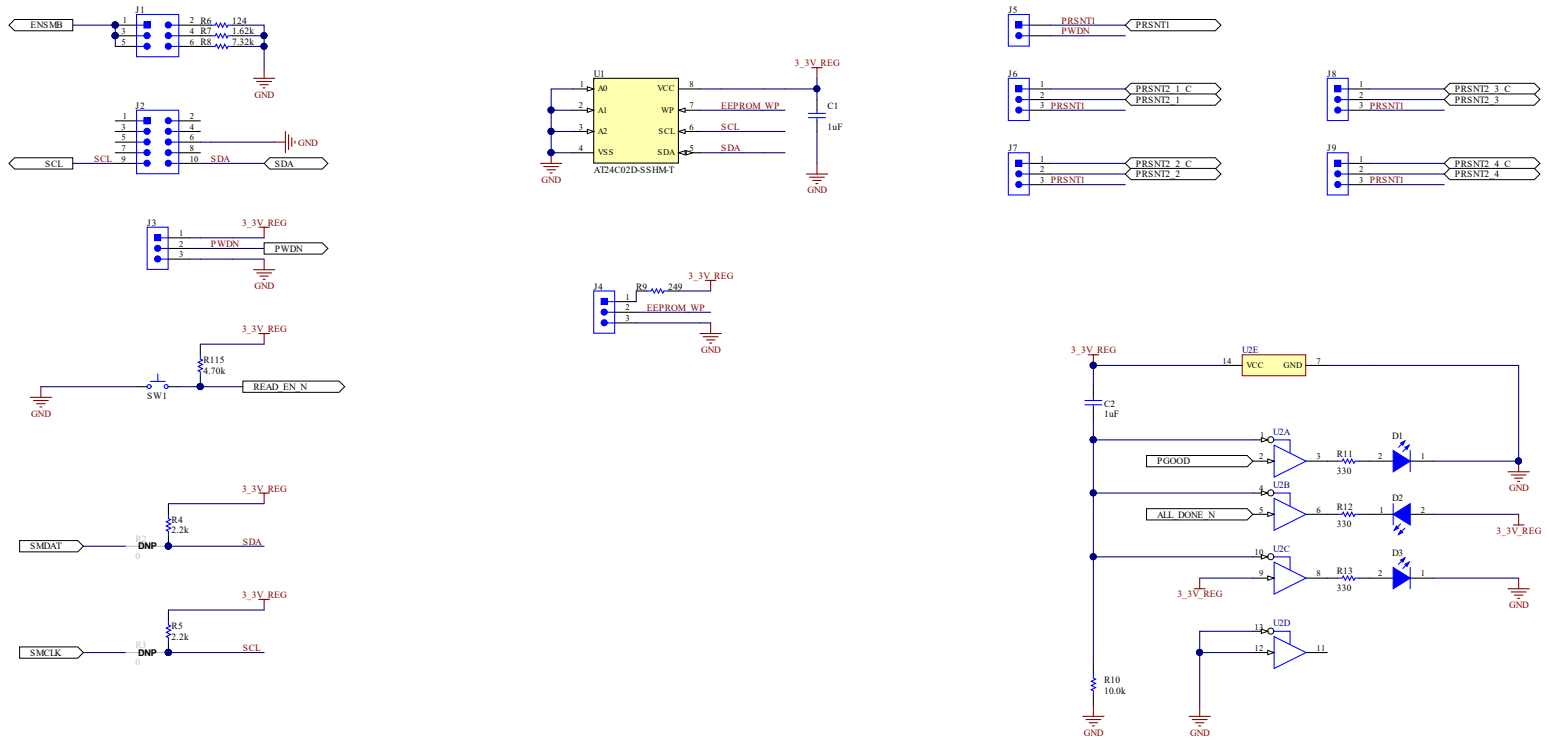

Figure 4-2. Control and Status Schematic Page

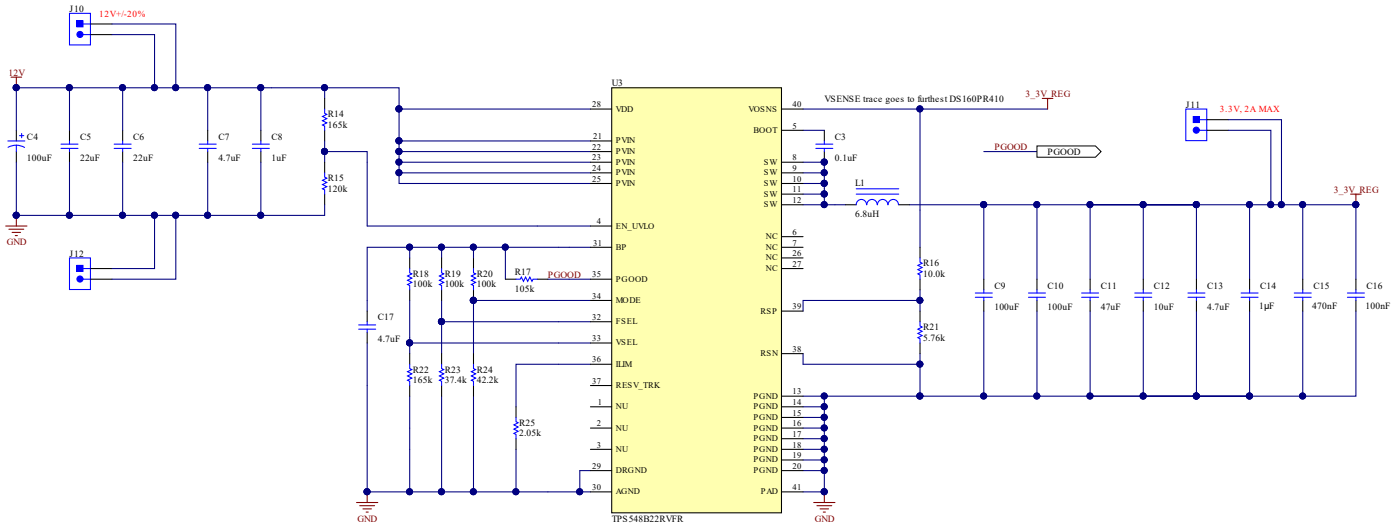

Figure 4-3. Voltage Regulator Schematic Page

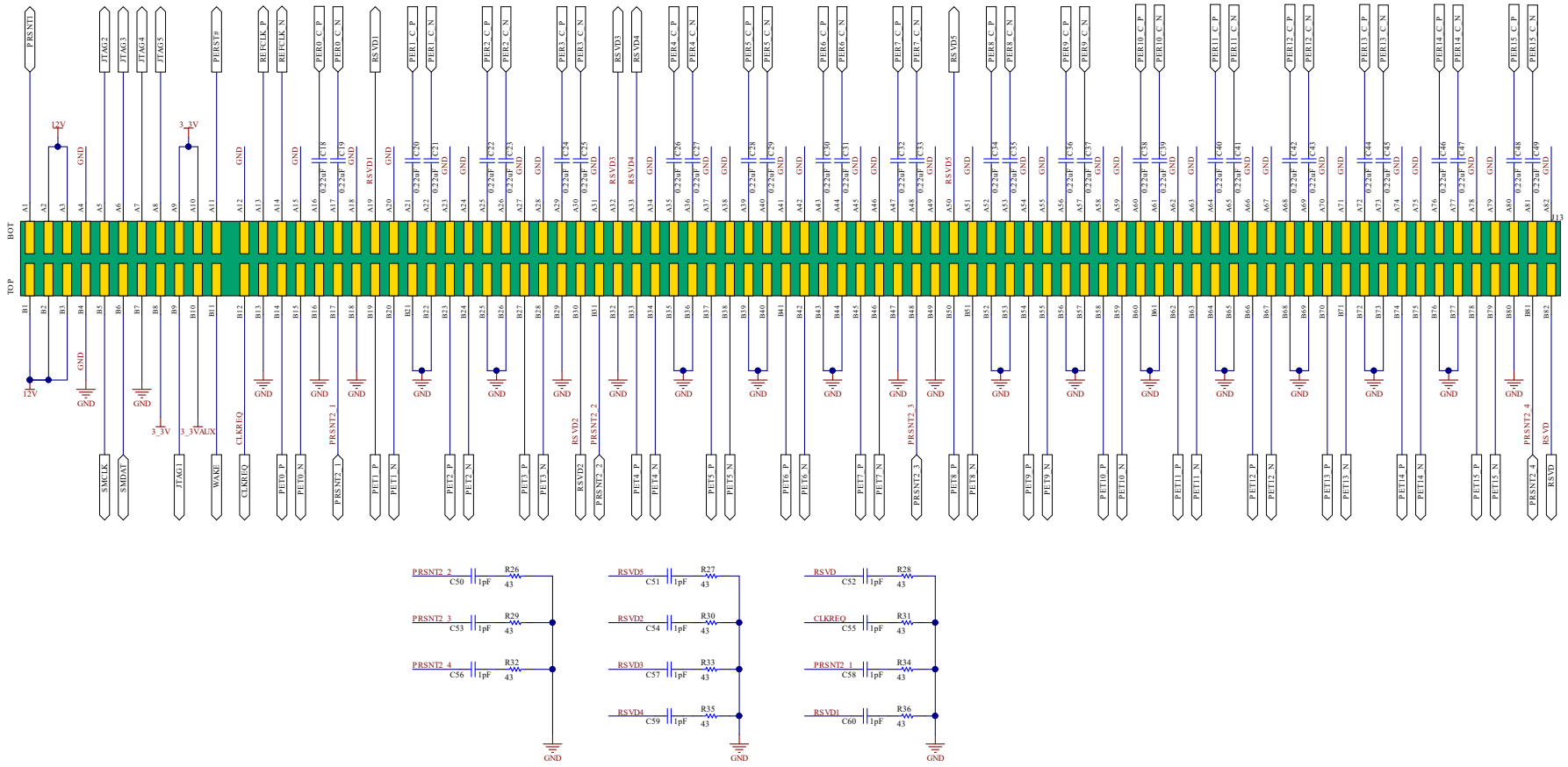

Figure 4-4. Gold Finger Connector Schematic Page

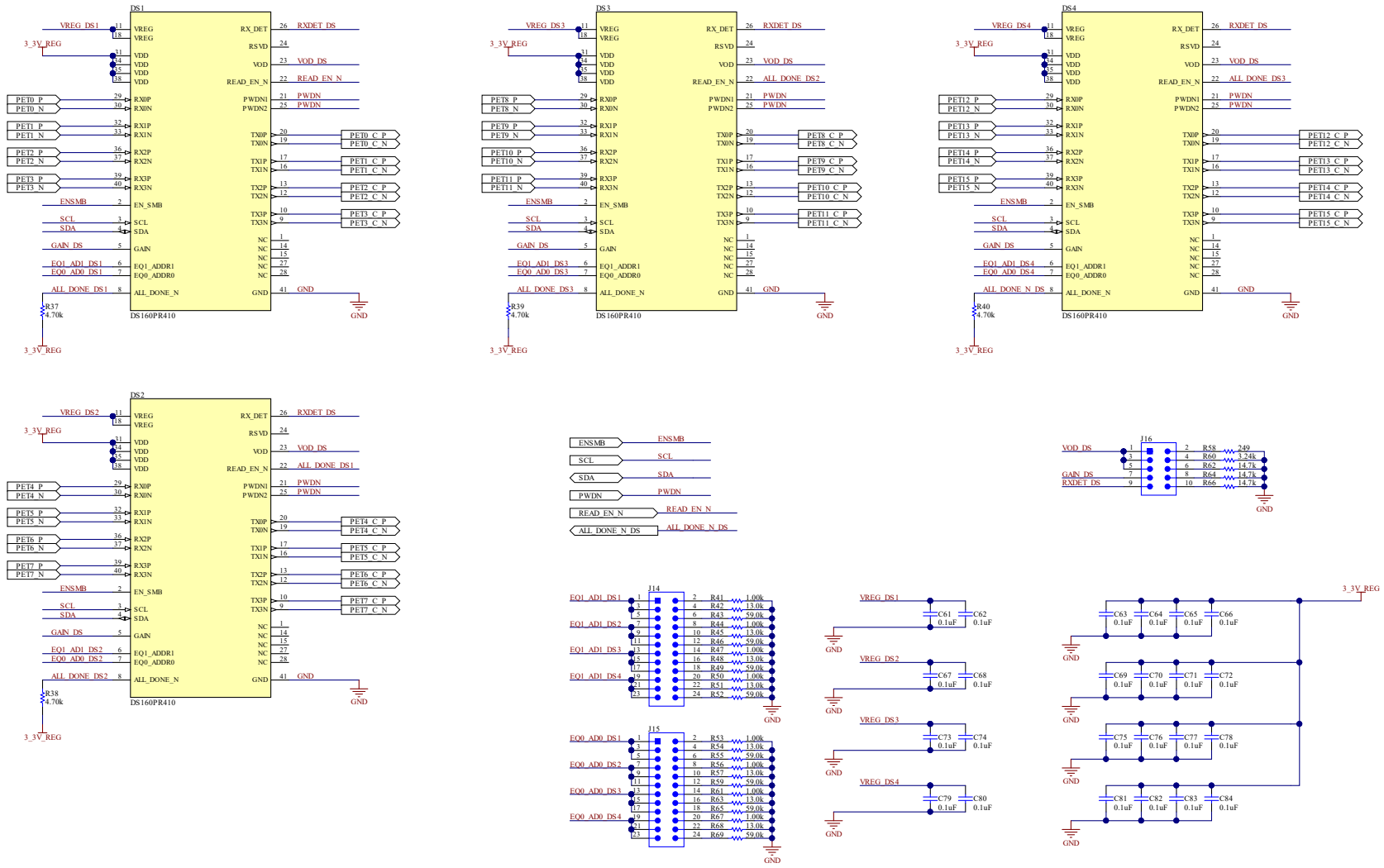

Figure 4-5. Downstream Devices Schematic Page

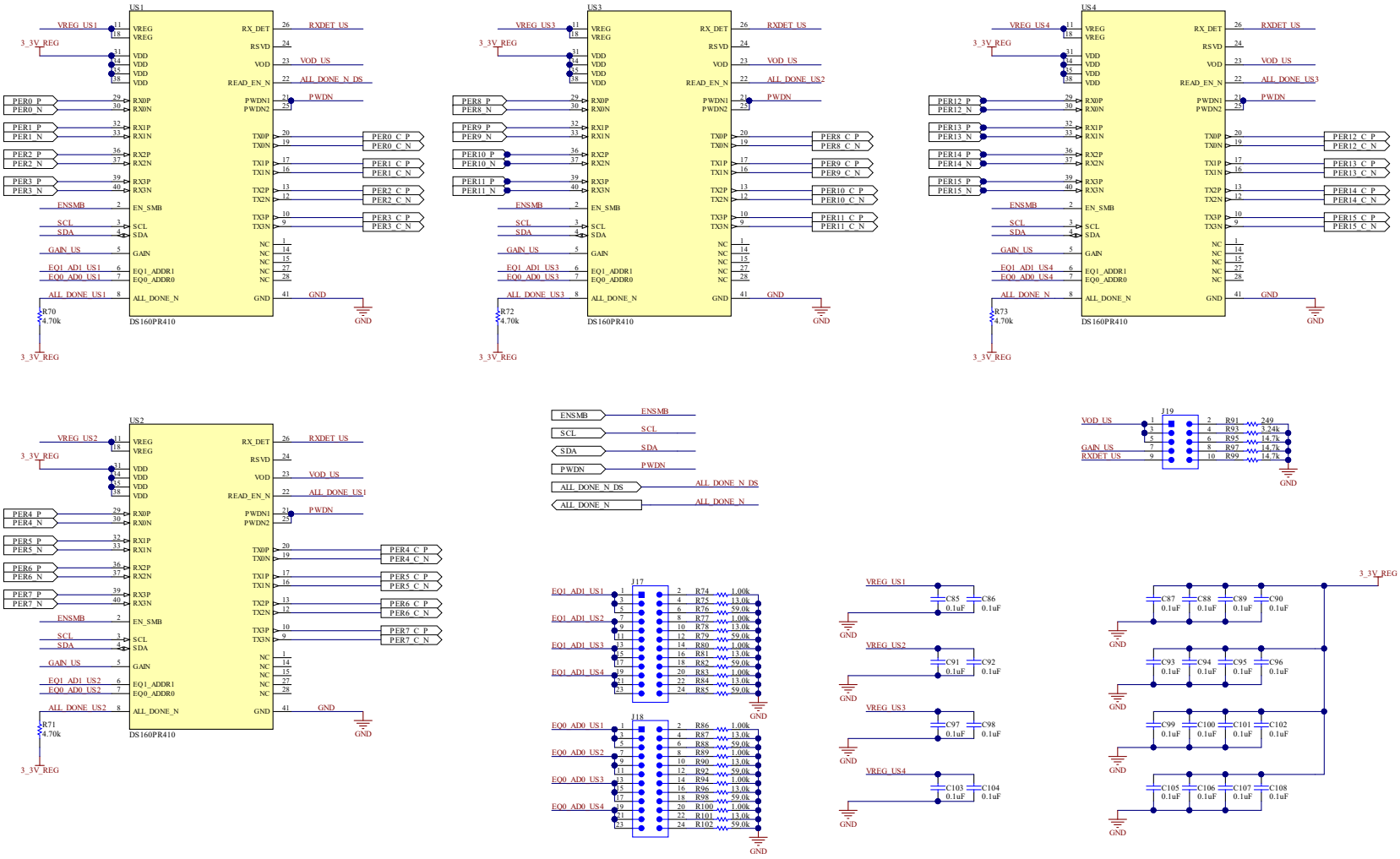

Figure 4-6. Upstream Devices Schematic Page

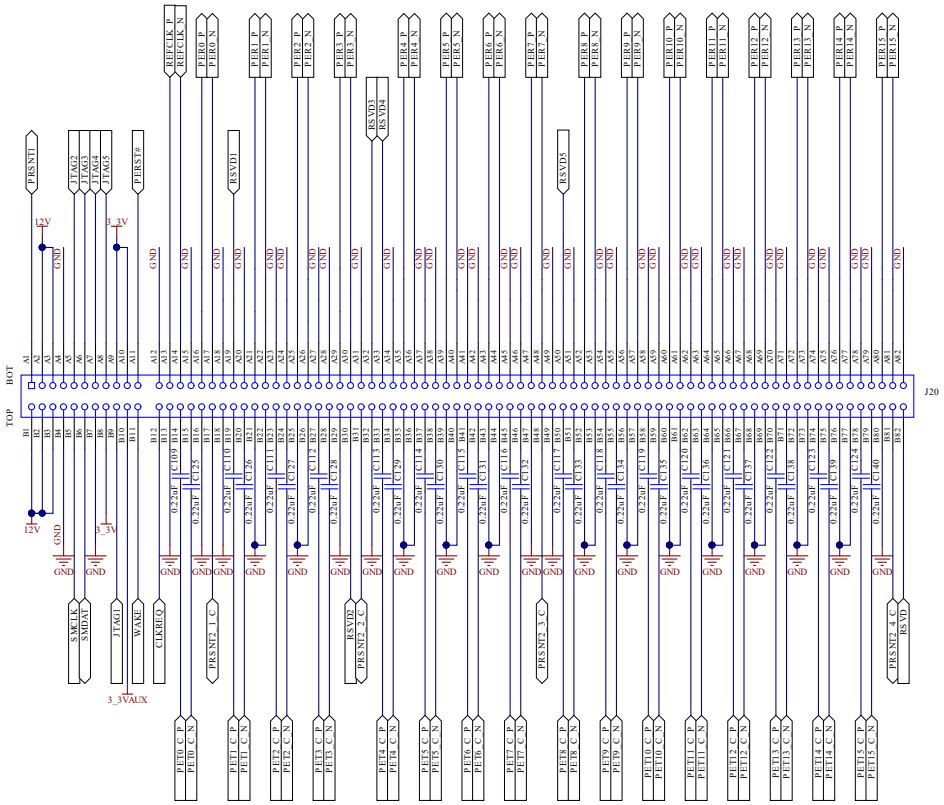

Figure 4-7. Straddle Connector Schematic Page

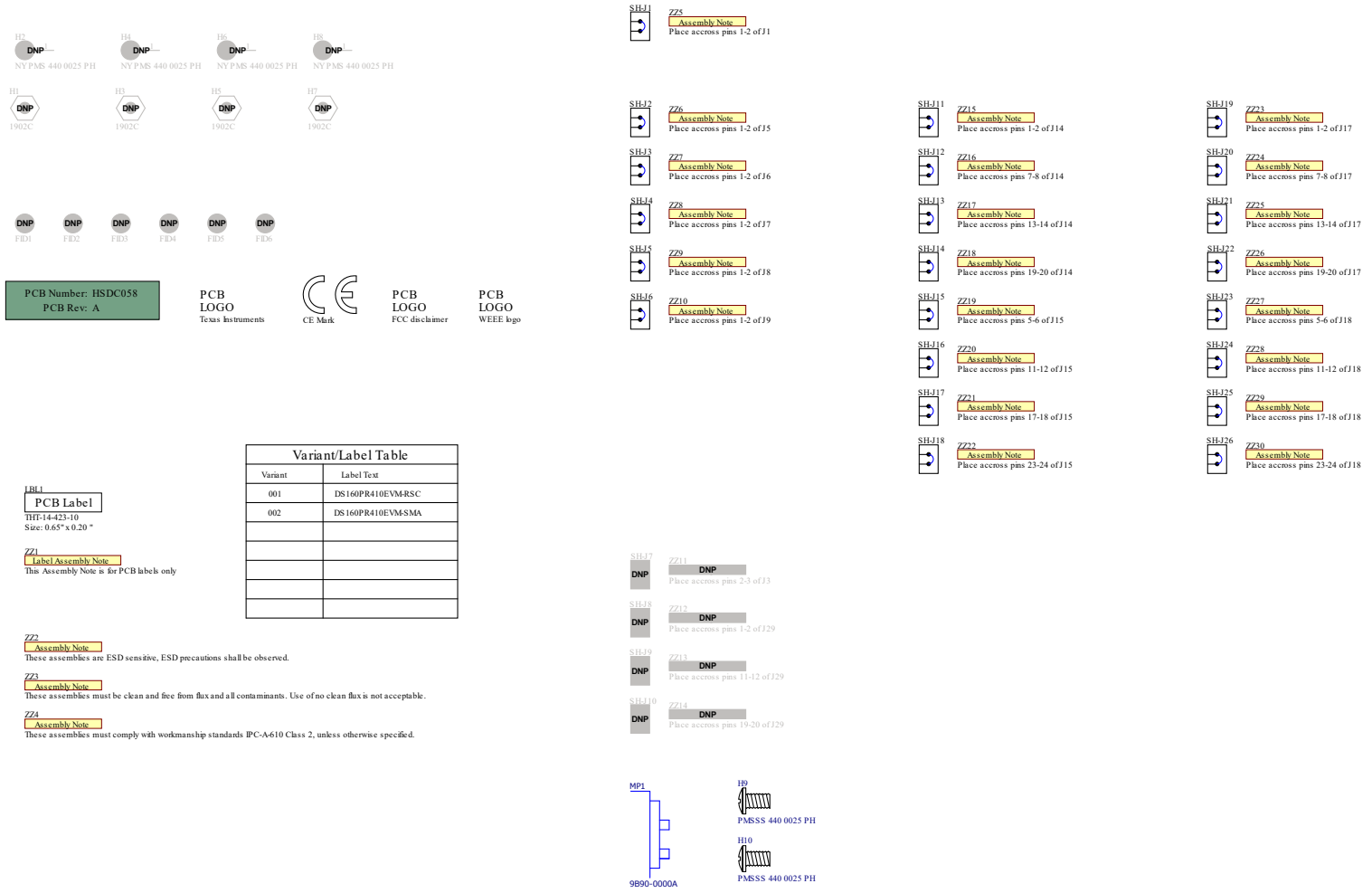

Figure 4-8. Hardware Page

5 Bill of Materials

Table 5-1. Bill of Materials

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
!PCB1	1		Printed Circuit Board		HSDC058	Any
C1, C2, C8	3	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X5R, 0402	0402	C1005X5R1E105K050BC	TDK
C3	1	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X5R, 0402	0402	GRM155R61E104KA87D	MuRata
C4	1	100uF	CAP, TA, 100 uF, 25 V, +/- 10%, 0.1 ohm, SMD	7360-38	T495E107K025ATE100	Kemet
C5, C6	2	22uF	CAP, CERM, 22 uF, 25 V, +/- 20%, X5R, 1206_190	1206_190	TMK316BBJ226ML-T	Taiyo Yuden
C7, C17	2	4.7uF	CAP, CERM, 4.7 uF, 25 V, +/- 10%, X6S, 0603	0603	GRM188C81E475KE11D	MuRata
C9, C10	2	100uF	CAP, CERM, 100 uF, 6.3 V, +/- 20%, X5R, 0805	0805	GRM21BR60J107M	MuRata
C11	1	47uF	CAP, CERM, 47 uF, 6.3 V, +/- 20%, X5R, 0805	0805	GRM219R60J476ME44D	MuRata
C12	1	10uF	CAP, CERM, 10 uF, 6.3 V, +/- 10%, X5R, 0805	0805	GRM219R60J106KE19D	MuRata
C13	1	4.7uF	CAP, CERM, 4.7 uF, 6.3 V, +/- 10%, X5R, 0603	0603	GRM188R60J475KE19D	MuRata
C14	1	1uF	CAP, CERM, 1 uF, 6.3 V, +/- 10%, X7R, 0603	0603	GRM188R70J105KA01D	MuRata
C15	1	0.47uF	CAP, CERM, 0.47 uF, 6.3 V, +/- 10%, X7R, 0603	0603	GRM188R70J474KA01D	MuRata
C16	1	0.1uF	CAP, CERM, 0.1 uF, 6.3 V, +/- 10%, X7R, 0603	0603	GRM188R70J104KA01D	MuRata
C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C128, C129, C130, C131, C132, C133, C134, C135, C136, C137, C138, C139, C140	64	0.22uF	CAP, CERM, 0.22 uF, 10 V, +/- 20%, X5R, 0201	0201	LMK063BJ224MP-F	Taiyo Yuden
C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60	11	1pF	CAP, CERM, 1 pF, 50 V, +/- 10%, C0G/NP0, 0402	0402	GJM1555C1H1R0BB01D	MuRata
C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108	48	0.1uF	CAP, CERM, 0.1 uF, 6.3 V, +/- 10%, X5R, 0201	0201	C0603X5R0J104K030BC	TDK
D1, D2, D3	3	Green	LED, Green, SMD	2x1.4mm	LG M67K-G1J2-24-Z	OSRAM
DS1, DS2, DS3, DS4, US1, US2, US3, US4	8		DS160PR410, RNQ0040A (WQFN-40)	RNQ0040A	DS160PR410	Texas Instruments

Table 5-1. Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
H9, H10	2		MACHINE SCREW PAN PHILLIPS 4-40	Machine Screw, 4-40, 1/4 inch	PMSSS 440 0025 PH	B and F Fastener Supply
J1	1		Header, 100mil, 3x2, Gold, TH	3x2 Header	TSW-103-07-G-D	Samtec
J2, J16, J19	3		Header, 100mil, 5x2, Gold, TH	5x2 Header	TSW-105-07-G-D	Samtec
J3, J4, J6, J7, J8, J9	6		Header, 2.54mm, 3x1, Gold, TH	Header, 2.54mm, 3x1, TH	961103-6804-AR	3M
J5, J10, J11, J12	4		Header, 2.54mm, 2x1, TH	Header, 2.54mm, 2x1, TH	961102-6404-AR	3M
J14, J15, J17, J18	4		Header, 100mil, 12x2, Gold, TH	12x2 Header	TSW-112-07-G-D	Samtec
J20	1		Receptacle, 1mm, 82x2, Gold, SMT	Receptacle, 1mm, 82x2, SMT	GWE82DHRN-T9410	Sullins Connector Solutions
L1	1	6.8uH	Inductor, Drum Core, Ferrite, 6.8 uH, 3.2 A, 0.04 ohm, SMD	SDR0805	SDR0805-6R8ML	Bourns
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
MP1	1		PCI bracket	PCI_BRCKT_NPTH_2	9B90-0000A	Gompf Brackets, Inc.
R4, R5	2	2.2k	RES, 2.2 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K20JNED	Vishay-Dale
R6	1	124	RES, 124, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402124RFKED	Vishay-Dale
R7	1	1.62k	RES, 1.62 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K62FKED	Vishay-Dale
R8	1	7.32k	RES, 7.32 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04027K32FKED	Vishay-Dale
R9, R58, R91	3	249	RES, 249, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF2490X	Panasonic
R10	1	10.0k	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	AC0402FR-0710KL	Yageo America
R11, R12, R13	3	330	RES, 330, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402330RJNED	Vishay-Dale
R14	1	165k	RES, 165 k, 1%, 0.1 W, 0603	0603	RC0603FR-07165KL	Yageo
R15	1	120k	RES, 120 k, 1%, 0.1 W, 0603	0603	RC0603FR-07120KL	Yageo
R16	1	10.0k	RES, 10.0 k, 1%, 0.063 W, 0402	0402	RC0402FR-0710KL	Yageo America
R17	1	105k	RES, 105 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402105KFKED	Vishay-Dale
R18, R19, R20	3	100k	RES, 100 k, 1%, 0.0625 W, 0402	0402	RC0402FR-07100KL	Yageo America
R21	1	5.76k	RES, 5.76 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04025K76FKED	Vishay-Dale
R22	1	165k	RES, 165 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF1653X	Panasonic
R23	1	37.4k	RES, 37.4 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040237K4FKED	Vishay-Dale
R24	1	42.2k	RES, 42.2 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040242K2FKED	Vishay-Dale

Table 5-1. Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
R25	1	2.05k	RES, 2.05 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K05FKED	Vishay-Dale
R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36	11	43	RES, 43, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040243R0JNED	Vishay-Dale
R37, R38, R39, R40, R70, R71, R72, R73	8	4.70k	RES, 4.70 k, 1%, 0.063 W, 0402	0402	CRG0402F4K7	TE Connectivity
R41, R44, R47, R50, R53, R56, R61, R67, R74, R77, R80, R83, R86, R89, R94, R100	16	1.00k	RES, 1.00 k, 1%, 0.063 W, 0402	0402	MCR01MZPF1001	Rohm
R42, R45, R48, R51, R54, R57, R63, R68, R75, R78, R81, R84, R87, R90, R96, R101	16	13.0k	RES, 13.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040213K0FKED	Vishay-Dale
R43, R46, R49, R52, R55, R59, R65, R69, R76, R79, R82, R85, R88, R92, R98, R102	16	59.0k	RES, 59.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040259K0FKED	Vishay-Dale
R60, R93	2	3.24k	RES, 3.24 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04023K24FKED	Vishay-Dale
R62, R64, R66, R95, R97, R99	6	14.7k	RES, 14.7 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040214K7FKED	Vishay-Dale
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J11, SH-J12, SH-J13, SH-J14, SH-J15, SH-J16, SH-J17, SH-J18, SH-J19, SH-J20, SH-J21, SH-J22, SH-J23, SH-J24, SH-J25, SH-J26	22	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
SW1	1		Switch, Tactile, SPST-NO, 0.02A, 15V, TH	6.0x5.0x6mm	EVQ-21505R	Panasonic
U1	1		I2C-Compatible (2-wire) Serial EEPROM 2-Kbit (256 x 8), SOIC-8	SOIC-8	AT24C02D-SSHM-T	Atmel
U2	1		Quadruple Bus Buffer Gate With 3-State Outputs, PW0014A, LARGE T and R	PW0014A	SN74LVC125APWRG3	Texas Instruments
U3	1		1.5-V to 16-V VIN, 4.5-V to 22-V VDD, 25-A SWIFT Synchronous Step-Down Converter with Full Differential Sense, RVF0040A (LQFN-CLIP-40)	RVF0040A	TPS548B22RVFR	Texas Instruments
C141, C142, C143, C144, C145, C146, C147, C148, C155, C156, C157, C158, C159, C160, C161, C162	0	0.22uF	CAP, CERM, 0.22 uF, 10 V, +/- 20%, X5R, 0201	0201	LMK063BJ224MP-F	Taiyo Yuden
C149, C150, C151, C152, C153, C154	0	0.1uF	CAP, CERM, 0.1 uF, 6.3 V, +/- 10%, X5R, 0201	0201	C0603X5R0J104K030BC	TDK
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H3, H5, H7	0		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
H2, H4, H6, H8	0		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B and F Fastener Supply

Table 5-1. Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
J21, J22, J27, J28, J30, J31, J32, J33, J38, J39, J40, J41	0		SMA, Straight Jack, SMT	SMA Connector, SMT	732511352	Molex
J23, J24, J25, J26, J34, J35, J36, J37	0		SMA JACK 50 OHM, R/A, SMT	SMA JACK, R/A, SMT	32K243-40ML5	Rosenberger
J29	0		Header, 100mil, 12x2, Gold, TH	12x2 Header	TSW-112-07-G-D	Samtec
R103	0	4.70k	RES, 4.70 k, 1%, 0.063 W, 0402	0402	CRG0402F4K7	TE Connectivity
R104, R107, R110	0	1.00k	RES, 1.00 k, 1%, 0.063 W, 0402	0402	MCR01MZPF1001	Rohm
R105, R108, R111	0	13.0k	RES, 13.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040213K0FKED	Vishay-Dale
R106, R109, R112, R113, R114	0	59.0k	RES, 59.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040259K0FKED	Vishay-Dale
SA1	0		DS160PR410, RNQ0040A (WQFN-40)	RNQ0040A	DS160PR410	Texas Instruments
SH-J7, SH-J8, SH-J9, SH-J10	0	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions

6 References

For references, see the following:

1. Texas Instruments, *DS160PR410 4-Channel PCI-Express Gen-4 Linear Redriver Datasheet* (SNLS645)
2. Texas Instruments, *DS160PR410 Programming Guide* (SNLU255)
3. Texas Instruments, *Understanding EEPROM Programming for DS160PR410 PCI-Express Gen-4 Redriver* (SNLA320)

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2020) to Revision B (July 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	3

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

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