

Application Note

Low Pixel Clock Display Link Design Guide



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Abstract

This document was translated from a simplified Chinese source. ([ZHCAGD5](#))

This article focuses on low pixel clock display links adopting DS90UB927Q-Q1 and DS90UB926Q-Q1.

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1 Introduction

The PCLK range supported by FPD-Link DS90UB926Q-Q1 and DS90UB927Q-Q1 is $5\text{MHz} \leq \text{PCLK} < 15\text{MHz}$ (LFMODE = 1) and $15\text{MHz} \leq \text{PCLK} \leq 85\text{MHz}$ (LFMODE = 0). This corresponds to application payload rates from 155Mbps to 2.635Gbps, and actual forward line rates from 525Mbps to 2.975Gbps. The forward link adopts NRZ encoding, and the Nyquist frequency is half of the line rate, which is 262.5MHz to 1.4875GHz.

For animated displays such as automotive headlights and ground projections, SoC data can be serialized and deserialized and successfully transmitted via DS90UB926Q-Q1 and DS90UB927Q-Q1 devices.

Figure 1-1. Design Path



Table 1-1. Design Requirements under Different Resolutions

PCLK Range	DS90UB927Q-Q1	DS90UB926Q-Q1	Design Conclusion
$5\text{MHz} \leq \text{PCLK} < 15\text{MHz}$	LFMODE = 1	LFMODE = High	Must use Low-Frequency Mode
$15\text{MHz} \leq \text{PCLK} \leq 85\text{MHz}$	LFMODE = 0	LFMODE = Low	Use default high-frequency configuration

2 Regarding Design for Low-Resolution / Low-Frame-Rate Displays

2.1 How to Calculate Pixel Clock

Pixel Clock is the number of pixels transmitted per second in a display system.

Pixel clock = Total horizontal pixels × Total vertical pixels × Refresh rate

The total pixels here include active pixels and blanking pixels; for example, the standard parameters for a 720P @ 60Hz screen are as follows:

- Horizontal direction: 1280 (active) + 370 (blanking) = 1650
- Vertical direction: 720 (active) + 30 (blanking) = 750

Pixel clock = 1650 × 750 × 60 = 74,250,000 ≈ 74.25MHz

2.2 How to Design Low-Resolution Displays Using DS90UB926-Q1 and DS90UB927-Q1

2.2.1 Pin Control or Register Override

Table 2-1. DS90UB927Q-Q1 Design Specification

Configuration Method	5-15MHz Recommended Settings	Description
Hardware Strap	LFMODE pin pulled up to logic power supply with 10kΩ	LFMODE=1; TI explicitly requires using a 10kΩ pull-up when set high.
Software Override	Reg 0x04[1:0] = 11b	bit1 selects register control, bit0 selects Low-Frequency Mode; for example, 0x80 becomes 0x83.

Table 2-2. DS90UB926Q-Q1 Design Specification

Configuration Method	5-15MHz Recommended Settings	Description
Hardware Strap	MODE_SEL selects Mode #5: R3=226kΩ, R4=102kΩ (1%)	Corresponds to LFMODE High, i.e., 5MHz to <15MHz; not a standalone 10kΩ pull-up.
Software Override	Reg 0x02[1:0] = 11b	bit1 enables register override, bit0 selects LFMODE; Read back Reg 0x23[3]=1 to confirm actual status.

MODE_SEL is an analog configuration input, and the voltage divider target for Mode #5 is approximately 0.311 of VDD33. For hardware design, please refer to the DS90UB926Q-Q1 Pin Functions table and the actual package pinout: MODE_SEL is pin 15; the two voltage divider resistors at this node should be checked rather than simply adding a pull-up.

Software override is only applicable for bench verification with an accessible configuration path. The datasheet specifies that a PDB reset is required after LFMODE changes; meanwhile, PDB power-down will reset the control registers. 927 can be configured by the local SoC I2C; if 926 can only be accessed via BCC, an available BCC must exist first, or a local I2C master must be used on the deserializer side. If BCC is completely unavailable under the default strap and software cannot write to 926 0x02 from the SoC side, the hardware strap should be modified first in this case.

3 Debug Guide

This debug guide is mainly aimed at BCC CRC error accumulation and remote I2C access failure issues encountered while using DS90UB926Q-Q1 and DS90UB927Q-Q1 devices. BCC (bidirectional back channel) serves as the back channel, transmitting I2C, CRC, and 4bit standard GPIO information primarily at a rate of 10Mbps (5MHz)

3.1 Correct Configuration of Low Frequency Mode [LF Mode]

When an I2C access timeout occurs from the SoC to the remote 926 or downstream devices; because the occurrence path is on the BCC, it is easily misjudged as I2C frequency interference, BCC watchdog, or cable signal integrity issues.

However, if the LF Mode is not correctly matched on both sides, the devices will operate under conditions that do not meet the specified range of the current Frequency Mode, which may manifest as LOCK, BCC, or Remote I2C anomalies.

10MHz PCLK	☐	Both ends remain in high-frequency mode	☐	Link is not within the guaranteed range	☐	LOCK / BCC boundary is unstable
BCC packet reliability decreases	→	Remote I2C access anomaly	→	Software sees I2C timeout / intermittent fail		

Debug Flowchart:

1. Measure actual PCLK (min / typ / max)	Measure PCLK frequency using an oscilloscope
PCLK < 15MHz?	Yes: Enter Low-Frequency Mode check No: Debug according to conventional link
2. Check 927	LFMODE strap or 0x04[1:0]; 10MHz target is 11b
3. Check 926	MODE_SEL / 0x02[1:0]; read 0x23[3] to confirm status

3.2 I2C Communication

3.2.1 I2C Fundamental Frequency Modification

The registers in [Table 3-1](#) only change the SCL high/low timing output by the device as a local I2C master: 926 0x26/0x27 act on the deserializer local I2C bus; 927 0x18/0x19 act on the serializer local I2C bus. They do not change the I2C frequency from the SoC to 927, nor do they change the 10Mbps BCC line rate; the local I2C timings on both sides of the link can be configured independently.

Table 3-1. I2C Configuration Register

Device	Register	Description	Default Setting
DS90UB926Q-Q1	0x26=SCL High Time 0x27=SCL Low Time	Approx. 50ns per LSB	0x26=0x83 0x27=0x84 I2C frequency: 76.0kHz 0x26=0x14 0x27=0x26 I2C frequency: 345.0kHz
DS90UB927Q-Q1	0x18=SCL High Time 0x19=SCL Low Time	Approx. 50ns per LSB	0x18=0xA1 0x19=0xA5 I2C frequency: 76.7kHz

3.2.2 I2C Watchdog Mechanism

The BCC watchdog of 926 and 927 is used to terminate control-channel transactions that are not completed within the set time, such as when the remote SDA is continuously pulled low or the transaction cannot be completed. Watchdog expiration does not guarantee resetting the state machine, releasing all bus conditions, or completing a full bus recovery; if the anomaly persists, check the status and use the appropriate Digital RESET or PDB toggle according to the datasheet to complete recovery.

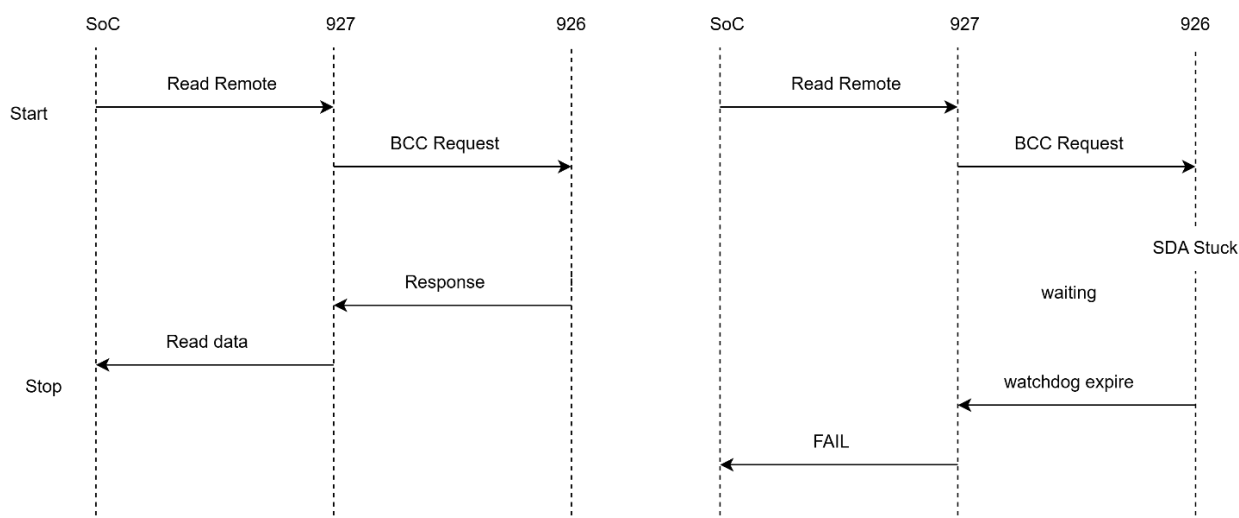


Figure 3-1. I2C Communication Mechanism

Read and record 926 0x04 and 927 0x16 simultaneously. It is recommended to capture SDA/SCL waveforms on the SoC side using Remote I2C read and compare at least two significantly different timeout settings; the enable/disable status of bit0 must be retained when writing to the timer. When only 926 0x04 is modified while 927 0x16 remains at its default value, the timeout observed on the SoC side may not necessarily change accordingly.

Device	Register	Description	Default Value	Default Timeout
DS90UB926Q-Q1	0x04[7:1]	2ms/LSB	0xFE	254ms
DS90UB927Q-Q1	0x16[7:1]	2ms/LSB	0xFE	254ms

3.2.3 DS90UB927Q-Q1 Auto-ACK Mechanism

When 927 0x03[5] Auto ACK is enabled, I2C writes targeting the deserializer or remote slaves meeting the I2C PASS ALL conditions are immediately ACKed without waiting for a remote response. This mechanism may mask remote NACKs or read/write errors and cannot serve as evidence that the remote operation has completed normally; use remote read preferentially when verifying watchdog or remote reachability.

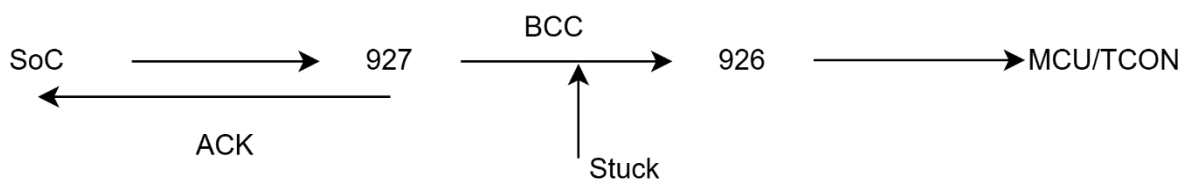


Figure 3-2. DS90UB927Q AUTO ACK Mechanism

Register	Description
0x03[5]	Auto ACK: Applicable only to remote I2C writes. Once enabled, when writing to the deserializer (or remote slave under I2C PASS ALL conditions), 927 returns ACK without waiting for the remote response; this function masks remote NACKs/errors and cannot be used to prove successful remote operation. 0: Disable (default) 1: Enable

3.3 Signal Integrity Testing

DS90UB926Q-Q1 can work with the supported Margin Analysis Program (MAP) in ALP to evaluate link margin. MAP scans error-free/lock-loss-free combinations of EQ level and strobe position, outputting a pass/fail margin map rather than an oscilloscope physical eye diagram, and cannot replace S-parameters or complete channel compliance testing. For specific operations, please refer to [SNLU243](#).

When the Frequency Mode, power supply, and reset conditions of low PCLK have been confirmed correct, but faults are still related to temperature, vibration, harness/connector stress, or noise, S-parameters can be used as compliance verification for the complete channel. For a single-channel link of DS90UB927Q-Q1 + DS90UB926Q-Q1, the calculation is as follows:

- Forward-channel line rate = $PCLK \times 35$
- Nyquist frequency = Forward-channel line rate / 2 = $PCLK \times 17.5$

Insertion loss and return loss RL/IL must be compared across the specified full frequency band.

Define pin-to-pin range	→	VNA calibration and de-embedding	→	Measure complete signal channel	→	Export S2P/S4P files	→	Judge according to TI channel spec specifications
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VNA measurement ports should be set between the FPD-Link pins and reference planes of 927 and 926, and test objects must include the serializer PCB, HSD/intermediate connector, cable assembly, and deserializer PCB. For a 100ohm differential channel, differential-mode S-parameters can be used: SDD11/SDD22 to evaluate return loss, SDD21/SDD12 to evaluate insertion loss; if required by project specifications, metrics such as mode conversion should also be evaluated. Retain calibration methods, fixture models, de-embedding settings, and raw .sNp files. Measuring only the PCB or only the cable can only serve as budget analysis and cannot replace total-channel PASS/FAIL. For detailed S-parameters, please refer to: [ZHCAG93](#) – AUGUST 2026

DS90UB926Q-Q1 and DS90UB927Q-Q1 belong to 3rd-generation FPD devices; therefore, channel specifications need to comply with FPD3-Channel-Requirements-DS90UH94xA_Rev0p5.pdf;

4 Reference Documents

Texas Instruments, DS90UB927Q-Q1 [SNLS416](#)

Texas Instruments, DS90UB926Q-Q1 [SNLS422](#)

Texas Instruments, [ZHCAG93](#); S-Parameters and FPD-Link Channel Spec Detailed Explanation

Texas Instruments, [SNLU243](#); FPD-Link Margin Analysis Program (MAP) user's guide

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